

# DESIGN OF HIGH POWER DENSITY SWITCHED CAPACITOR DC-DC CONVERTER

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Graduate School

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**Title**

DESIGN OF HIGH POWER DENSITY SWITCHED CAPACITOR DC-  
DC CONVERTER

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The Supervisory Committee certifies that this *disquisition* complies with North Dakota  
State University's regulations and meets the accepted standards for the degree of

**MASTER OF SCIENCE**

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## **ABSTRACT**

Design and implementation of high power density and high efficiency dc-dc converters has been a primary component for reducing energy cost. Traditionally dc-dc converters are composed with silicon based technology that has limited switching frequency hence, increased volume of passive components and lower efficiency.

This research presents a novel type of multilevel modular switched capacitor dc-dc converters with comprehensive design and multiple variant prototypes. Previous versions of traditional multilevel modular switched-capacitor dc-dc converters have a low switching device voltage rating. Additionally, the proposed circuits share all the advantages from the multilevel modular switched capacitor type converters such as soft switching, low voltage device rating, bidirectional operation, high conversion ratio, extremely high or low environment temperature operation, basic control algorithm, and modular structure. The converters in this research are found to be superior due to the simple structure, soft switching, and low conduction loss and, 97% or higher efficiency.

## **ACKNOWLEDGEMENTS**

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I feel fortunate to be the part of the Electrical Engineering department here at North Dakota State University and I am grateful for all technical and the financial support that the E.E. department had to offer during my masters' studies.

## **DEDICATION**

This work is dedicated to my family and close friends. Austin, thank you for placing your trust and confidence in my abilities.

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## LIST OF ABBREVIATIONS

MMSCC.....	multilevel modular switched-capacitor.
SWRMC.....	single-wing resonant multilevel converter
GaN.....	gallium nitride
SiC.....	silicon carbide
PWM.....	pulse width modulation
PCB.....	printed circuit board
DSP.....	digital signal processing
FPGA.....	field-programmable gate array
CPLD.....	complex programmable logic device
EPC.....	efficient power conversion
COG.....	stable temperature compensating ceramic capacitor
NPO.....	stable temperature compensating ceramic capacitor
ZCS.....	zero current switching
ZVS.....	zero voltage switching
kHZ.....	kilo hertz
nH.....	nano Henry
uF.....	micro Farad

## 1. INTRODUCTION

Development of the Wide Band-gap devices such as gallium nitride (GaN) and silicon carbide (SiC) has led to comprehensive benefits and advancements in the power electronics community. Many industry leading companies are investing in research and development within the wide band-gap area. High power density, high switching frequency, and high temperature operation of dc-dc and many other types of converters are requirements by many industry applications. By using SiC and GaN semiconductors it is possible to increase the switching frequency to the megahertz level, which leads to a high power density due to the reduction in the passive component size. Switched-capacitor dc-dc converter without a magnetic core has been used for low power on-chip applications since the 1970's [1]. Through the last two decades several new types of magnetic-less multilevel dc-dc converters were derived from high power multilevel inverter structures, which were proposed for high power automotive applications. Moreover, very high power high current dc-dc converter prototypes have been built and tested, i.e. 10 kW and 55 kW and their efficiency has reached 99%. However, these dc-dc converters suffer from high device conduction loss and high device current stress issues, especially with a high voltage conversion ratio. By inserting a small inductor with a magnetic-core to the switched-capacitor dc-dc converter, the converter can achieve resonant operation. This also allows the converter to reach the zero current switching [2]. However, inserting a magnetic-core may limit the benefits of the switched-capacitor dc-dc converter with high temperature and high frequency. First version of switched capacitor converter does not utilize the magnetic core inductors which are known to produce EMI due to ringing and have additional power loss at higher frequencies [3]. Other disadvantages of magnetic core inductors are the low temperature operation and the physical size of the passive

components which compromise the power density leading to the large size and overall cost of the converter.

The structure of the multilevel switched capacitor converters can be very complex and lots of research has been conducted to reduce the number of switching devices without sacrificing the advantages [4], [5]. By utilizing stray inductance or air core inductors and wide band-gap devices it is possible to build a novel switched capacitor multilevel converter. Previously there were many multilevel switched capacitor converters built, that have a high conversion ratio, high power output, and large capacitor banks with significant capacitance. However, the switches employ a hard switching mode and while charging the capacitors with another capacitor, very large transient current spikes take place due to the voltage difference [6]. These types of converters suffer high voltage overshoot across the device due to a large turn off current which limits the converter delivering the higher power level and operation at higher switching frequencies. However, resonant operation is accomplished by inserting an inductor and zero current switching can be achieved and the conversion can reach a megawatt level of power [2],[7],[8] . Resonant converter operation controls the switching losses and significantly lowers the high current transients by accomplishing zero current switching. Resonant operation and zero current switching can lower losses due to the concurrent high voltage across the switches [9].

This document presents an innovative switched capacitor dc-dc converter that utilizes stray inductance to achieve resonant operation and zero current switching by all of the switching devices. The proposed converter is modular in structure and a higher conversion ratio can be easily acquired by integrating the multiple modules together. Double-Wing and Single-Wing Resonant Multilevel Converters utilize ceramic capacitors, wide band-gap devices, and are suitable for high voltage, high power, and extreme environment temperature operation [10]. Due to their structure,

the exceptional technique for reducing the number of switching devices[9],[11], and lowering the voltage stress across the switches as well as the capacitors, the proposed converter combines the benefits with previously mentioned designs. The multiple converter prototypes designed in the SPEED lab have a power rating of 600W and are composed of EPC GaN switches and COG/NPO ceramic capacitors.

## 2. CONVERTER IMPLEMENTATION AND ANALYSIS

### 2.1. Steady State Resonant Operating Principle

The converter structure shown in Figure 1 is based on 8 times the conversion ratio and bidirectional operation without any control algorithm change. This means that the load and source can exchange places and converter can operate in buck or boost mode. The detailed converter analysis (step up) boost mode will be shown and described.

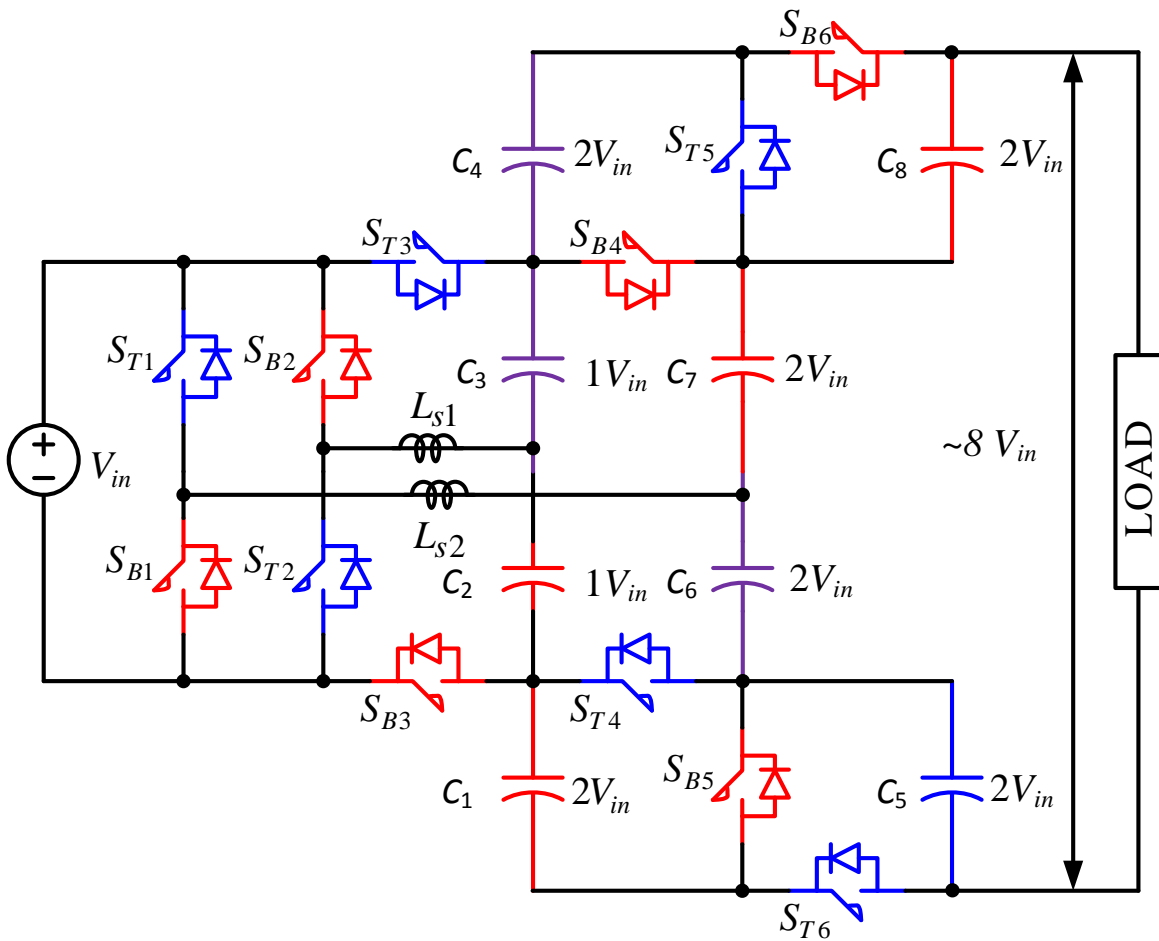


Figure 1. Multilevel switched-capacitor dc-dc converter with 8 times conversion ratio



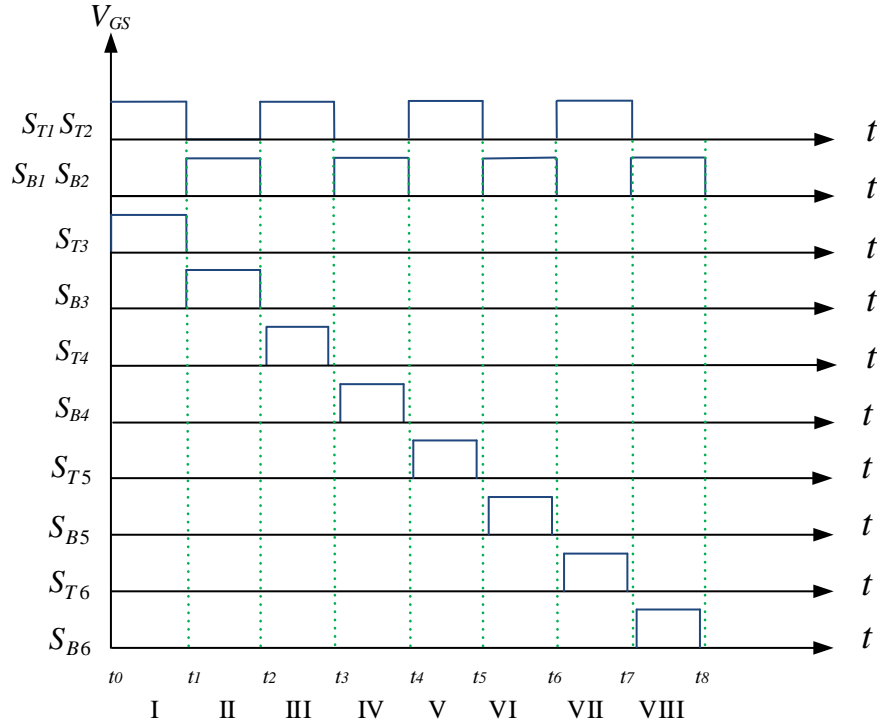


Figure 2. Eight state gate control signal of the proposed dc-dc converter

The converter shown in Figure 1 can reach N times conversion ratio without increasing the voltage stress on the switching devices and the resonant capacitors. However, due to the lab limit and the simplicity of the converter design Figure 1 shows the converter circuit topology at 8 times conversion ratio. As mentioned previously, two different control methods are shown. However, for easier understanding and analysis of the converter's resonant operation, the control gate signal using four switching states in Figure 2 is examined in detail. The initial capacitor voltage and the current through the inductor is assumed to be zero. For the underdamped case the damping ratio is  $\zeta = R\sqrt{C/L} / 2$  and once the RLC circuit meets the underdamped operation the current waveform will be oscillatory meaning the current waveform is sinusoidal. By using an eight-state gate control the Double-Wing Resonant Multilevel Converter can be further separated in to eight different switching states.

In every switching state, the simplified equivalent circuits of the proposed converter can be considered as a series  $RLC$  circuit with a voltage source. Switch conduction loss is modeled using  $R_{on}$  and the capacitor power loss is modeled using  $RESR$ .  $L$  can be considered as the sum of the stray inductance, in one switching loop  $L = \sum L_{SN}$ .  $C$  can be considered as the value of all the capacitance in series in one switching loop.  $R$  can be considered as the sum of all the turn ON resistance and the capacitor ESR in one switching loop,  $R = \sum R_{on} + \sum R_{ESR}$ . In every switching state, the circuit behavior can be considered as the step response of this series  $RLC$  circuit. The initial value of capacitor voltage is  $V_c$ , and the initial value of inductor current is zero. When the value of  $R$ ,  $L$ , and  $C$  meets the underdamped circuit operation, the circuit is able to operate in the resonant case with zero current switching for the switching devices. The natural frequency is  $\omega_0 = \frac{1}{\sqrt{LC}}$ . For the underdamped case  $\omega_0 = \frac{1}{\sqrt{LC}}$ . The resonant frequency of each loop is  $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ , where  $\alpha_0 = \frac{R}{2L}$  represents the neper frequency. If gate signal switching algorithm in Fig. 2 is used, the proposed multilevel switched capacitor dc-dc converter can be separated in eight different loops and can be analyzed separately.

A. State I ( $t_0 - t_1$ ):

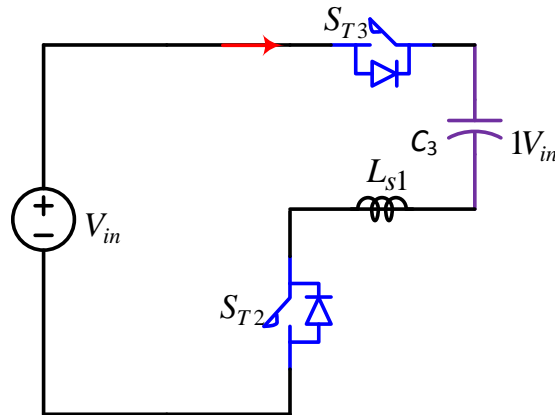


Figure 3. Simplified equivalent circuit during state I

During state I, the switches  $S_{T2}$  and  $S_{T3}$  are conducting and capacitor  $C_3$  is charged to  $1V_{in}$ . Moreover, as mentioned previously to model the conduction loss and capacitor power loss, assuming the turn on resistance of the switches and is  $R_t$  and  $R_t$  respectively, and the Equivalent Series Resistance (ESR) of the capacitor is  $R$ . The required resonant frequency for the soft switching can be calculated using the equations mentioned previously. The equivalent inductance of the loop is  $L$ . The resonant frequency is shown in (1) ~ (3).

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1})(C_3)}} \quad (1)$$

$$\alpha_0 = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{on3} + \sum R_{ESR3})}{2(L_{S1})} \quad (2)$$

$$\omega_d = \sqrt{\omega_{01}^2 + \alpha_{01}^2} \quad (3)$$

B. State II ( $t_1 - t_2$ ):

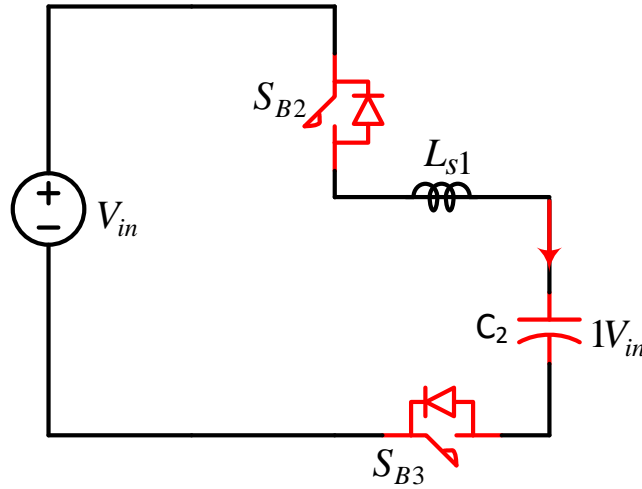


Figure 4. Simplified equivalent circuit during state II

During state II,  $S_{B2}$  and  $S_{B3}$  are turned on and capacitor  $C_2$  is being charged by the voltage source to  $1V_{in}$ . Similarly as in previous state, conduction loss model of the switches  $S_{B2}$  and  $S_{B3}$  is  $R_{b_{on2}}$  and  $R_{b_{on3}}$  and the ESR of the capacitor  $C_2$  is  $R_{ESR2}$ . The equations for calculating the resonant frequency are listed below as shown in (4) ~ (6):

$$\omega_{01} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1})(C_2)}} \quad (4)$$

$$\alpha_{01} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2L_{S1}} = \frac{(R_{b_{on2}} + R_{b_{on3}} + R_{ESR2})}{2L_{S1}} \quad (5)$$

$$\omega_{d01} = \sqrt{\omega_{01}^2 + \alpha_{01}^2} \quad (6)$$

C. State III ( $t_2 - t_3$ ):

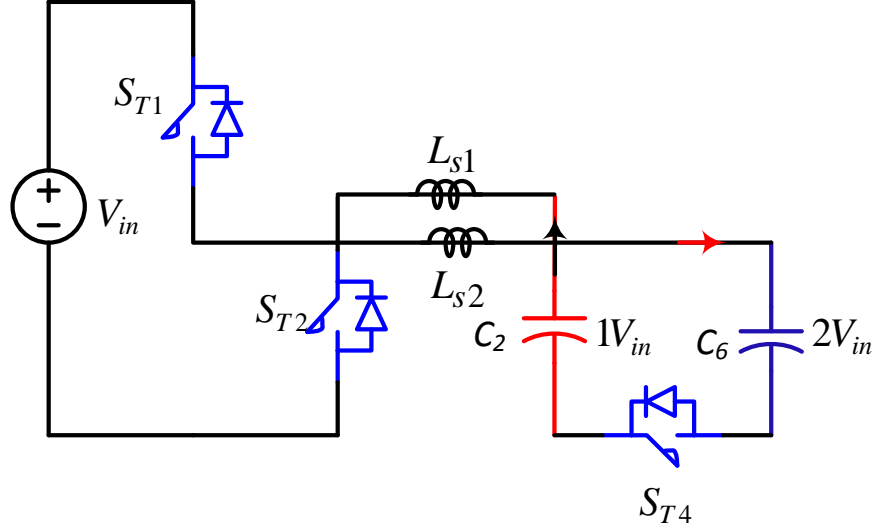


Figure 5. Simplified equivalent circuit during state III

During the state III, the switching devices  $S_{T1}$ ,  $S_{T2}$  and  $S_{T4}$  are turned on. Capacitor  $C_2$  and the voltage source are connected in series to charge the capacitor  $C_6$  to  $2V_{in}$ . Turn on resistance of the switches  $S_{T1}$ ,  $S_{T2}$  and  $S_{T4}$  are  $R_{t_{on1}}$ ,  $R_{t_{on2}}$ ,  $R_{t_{on4}}$ , and the ESR of the capacitors  $C_2$ ,  $C_6$  are  $R_{ESR2}$  and  $R_{ESR6}$  respectively. Similarly, the equations for calculating the resonant frequency are listed below in (7) ~ (9). Where equivalent inductance for the loop is the sum  $L_{S1}$  and  $L_{S2}$ , equivalent capacitance is  $C_2$  in series with  $C_3$  and equivalent resistance is the sum of  $R_{t_{on1}}$ ,  $R_{t_{on2}}$ ,  $R_{t_{on4}}$ ,  $R_{ESR2}$  and  $R_{ESR6}$ .

$$\omega_{02} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1} + L_{S2}) \frac{1}{\frac{1}{C_2} + \frac{1}{C_3}}}}} \quad (7)$$

$$\alpha_{02} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1} + L_{S2})} = \frac{(R_{b_{on1}} + R_{b_{on2}} + R_{b_{on4}} + R_{ESR2} + R_{ESR6})}{2(L_{S1} + L_{S2})} \quad (8)$$

$$\omega_{d02} = \sqrt{\omega_{02}^2 + \alpha_{02}^2} \quad (9)$$

D. State IV ( $t3 - t4$ ):

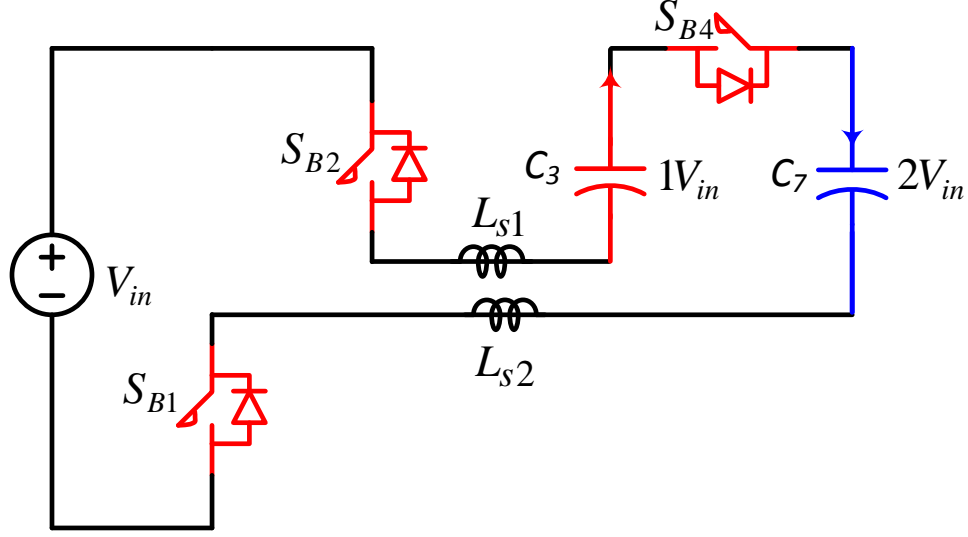


Figure 6. Simplified equivalent circuit during state IV.

During state IV, the switches  $S_{B1}$ ,  $S_{B2}$ ,  $S_{B4}$  are conducting. Capacitor  $C_3$  and the voltage source are connected in series to charge the capacitor  $C_7$  to  $2V_{in}$ . Conduction loss model of the switches  $S_{B1}$ ,  $S_{B2}$  and  $S_{B4}$  are  $R_{b_{on1}}$  and  $R_{b_{on2}}$  and the ESR of the capacitors  $C_3$  and  $C_7$  are  $R_{ESR3}$  and  $R_{ESR7}$  respectively. The equations for calculating the resonant frequency are showed below. Where equivalent inductance for the loop is the same as in state three. Equivalent capacitance is  $C_3$  in series with  $C_7$ , and equivalent resistance is the sum of  $R_{b_{on1}}$ ,  $R_{b_{on2}}$ ,  $R_{b_{on4}}$ ,  $R_{ESR3}$  and  $R_{ESR7}$ .

$$\omega_{04} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1}+L_{S2})\frac{1}{\frac{1}{C_3}+\frac{1}{C_7}}}} \quad (10)$$

$$\alpha_{04} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1}+L_{S2})} = \frac{(R_{b_{on1}}+R_{b_{on2}}+R_{b_{on4}}+R_{ESR3}+R_{ESR7})}{2(L_{S1}+L_{S2})} \quad (11)$$

$$\omega_{d3} = \sqrt{\omega_{03}^2 + \alpha_{03}^2} \quad (12)$$

E. State V ( $t4 - t5$ ):

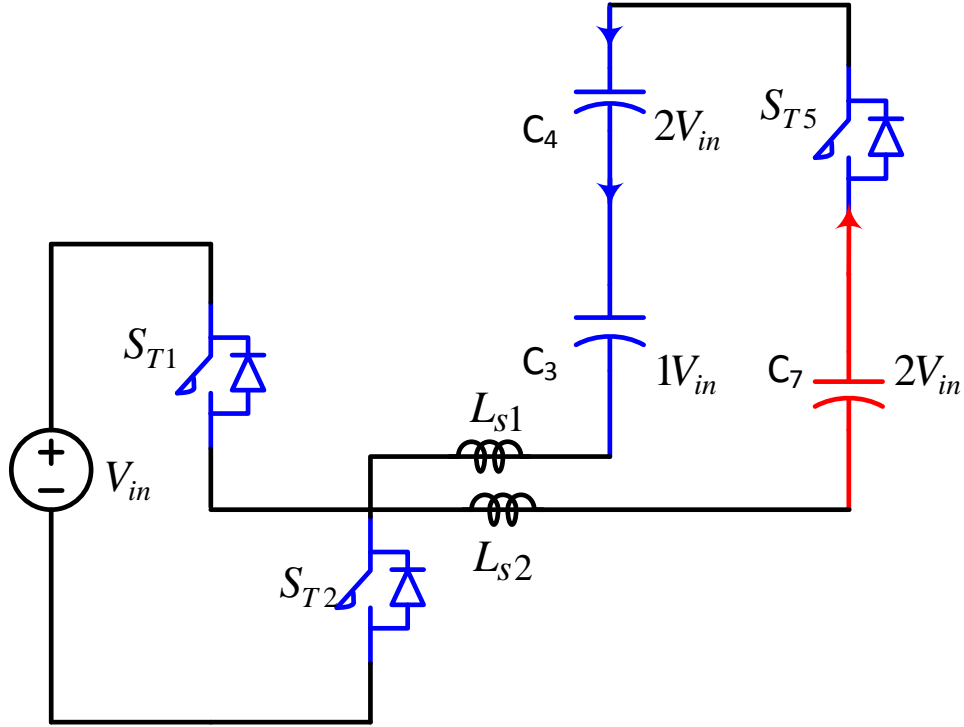


Figure 7. Simplified equivalent circuit during state V

During state V, the switches  $S_{T1}$ ,  $S_{T2}$  and  $S_{T5}$  are conducting. Voltage source and capacitor  $C_7$  are connected in series to charge the capacitors  $C_3$  and  $C_4$ . Since  $C_3$  is previously charged to  $1V_{in}$ ,  $C_4$  is being charged to  $2V_{in}$ . The equivalent inductance is the same as in state three and the equivalent capacitance is  $C_3$ ,  $C_4$ , and  $C_7$  in series with each other. Equivalent resistance is the sum of  $R_{ton1}$ ,  $R_{ton2}$ ,  $R_{ton5}$ ,  $R_{ESR3}$ ,  $R_{ESR4}$  and  $R_{ESR7}$ . Assuming turn on resistance of the switches  $S_{T1}$ ,  $S_{T2}$  and  $S_{T5}$  are  $R_{ton1}$ ,  $R_{ton2}$  and  $R_{ton5}$  and the ESR of the capacitors  $C_3$ ,  $C_4$  and  $C_7$  are  $R_{ESR3}$ , and  $R_{ESR7}$  respectively. Since more capacitors are connected in series in this case, the resonant frequency is

higher than all the previous cases without considering the turn on resistant influences.

F. State VI ( $t_5 - t_6$ ):

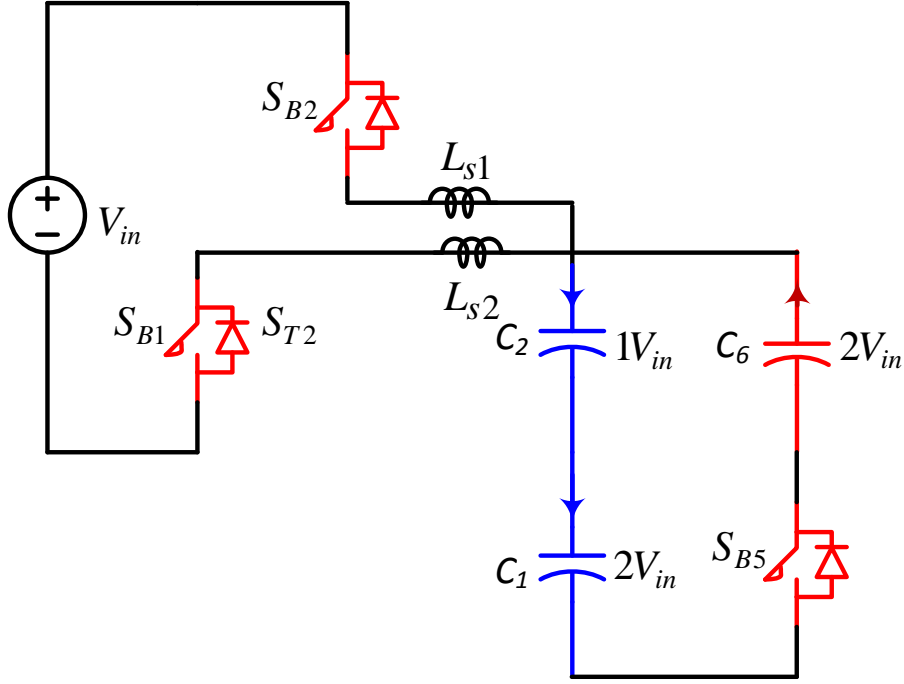


Figure 8. Simplified equivalent circuit during state VI.

During state VI, the switching devices  $S_{B1}$ ,  $S_{B2}$  and  $S_{B5}$  are conducting. Voltage source and capacitor  $C_6$  are connected in series to charge the capacitors  $C_1$  and  $C_2$ . Since  $C_2$  is previously charged to  $1V_{in}$ ,  $C_1$  is being charged to  $2V_{in}$ . Similarly, the equivalent inductance is the same as in state III. Assuming conduction loss model of the switches  $S_{B1}$ ,  $S_{B2}$  and  $S_{B5}$  are  $R_{b_{on1}}$ ,  $R_{b_{on2}}$ ,  $R_{b_{on5}}$  and the ESR of the capacitors  $C_2$ , and  $C_6$  are  $R_{ESR1}$ ,  $R_{ESR2}$  and  $R_{ESR6}$  respectively. Equivalent capacitance is  $C_1$ ,  $C_2$ , and  $C_6$  in series with each other and equivalent resistance is the sum of  $R_{ESR1}$ ,  $R_{ESR2}$  and  $R_{ESR6}$ . The resonant frequency equations are listed below.

$$\omega_{04} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1} + L_{S2}) \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_6}}}} \quad (13)$$

$$\alpha_{04} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1} + L_{S2})} = \frac{(R_{b_{on1}} + R_{b_{on2}} + R_{b_{on5}} + R_{ESR1} + R_{ESR2} + R_{ESR6})}{2(L_{S1} + L_{S2})} \quad (14)$$

$$\omega_{d3} = \sqrt{\omega_{03}^2 + \alpha_{03}^2} \quad (15)$$

G. State VII ( $t_6-t_7$ )

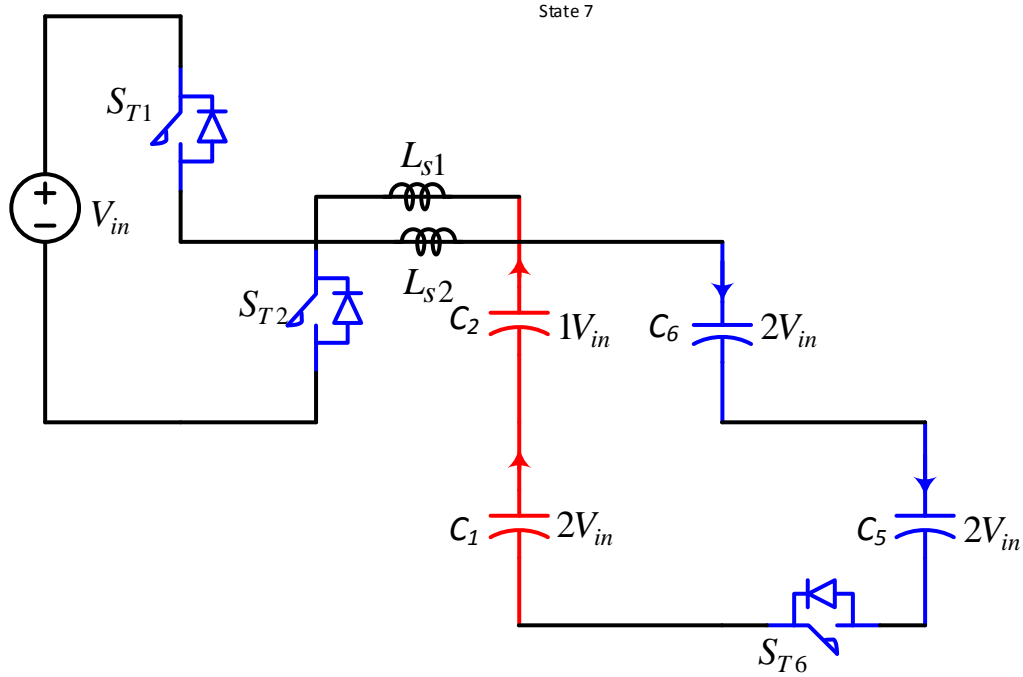


Figure 9. Simplified equivalent circuit during state VII

During state VII, the switches  $S_{T1}$ ,  $S_{T2}$  and  $S_{T6}$  are conducting. During this state,  $C_5$  and  $C_6$  are being charged while the  $C_1$ ,  $C_2$  and the input voltage sources are connected in series. The equivalent inductance is the same as in the previous state and the equivalent capacitance is  $C_1$ ,  $C_2$ ,  $C_6$  and  $C_7$  in series with each other. Meaning that the  $C_1$ ,  $C_2$  are being discharged. Equivalent resistance is the sum of the  $R_{t_{on1}}$ ,  $R_{t_{on2}}$ ,  $R_{t_{on6}}$ ,  $R_{ESR1}$ ,  $R_{ESR2}$ ,  $R_{ESR5}$  and  $R_{ESR6}$ . Assuming conduction loss model of the switches  $S_{T1}$ ,  $S_{T2}$  and  $S_{T6}$  are  $R_{t_{on1}}$ ,  $R_{t_{on2}}$  and  $R_{t_{on6}}$ , and the ESR of the capacitors  $C_1$ ,  $C_2$ ,  $C_5$  and  $C_6$  are  $R_{ESR1}$ ,  $R_{ESR2}$ ,  $R_{ESR5}$  and  $R_{ESR6}$  respectively. The resonant frequency equations are showed below. For this case, more capacitors are connected in series and the resonant frequency is even higher than all the previous cases, but since the turn on time of the switch  $S_{T6}$  could be controlled independently, this won't cause a problem. The resonant frequency equations for this particular loop are listed below.



$$\omega_{04} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1}+L_{S2})\frac{1}{\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_5}+\frac{1}{C_6}}}}} \quad (16)$$

$$\alpha_{04} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1}+L_{S2})} = \frac{(R_{t_{on1}} + R_{t_{on2}} + R_{t_{on6}} + R_{ESR1} + R_{ESR2} + R_{ESR5} + R_{ESR6})}{2(L_{S1}+L_{S2})} \quad (17)$$

$$\omega_{d3} = \sqrt{\omega_{03}^2 + \alpha_{03}^2} \quad (18)$$

H. State VIII ( $t_7 - t_8$ ):

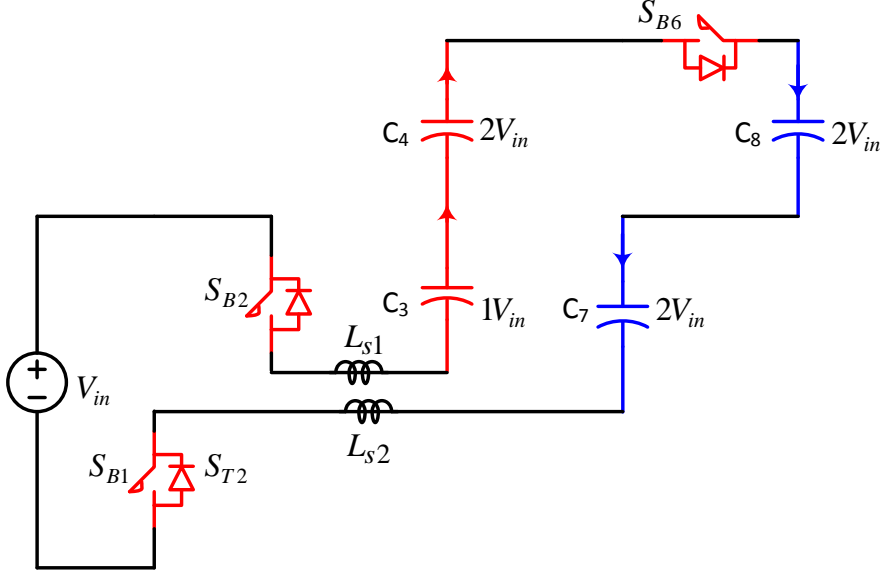


Figure 10. Simplified equivalent circuit during state VIII

During state VIII, the switches  $S_{B1}$ ,  $S_{B2}$  and  $S_{B6}$  are conducting. During this state, the capacitors  $C_7$  and  $C_8$  are being charged while the  $C_3$ ,  $C_4$  and the input voltage source are connected in series meaning that the  $C_3$ ,  $C_4$  are being discharged. The equivalent inductance is the same as in state three and the equivalent capacitance is  $C_3$ ,  $C_4$ ,  $C_7$  and  $C_8$  in series with each other. Assuming turn on resistance of the switches  $S_{B1}$ ,  $S_{B2}$  and  $S_{B5}$  are  $R_{b_{on1}}$ ,  $R_{b_{on2}}$ ,  $R_{b_{on6}}$  and the ESR of the capacitors  $C_3$ ,  $C_4$ ,  $C_7$ ,  $C_8$  are  $R_{ESR3}$ ,  $R_{ESR4}$ ,  $R_{ESR7}$  and  $R_{ESR8}$  respectively. Equivalent resistance is the sum of the  $R_{b_{on1}}$ ,  $R_{b_{on2}}$ ,  $R_{b_{on6}}$ ,  $R_{ESR3}$ ,  $R_{ESR4}$ ,  $R_{ESR7}$  and  $R_{ESR8}$ . The resonant frequency of this case should be the same as the state VII.

$$\omega_{04} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1}+L_{S2})\frac{1}{\frac{1}{C_4}+\frac{1}{C_3}+\frac{1}{C_7}+\frac{1}{C_8}}}}} \quad (19)$$

$$\alpha_{04} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1}+L_{S2})} = \frac{(R_{b_{on1}} + R_{b_{on2}} + R_{b_{on6}} + R_{ESR3} + R_{ESR4} + R_{ESR7} + R_{ESR8})}{2(L_{S1}+L_{S2})} \quad (20)$$

$$\omega_{d3} = \sqrt{\omega_{03}^2 + \alpha_{03}^2} \quad (21)$$

Table 1. Capacitor states

Capacitor Charging Path	On-State FET Switch	Capacitor Charging Path	On-State FET Switch
State I		State II	
C <sub>3</sub> ↓	S <sub>T2</sub> , S <sub>T3</sub>	C <sub>2</sub> ↓	S <sub>B2</sub> , S <sub>B3</sub>
State III		State IV	
C <sub>6</sub> ↓    C <sub>2</sub> ↑	S <sub>T1</sub> , S <sub>T3</sub> , S <sub>T4</sub>	C <sub>7</sub> ↓    C <sub>3</sub> ↑	S <sub>B1</sub> , S <sub>B2</sub> , S <sub>B4</sub>
State V		State VI	
C <sub>3</sub> , C <sub>4</sub> ↓    C <sub>7</sub> ↑	S <sub>T1</sub> , S <sub>T2</sub> , S <sub>T5</sub>	C <sub>1</sub> , C <sub>2</sub> ↓    C <sub>6</sub> ↑	S <sub>B1</sub> , S <sub>B2</sub> , S <sub>B5</sub>
State VII		State VIII	
C <sub>5</sub> , C <sub>6</sub> ↓    C <sub>1</sub> , C <sub>2</sub> ↑	S <sub>T1</sub> , S <sub>T2</sub> , S <sub>T6</sub>	C <sub>7</sub> , C <sub>8</sub> ↓    C <sub>3</sub> , C <sub>4</sub> ↑	S <sub>B1</sub> , S <sub>B2</sub> , S <sub>B6</sub>
↓ = Capacitor charging		↑ = Capacitor discharging	

## 2.2. 8x Conversion Ratio Simulation

This section focusses on the simulation results of the eight times the conversion ratio MSCCC. The simulation software used during simulation is Saber Simulator. The Converter is simulated at its maximum power rating which is 1000 watts. Input voltage is set to be 15 volts and the expected output voltage is 120 volts. The capacitance of all the capacitors  $C_1 \sim C_8$  are assumed to be 47 uF, and the two resonant air core inductors  $L_{S1}$ ,  $L_{S2}$  are 216 nH. The switching frequency of the proposed converter is 50 kHz. The turn on resistance of the low voltage switching devices are assumed to be 0.5 Ohm, and the turn on resistance of the high voltage device  $S_{T4,5}$ ,  $S_{B4,5}$ . The results show that the output voltage is has quite large ripple, however; the real application converter

will have input and output ceramic capacitor banks that will not affect the output voltage and will minimize the ripple.

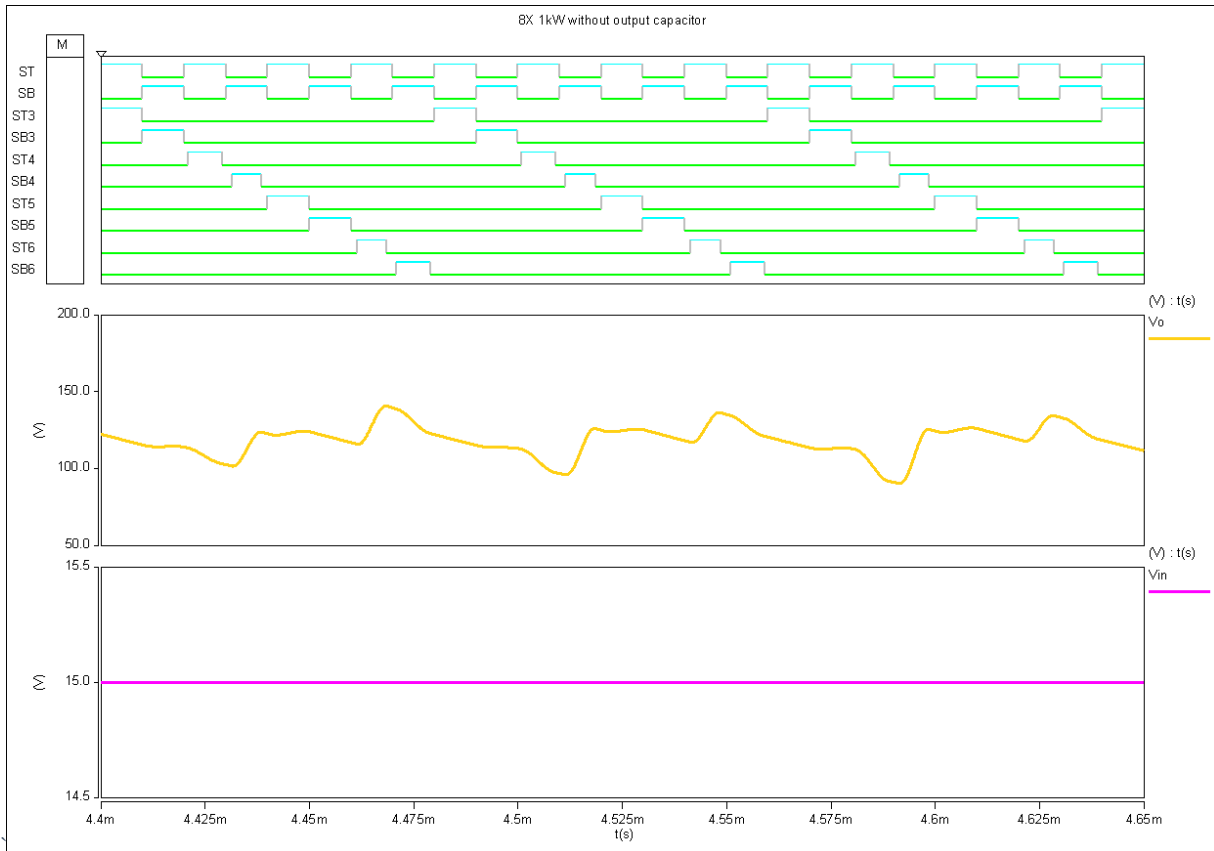


Figure 11. Simulated converter without output capacitor

### 2.3. Single Wing with Common Ground

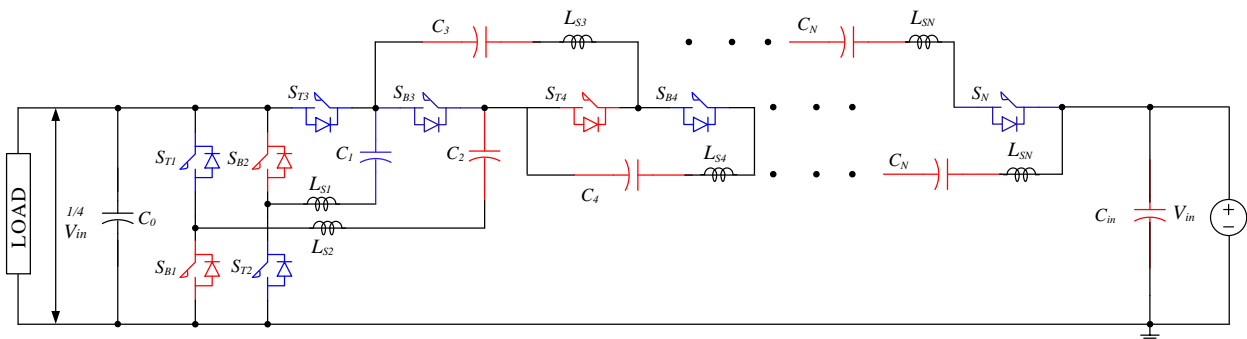


Figure 12. Single-Wing Ladder Resonant Multilevel Converter with common ground

Figure 12 displays the single wing ladder resonant multilevel converter structure for high conversion ratio. The stray inductors are represented as  $L_{S1}$ ,  $L_{S2}$  and  $L_{SN}$ . The individual capacitor

banks are labeled as  $C_0$ - $C_N$ . Even though the proposed converter topology has the capability of the bidirectional power flow, this paper focuses on the step down (buck mode) operation. Due to the lab limitation, the proposed converter prototype power rating is 600W. Single-Wing Ladder Resonant Multilevel Converter is composed of the GaN switching devices made by EPC, COG ceramic capacitors and air core inductors. The topology of the converter allows the inductors as well as the capacitors to have the same values respectively; however, individual converter resonant loops can be fine-tuned by properly adjusting the capacitance and the inductance. The converter control methods can vary from the simple two state control method where either all of the  $S_T$  or  $S_B$  switches are turned on at the same time. Fig.3 shows the control gate signal by using only two switching states. During each switching state by utilizing the control scheme in Fig.4 the individual equivalent circuits can be analyzed as a series RLC circuit. Throughout the switching state the circuit behaves as a step response of the RLC circuit.  $R$  can be expressed as the sum of all resistance during one switching loop  $R = \sum R_{on} + \sum R_{ESR}$  where  $R_{on}$  represents the device conduction loss and  $R_{ESR}$  is the capacitor power loss. Equivalent series capacitance for the individual switching states can be calculated with the assumption that  $C = \sum C_1 + C_2 + C_N$ . Natural frequency is obtained with the following equation  $\omega_0 = \frac{1}{\sqrt{LC}}$ . For this case the natural frequency of the individual switching loop is  $\omega_0 = \frac{1}{\sqrt{LC}}$  and the  $\omega_d$  is the switching frequency where  $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$  and  $\alpha_0 = \frac{R}{2L}$  is the neper frequency. Applying either one of the control methods proposed the equivalent series inductance of each switching loop is  $L = \sum L_{S1} + L_{SN}$  or  $L = \sum L_{S2} + L_{SN}$ . To achieve the zero-current switching the resonant frequency for each switching state can be calculated by using the following equation set:

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1}+L_{SN})\left(\frac{1}{C_1+C_2+C_N}\right)}} \quad (22)$$

$$\alpha_0 = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1}+L_{SN})} \quad (23)$$

$$\omega_d = \sqrt{\omega_{01}^2 - \alpha_{01}^2} \quad (24)$$

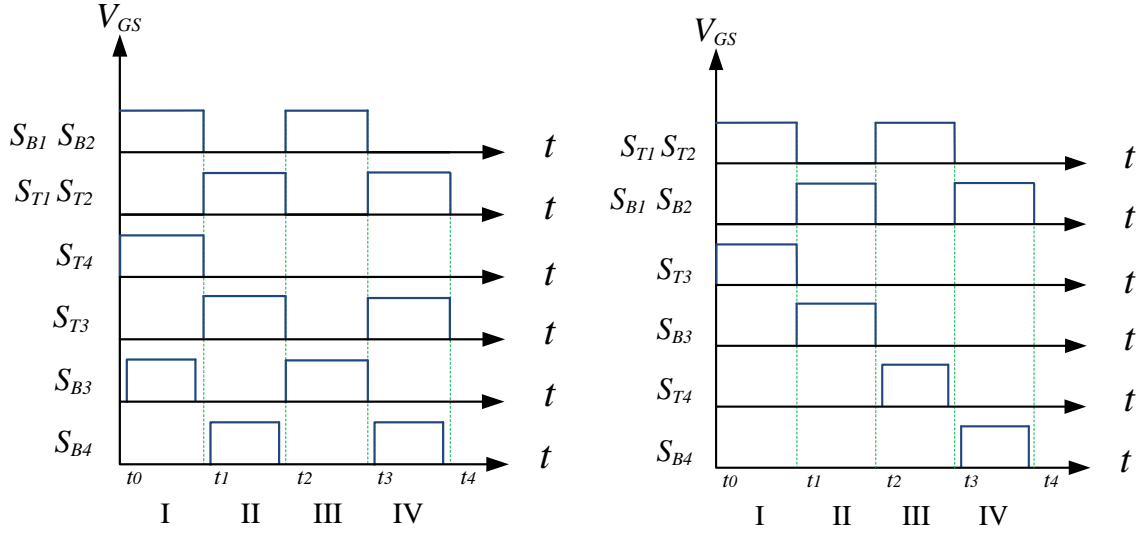


Figure 13. Two and four state gate control

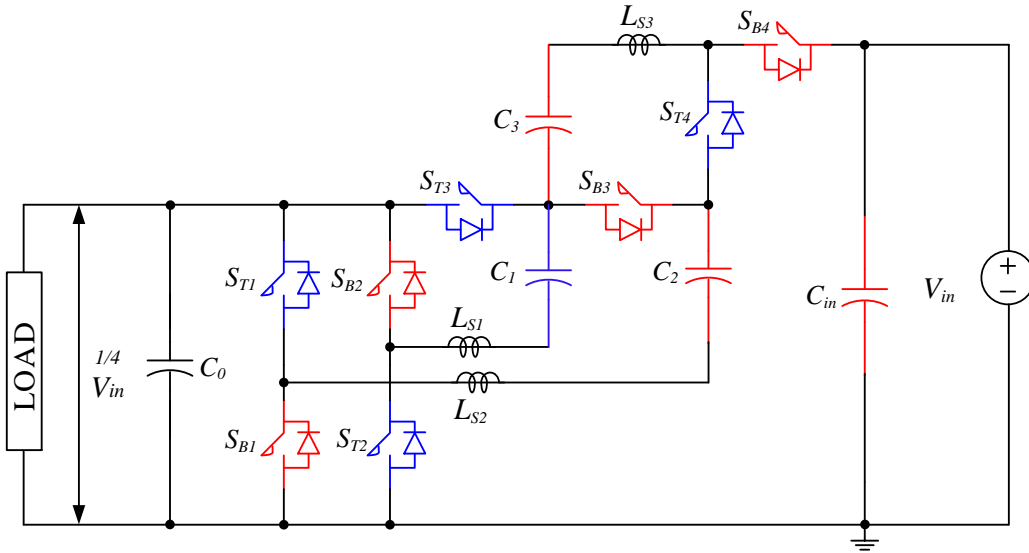


Figure 14. Main circuit structure with  $\frac{1}{4} V_{in}$  conversion ratio

The voltage output ripple can be controlled by increasing the output capacitor size without having much of an effect on the resonant operation. Capacitor charging, and the converter operation can be easily examined by using the four-state gate control method displayed in Fig.4. Furthermore, much simpler two switching states gate signal arrangement can be used as in Fig.3 by using only two switching states. With two state control method applied, either  $S_T$  or  $S_B$  switches are conducting at the same time. Switching device voltage stress is two times the converter low voltage side. If all the capacitor banks have the same capacitance value, few of the switching resonant loops will have the decrease in the capacitance due to the capacitors being connected in series. For the capacitors that are connected in series during the switching cycle the resonant frequency will rise and will be higher than the switching frequency. This effect implies that the turn on time of the corresponding switching devices should be shorter. The converter individual state breakdown and the detailed resonant analysis is explained in the following section.

#### **2.4. Steady State Resonant Operation**

As mentioned previously, two different control methods are shown in Fig.3 and Fig.4. However, for easier understanding and analysis of the converter's resonant operation, control gate signal using four switching states in Fig.4 is examined in detail. The initial capacitor voltage and the current through the inductor is assumed to be zero. For the underdamped case the damping ratio is  $\zeta = R\sqrt{C/L} / 2$  and once the RLC circuit meets the underdamped operation the current will be oscillatory which means that the current waveform is sinusoidal. By using four state gate control Single-Wing Ladder Resonant Multilevel Converter can be further separated in to four different switching states.

A. State I ( $t_0-t_1$ ):

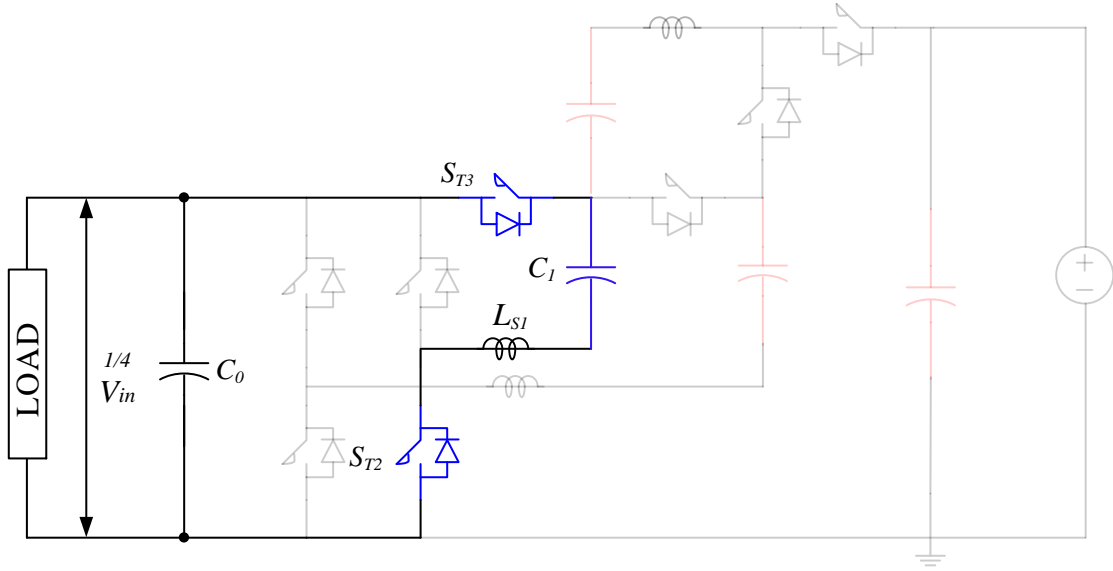


Figure 15. Converter equivalent circuit during state I

Once the converter has reached the steady state operation it can be noticed that during state one as shown in Figure 1 switches  $S_{T1}$ , and  $S_{T3}$  are conducting and the voltage across capacitor  $C_1$  is equal to  $\frac{1}{4} V_{in}$ . The capacitor power loss is modeled as  $R_{ESR1}$  and the switching devices  $S_{T1}$ , and  $S_{T3}$  turn on resistance is  $R_{ton2}$  and  $R_{ton3}$  respectively. During the switching loop the equivalent series inductance is  $L_{S1}$ . The resonant frequency is calculated by using equation set listed below (25) ~ (27):

$$\omega_{01} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1})(C_1)}} \quad (25)$$

$$\alpha_{01} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2L_{S1}} = \frac{(R_{ton2} + R_{ton3} + R_{ESR1})}{2L_{S1}} \quad (26)$$

$$\omega_{d01} = \sqrt{\omega_{01}^2 + \alpha_{01}^2} \quad (27)$$

B. State II ( $t_1-t_2$ ):

Throughout state II switching devices  $S_{B1}$ ,  $S_{B2}$  and  $S_{B3}$  are conducting and since the capacitor  $C_1$  has been previously charged to  $\frac{1}{4} V_{in}$ , the voltage across the capacitor  $C_2$  is equal to  $\frac{1}{2} V_{in}$ . Turn on resistance of the switching devices  $S_{B1}$ ,  $S_{B2}$  and  $S_{B3}$  is  $R_{bon1}$ ,  $R_{bon2}$  and  $R_{bon3}$ .

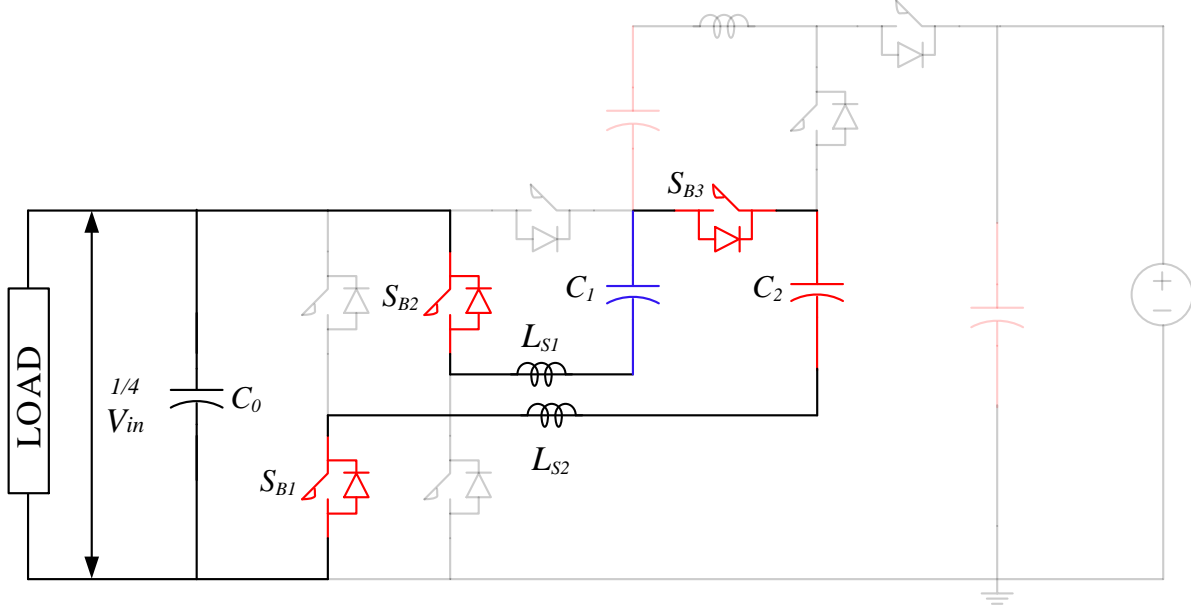


Figure 16. Converter equivalent circuit during state II

The *ESR* of the capacitors  $C_1$  and  $C_2$  is modeled as  $R_{ESR1}$  and  $R_{ESR2}$ . The total inductance of the switching loop is  $L = \sum L_{S1} + L_{S2}$ . Similarly as in the previous state the resonant frequency can be calculated by using the equations (28) ~ (30).

$$\omega_{02} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1} + L_{S2}) \frac{1}{\frac{1}{C_1} + \frac{1}{C_2}}}} \quad (28)$$

$$\alpha_{02} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1} + L_{S2})} = \frac{(R_{b_{on1}} + R_{b_{on2}} + R_{b_{on3}} + R_{ESR1} + R_{ESR2})}{2(L_{S1} + L_{S2})} \quad (29)$$

$$\omega_{d02} = \sqrt{\omega_{02}^2 + \alpha_{02}^2} \quad (30)$$



C. State III ( $t_2$ - $t_3$ ):

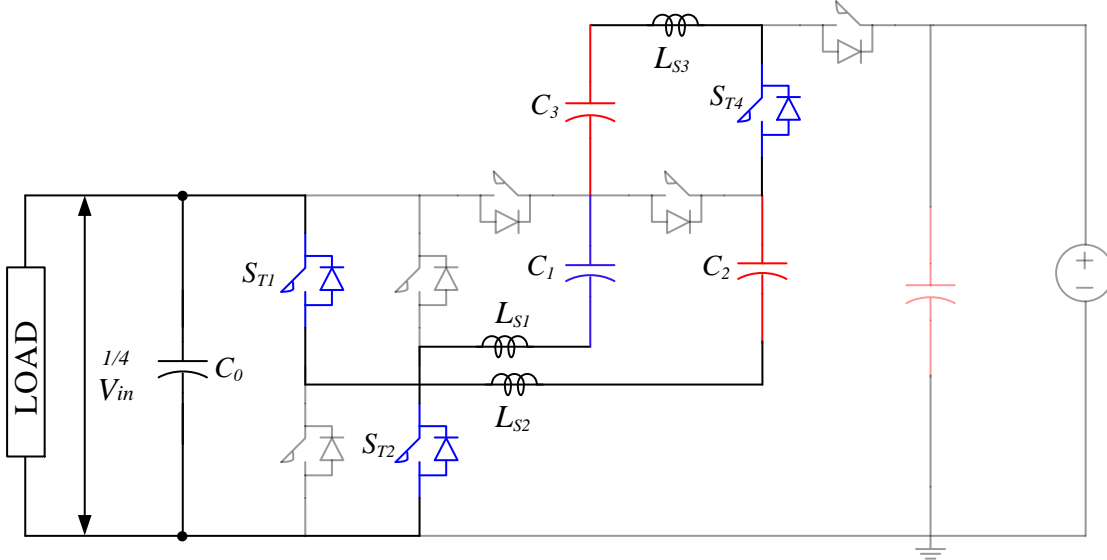


Figure 17. Converter equivalent circuit during state III

Similarly, as in the previous state throughout state III switching devices  $S_{T1}$ ,  $S_{T2}$  and  $S_{T4}$  are turned on. During the previous state the capacitor  $C_1$  has been charged to  $\frac{1}{4} V_{in}$  and capacitor  $C_2$  to  $\frac{1}{2} V_{in}$  resulting to voltage across the capacitor  $C_3$  equaling  $\frac{1}{2} V_{in}$ . Equivalent turn on resistance is the sum of  $R_{t_{on1}}$ ,  $R_{t_{on2}}$ ,  $R_{t_{on4}}$ ,  $R_{ESR1}$ ,  $R_{ESR1}$ ,  $R_{ESR2}$  and  $R_{ESR3}$ . The total inductance of the loop is the same as in the previous state  $L = \sum L_{S1} + L_{S2}$ . The resonant frequency can be calculated in the by using equations (31) ~ (33).

$$\omega_{04} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1} + L_{S2}) \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}}} \quad (31)$$

$$\alpha_{04} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1} + L_{S2})} = \frac{(R_{t_{on1}} + R_{t_{on2}} + R_{t_{on4}} + R_{ESR1} + R_{ESR2} + R_{ESR3})}{2(L_{S1} + L_{S2})} \quad (32)$$

$$\omega_{d3} = \sqrt{\omega_{03}^2 + \alpha_{03}^2} \quad (33)$$

D. State IV ( $t_3-t_4$ ):

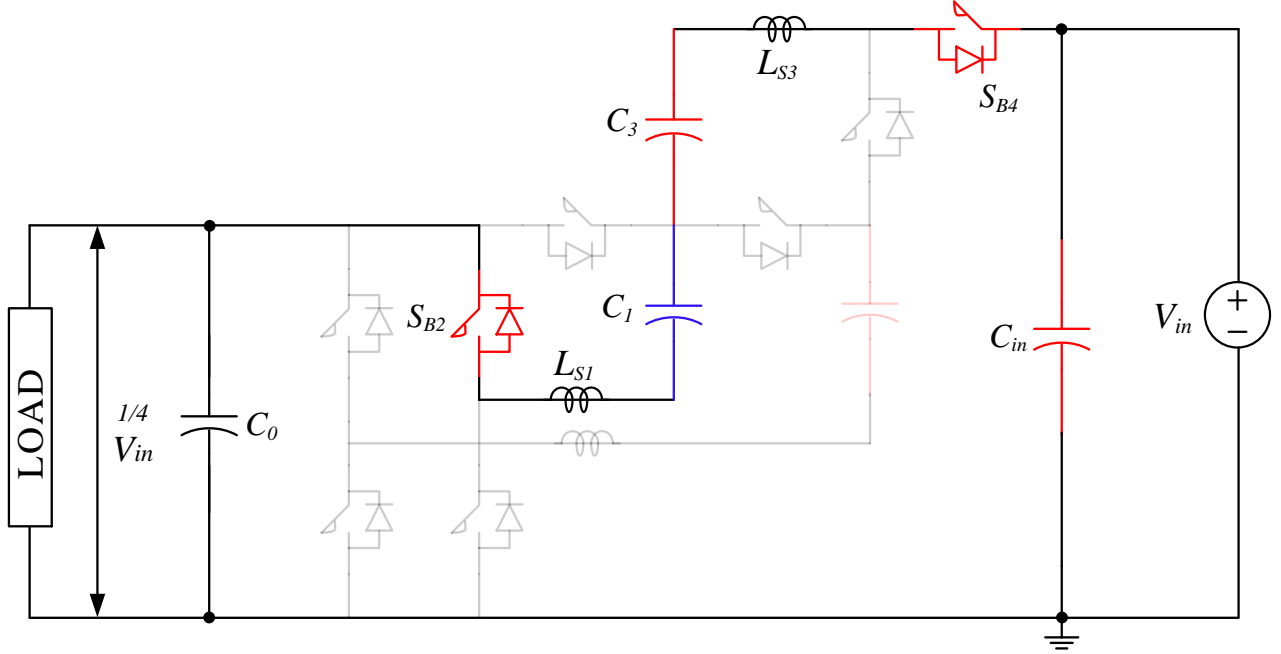


Figure 18. Converter equivalent circuit during state IV

During state four switching devices  $S_{B1}$ ,  $S_{B2}$  and  $S_{B3}$  are conducting. Since the steady state has been reached the voltage across the load and capacitor  $C_0$  is  $\frac{1}{4} V_{in}$ . Referring to the previous state the capacitor  $C_1$  has been charged to  $\frac{1}{4} V_{in}$  and  $C_3$  has been charged to  $\frac{1}{2} V_{in}$ . Summing the capacitor voltages together leads to the voltage across  $C_{in}$  to equal  $1V_{in}$ . Turn on resistance of the switching devices  $S_{B2}$  and  $S_{B4}$  is modeled as  $Rb_{on2}$  and  $Rb_{on4}$  and the  $ESR$  of the capacitors  $C_1$  and  $C_3$  is  $R_{ESR1}$  and  $R_{ESR3}$ . The total inductance of the switching loop is  $L = \sum L_{S1} + L_{S2} + L_{S3}$ . The resonant frequency is calculated by using the equations (34) ~ (36).

$$\omega_{06} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{(L_{S1} + L_{S2} + L_{S3}) \frac{1}{\frac{1}{C_1} + \frac{1}{C_3}}}} \quad (34)$$

$$\alpha_{04} = \frac{R}{2L} = \frac{(\sum R_{on} + \sum R_{ESR})}{2(L_{S1} + L_{S2} + L_{S3})} = \frac{(Rb_{on2} + Rb_{on4} + R_{ESR1} + R_{ESR3})}{2(L_{S1} + L_{S2} + L_{S3})} \quad (35)$$

$$\omega_{d06} = \sqrt{\omega_{06}^2 + \alpha_{06}^2} \quad (36)$$

## 2.5. Simulation

The simulation has been completed to verify the proposed converter resonant operation and the zero current switching as shown in Fig.9, Fig10, and Fig.11. The difference between the Fig.9 and Fig.10 is applied gate control method. The simulation results are obtained by using resistive load with input and output capacitors included during the simulation. Power rating of the designed converter is 600W. Input voltage  $V_{in}=60V$  and output voltage  $V_O=15$  and are both shown in Fig.10 and Fig.11. The capacitance of capacitor banks  $C_1\sim C_3$  is set to 47uF.  $C_{in}$  and  $C_o$  are input and output capacitors respectively. Both of the capacitance values for the  $C_{in}$  and  $C_o$  are equal to 470uF. If higher power output is desired the output capacitor can be increased without having significant effect on the resonant operation. Moreover, the switching frequency for this case will have to be recalculated but will not be excessively alternated. With two state gate control method used it can be seen that the output voltage  $V_o$  has relatively small voltage ripple of 0.2V and with four state gate control the voltage ripple is 0.3V. The current through the switching devices is shown for both of the gate control methods. Fig.10 shows that the two state control method has uniformly distributed current waveform for all of the switching devices and it has  $\frac{1}{2}$  smaller peak compared to the Fig.9 where four state control method is used. The inductance value of all of the inductors in the circuit  $L_{S1}$ ,  $L_{S2}$  and  $L_{S3}$  is equal to 216nH. The inductors in the circuit are considered as stray inductance or air core inductors, they also can be designed as internal structure of the printed circuit board. The switching frequency of the converter  $f_s= 50$  kHz; however, by correctly selecting the capacitance and the inductance converter can easily achieve switching frequency of 2 MHz or higher. Fig.11 shows the voltage of the capacitors  $C_1\sim C_3$  during the resonant operation of the converter.

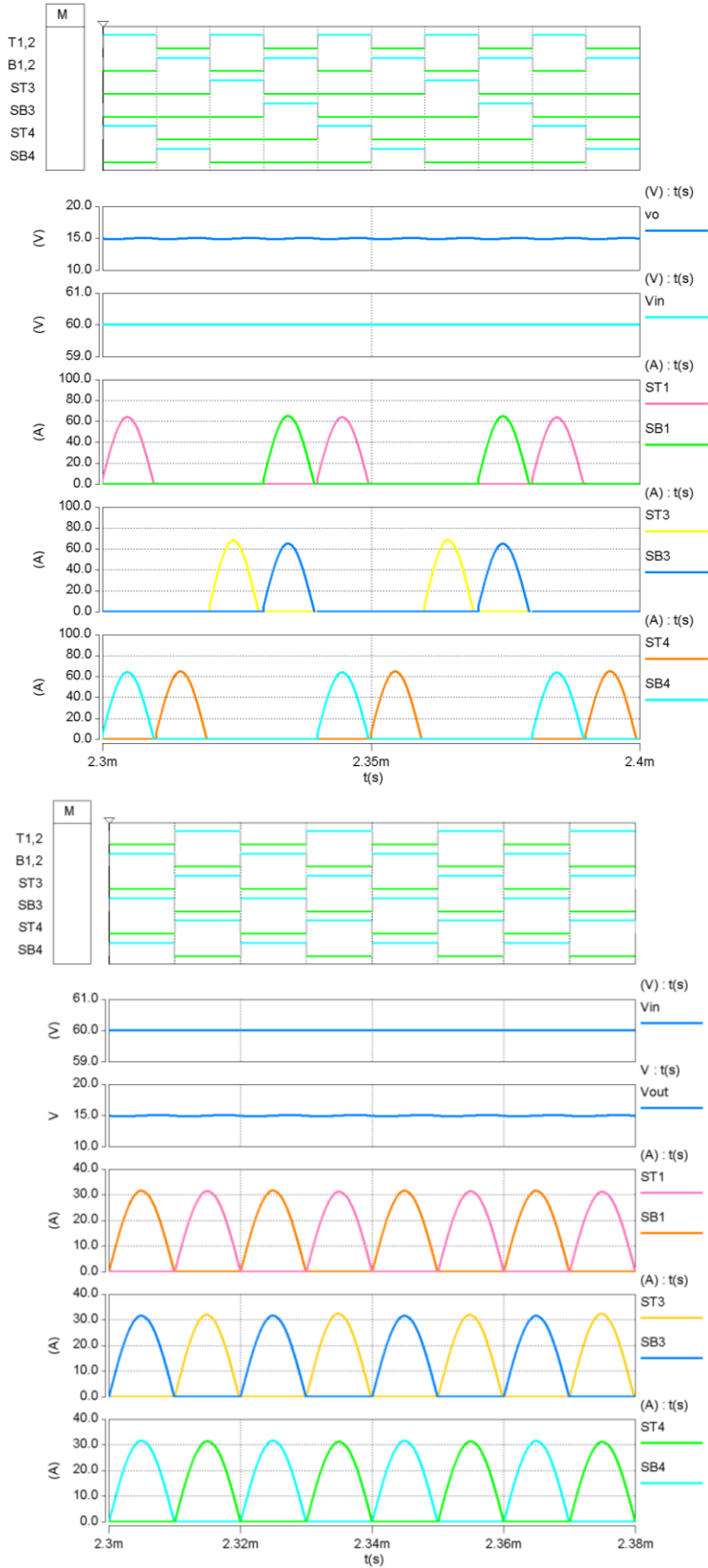


Figure 19. Device current stress using 4 and 2 state gate control algorithms

### 3. 4X TOPOLOGY AND HARDWARE DESIGN

#### 3.1. Four Times the Conversion Ratio

For the first hardware prototype the decision was made to build four times the conversion ratio converter due to the reduced amount of the components and its simplicity. The converter circuit topology stays the same except the wing side of the converter has 4 switches less. The first prototype is composed of four modular boards and one main board. The 4X Converter is composed of four 30V EPC GaN FET devices on the bridge side and four 60V devices on the wing side. Input voltage is 15V and the expected output voltage is 60V. The resonant loops are exactly the same as the first 4 states of the 8x version shown in detail in the previous section. The converter switching frequency is 233 kHz and input capacitor bank is 470uF. Resonant ceramic capacitors  $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_4$  have the same value of 5.2uF and the air core inductors  $L_{S1}$  and  $L_{S2}$  are 33nH.

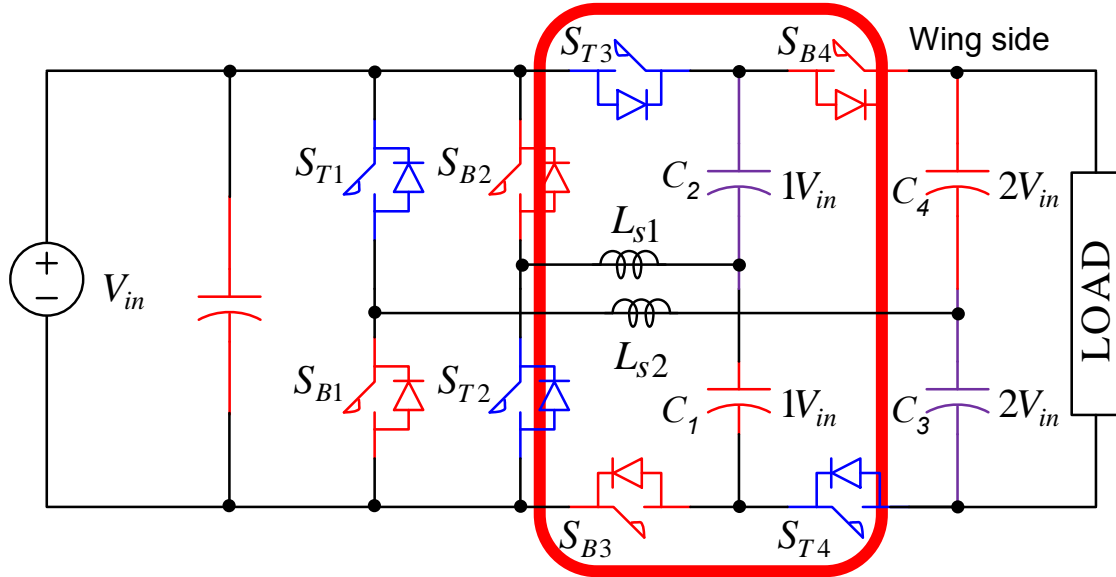


Figure 20. Four times the conversion ratio SCC

Since  $\omega_{01} = \frac{1}{\sqrt{LC}}$  the switching frequency increase will result to minimization of the passive component size. Essentially the converter is capable of 1MHz switching frequency and the inductor can be an internal part (multilayer trace) of the PCB, having only 10nH or less. The main

board has multiple layers; it is mostly composed of ceramic capacitors and low voltage isolated auxiliary power supplies. The number of modular boards with GaN FET switching devices depends on the conversion ratio of the converter. For the converter shown in Figure 21, two half bridge and two double switch modular boards are used. The control circuit and the low power auxiliary power supplies are located on the top and back sides of the main board and are fully isolated from the high voltage side. Digital signal processing controller provides the individual eight signals to each switch and it is located externally on another board which will be shown in further sections. Main board receives the gate control signal and the signal is bypassed through the CPLD.

### 3.2. Modular Hardware Design

As mentioned previously the main board is composed of four modular boards that will be examined in detail in this section. The design and the functionality of half bridge and the double switch module will be shown in this section.

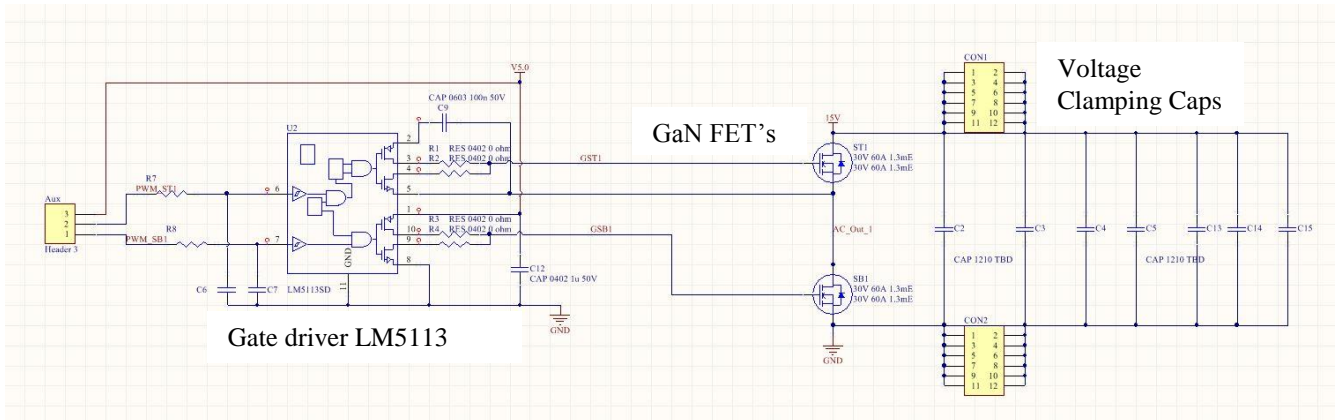


Figure 21. Half bridge schematics

The half bridge schematics is very simple in structure and is shown in Figure 22. Looking from the left auxiliary connector provides the low voltage power supply and two PWM signals for the top and bottom GaN FET's respectively. For the proper switching device operation, the gate driver is configured to work as a bootstrap. This means that the top and the bottom device VGS

has the same value. Right side of the schematic shows the switching devices and the main power input connectors.

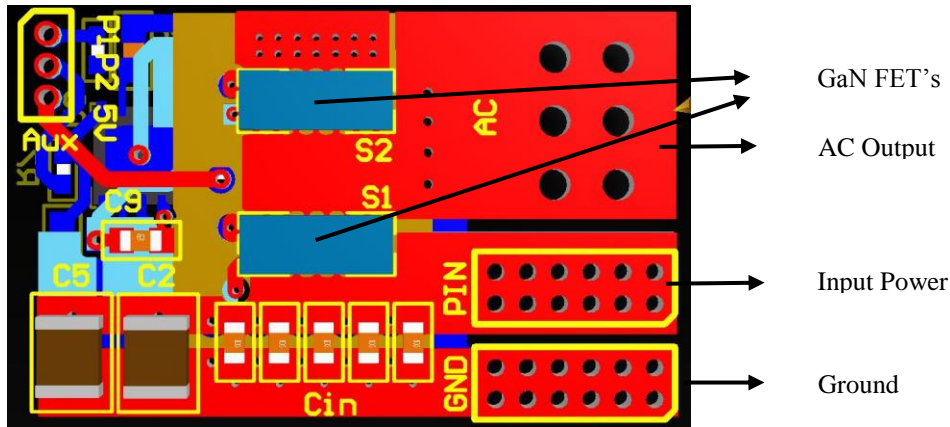


Figure 22. Transparent 3D image with all four layers turned on

Figure 22 displays the finished four-layer 3D half bridge printed circuit board designed in Altium Designer with all the components on the board. As shown, the switching devices and the voltage clamping capacitors are located on the top of the board. Moreover, the gate driver and the charge-discharge gate resistors are on the bottom side and they are connected to the devices gate by VIA's. The reason for the gate driver being on the bottom is to increase the power density of the board and, it becomes much easier to solder the rest of the components. During the assembly of the switching devices if the switch was too close to the gate driver and the hot air gun is used, the gate driver solder will melt and move the gate driver from its pads. By correctly inserting the gate driver on the back-side solder melting problem was eliminated. Furthermore, the entire board can be placed on the aluminum or a copper sheet that is at least 1/3 inch of thickness. The bottom side of the board will dissipate the heat in to the aluminum plate and this way the PCB is not overheated. This method assures that the gate driver stays in place while the devices are being soldered. The assembly of the rest of the modular and main boards is explained in further chapters.

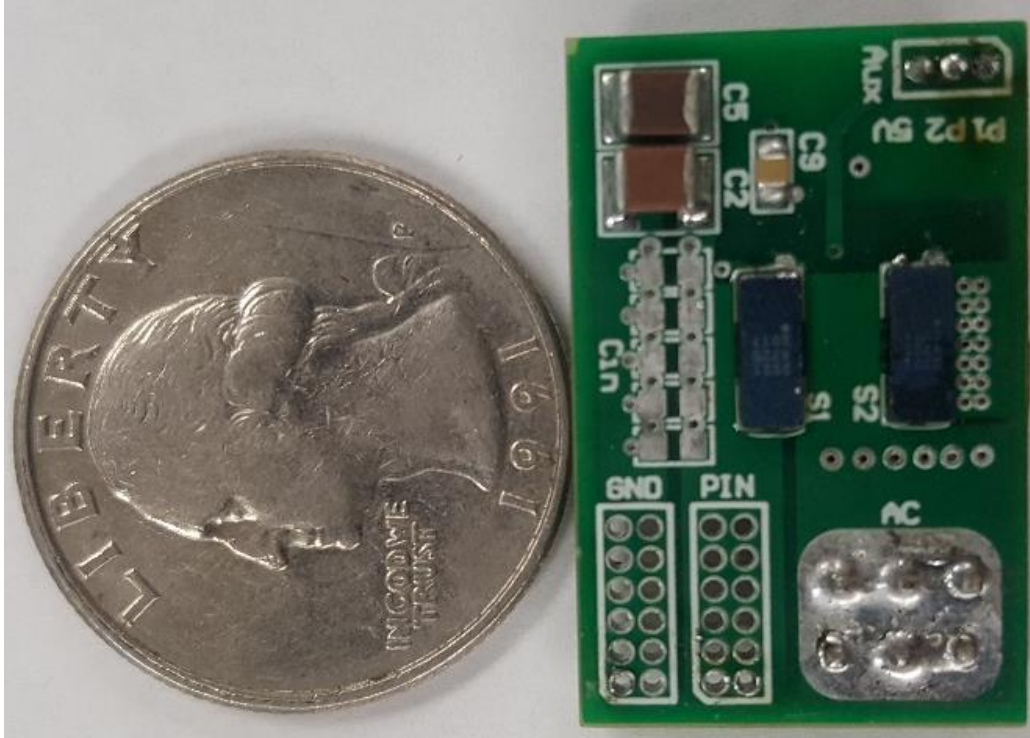


Figure 23. Half Bridge module assembled

### 3.3. D-Switch Module

Figure 20 shows the 4x converter and the wing side switching devices (circled in red).  $S_{T3}$  and  $S_{B4}$  are located on the top side of the converter while  $S_{B3}$  and  $S_{T4}$  are on the bottom. D-switch module contains two switching devices and it can be interchanged. This means that same module can take the place for  $S_{T3}$ ,  $S_{B4}$  or  $S_{B3}$ ,  $S_{T4}$ .

Since the switched devices are located on the wing side of the converter their source pin is not in respect to ground. Furthermore, individual switching device gate driver is equipped with digital isolator that is on the same board and its own isolated power supply that is located on the main board. This previously mentioned configuration allows the gate driver to work correctly and provide the correct gate signal to the individual switch. The module is composed of gate drivers,



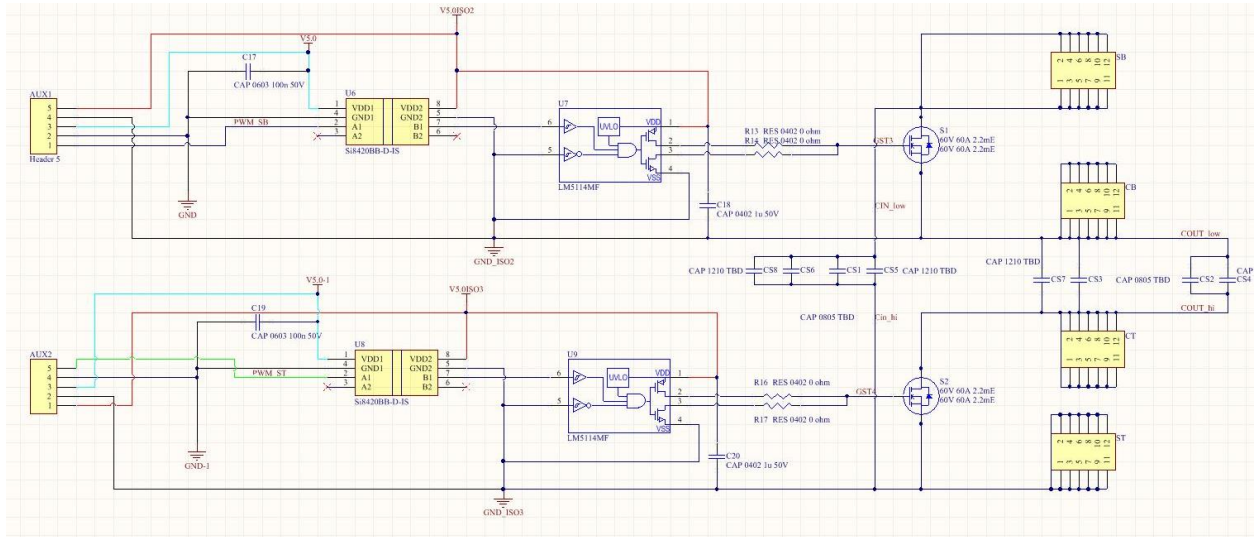


Figure 24. Double switch schematic

digital isolators and two EPC2020 60V<sub>DS</sub>, 90A I<sub>D</sub>. Another interesting fact is that the size of the device is 6.05mm x 2.3mm. The same PCB software is used as for the half bridge to design and optimize the D-switch module. Figure 25 shows the module with all components assembled and tested. Assembled Board Left to right: isolator, gate driver, switch, source and drain connectors.

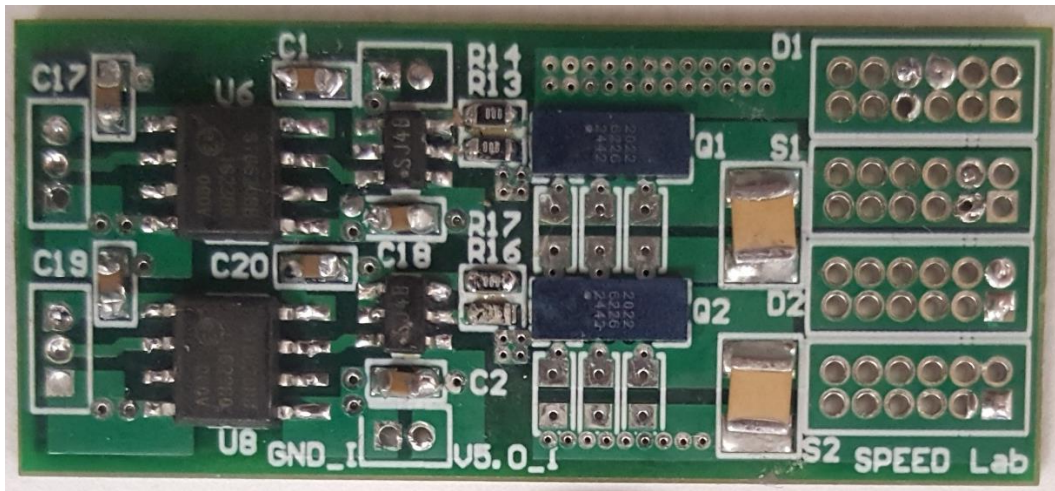


Figure 25. D-switch module

### 3.4. D-Switch Functional Test

Purpose of the test is to make sure that all individual boards are working and are assembled properly before they are joined together on the main circuit. The PCB was placed to the breadboard and small wires were inserted to interconnect the PCB to the breadboard. 5V power supply and 5V isolated power as well as the ground was connected to the board. Gate signal was provided and the resistance across the S-D switched from INF to 0.1 Ohm. This showed that the control for the switching device including the isolator and the gate driver worked as it supposed to. Furthermore, it means that the switch is attached to the PCB correctly.

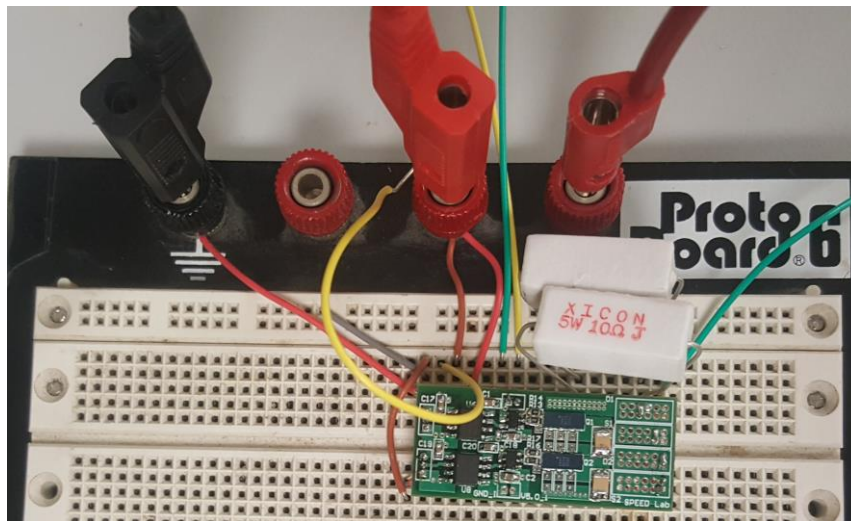


Figure 26. Module test setup

Due to the thin wires and the breadboard setup the current was only pushed to 2.7A. The main goal was to test if the board works before it is docked to the main board. Another important fact is that the switches are extremely difficult to solder by hand. There are many methods for the switch attachment that are recommended by the manufacturer. However; method developed here is based on using correct amount of flux and the air gun time and temperature settings. Main types of failure are caused by the characteristic that the switch must be position exactly inside the overlay line, otherwise it is guaranteed that the device is not going to operate. Moreover, it is more than

likely that the source and drain are soldered together and the short circuit will destroy the switch and possibly other components on the board. The air gun temperature that works the best is 300C and the flow rate is set to 28. The air gun should be positioned 5mm above the device while soldering.

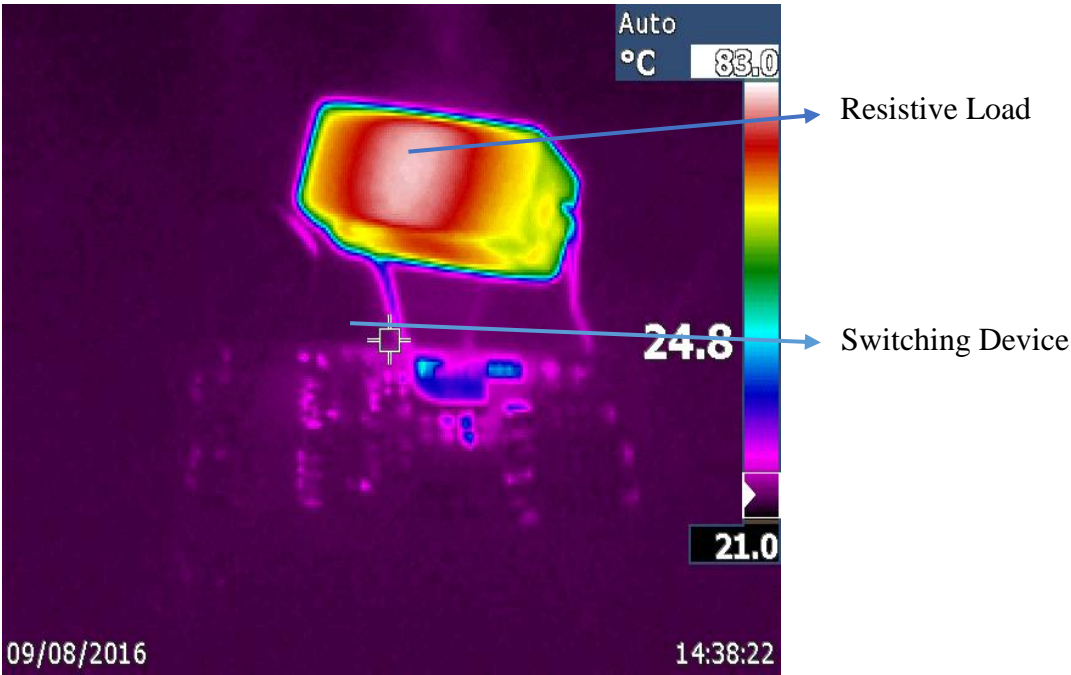


Figure 27. Thermal test

Figure 28 shows the module test under the load and the image has been taken with the thermal camera. The test was performed with total power being 35 W due to the thin wires and the limited power supply. The GaN switching device is operating at the room temperature and the resistor is glowing at 83°C. Entire board including the resistors and the capacitors are also operating at the room temperature.

**3.5. Main Board and the Complete 4X Conversion Ratio Hardware**

Main board is composed of one full bridge and two D-switch modules. All of the modules are connected to the main board via 12 pin 50 mil spaced connectors. The idea behind the design is mainly because the modules can be replaced instead of trying to replace the switch by hand,

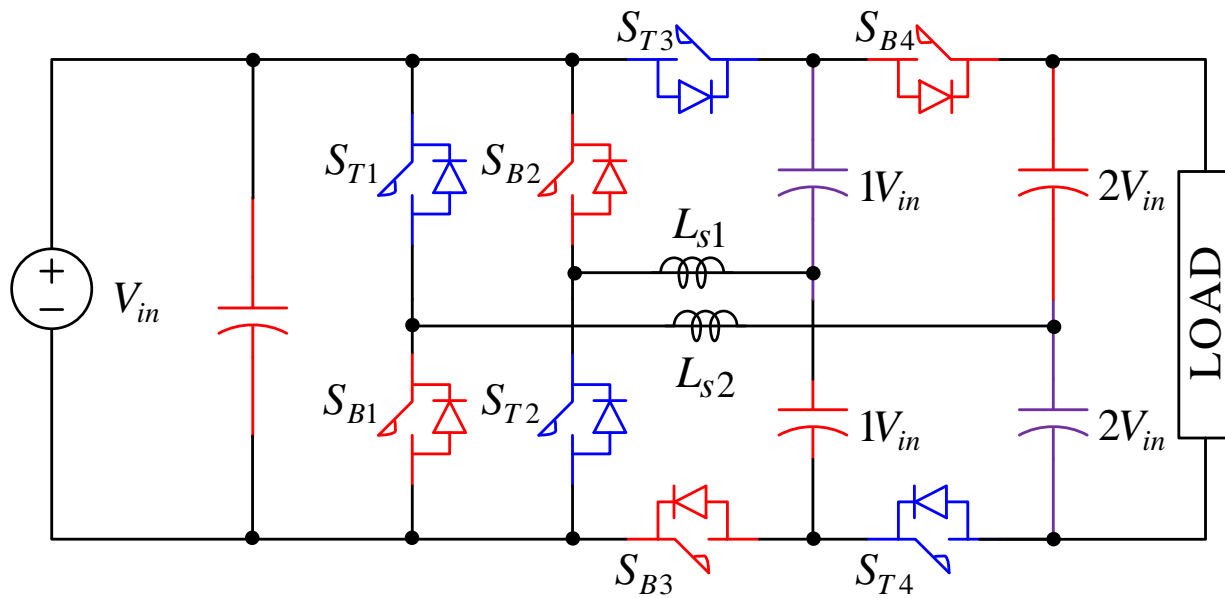


Figure 28. 4X conversion ratio schematic

which can be extremely challenging. Main board is composed of four layers and the copper weight is 1oz (1 ounce of copper spread out to an area of 1 square foot). The weight of the copper controls the amount of current capability; however, it can impact the design in many ways. Increased copper thickness increases the clearance between the traces and minimum widths of the annular rings. Main board is virtually split in two parts, low voltage (auxiliary power supplies, digital isolators, control, 5V supply etc.) and high voltage (resonant capacitors, inductors and connectors).



Figure 29. Front and back side

As it can be seen in Figure 30 the full-bridge is located on the left side of the converter and the wing side is next to the inductors on the right. The back-side contains capacitor banks and auxiliary power supplies (needed for the wing side GaN FET operation). The first obstacle in the way was to assemble the switches and test the modular boards. The second was to program the CPLD and obtain the correct PWM synchronization including the dead time. The code for the PWM generation occupied 60% of the memory alone. By adding the code for the dead-band control the CPLD Macro-cells used were 100% and at that point it was clear that the CPLD can't accomplish the job on its own. The DSP connector was already built and the PWM was controlled externally. CPLD input and output pins were programmed as bypass and the entire control code was written by using DSP.

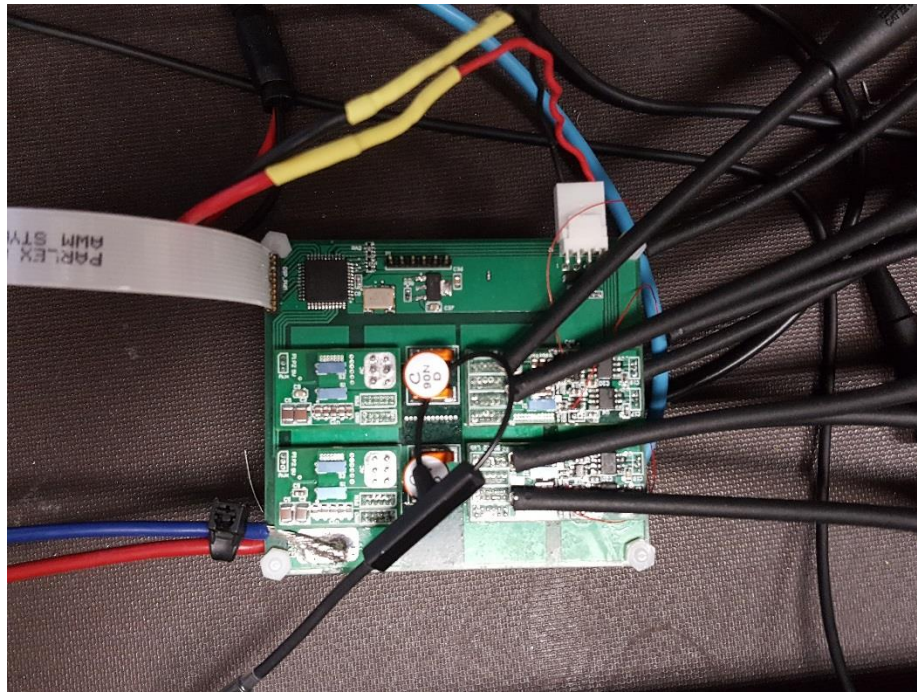


Figure 30. Assembled converter

Figure 30 shows the assembled converter prior to testing. Blue and red wire leads are the input power to the converter. The output is located on the back side of the board. Ribbon cable is used for the external DSP control and the rest of the wires are current probes and the differential

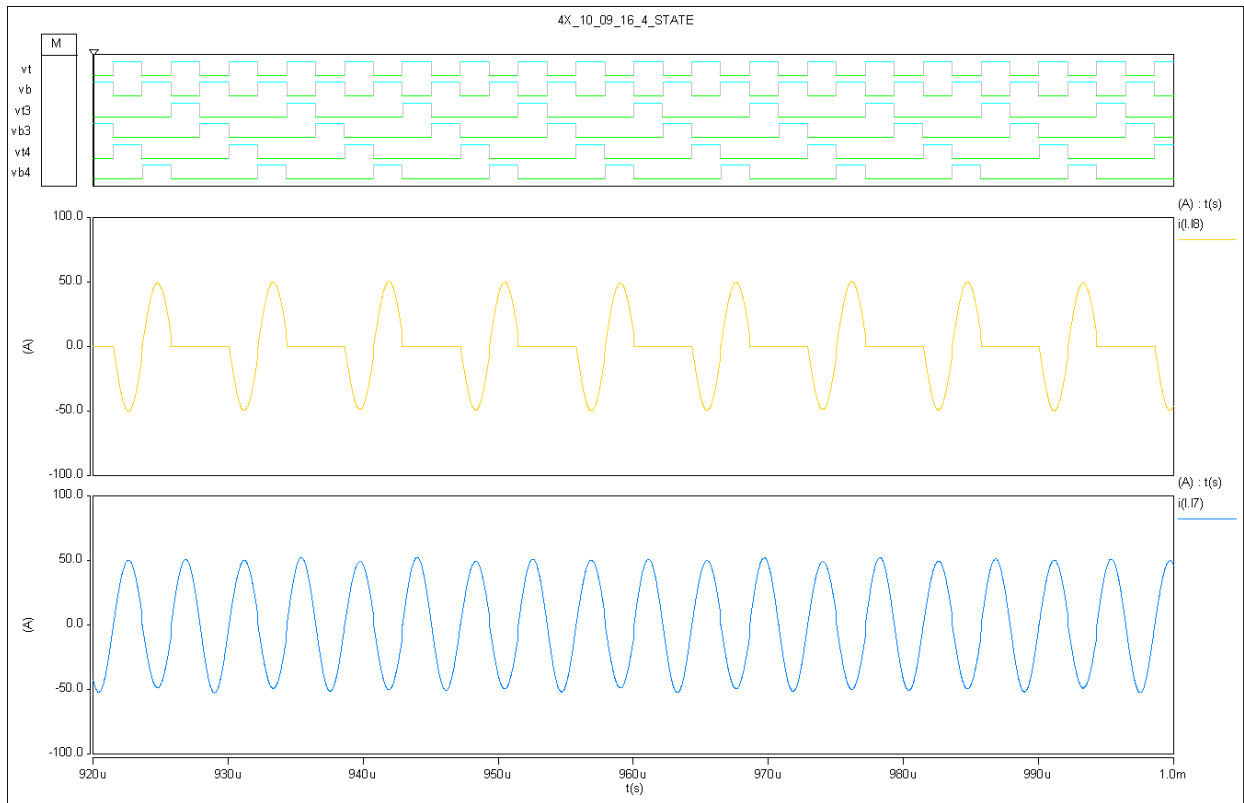


Figure 31. Inductor currents

probes. For the converters first run the voltage and current will be set at low values, approximately 2 or 3 watts. The reason for it is to make sure that the control is correctly synchronized and the GaN FET's are operating correctly. Utilizing only few Watts of power also assures that the resonant operation and zero current switching is accomplished without stressing the devices. Furthermore, the resonant frequency can be fine-tuned if the tolerance of the capacitors and the inductor is out of nominal range. After the current waveform through the inductors  $L_{S1}$  and  $L_{S2}$  is obtained it can be determined if the frequency has to be lowered or increased. Another possible way is to change the value of the capacitor or the inductor to match the resonant frequency. However, this is not as convenient as changing the period value and compiling the DSP c-code. Four state control method in Figure 2 was programmed for the converters first run. The control PWM train pulse can be also seen in the image below which was simulated in SABER simulator.

Table 2. Passive component specifications

Input Capacitance:	Resonant Capacitors	Inductor values	Switching Frequency
$94\mu F$ (X7R)	$5.17\mu F$ (COG)	Colicraft Air Core	$f_{sw}=233kHz$
$20*4.7\mu F$	$11*0.47\mu F$	$LS1,LS2=90nH$	

Bill of Materials					
Bill of Materials For PCB Document [Main_9_2_16.PcbDoc]					
Source Data From:		Main_9_2_16.PcbDoc			
Project:		Main Board			
Variant:		1.1			
Creation Date:		10/11/2016 7:40:33 PM			
Print Date:		42654 42654.82106			
Footprint	Comment	LibRef	Designator	Description	Quantity
CAPC1608N	CAP 0603 100n 50V	CAP 0603 TBD	C1, C3, C4, C5, C6, C7	CAP 0603 TBD	6
CAPC1608N	CAP 0603 10u 10V	CAP 0603 TBD	C2, C8	CAP 0603 TBD	2
CAPC3225N	CAP 1210 TBD	CAP 1210 TBD	C5V, C5V1	CAP 1210 TBD	2
CAPC1608N	CAP 0603 10n 50V	CAP 0603 TBD	C33	CAP 0603 TBD	1
CAPC2012N	CAP 0805 10u 16V	CAP 0805 TBD	C34, C35, C36, C37	CAP 0805 TBD	4
CAPC1608N	CAP 0603 2.2uF 30V	CAP 0603 TBD	C39, C42, C45, C48, C51, C54, C57, C60	CAP 0603 TBD	8
CAPC1608N	CAP 0603 1uF 30V	CAP 0603 TBD	C43, C49, C55, C61	CAP 0603 TBD	4
CAPC1005N	CAP 1210 TBD	CAP 1210 TBD	CI1, CI2, CI3, CI4, CL3, CL4, COH, COL	CAP 1210 TBD	8
4-SMD (DFN)	OSC 50.0000MHZ 3.3V	CWX813	CO1	OSC 50.0000MHZ 3.3V +25PPM SMD	1
SOD-123	TVS Diode 7V	TVS Diode TBD	D1	TVS Diode TBD	1
LED1608N	LED	LED	D2	LED	1
8X	Header 8	Header 8	DSP_PWM	Header, 8-Pin	1
RES1608N	Fuse 0603	Fuse 0603	F1, F2	Fuse 0603	2
Half_Bridge	Half_Bridge	Half_Bridge	H1, H2	Half_Bridge	2
KK 7478 RA 4	KK 7478 RA 4POS	KK 7478 RA 4POS	J1	1x4 Locking Header	1
1212VS_IND	1212VS-66n	Inductor	L1, L2		2
Double_Switch	Double_Switch	Double_Switch	M1, M2	Double_Switch	2
HDR1X6	PROGRAM_CPLD	Header 6	P1	Header, 6-Pin	1
RES1608N	RES 0603 2k ohm	RES 0603 TBD	R31	RES 0603 TBD	1
RES1608N	RES 0603 0 ohm	RES 0603 TBD	R38	RES 0603 TBD	1
RES1608N	RES 0603 10k ohm	RES 0603 TBD	R42, R43, R46, R47, R50, R51, R54, R55	RES 0603 TBD	8
EXB38V	EXB38V 0 ohm	EXB38V	RA2	EXB38V 0603*4 TBD	1
EXB38V	EXB38V 100K	EXB38V 0603X4 TB	RA3	EXB38V 0603X4 TBD	1
VQ44_L	XC2C32A-4VQ44C	XC2C32A-4VQ44C	U1	CoolRunner-II 1.8V, 32 Macrocell CPLD, 33 K	1
SOT-223-6	TPS79633DCQ	TPS79633	U3	Single Output LDO, 1.0A, Fixed(3.3V), Low N	1
SOT223-4	TLV117118 REG LDO S	TLV1171XX REG L	U5	TLV1171XX REG LDO SOT223-4	1
DVB12	DCR010505_DVB_12	DCR010505_DVB	U24, U26, U28, U30	Imported	4
					68

Figure 32. Bill of materials

Table 2 and Figure 32 include complete bill of the materials and part numbers used for the double wing four times the conversion ratio converter prototype. The board was assembled by

hand using soldering iron, heat gun station and the microscope. Low power supplies and the controlled circuit was assembled first. Low power diagnosis and the troubleshooting was the next step, making sure that all of the control signals and the power supplies operate correctly before tuning on the converter. Furthermore, the final step was installation of the capacitors, inductors and the modular boards.

Another advantage of using DSP is that each PWM signal can be programmed separately, meaning that each signal can have individual dead-band control and it can also be phase shifted if needed. Figure 33 shows all of the control signals captures at the gate of each device. After the control signal is collected the input power can be turned on and slowly increased to few watts. The next step is to measure the inductor current and confirm that the resonant operation (ZCS) is accomplished. If the current waveform is not purely sinusoidal it means that the switching frequency have to be reprogrammed.

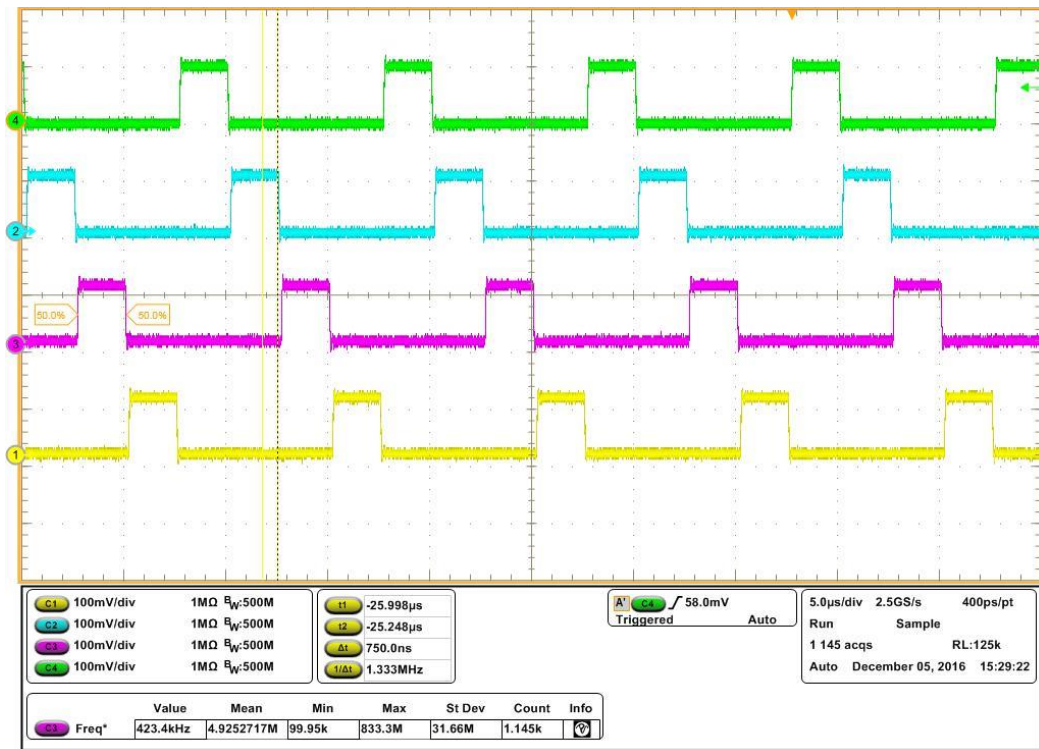


Figure 33. PWM at the gate of each GaN FET



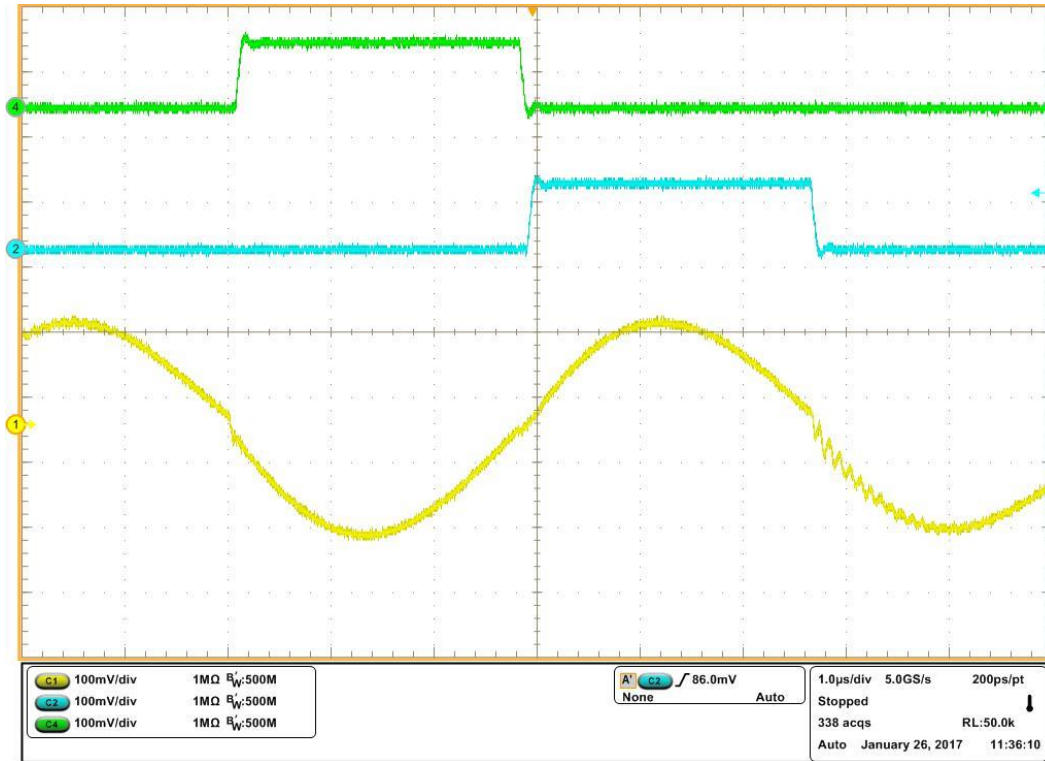


Figure 34.  $L_{S1}$  Inductor Current

Figure 34 shows the current through the inductor  $L_{S1}$  and it can be noted that the switching frequency needs an adjustment. The sine wave is distorted and is also chopped right after the first half cycle at the zero point. The dead time setting for the first run was set to 70ns and needs to be decreased since too much dead-time resulted in chopped waveform. Both of the inductor current waveforms can be compared to the simulation in the Figure 32 and it can be seen that the waveform is identical. After the dead time was decreased to 50ns the inductor current became fully sinusoidal and it can be seen in the Figure 36. This assures that the switching frequency and the dead time control has been set correctly. Moreover, the converter functionality was confirmed and the final test is to power the converter to moderate power level and test the current capability as well as the thermal performance.

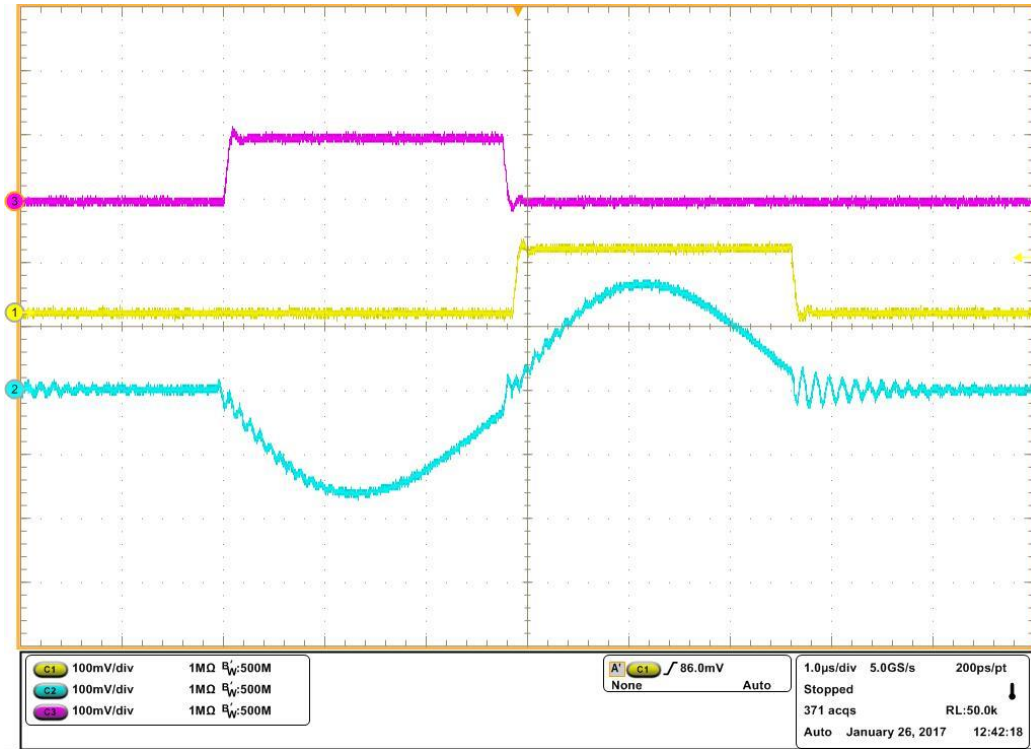


Figure 35.  $L_{S2}$  Inductor current

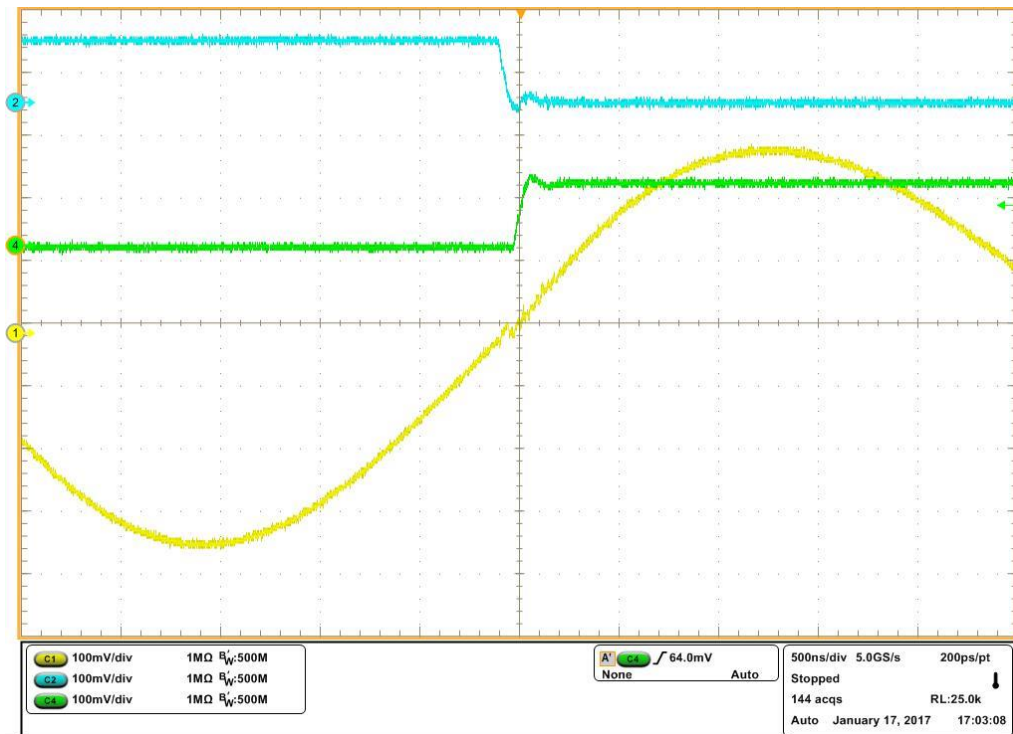


Figure 36. Inductor current (dead time decreased to 50ns)

### **3.6. Summary and the Conclusion**

Even though the resonant operation is accomplished and the converter is operating correctly, limit of this design is the incapability to work at maximum power. Not enough vias next to the switches causes increased copper temperature. This is due to the PCB manufacturer not being able to fabricate micro-vias next to the switches and the copper area is decreased causing temperature to rise fast during the operation. The thermal performance of the converter was not acceptable and measured temperature of the half bridges was 54° Celsius at 60W of power, which is only 10% of the total rated power. The conclusion is that the GaN devices have to be placed on 2 OZ copper instead of 1OZ and that multiple micro-vias are needed together with multiple layers to be able to support rated current and minimize the  $I^2R$  Losses.

## 4. DWSCC VERSION II

### 4.1. Schematic Improvements

For the version 2 the schematic is modified and the current stress on the GaN FET's and the passive devices is reduced. As it can be seen in the Figure 37, the converter has additional half bridge. The resonant capacitors  $C_1$  and  $C_2$  are individually charged by one bridge. The number of high frequency current loops has been minimized as well and it will be explored in detail later on in this chapter.

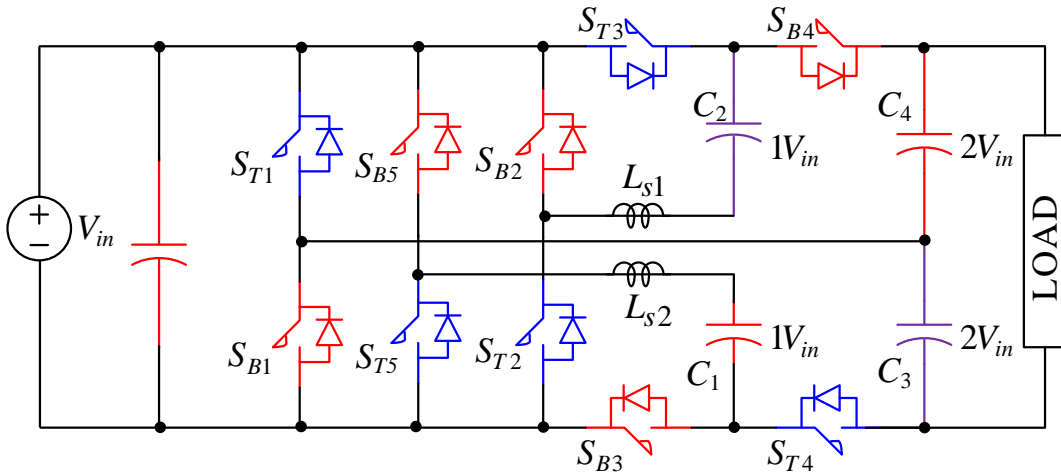


Figure 37. Improved schematics

The converter features two inductors  $L_{S1}$ ,  $L_{S2}$  two resonant capacitors  $C_1$ ,  $C_2$  and two non-resonant capacitors  $C_3$  and  $C_4$ . This topology permits the resonant inductor and the capacitor to change places if needed. This feature is useful in the PCB layout optimization. The non-resonant capacitors  $C_3$  and  $C_4$  are around 10 times larger in value and will not affect the resonant frequency by much. If switching frequency is set to be 520 kHz and the non-resonant capacitor value is 30uF by using equation (37) ~ (39) the resonant capacitor values can be calculated in the following manner:

$$\frac{1}{C_T} = \frac{1}{(C_{NR} + C_R)} \quad (37)$$

$$f_{sw} = \frac{1}{2\pi\sqrt{LC}} \Rightarrow f_{sw} = \frac{1}{2\pi\sqrt{(L)\frac{1}{\frac{1}{C_{NR}} + \frac{1}{C_R}}}} \quad (38)$$

$$520kHz = \frac{1}{2\pi\sqrt{(36nH)\frac{1}{\frac{1}{(30\mu F)} + \frac{1}{C_R}}}} \quad (39)$$

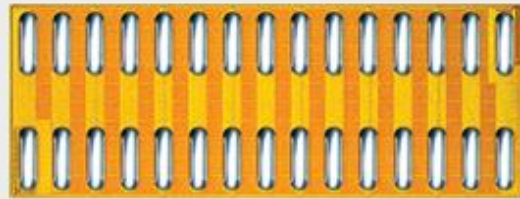
$$\Rightarrow C_{NR} = 30\mu F, C_R = 2.84\mu F.$$

The plan is to have at least 6 for each resonant capacitors on the board (6\*470nF for the  $C_1$  and 6\*470nF for the  $C_2$ ).The Switching devices remain the same as in the previous converter EPC2020 for the low side and the EPC2022 for the wing side GaN FET's.

### EPC2020 - Enhancement Mode Power Transistor

### Low Side

$V_{DS}$ , 60 V  
 $R_{DS(on)}$ , 2.2 m $\Omega$   
 $I_D$ , 90 A  
 Pulsed  $I_D$ , 470 A  
 $T_J$ 150°C  
 RoHS 6/6, Halogen Free

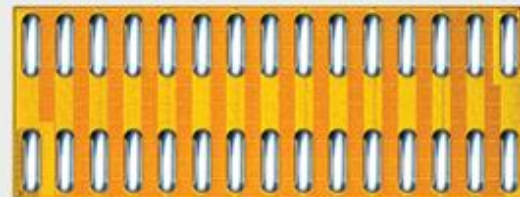


Die Size: 6.05 mm x 2.3 mm

### EPC2022 - Enhancement Mode Power Transistor

### Wing Side

$V_{DS}$ , 100 V  
 $R_{DS(on)}$ , 3.2 m $\Omega$   
 $I_D$ , 90 A  
 Pulsed  $I_D$ , 390 A  
 $T_J$ 150°C  
 RoHS 6/6, Halogen Free



Die Size: 6.05 mm x 2.3 mm

Figure 38. GaN FET's

## 4.2. Simulation

Simulation was completed by using SABER Simulator. The simulation confirms and verifies the theoretical analysis of the converter. Schematic was modified accordingly to the circuit in Figure 37 and the simulation was recreated with correct device parameters such as *ESR* and *RDS*. The control method used this time was two state method shown in the Figure 13 (a). Two state control can be seen on the image below as well. Simulation was performed at maximum power output which is 600W. The simulation shows excellent results and the current stress is reduced by more than half. Figure 42 and figure 43 display all of the high frequency mail loops currents. As it can be seen the non-resonant and resonant capacitor currents are quite low. This allows the converter to achieve maximum power density by reducing the capacitor banks hence, making the converter much smaller. The output voltage is stable at the output of 119.8V and the

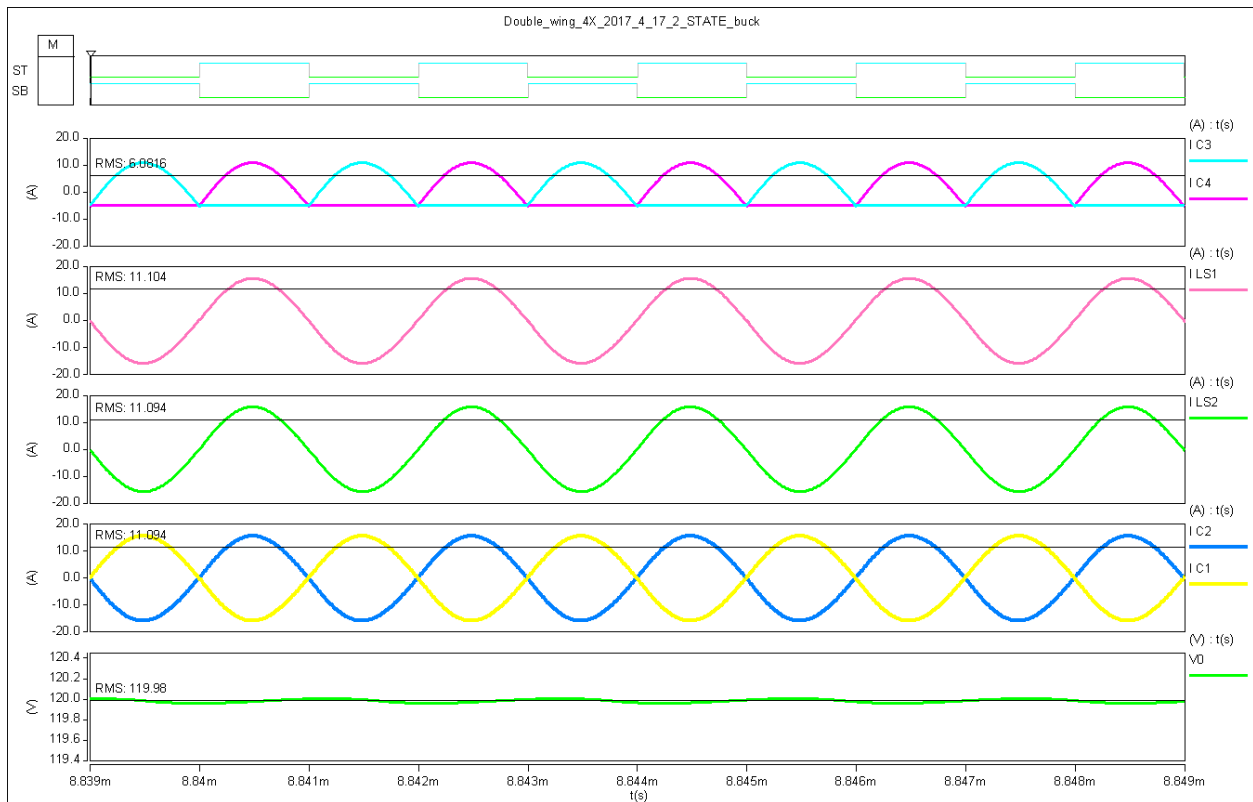


Figure 39. Capacitor and the inductor currents

current ripple is minimized. The major factor for the current ripple minimization is because the capacitors  $C_3$  &  $C_4$  are about ten times larger than the previous design. Figure 39 shows all of switches currents and current stress is only 7.8A for each device.

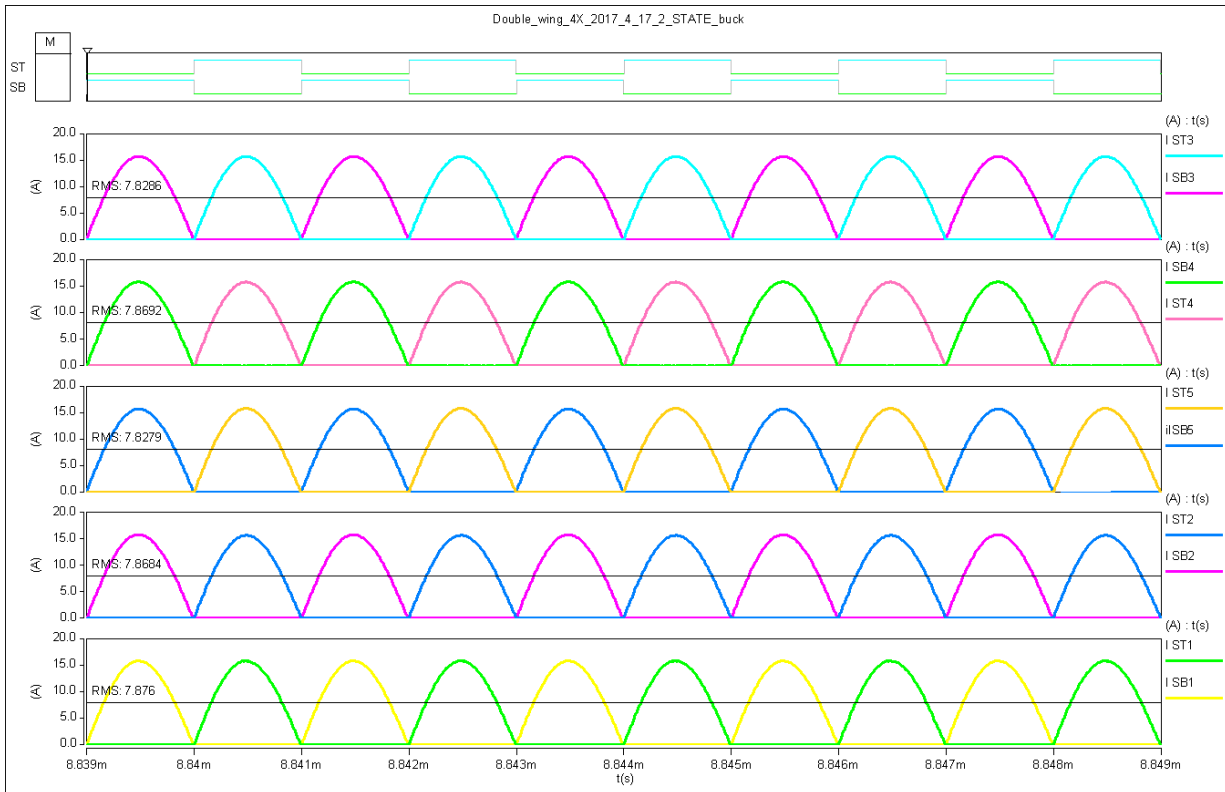


Figure 40. Current stress

### 4.3. Multilayer Design

The converter has to conduct high current through the printed circuit board therefore, the PCB is required to have multiple layers. Switching devices source and drain pads have to be connected to multiple layers in order to distribute high current without effecting thermal performance of the entire board. The devices clearances are very low and the track distance from source to drain is only 5.7mil. This type of device package creates steep design learning curve and also challenges the PCB manufacturer. Not every PCB manufacturer has the equipment to design such boards due to the tight clearances, micro-vias, more than 1Oz copper weight, and multilayer

configuration. In the section it is important to understand why extensive amount of time was dedicated to the printed circuit board design. One among many reasons is the large amount of micro-vias used next to the switching device. The micro-vias are necessary since they distribute the current to multiple layers; however, micro-vias create large number of drill holes which occupy board space. Dense drill holes make the board space unusable for other components. Most important part before the actual layout begins is to properly place the components. Moreover, high frequency current loops have to be optimized to reduce the  $I^2R$  loss. Figure 40 show two main high frequency current loops. The idea behind it is to minimize the loops on the board and the only way to do it is to place the components as close as possible; however, depending on the circuit topology this can be very challenging. Yellow and green loops represent high frequency currents and the signal that control the switches is complimentary. Moreover, by applying the control method two in Figure 30 either blue or red switches are on at the same time. Starting at the  $V_{in+}$  side and following the purple current path it can be seen that current is flowing through switch  $S_{T3}$  capacitor  $C_2$ , inductor  $L_{S1}$ , and the switch  $S_{B1}$ . Referring at the Figure 41 and starting at the  $C_{in}$  the high frequency loop can be followed and it is clear that the physical length of the loop is minimized. Note that the  $L_{S1}$  inductor and the capacitor  $C_2$  have swapped positions and since they are in series this does not affect the resonance. The reason for the change is because the capacitor pad is wider and it provides more area to connect it to the half bridge. Also the inductor current probe holes are in better position. Second green color high frequency current loop can be followed starting at  $V_{in+}$ . The high frequency current is flowing through switch  $S_{B2}$  inductor  $L_{S1}$ , capacitor  $C_2$ , switch  $S_{B4}$ , capacitor  $C_4$ , and switch  $S_{B1}$ . The green loop can be seen on the PCB image and it is evident that the loop is minimized. Furthermore, the left side of the board is symmetric to the right side of the board. Figure 41 shows the loop paths of the right side of the board. Starting at



$V_{in+}$  high frequency current flows through switch  $S_{B5}$ , inductor  $L_{S2}$ , and switch  $S_{B3}$ . As mentioned previously the red loop on the board is the same length as the purple loop on the left side.

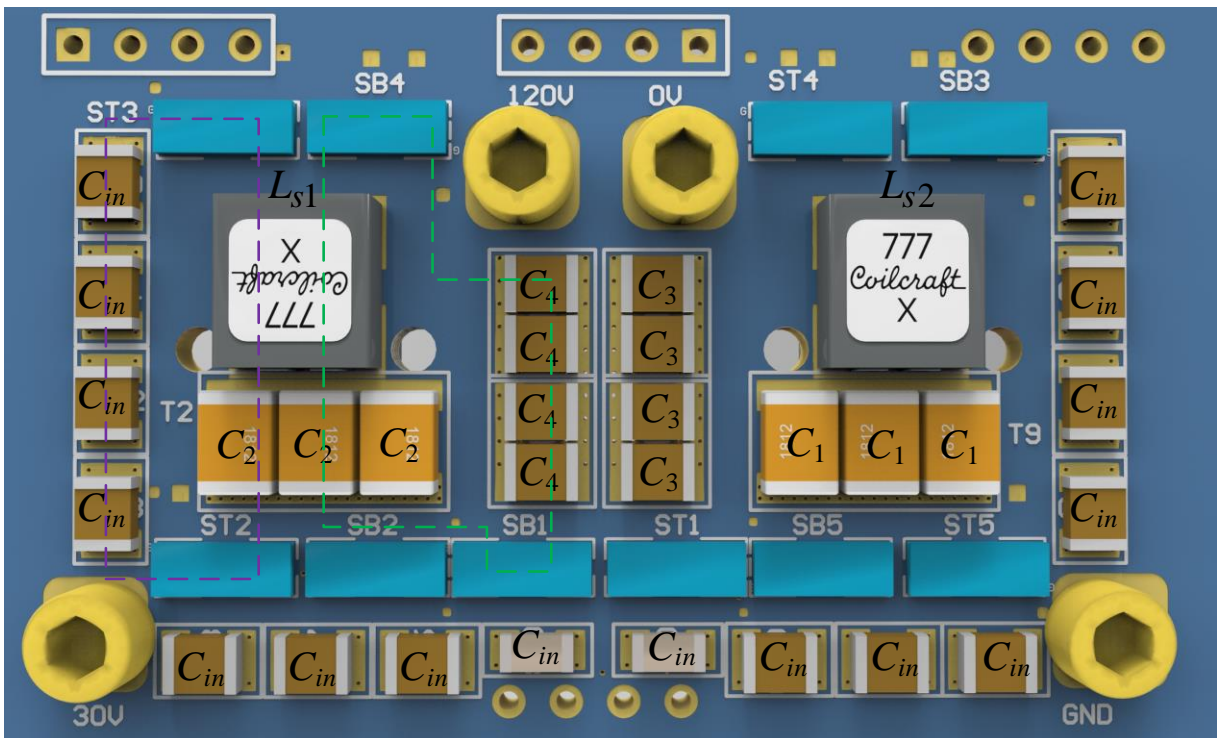
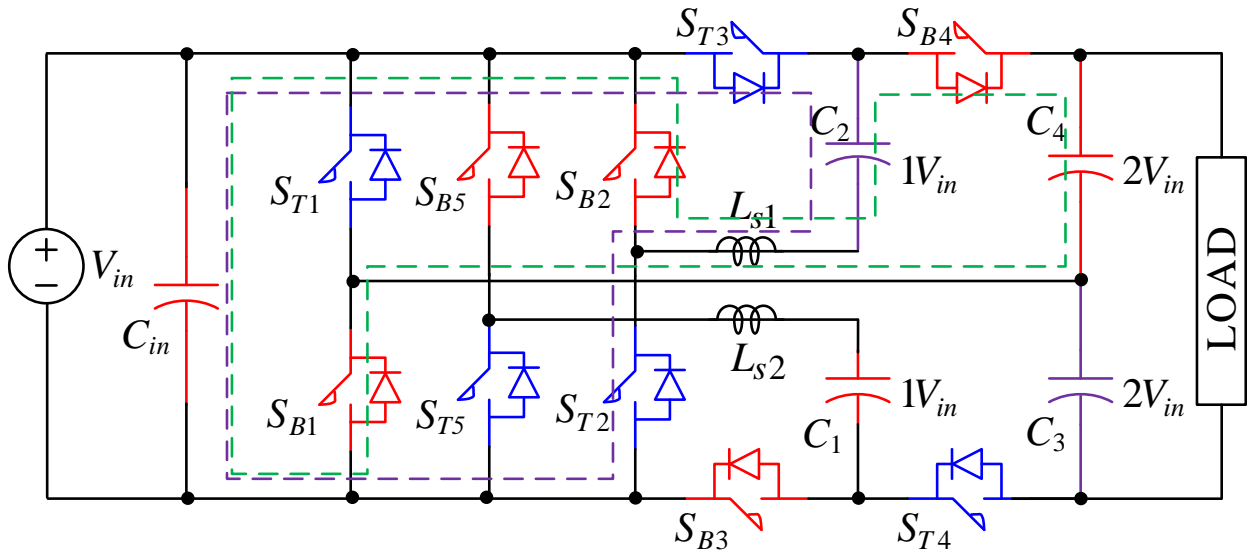


Figure 41. High frequency loops left side

Yellow loop can be followed starting at  $V_{in+}$  and the current flows through switch  $S_{T1}$ , capacitor  $C_3$ , switch  $S_{T4}$ , capacitor  $C_1$ , inductor  $L_{S2}$ , and switch  $S_{T5}$ . Another important part is to isolate the low voltage from the output. All three half bridges are located on the lower portion of the board.

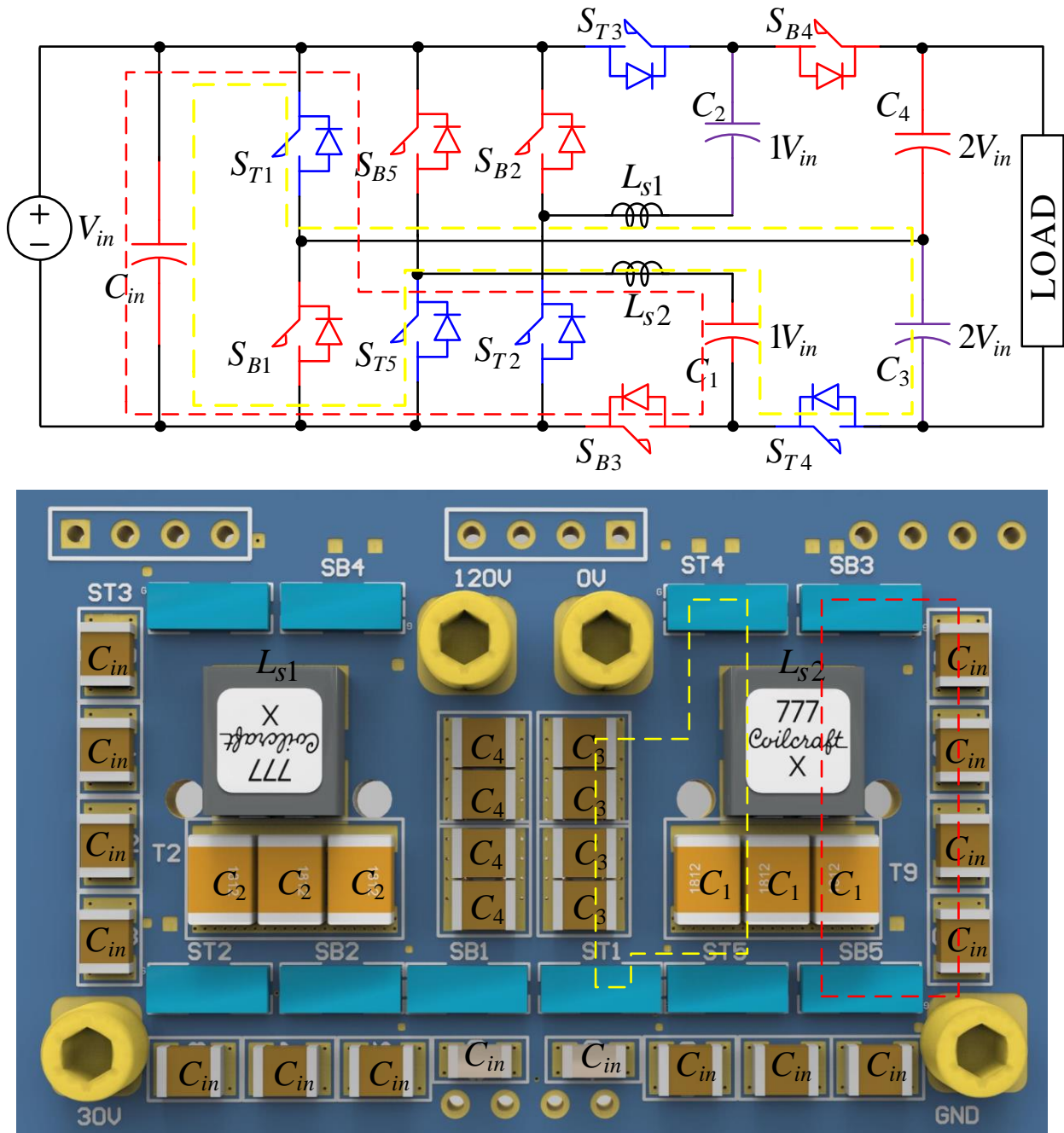


Figure 42. High frequency loops right side

#### 4.4. Efficiency Estimation

Total power loss ( $PT_{loss}$ ) can be estimated by using the following equation below:

$$PT_{loss} = \sum P_{loss\_con} + \sum P_{loss\_coss} + \sum P_{loss\_gate} + \sum P_{loss\_cap} + \sum P_{loss\_ind}$$

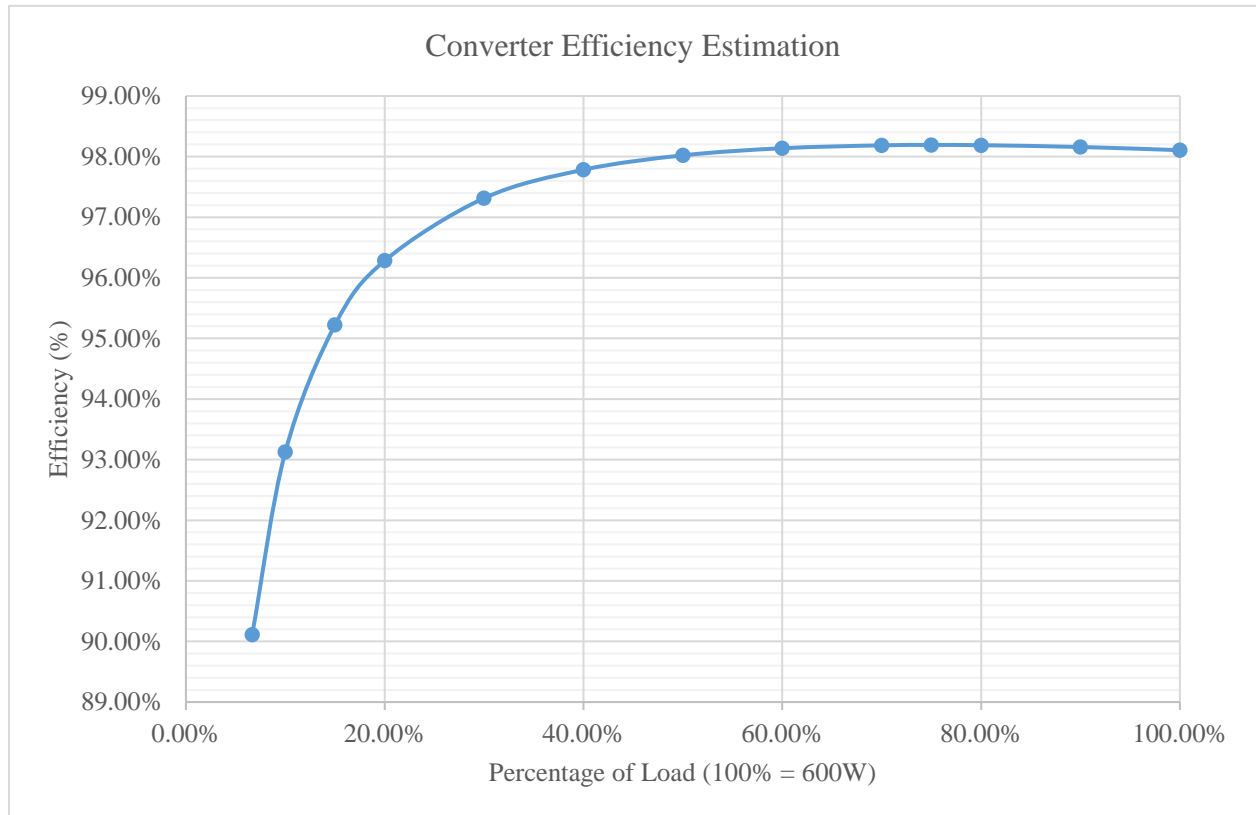


Figure 43. Estimated efficiency

Where:  $P_{loss\_con}$  = mosfet conduction loss,  $P_{loss\_coss}$  = mosfet output capacitance loss,  $P_{loss\_gate}$  = gate charge loss,  $P_{loss\_cap}$  = capacitor ESR loss,  $P_{loss\_ind}$  = Inductor core + inductor DC + inductor AC losses.

The importance of the power losses is directly related to the reliability of the converter. There are number of estimation methods presented in the literature; however, depending on the complexity of the modeled system power losses are usually complicated. For this converter power losses estimation is presented by using not very complicated but accurate estimation method. The

equation estimates the total converter power loss and the efficiency. Estimated efficiency can be seen in Figure 43. The peak converter efficiency including the PCB copper losses at 80% of the load is  $\eta \approx 98.22\%$ .

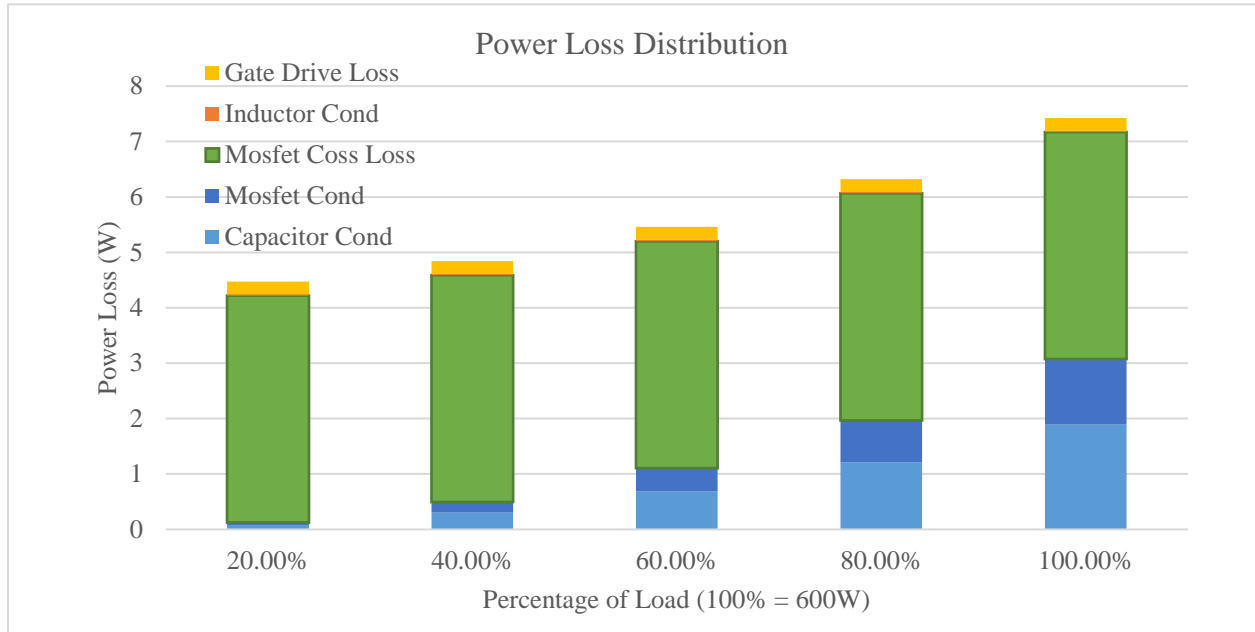


Figure 44. Power loss distribution

As the switching frequency is increased the GaN FET power transistor parasitic parameters need to be defined in the power loss estimation. The value of output capacitance is a nonlinear function that depends on drain to source voltage [12]. Power loss distribution chart shows that the majority of loss is due to the output capacitance of the GaN FET.

#### 4.5. Converter Prototype

Wing side high voltage switches are located on the upper side of the PCB next to the output connectors. The board will have external control and another other docking board that consists of auxiliary power supplies that supply the voltage to the bootstrap and the wing side gate drivers. Docking board also contains the 5V supply for the low side half bridges gate drivers. Docking control board will be connected to the main board from the bottom side. Even though the converter needs only two inductors the prototype will have four inductors since there is enough space on the

bottom of the board. It means that  $L_{S1}$  &  $L_{S2}$  will have an additional optional inductor in parallel.

Figure 44 and Figure 45 show the finished top and bottom side of the converter prototype.

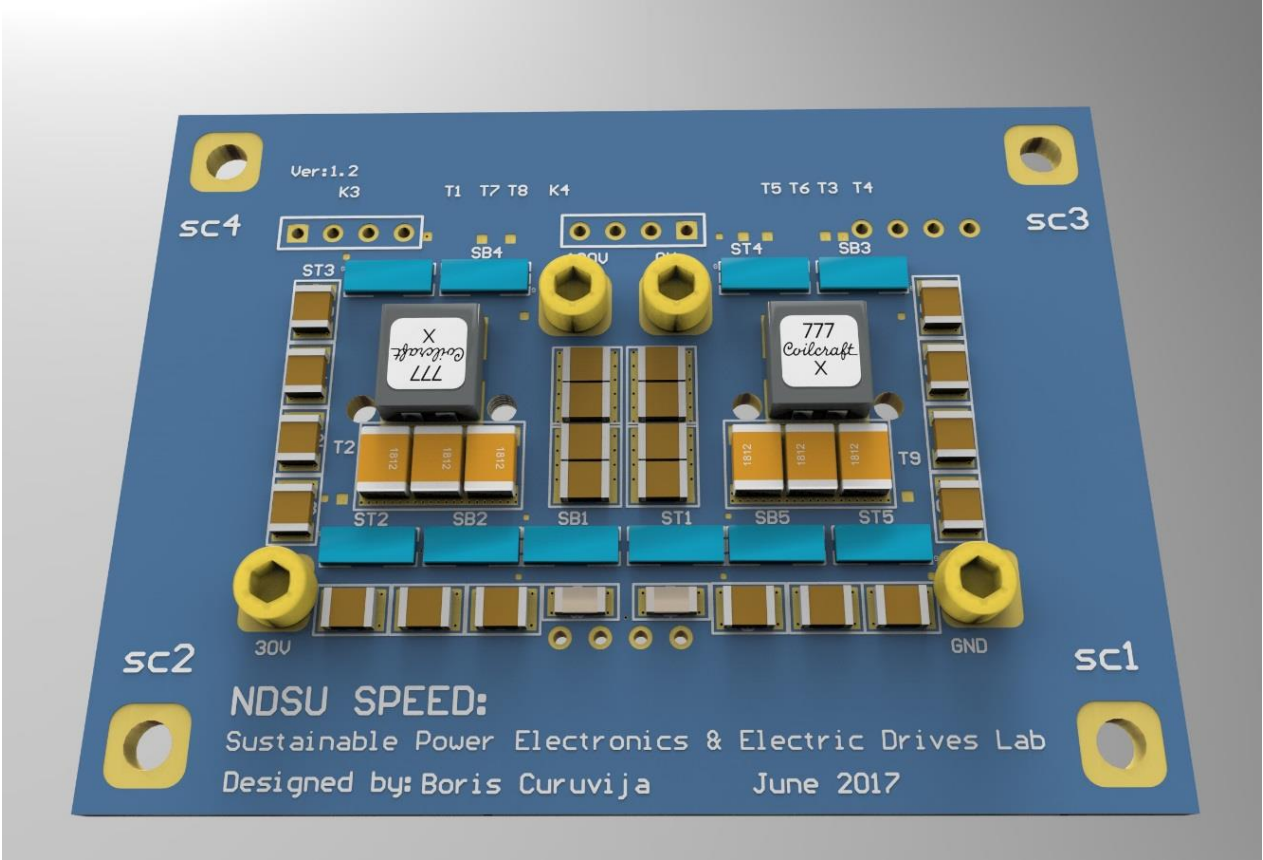


Figure 45. Converter prototype front

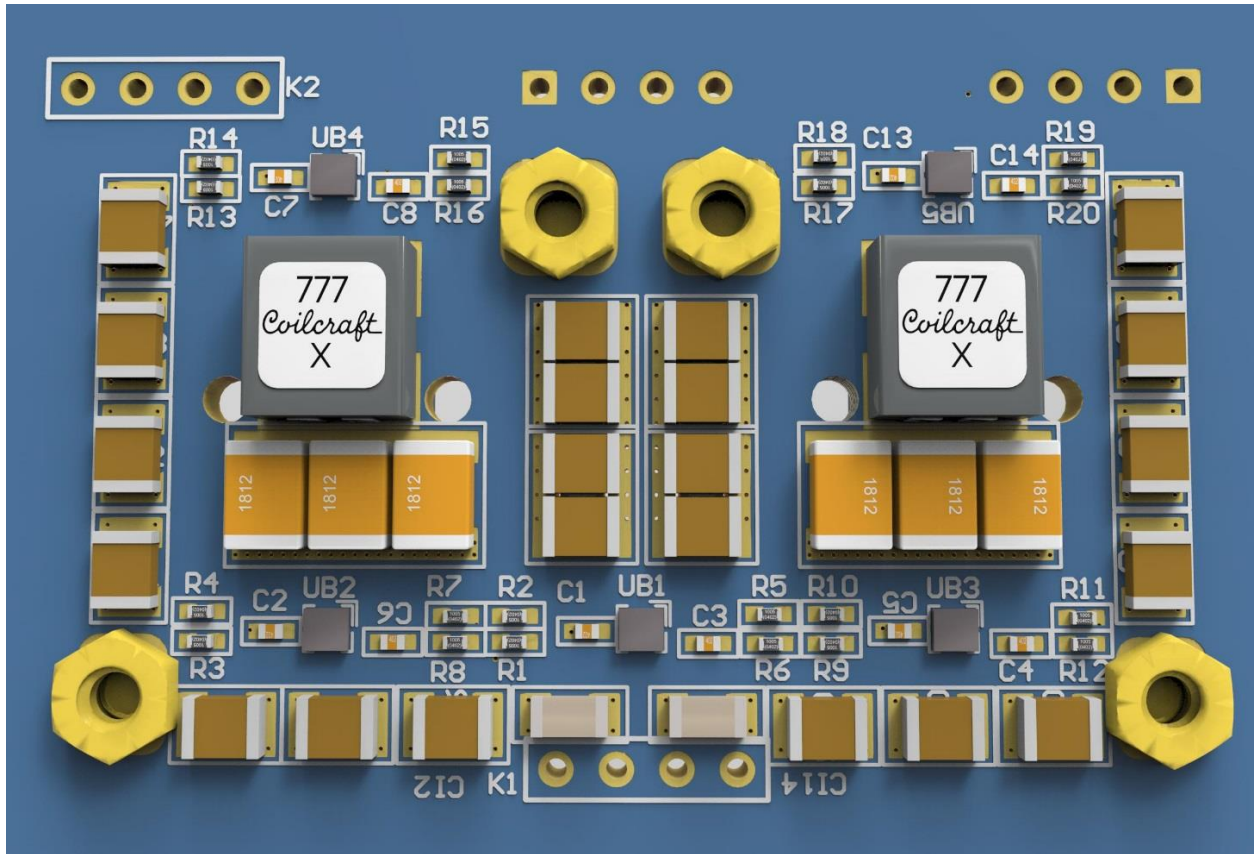


Figure 46. Converter prototype back

## 5. CONCLUSION

In this thesis multiple switched capacitor converters are shown and analyzed. The majority of work is related to the four times the conversion ratio double wing switched capacitor dc-dc converter. The converter design steps and individual module design are explained in detail. Large portion of the research focus is dedicated to high power density multilayer design. This type of design has to be carefully analyzed and peer reviewed due to the complexity of multilayer boards and manufacturing challenges. In this thesis two different designs were explained and shown. Modular converter design shows to have benefits as far as board structure simplicity and easier troubleshooting. Moreover, according to the experimental data and the thermal performance of the modular design it is concluding that modular design has disadvantages. It is difficult to drive large amount of current through the connectors and the connectors can be redesigned or as shown in the second version, connectors are removed and high power switches are placed on one board. Second design is superior and the power density is pushed to the limit. High frequency current loop optimization minimizes the converter losses and it is very important element of high power density design. Beyond shadow of doubt it is shown that is possible to construct high switching frequency and high power density switched capacitor dc-dc converter and reach 98% or higher efficiency. Superiority of GaN switching devices and thermally stable ceramic capacitors enables the converter to work in harsh environment and makes it suitable for variety of applications.

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## APPENDIX. DIGITAL SIGNAL PROCESSING CODE THAT IS USED TO CONTROL THE PWM SIGNALS

```
#include "DSP28x_Project.h"    // Device Headerfile
#include "stdio.h"
#include "math.h"
#include "string.h"

#define Period_FB 425//375=200kHz    150M/(fs*2)
#define Duty_FB 212//364

#define Period_SB 850//750
#define Duty_SB 212//187

#define Dead_time 11    // 1 = 6.667ns

/*
#define Period_FB 872//859
#define Duty_FB 364//364

#define Period_SB 1718
#define Duty_SB 1223

#define Dead_time 20    // 1 = 6.667ns

#define Phase_1 0
#define Phase_2 0
*/

// Global variables used in this example

int timer = 0;
int mode = 0;
int n = 0;
float modulation_ref = 0;
float test2[1000];
int n_test2 = 0;

// Prototype statements for functions found within this file.
void GPIO_CONF (void);
void PWM_CONF(void);
void ADC_CONF (void);
interrupt void adc_isr(void);
void Sample1000 (float sample);
void Modulation_ref_saturate (float i);
void ALL_PWM_OFF(void);
void ALL_PWM_ON(void);

void main(void)
{
```

```

// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP2833x_SysCtrl.c file.
    InitSysCtrl();

// Step 2. Initialize GPIO:
// This example function is found in the DSP2833x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
// InitGpio(); // Skipped for this example

// For this case just init GPIO pins for ePWM1, ePWM2, ePWM3
// These functions are in the DSP2833x_EPwm.c file

    GPIO_CONF();
    //InitEPwm1Gpio();
    //InitEPwm2Gpio();
    //InitEPwm3Gpio();
    //InitEPwm4Gpio();
    //InitEPwm5Gpio();
    //InitEPwm6Gpio();
// Step 3. Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP2833x_PieCtrl.c file.
    InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
IER = 0x0000;
IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example. This is useful for debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
    InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
EALLOW; // This is needed to write to EALLOW protected registers
PieVectTable.ADCINT = &adc_isr;
EDIS; // This is needed to disable write to EALLOW protected registers

// Step 4. Initialize all the Device Peripherals:
// This function is found in DSP2833x_InitPeripherals.c
// InitPeripherals(); // Not required for this example

EALLOW;
SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
EDIS;

```

```

PWM_CONF();

EALLOW;
SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
EDIS;

// Step 5. User specific code, enable interrupts
// Initialize counters:

// Enable CPU INT1 which is connected to ADC INT:
IER |= M_INT1;

// Enable EPWM INTn in the PIE: Group 3 interrupt 1-3
PieCtrlRegs.PIEIER1.bit.INTx6 = 1;

// Enable global Interrupts and higher priority real-time debug events:
EINT; // Enable Global interrupt INTM
ERTM; // Enable Global realtime interrupt DBGM

ADC_CONF ();

// Step 6. IDLE loop. Just sit and loop forever (optional):
for(;;)
{

}

}

void PWM_CONF(void)
{
//-----PWM1 Initialization, PWM1 is used to drive ST3 Switch-----//
EPwm1Regs.TBCTL.bit.PRDL = TB_IMMEDIATE; // set Immediate load
EPwm1Regs.TBPRD = Period_SB;
EPwm1Regs.TBPHS.half.TBPHS = 0;
EPwm1Regs.TBCTR = 0;
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm1Regs.TBCTL.bit.PHSEN = TB_ENABLE;
EPwm1Regs.TBCTL.bit.SYNCSEL = TB_CTR_ZERO;

// Counter compare submodule registers
EPwm1Regs.CMPCTL.bit.LOADAMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
EPwm1Regs.CMPCTL.bit.LOADBMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
// EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_PRD;
// EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_PRD;
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;

// Action Qualifier SubModule Registers
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;

```

```

EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;

// Deadband SubModule Registers
EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL; // EPWMxA is the source for
both falling-edge and rising-edge delay
EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; //Both rising and
falling edge
EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active high complementary
(AHC). EPWMxB is inverted.

EPwm1Regs.DBFED = Dead_time; // Deadtime
is ~(20+20)ns @ 150MHz, 3 for 20ns
EPwm1Regs.DBRED = Dead_time;

/*
// Configure the Tripzone Registers
// TZA events can force EPWMxA
// TZB events can force EPWMxB
EALLOW;
EPwm1Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM1A will go low
EPwm1Regs.TZCTL.bit.TZB = TZ_FORCE_LO; // EPWM1B will go low
EPwm1Regs.TZFCR.bit.OST = 1; // Turn off the PWM
EDIS;
*/
//EPwm1Regs.CMPA.half.CMPA = 807; //Initialize the CMP
register
//EPwm1Regs.CMPB = 807;
EPwm1Regs.CMPA.half.CMPA = 0; //Initialize the CMP register
EPwm1Regs.CMPB = 0;

//-----PWM2 Initialization, PWM2 is used to drive SB3 Switch-----
----//
EPwm2Regs.TBCTL.bit.PRDL = TB_IMMEDIATE; // set Immediate load
EPwm2Regs.TBPRD = Period_SB;
EPwm2Regs.TBPHS.half.TBPHS = Period_SB*0.5;
EPwm2Regs.TBCTR = 0;
EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE; //TB_ENABLE;
EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; //DISABLE //TB_SYNC_IN;

// Counter compare submodule registers
EPwm2Regs.CMPCTL.bit.LOADAMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
EPwm2Regs.CMPCTL.bit.LOADBMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
// EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_PRD;
// EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_PRD;
EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;

// Action Qualifier SubModule Registers
EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR; //AQ_SET;
EPwm2Regs.AQCTLA.bit.CAD = AQ_SET; //AQ_CLEAR;

```

```

EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;

// Deadband SubModule Registers
EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL; // EPWMxA is the source for
both falling-edge and rising-edge delay
EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; //Both rising and
falling edge
EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active high complementary

EPwm2Regs.DBFED = Dead_time; // Deadtime
is ~(20+20)ns @ 1500MHz
EPwm2Regs.DBRED = Dead_time;

/*
// Configure the Tripzone Registers
// TZA events can force EPWMxA
// TZB events can force EPWMxB
EALLOW;
EPwm2Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM1A will go low
EPwm2Regs.TZCTL.bit.TZB = TZ_FORCE_LO; // EPWM1B will go low
EPwm2Regs.TZFRM.bit.OST = 1; // Turn off the PWM
EDIS;
*/
//EPwm2Regs.CMPA.half.CMPA = 807; //Initialize the CMP
register
//EPwm2Regs.CMPB = 807;
EPwm2Regs.CMPA.half.CMPA = Period_SB; //Initialize the CMP
register
EPwm2Regs.CMPB = Period_SB;

//-----PWM3 Initialization -----//
EPwm3Regs.TBCTL.bit.PRDL = TB_IMMEDIATE; // set Immediate load
EPwm3Regs.TBPRD = Period_SB;
EPwm3Regs.TBPHS.half.TBPHS = Period_SB*1;
EPwm3Regs.TBCTR = 0;
EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE; //TB_ENABLE;
EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; //TB_CTR_ZERO;

// Counter compare submodule registers
EPwm3Regs.CMPCTL.bit.LOADAMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
EPwm3Regs.CMPCTL.bit.LOADBMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
// EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_PRD;
// EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_PRD;
EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;

// Action Qualifier SubModule Registers
EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm3Regs.AQCTLA.bit.CAD = AQ_SET;

```

```

EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;

// Deadband SubModule Registers
EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL; // EPWMxA is the source for
both falling-edge and rising-edge delay
EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; //Both rising and
falling edge
EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active high complementary

EPwm3Regs.DBFED = Dead_time; // Deadtime
is ~(20+20)ns @ 150MHz
EPwm3Regs.DBRED = Dead_time;

/*
// Configure the Tripzone Registers
// TZA events can force EPWMxA
// TZB events can force EPWMxB
EALLOW;
EPwm2Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM1A will go low
EPwm2Regs.TZCTL.bit.TZB = TZ_FORCE_LO; // EPWM1B will go low
EPwm2Regs.TZFRM.bit.OST = 1; // Turn off the PWM
EDIS;
*/
//EPwm3Regs.CMPA.half.CMPA = 807; //Initialize the CMP
register
//EPwm3Regs.CMPB = 807;
EPwm3Regs.CMPA.half.CMPA = 0; //Initialize the CMP register
EPwm3Regs.CMPB = 0;

//-----PWM4 Initialization -----//
EPwm4Regs.TBCTL.bit.PRDL = TB_IMMEDIATE; // set Immediate load
EPwm4Regs.TBPRD = Period_SB;
EPwm4Regs.TBPHS.half.TBPHS = Period_SB*0.5;
EPwm4Regs.TBCTR = 0;
EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE; //TB_ENABLE;
EPwm4Regs.TBCTL.bit.PHSDIR = TB_UP;
EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; //TB_CTR_ZERO;

// Counter compare submodule registers
EPwm4Regs.CMPCTL.bit.LOADAMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
EPwm4Regs.CMPCTL.bit.LOADBMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
// EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_PRD;
// EPwm4Regs.CMPCTL.bit.LOADBMODE = CC_CTR_PRD;
EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm4Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;

// Action Qualifier SubModule Registers
EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm4Regs.AQCTLA.bit.CAD = AQ_SET;

```

```

EPwm4Regs.AQCTLB.bit.CAU = AQ_SET;
EPwm4Regs.AQCTLB.bit.CAD = AQ_CLEAR;

// Deadband SubModule Registers
EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL; // EPWMxA is the source for
both falling-edge and rising-edge delay
EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; //Both rising and
falling edge
EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active high complementary

EPwm4Regs.DBFED = Dead_time; // Deadtime
is ~(20+20)ns @ 150MHz
EPwm4Regs.DBRED = Dead_time;

/*
// Configure the Tripzone Registers
// TZA events can force EPWMxA
// TZB events can force EPWMxB
EALLOW;
EPwm2Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM1A will go low
EPwm2Regs.TZCTL.bit.TZB = TZ_FORCE_LO; // EPWM1B will go low
EPwm2Regs.TZFRC.bit.OST = 1; // Turn off the PWM
EDIS;
*/
//EPwm4Regs.CMPA.half.CMPA = 807; //Initialize the CMP
register
//EPwm4Regs.CMPB = 807;
EPwm4Regs.CMPA.half.CMPA = Period_SB; //Initialize the CMP
register
EPwm4Regs.CMPB = Period_SB;

//-----PWM5 Initialization-----//
EPwm5Regs.TBCTL.bit.PRDL = TB_IMMEDIATE; // set Immediate load
EPwm5Regs.TBPRD = Period_FB;
EPwm5Regs.TBPHS.half.TBPHS = 0;
EPwm5Regs.TBCTR = 0;
EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm5Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm5Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE; //TB_ENABLE;
EPwm5Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;

// Counter compare submodule registers
EPwm5Regs.CMPCTL.bit.LOADAMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
EPwm5Regs.CMPCTL.bit.LOADBMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
// EPwm5Regs.CMPCTL.bit.LOADAMODE = CC_CTR_PRD;
// EPwm5Regs.CMPCTL.bit.LOADBMODE = CC_CTR_PRD;
EPwm5Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm5Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;

// Action Qualifier SubModule Registers
EPwm5Regs.AQCTLA.bit.CAU = AQ_SET;
EPwm5Regs.AQCTLA.bit.CAD = AQ_CLEAR;

EPwm4Regs.AQCTLB.bit.CAU = AQ_CLEAR;

```



```

EPwm4Regs.AQCTLB.bit.CAD = AQ_SET;

// Deadband SubModule Registers
EPwm5Regs.DBCTL.bit.IN_MODE = DBA_ALL; // EPWMxA is the source for
both falling-edge and rising-edge delay
EPwm5Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; //Both rising and
falling edge
EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active high complementary

// TRANPHORM: Don't enable trip zone until current sensors are properly
scaled in the hardware
EPwm5Regs.DBFED = Dead_time; // Deadtime
is ~(20+20)ns @ 150MHz
EPwm5Regs.DBRED = Dead_time;

/*
// Configure the Tripzone Registers
// TZA events can force EPWMxA
// TZB events can force EPWMxB
EALLOW;
EPwm4Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM1A will go low
EPwm4Regs.TZCTL.bit.TZB = TZ_FORCE_LO; // EPWM1B will go low
EPwm4Regs.TZFCR.bit.OST = 1; // Turn off the PWM
EDIS;
*/
//EPwm5Regs.CMPA.half.CMPA = 236; //Initialize the CMP
register
//EPwm5Regs.CMPB = 236;
EPwm5Regs.CMPA.half.CMPA = Period_FB; //Initialize the CMP
register
EPwm5Regs.CMPB = Period_FB;

//-----PWM6 Initialization -----
---//
EPwm6Regs.TBCTL.bit.PRDL = TB_IMMEDIATE; // set Immediate load
EPwm6Regs.TBPRD = Period_FB;
EPwm6Regs.TBPHS.half.TBPHS = 0;
EPwm6Regs.TBCTR = 0;
EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm6Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm6Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE; //TB_ENABLE;
EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN; //TB_CTR_ZERO;

// Counter compare submodule registers
EPwm6Regs.CMPCTL.bit.LOADAMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
EPwm6Regs.CMPCTL.bit.LOADBMODE = 2; //2 = Load on either (CTR =
Zero) or (CTR = PRD)
// EPwm6Regs.CMPCTL.bit.LOADAMODE = CC_CTR_PRD;
// EPwm6Regs.CMPCTL.bit.LOADBMODE = CC_CTR_PRD;
EPwm6Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm6Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;

// Action Qualifier SubModule Registers
EPwm6Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm6Regs.AQCTLA.bit.CAD = AQ_SET;

```

```

EPwm6Regs.AQCTLB.bit.CAU = AQ_SET;
EPwm6Regs.AQCTLB.bit.CAD = AQ_CLEAR;

// Deadband SubModule Registers
EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL; // EPWMxA is the source for
both falling-edge and rising-edge delay
EPwm6Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; //Both rising and
falling edge
EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC; // Active high complementary

// TRANPHORM: Don't enable trip zone until current sensors are properly
scaled in the hardware
EPwm6Regs.DBFED = Dead_time; // Deadtime
is ~(20+20)ns @ 150MHz
EPwm6Regs.DBRED = Dead_time;

/*
// Configure the Tripzone Registers
// TZA events can force EPWMxA
// TZB events can force EPWMxB
EALLOW;
EPwm2Regs.TZCTL.bit.TZA = TZ_FORCE_LO; // EPWM1A will go low
EPwm2Regs.TZCTL.bit.TZB = TZ_FORCE_LO; // EPWM1B will go low
EPwm2Regs.TZFRC.bit.OST = 1; // Turn off the PWM
EDIS;
*/
//EPwm6Regs.CMPA.half.CMPA = 236; //Initialize the CMP
register
//EPwm6Regs.CMPB = 236;
EPwm6Regs.CMPA.half.CMPA = 0; //Initialize the CMP register
EPwm6Regs.CMPB = 0;

//-----Used to generate SOC to ADC-----//
EPwm6Regs.ETSEL.bit.SOCAEN = 1; // Enable the ADC Start of
Conversion A (EPWM6SOCA) Pulse
EPwm6Regs.ETSEL.bit.SOCASEL = 1; // Enable event time-base
counter equal to period (TBCTR = 0), These bits determine when a EPWMxSOCA
pulse will be generated.
EPwm6Regs.ETPS.bit.SOCAPRD = 1; // Generate pulse on 1st
event
}

void ADC_CONF (void)
{
AdcRegs.ADCTRL3.bit.SMODE_SEL = 0x1; // 0 = Sequential sampling mode, 1 =
Simultaneous sampling mode.
AdcRegs.ADCTRL1.bit.SEQ_CASC = 0x1; // Setup cascaded sequencer mode
AdcRegs.ADCMAXCONV.all = 0x0007; // 16 chanel sampling
AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0; // Setup conv from ADCINA0 &
ADCINB0
AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x1; // Setup conv from ADCINA1 &
ADCINB1
AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x2; // Setup conv from ADCINA2 &
ADCINB2
AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x3; // Setup conv from ADCINA3 &
ADCINB3

```

```

    AdcRegs.ADCCHSELSEQ2.bit.CONV04 = 0x4; // Setup conv from ADCINA4 &
ADCINB4
    AdcRegs.ADCCHSELSEQ2.bit.CONV05 = 0x5; // Setup conv from ADCINA5 &
ADCINB5
    AdcRegs.ADCCHSELSEQ2.bit.CONV06 = 0x6; // Setup conv from ADCINA6 &
ADCINB6
    AdcRegs.ADCCHSELSEQ2.bit.CONV07 = 0x7; // Setup conv from ADCINA7 &
ADCINB7
    AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 1; // Allows SEQ1/SEQ to be started by
ePWMx SOCA trigger
    AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1; // Enable SEQ1 interrupt (every
EOS)
}

interrupt void adc_isr(void)
{
    if(timer < 10)
    {
        EPwm1Regs.CMPA.half.CMPA = Duty_SB;
        EPwm1Regs.CMPB = Duty_SB;
        EPwm2Regs.CMPA.half.CMPA = Duty_SB;
        EPwm2Regs.CMPB = Duty_SB;
        EPwm3Regs.CMPA.half.CMPA = Duty_SB;
        EPwm3Regs.CMPB = Duty_SB;
        EPwm4Regs.CMPA.half.CMPA = Duty_SB;
        EPwm4Regs.CMPB = Duty_SB;
        EPwm5Regs.CMPA.half.CMPA = Duty_FB;
        EPwm5Regs.CMPB = Duty_FB;
        EPwm6Regs.CMPA.half.CMPA = Duty_FB;
        EPwm6Regs.CMPB = Duty_FB;

        //timer++;
    }
    else
    {
        ALL_PWM_OFF();

        /*
        EPwm1Regs.CMPA.half.CMPA = 1141;
        EPwm1Regs.CMPB = 1141;
        EPwm2Regs.CMPA.half.CMPA = 0;
        EPwm2Regs.CMPB = 0;
        EPwm3Regs.CMPA.half.CMPA = 1141;
        EPwm3Regs.CMPB = 1141;
        EPwm4Regs.CMPA.half.CMPA = 0;
        EPwm4Regs.CMPB = 0;

        EPwm5Regs.CMPA.half.CMPA = 570;
        EPwm5Regs.CMPB = 570;
        EPwm6Regs.CMPA.half.CMPA = 0;
        EPwm6Regs.CMPB = 0;
        */
    }

    /*
    if(mode == 0) //55

```

```

    {
    EPwm1Regs.CMPA.half.CMPA = 807;
    EPwm1Regs.CMPB = 807;
    EPwm2Regs.CMPA.half.CMPA = 807;
    EPwm2Regs.CMPB = 807;
    EPwm3Regs.CMPA.half.CMPA = 807;
    EPwm3Regs.CMPB = 807;
    EPwm4Regs.CMPA.half.CMPA = 807;
    EPwm4Regs.CMPB = 807;
    EPwm5Regs.CMPA.half.CMPA = 236;
    EPwm5Regs.CMPB = 236;
    EPwm6Regs.CMPA.half.CMPA = 236;
    EPwm6Regs.CMPB = 236;
    }

while(timer < 60) //73,      13 per run
{
    timer++;
    if(timer == 60)
    {
        mode = 1;
        mode = 0;
        mode = 1;
    }
}

if(mode == 1)      //93+570
{
    EPwm1Regs.CMPA.half.CMPA = 0;
    EPwm1Regs.CMPB = 0;
    EPwm2Regs.CMPA.half.CMPA = 1141;
    EPwm2Regs.CMPB = 1141;
    EPwm3Regs.CMPA.half.CMPA = 0;
    EPwm3Regs.CMPB = 0;
    EPwm4Regs.CMPA.half.CMPA = 1141;
    EPwm4Regs.CMPB = 1141;
    EPwm5Regs.CMPA.half.CMPA = 570;
    EPwm5Regs.CMPB = 570;
    EPwm6Regs.CMPA.half.CMPA = 0;
    EPwm6Regs.CMPB = 0;
}
*/
AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;          // Reset SEQ1
AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;       // Clear INT SEQ1 bit
PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;  // Acknowledge interrupt to
PIE
}

void ALL_PWM_ON(void)
{
    EALLOW;
    EPwm1Regs.TZCLR.bit.OST = 1;
    EPwm2Regs.TZCLR.bit.OST = 1;
    EPwm3Regs.TZCLR.bit.OST = 1;
    EPwm4Regs.TZCLR.bit.OST = 1;
    EPwm5Regs.TZCLR.bit.OST = 1;
    EPwm6Regs.TZCLR.bit.OST = 1;
}

```

```

    EDIS;
}

void ALL_PWM_OFF(void)
{
    EALLOW;
    EPwm1Regs.TZFRC.bit.OST = 1;
    EPwm2Regs.TZFRC.bit.OST = 1;
    EPwm3Regs.TZFRC.bit.OST = 1;
    EPwm4Regs.TZFRC.bit.OST = 1;
    EPwm5Regs.TZFRC.bit.OST = 1;
    EPwm6Regs.TZFRC.bit.OST = 1;
    EDIS;
}

void GPIO_CONF (void)
{
    EALLOW;

    GpioCtrlRegs.GPAPUD.bit.GPIO0 = 1;    // Disable pull-up on GPIO0
    (EPWM1A), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAPUD.bit.GPIO1 = 1;    // Disable pull-up on GPIO1
    (EPWM1B), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;    // Configure GPIO0 as EPWM1A
    GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;    // Configure GPIO1 as EPWM1B

    GpioCtrlRegs.GPAPUD.bit.GPIO2 = 1;    // Disable pull-up on GPIO2
    (EPWM2A), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAPUD.bit.GPIO3 = 1;    // Disable pull-up on GPIO3
    (EPWM2B), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;    // Configure GPIO2 as EPWM2A
    GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;    // Configure GPIO3 as EPWM2B

    GpioCtrlRegs.GPAPUD.bit.GPIO4 = 1;    // Disable pull-up on GPIO4
    (EPWM3A), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAPUD.bit.GPIO5 = 1;    // Disable pull-up on GPIO5
    (EPWM3B), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 1;    // Configure GPIO4 as EPWM3A
    GpioCtrlRegs.GPAMUX1.bit.GPIO5 = 1;    // Configure GPIO5 as EPWM3B

    GpioCtrlRegs.GPAPUD.bit.GPIO6 = 1;    // Disable pull-up on GPIO6
    (EPWM4A), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAPUD.bit.GPIO7 = 1;    // Disable pull-up on GPIO7
    (EPWM4B), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAMUX1.bit.GPIO6 = 1;    // Configure GPIO6 as EPWM4A
    GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 1;    // Configure GPIO7 as EPWM4B

    GpioCtrlRegs.GPAPUD.bit.GPIO8 = 1;    // Disable pull-up on GPIO8
    (EPWM5A), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAPUD.bit.GPIO9 = 1;    // Disable pull-up on GPIO9
    (EPWM5B), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAMUX1.bit.GPIO8 = 1;    // Configure GPIO8 as EPWM5A
    GpioCtrlRegs.GPAMUX1.bit.GPIO9 = 1;    // Configure GPIO9 as EPWM5B

    GpioCtrlRegs.GPAPUD.bit.GPIO10 = 1;    // Disable pull-up on GPIO10
    (EPWM6A), thus Trip-zone can ensure all pwm is LOW

```

```

    GpioCtrlRegs.GPAPUD.bit.GPIO11 = 1;    // Disable pull-up on GPIO11
    (EPWM6B), thus Trip-zone can ensure all pwm is LOW
    GpioCtrlRegs.GPAMUX1.bit.GPIO10 = 1;    // Configure GPIO10 as EPWM6A
    GpioCtrlRegs.GPAMUX1.bit.GPIO11 = 1;    // Configure GPIO11 as EPWM6B

    EDIS;
}

void Sample1000 (float sample)
{
    if(n_test2 < 999)
    {
        n_test2++;
    }
    else
    {
        n_test2 = 0;
    }
    test2[n_test2] = sample;
}

void Modulation_ref_saturate (float i)    // triangle wave changes from 0-
300, 300 = 60MHz/10kHz(sampling frequency)/2
{
    if (i > 140)
    {
        i = 140;
    }
    else if (i < 10)
    {
        i = 10;
    }
}
//=====
// No more.
//=====

```