HIGH-POWER HIGH-EFFICIENCY MULTI-FUNCTIONAL CMOS RADIO FREQUENCY INTEGRATED CIRCUITS FOR WIRELESS COMMUNICATION OF UNMANNED AIRCRAFT SYSTEM (UAS)

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High-Power High-Efficiency Multi-Functional CMOS Radio Frequency Integrated Circuits for Wireless Communication of Unmanned Aircraft System (UAS)

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ABSTRACT

Recently the Unmanned Aircraft System (UAS) has become very popular due to its current and projected opportunities in diversified applications from surveillance to security to militry. The Federal Aviation Administration (FAA) has mandated for all UASs to be equipped with an Automatic Dependent Surveillance Broadcast (ADS-B) transmitter by 2020.

ADS-B is a next generation aircraft communication system, operating with two frequencies, 978 MHZ and 1090 MHz, which will transmit the information of identification, and precise position of an airplane to the nearby airplanes and ground station. At present, the ADS-B transmitter is fabricated with hybrid integrated circuits (HICs) in three different modules: a Phase Locked Loop (PLL) module, an Up-converter (modulator) module and a Power Amplifier (PA) module [8-10] which makes the system very large in size and expensive.

In this work, for the first time an ADS-B transmitter as a part of Universal Access Transceievr (UAT) and Universal Beacon Radio (UBR) has beeen developed in a fully integrated single chip using the Complementary Metal Oxide Semiconductor (CMOS) process which is capable of operating both at 978 MHz UAT and 1090 MHz Extended Squitter (ES) modes. The chip provides the modulated output power of 23 dBm which is sufficient for the UAS to operate below class-A airspace. If the UAS needs to operate above this range or needs to operate for a manned aircraft system, this single chip ADS-B transmitter can be interfaced to drive an off-chip high-power PA, and, thus, it will reduce the burden of the input power and the gain of the off-chip PA. The chip supports both single tone and modulated baseband signals. In addition, this chip is capable of operating a part of new datalinks (960 MHz to 1164 MHz) and DME bands for UAS.

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DEDICATION

To my loving wife:

Soumi Bairagi

And

My inspiring parents:

Ramesh Ch Roy

&

Kanan Roy

TABLE OF CONTENTS

ABSTRACT iii

ACKNOWLEDGEMENTS iv

DEDICATION vi

LIST OF TABLES x

LIST OF FIGURES xi

LIST OF ABBREVIATIONS xv

CHAPTER 1. INTRODUCTION 1

1.1. Motivation 1

1.2. Background 2

1.2.1. Previous work on ADS-B system 6

1.2.2. Literature Survey of Other Transmitters 7

1.3. Organization of the Dissertation 8

CHAPTER 2. HIGH-POWER AND HIGH-EFFICIENCY SIGNAL GENERATION FOR ADS-B TRANSMITTER 10

2.1. A Short Introduction of Voltage Controlled Oscillator 10

2.2. Circuit Design Methodology 11

2.2.1. Start-up of VCO 13

2.2.2. Output Amplitude 15

2.2.3. Frequency of Oscillation 20

2.2.4. Frequency Tuning Range 20

2.2.5. Phase Noise 23

2.2.6. Figure-of-Merit (FOM) 25

2.3. Measurement Results 26

2.4. Conclusion 33

CHAPTER 3. HIGH-POWER AND HIGH-GAIN CMOS POWER AMPLIFIER FOR ADS-B TRANSMIITER 35
3.1. Introduction 35
3.2. Output Power and Power Gain 36
3.3. Linearity 37
3.3.1. P_{1dB} 37
3.3.2. Intermodulation (IM) Product 38
3.3.3. AM/PM Conversion 40
3.4. Efficiency and Power Added Effficiency 40
3.5. Stability of Power Amplifier 41
3.6. Class of Operation of Power Amplifier 42
3.7. Challenges in Designing High-Power and High-Gain PA 44
3.8. Classification of Power Combining Technique 46
3.8.1. Direct Power Combining Technique 47
3.8.2. Voltage Combining Technique 48
3.8.3. Current Combining Technique 50
3.8.3.1. Reactive Current Combining Technique 51
3.8.3.2. Resistive Current Combining Technique 52
3.9. Figure-of-Merit (FOM) 53
3.10. Circuit Design Methodology 53
3.10.1. Combining Mechanism 54
3.10.2. Bandwidth Enhancement 59
3.10.3. Matching Network ..... .60
3.10.4. Overall Efficiency of PA 61
3.11. Measurement Results 62
3.12. Conclusion 67

CHAPTER 4. HIGH-POWER HIGH-EFFICIENCY FULLY INTEGRATED SINGLE-CHIP CMOS ADS-B TRANSMITTER FOR UAS 68
4.1. Introduction 68
4.2. Proposed ADS-B Transmitter 69
4.3. Circuit Design Methodology 71
4.3.1. VCO and Buffer 71
4.3.2. Hybrid 72
4.3.3. Up-converter 75
4.3.4. Balun 89
4.3.5. Power Amplifier 93
4.4. Design Challenges 99
4.5. Measurement Results 100
4.4. Conclusion 105
CHAPTER 5. CONCLUSIONS AND FUTURE WORKS 108
5.1. Technical Contributions 108
5.2. Future Works 109
BIBLIOGRAPHY 111
APPENDIX A. RELATED PUBLICATIONS 124

LIST OF TABLES

Table		Page
1.	Power required for different ranges and airspace class.	5
2.	Performance of the state-of-the-art transmitter operating around ADS-B frequencies	8
3.	Comparison of the performance of VCO type-1 with the state-of-the-art technology	32
4.	Comparison of the performance of VCO type-2 with the state-of-the-art technology	33
5.	Class of operation and efficiency of PA	43
6.	Peak voltage required across the device for different device plane impedance to deliver 1 W power	45
7.	Comparison of the performance of state-of-the-art CMOS PAs in the similar frequency range	66
8.	Performance of the hybrid	75
9.	Performance of the up-converter	88
10.	Performance of the balun	92
11.	Overall performance of integrated ADS-B transmitter	105
12.	Comparison of the performance of the state-of-the-art transmitters in L, S, C, and Ku bands..	……106

LIST OF FIGURES

Figure		Page
1.1.	Classification of national airspace depending on altitude	2
1.2.	Operation of ADS-B communication datalinks for the manned and unmanned aircraft system.	3
1.3.	Frequency spectrum showing bands for ADS-B, new datalinks (L-DASC 1 &2) and DME.	4
1.4.	The block diagram of functional architecture of UAT beacon radio (UBR).	6
1.5.	State-of-the-art ADS-B Transmitter for UAS System (Multiple Chips).	7
2.1.	The oscillator as a positive feedback amplifier.	10
2.2.	The oscillator as a negative resistance generator with passive resonant tank.	11
2.3.	The circuit diagram of the VCO type-1 with buffer.	12
2.4.	The circuit diagram of the VCO type-2 with buffer.	13
2.5.	The circuit of VCO core in Figure 2.3 and Figure 2.4 after reduction.	13
2.6.	Equivalent circuit of one part of two tuned circuits in Figure 2.5	14
2.7.	Simulated voltage waveforms at the nodes G1 (VGS1), D1 (VDS1), G2 (VGS2), D2 (VDS2), respectively and simulated current waveforms through the transistors TN1 and TN2, respectively.	16
2.8.	Variation of capacitance at the gate of NMOS diodes, TN3 and TN4 with tuning voltage.	22
2.9.	Elements for tuning the VCO frequency a) varactor diode b) diode-connected NMOS transistor and c) switched capacitor.	22
2.10.	Output spectrum of an ideal and real noisy oscillator	23
2.11.	Micrograph of (a) 0.738 mm X 0.606 mm (type-1) and (b) 0.713 mm X 0.638 mm (type-2) fabricated VCO chips.	26
2.12.	Simulated and measured tuning frequency range versus tuning voltage of the VCO type-1.	……26
2.13.	Simulated and measured tuning frequency range versus tuning voltage of the VCO type-2.	……27

2.14. Measured output power spectrum of the VCO (a) type-1 at 978 MHz and (b) type-2 at 980 MHz. 28

2.15. Simulated and measured single-ended output power of the VCO type -1 versus frequency..... 28

2.16. Simulated and measured single-ended output power and efficiency of the VCO type-2 versus frequency. 29

2.17. Phase noise of the VCO type-1 measured at the center frequency of 978 MHz at an offset of 1 MHz. 30

2.18. Phase noise of the VCO type-2 measured at the center frequency of 980 MHz at an offset of 1 MHz.. 30

2.19. Variation of phase noise @ 1-MHz offset and variation of FOM_{PE} with frequency. 31

3.1. Output power and gain versus input power showing P_{1dB} point and IP3 point 37

3.2. Class of operation of power amplifier depending on the output current conduction angle (left) and on the fixed device quiescent point (right).. 43

3.3. Stacked NMOS transistors showing voltage combining phenomena with increased impedance at the output. 49

3.4. N-stage of reactive current combining..... 51

3.5. N-stage resistive current combining. 52

3.6. Circuit diagram of 4-stage power amplifier with IMN and OMN..... 54

3.7. M-stage resistive current combining showing the combining mechanism with 1-transistor unit cell..... 55

3.8. AC equivalent circuit for resistive current combining at the 4^{th} stage of the PA 56

3.9. Smith chart of output impedance of the 4^{th} stage for 1-cell, 2-cell, and 4-cell resonators. 57

3.10. Output power versus frequency for resistive and reactive current combining. 59

3.11. Circuit schematic of OMN..... 60

3.12. Micrograph of a fully integrated 3.63 mm X 0.95 mm fabricated CMOS PA chip. 62

3.13. Measured S-parameters..... 63

3.14. Measured single-tone output power of the PA at 978 MHz.. 63

3.15. Measured modulated output power spectrum of the PA with 25 MHz baseband (a) GMSK, (b) 8PSK, (c) 16QAM, and (d) 64QAM signals. 64

3.16. Measured output power and gain versus input power. 64

3.17. Measured saturated output power versus frequency. 65

4.1. Objective of this thesis work..... 70

4.2. Block diagram of proposed CMOS ADS-B transmitter in a single-chip..... 70

4.3. The circuit diagram of the VCO with buffer. 71

4.4. Circuit diagram of passive hybrid. 72

4.5. Simulated voltage waveforms of differential inputs and outputs of two hybrids. 73

4.6. Simulated input and output spectrum of the hybrid. 74

4.7. The simulated results of the gain of the hybrid at I^+ and Q^+ ports versus the frequency..... 75

4.8. (a) Up-conversion mixer, (b) mixer as an ideal switch..... 76

4.9. Passive (a) single-ended mixer, and (b) single-ended sampling mixer. 78

4.10. Passive (a) single-balanced mixer, and (b) single-balanced sampling mixer. 78

4.11. Passive (a) double-balanced mixer, and (b) double-balanced sampling mixer. 79

4.12. Double-balanced passive sampling mixer consisting of two single-balanced mixers connected with the outputs summed in current domain. 80

4.13. Single-balanced active mixer. 81

4.14. Double-balanced active mixer consisting of two single-balanced mixers connected with the outputs summed in current domain. 82

4.15. I-Q double-balanced active mixer connected with the outputs summed in current domain..... 84

4.16. Simulated voltage waveforms of input and output of the up-converter in Figure 4.15..... 86

4.17. Simulated results of input and output spectrum of the up-converter. 86

4.18. Simulated results of output power and conversion gain versus baseband power. 87

4.19. Simulated results of the conversion gain of the up-converter versus frequency 88

4.20. Circuit diagram of the balun (topology-1). 89

4.21. Circuit diagram of the balun (topology-2). 90

4.22. Simulated result of frequency spectrum of single-ended input and single-ended output. 91

4.23. Simulated results of frequency spectrum of differential input and single-ended output. 91

4.24. Simulated results of the differential input to single-ended output gain versus the differential input voltage. 92

4.25. Circuit diagram of 4-stage PA which uses current combining technique (topology-1). 93

4.26. Circuit diagram of high-power and high-gain 4-stage PA which uses resistive current combining technique (topology-2).. 94

4.27. AC equivalent circuit of the power stage. 96

4.28. Equivalent circuit of the power stage considering one device unit as generator and other N-1 stages as load. 97

4.29. Circuit schematic of OMN. 98

4.30. Micrograph of a fully integrated 1.9 mm X 0.84 mm fabricated CMOS ADS-B transmitter chip for UAS (type-1).. 101

4.31. Micrograph of a fully integrated 4.38 mm X 3 0.95 mm fabricated CMOS ADS-B transmitter chip for UAS (type-2). 101

4.32. Measured single-tone CW output power spectrum of the transmitter (type-1) with carrier frequency of 978 MHz and baseband frequency of 65 MHz giving LSB signal of 913 MHz. 102

4.33. Measured modulated output power spectrum of the transmitter (type-2) with 25 MHz baseband a) GSM b) 8PSK c) 16QAM and d) GMSK signals. 103

4.34. Measured frequency characteristics of modulated output power of the transmitter of type-2. 104

LIST OF ABBREVIATIONS

ADS-B.....Automatic Dependent Surveillance-Broadcast.

AGL .....Above Ground Level.

ATC.....Air Traffic Control.

BB .....Baseband.

BiCMOS .....Bipolar CMOS.

BW .....Bandwidth.

CCA .....Current Conduction Angle.

CD .....Common Drain.

CG .....Common Gate.

CMOS .....Complementary Metal Oxide Semiconductor.

CORE .....Center of Research Excellence.

CPFSK .....Continuous Phase Frequency Shift Keying.

CS.....Common Source.

CW .....Continuous Wave.

dBm.....Unit of power measured with reference to 1 mW

=10*log $\left(\frac{P}{1\ \mathrm{mW}}\right)$, P=Power to be measured in dBm.

DME.....Distance Measuring Equipment.

EDGE.....Enhanced Data Rate for GSM Evolution.

EGSM .....Enhanced GSM.

ES.....Extended Squitter.

FAA.....Federal Aviation Administration.

FL.....Flight Level.

FOM.....Figure of Merit.

ft .....Feet.

FTR .....Frequency Tuning Range.

GaAs .....Gallium Arsenide.

GaN .....Gallium Nitride.

GNSS .....Global Navigation Satellite System.

GMSK .....Gaussian Minimum Shift Keying.

GSM .....Global System for Mobile Communications.

HEMT .....High-Electron-Mobility Transistor.

HIC .....Hybrid Integrated Circuits.

HPF .....High Pass Filter.

HT .....Harmonic Termination.

IC .....Integrated Circuit.

ICAO .....International Civil Aviation Organization.

IIP3 .....3^{rd} Order Input Intercept Point.

IMN .....Input Matching Network.

IM3 .....3^{rd} Order Intermodulation Distortion.

IP3 .....3^{rd} Order Intercept Point.

ISM .....Inter-Stage Matching.

L-DACS .....L-Band Digital Aeronautical Communications Systems.

LPF .....Low Pass Filter.

LO .....Local Oscillator.

LSB .....Lower Side Band.

LTE-a .....Long Term Evolution-Advanced.

mm-Wave .....Millimeter-Wave.

MSL .....Mean Sea Level.

NAS.....National Airspace System.

NM.....Nautical Mile.

OFDM.....Orthogonal Frequency Domain Modulation.

OIP3.....3^{rd} Order Output Intercept Point.

PA.....Power Amplifier.

PAE.....Power Added Efficiency.

PCB.....Printed Circuit Board.

PSK.....Phase Shift Keying.

QAM.....Quadrature Amplitude Modulation.

QPSK.....Quadrature Phase Shift Keying.

RADAR.....Radio Detection And Ranging.

R&D.....Research and Development.

RF.....Radio Frequency.

Rx.....Receiver.

TL.....Transmission Line.

Tx.....Transmitter.

UAV.....Unmanned Air Vehicle.

UAT.....Universal Access Transceiver.

UBR.....UAT Beacon Radio.

USB.....Upper Side Band.

VCO.....Voltage Control Oscillator.

WLAN.....Wireless Local Area Network.

CHAPTER 1. INTRODUCTION

1.1. Motivation

Unmanned Air Vehicles (UAV) or Unmanned Aircraft Systems (UAS) are becoming very popular recently due to their current and projected opportunities in diversified applications to human society. The UAS are now being widely used for the commercial, security, surveillance, public interest, scientific and military. R&D activities conducted by Federal Aviation Administration (FAA) opened some specific application areas such as aerial photography, precision agriculture, search and rescue/law enforcement, bridge inspection [1] and to support transportation, monitoring oil fields, mobile cellular system and natural disaster [2]. So, it is obvious that in near future aerospace industries are going to be dramatically global growing sectors. The number of UAS in the USA will increase from a few hundred in 2015 to over 230,000 in 2035 as mentioned in a report by the US Department of Transportation [3]. The majority of these UAS will comprise of "small" and "micro" class UAS [4]. So, it is very important to integrate UAS to the National Airspace System (NAS). However, integration of the UAS to the NAS, will pose a significant threat to the air safety of present manned aircraft until an operational restriction is proposed [2]. For the safety of the aircraft, the International Civil Aviation Organization (ICAO) categorized the airspace to different classes A to G according to the height from sea level. The US airspace (except class F which is not used in USA) is shown in the Figure 1.1. The controlled airspace which are provided with the Air Traffic Control (ATC) services are class A [which is from 1800 ft mean sea level (MSL) to flight level (FL) 600], class B [from surface to 10,000 ft MSL], class C [from surface to 400 ft above airport surface], class D [from surface to 2,500 ft above airport surface], class E [which are not classified as class A, B, C, and class D and which are mostly up to 700 ft or 1,200 ft above ground level (AGL) but below 14,500 ft MSL], whereas

the uncontrolled airspace which is not provided with the ATC services is class G airspace [which is the portion of the airspace that has not been designated as Class A, B, C, D, or E and which extends from the surface to the base of the overlying Class E airspace].

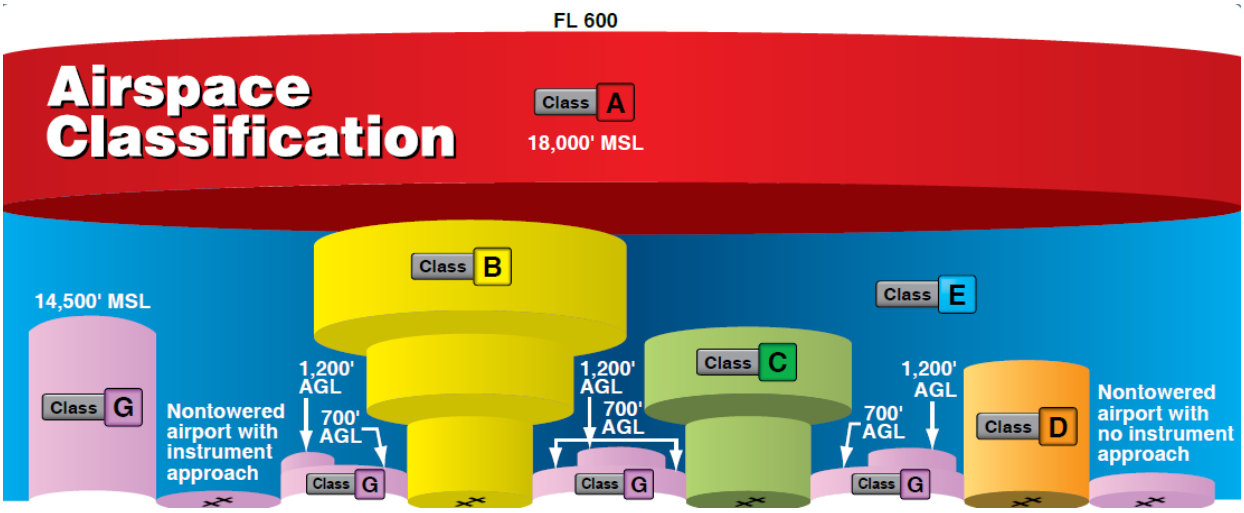

Figure 1.1. Classification of national airspace depending on altitude (source: FAA [5]).

Recently the FAA proposed prohibition on the operation of the UAS and thus accommodation of the UAS to the NAS has become realistic [7]. The FAA strictly prohibited the operation of small UAS in class A airspace (above 18,000 ft) but allowed the operation in class B, C, D, E airspace (from 700 ft to 18000 ft) with Air Traffic Control (ATC) permission and in G airspace without ATC permission [1]. According to the NAS roadmap, it has been mandatory for all UAS and manned aircrafts to equip with an Automatic Dependent Surveillance Broadcast (ADS-B) transmitter [8], and the FAA mandated it to complete the installation by 2020 [4]. So, a huge demand for a commercial ADS-B transmitter for both micro and small UAS will proliferate in avionics industries by and/or after the 2020.

1.2. Background

ADS-B is a next generation aircraft communication system which will enable each airplane (manned and unmanned) to automatically transmit the information of its identification &

type, precise position, velocity and emergency information to the nearby airplanes and ground station. The conventional ADS-B system operates in two modes – (i) 978 MHz universal access transceiver (UAT) which operates below 18,000 ft and (ii) 1090 MHz extended squitter (1090 ES) which operates above 18,000 ft. The Figure 1.2 shows the operation of UAS and manned aircrafts together in the national airspace using ADS-B communication link.

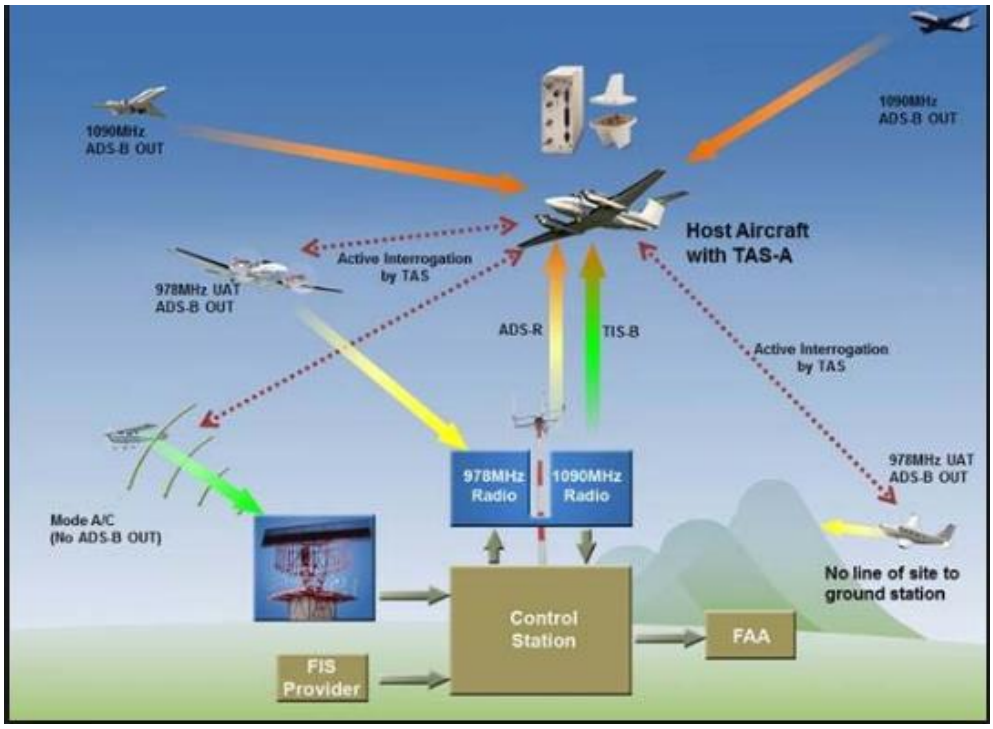

Figure 1.2. Operation of ADS-B communication datalinks for the manned and unmanned aircraft system (source: Maxcraft Avionics [6]).

With the huge demand of large data including video signals, new datalinks for both manned and unmanned aircrafts are going to be developed in near future [9]. This datalink for UAS will use a part of IEEE L-band from 960 MHz to 1164 MHz, named as L-Band Digital Aeronautical Communications Systems, L-DACS1 (975-1164 MHz) and L-DACS2 (960-975 MHz), and C-Band from 4 GHz to 8 GHz. The frequency use in L-band is shown in the Figure 1.3, where L-DACS1, L-DACS2, UAT, 1090 ES and DME bands are used between 960-1164 MHz [9].

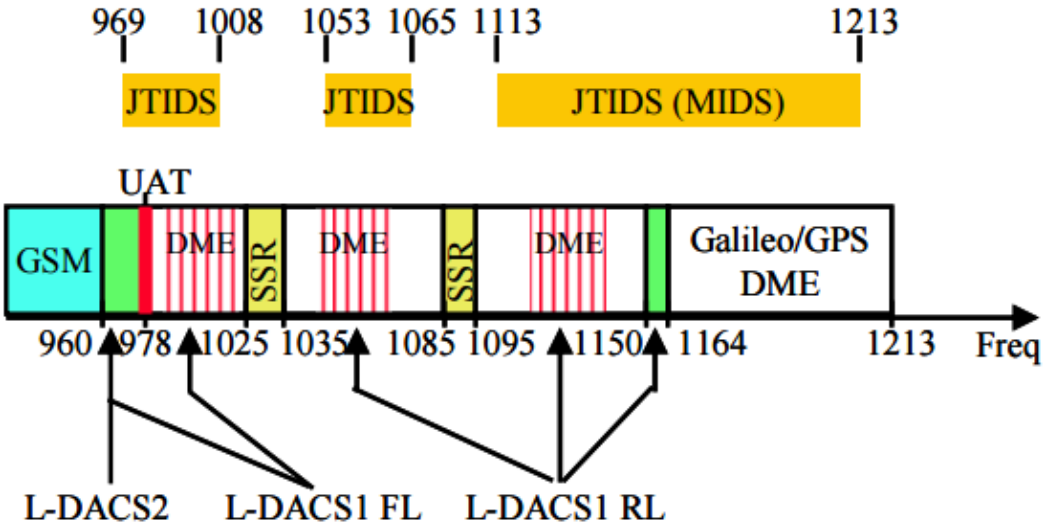

Figure 1.3. Frequency spectrum showing bands for ADS-B, new datalinks (L-DASC1 & L-DACS2) and DME (source: [9]).

The transmitter of radio frequency (RF) UAT beacon radio (UBR) of ADS-B system is a critical element, and its cost-performance trade-off greatly affects the entire air traffic surveillance of both manned aircraft and UAS system. The performance of the transmitter depends on the output power and the range of the transmitter. The power required from the transmitter for manned aircraft to get the range up to 12 NM (63,000ft) is approximately 7W (38 dBm) [10-11]. The range is calculated using Friis transmission equation according to [12] and given by

$$R_{\max} = a \times 10^{\left(-\frac{L_{FS}}{20}\right)} \tag{1.1}$$

where, a=1.475 e^{-5} mW-NM at f=978 MHz and 1.188 e^{-5} mW-NM at f=1090 MHz, and path loss, L_{FS} is given by

$$L_{FS} = MTL - \left(P_T + L_{TC} + G_T + G_R + L_{RC}\right) \tag{1.2}$$

where, P_T= Transmitter Power, L_{TC} = Transmitter Cable Loss, G_T= Transmitter Antenna Gain, G_R = Receiver Antenna Gain, and L_{RC} = Receiver Cable Loss, G_R = Receiver Antenna Gain. By considering a high-end receiver (i.e. MTL= -88.67 dBm), the cable loss for both transmitter and

receiver of 1.5 dB and antenna gain of 0 dB for both transmitter and receiver, the transmitter power required for the range of 5 NM is 30 dBm (1 W) at the frequency of 1090 MHz. With the above setting the power requirement to operate below the class-A airspace (below 18000 ft, i.e. 3 NM) at 978 MHz is 23~24 dBm. But considering the transmitter and receiver antenna gain of 1.5 dB each, the power required for range of 3 NM is 21 dBm. Although the power requirement for manned aircraft is very high, the power requirement for the UAS to operate below the class-A airspace can be targeted from 15 dBm to 30 dBm depending on the operating level of the UAS. Table 1 shows the power required for UAS to operate at different ranges and the class of airspace it can covers.

Table 1. Power required for different ranges and airspace class

Range	Airspace Class	Power (dBm)
0.1 NM (600 ft)	G	1
0.2 NM (1200 ft)	E	3
0.41 NM (2500 ft)	D	8
0.65 NM (4000 ft)	C	11
1 NM (6000 ft)	B	15
1.35 NM (8000 ft)	B	17
1.9 NM (9000 ft)	B	20
3 NM (18000 ft)	A	24
3.86 NM (20,400 ft)	A	28
4.86 NM (25,600 ft)	A	30
6 NM (32,000 ft)	A	32
12 NM (63,000 ft)	A	38

1.2.1. Previous work on ADS-B system

Figure 1.4 shows the block diagram of UBR developed by the MITRE Corporation [13] which includes ADS-B transceiver (UAT transmitter and UAT receiver), Global Navigation Satellite System (GNSS) receiver, microcontroller, power supply circuitry and antenna circuitry. The power supply and microcontroller are connected to the external by external bus/interface. If UAT receiver and antenna are considered high-end candidates, the UAT transmitter is the only block to determine the range of the UBR, and hence the UAT transmitter plays a vital role in the overall performance of the UBR. So, designing the ADS-B transmitter with high power and high efficiency will have an enormous impact on the performance and, hence the growth of the whole UAS system. As was mentioned earlier, MITRE and ERAU are at present involved in the development of the UBR, but the ADS-B transmitter (UAT Transmitter in Figure 1.4) is not optimized in terms of size, cost and overall performance. State-art-of-the ADS-B transmitters are fabricated with hybrid integrated circuits (HICs) in three different modules: a Phase Locked Loop (PLL) module, an Up-converter (modulator) module and a Power Amplifier (PA) module as shown

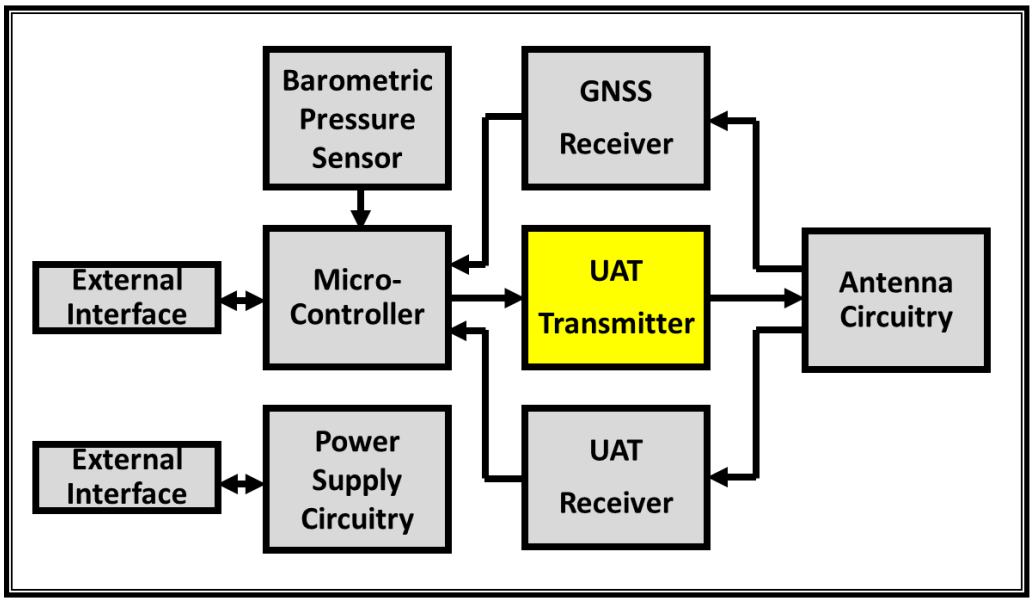

Figure 1.4. The block diagram of functional architecture of UAT beacon radio (UBR).

in the Figure 1.5 [14]. Thus, state-of-the-art ADS-B system are very large in size. Currently the PLL chip and modulator chip are being fabricated either in well matured complementary metal-oxide semiconductor (CMOS) or in BiCMOS (Bipolar CMOS) technology but the PA chip is fabricated in GaAs or in GaN High-Electron-Mobility Transistor (HEMT) technology which is not mature technology and is expensive to fabricate compared to CMOS technology. So, the present ADS-B transmitters are very expensive and very bulky. Hence, it is not a viable approach to use the state-of-the-art ADS-B transmitter for UAS, as micro and small UAS require very smaller payloads. Thus, a lot of R&D is needed to make the ADS-B transmitter compatible for UAS so that UAS can easily be integrated into the NAS.

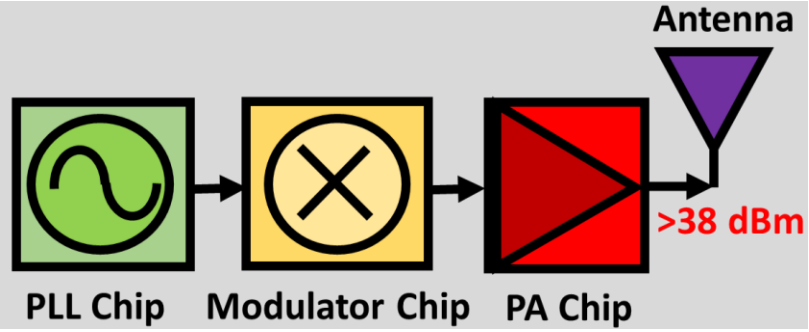

Figure 1.5. State-of-the-art ADS-B Transmitter for UAS System (Multiple Chips).

1.2.2. Literature Survey of Other Transmitters

State-of-the-art performance of the transmitter operating around ADS-B transmitter's frequency and in L (1-2 GHz) / S (2 -4 GHz) / C (4-8 GHz) / Ku (12-18 GHz) is shown in the table 2. The transmitters reported in [15], [20] show the average output power of 20-21.6 dBm, but their target applications are for IEEE WLAN. The transmitter reported in [19] operating in L-band has output power of 15 dBm only and is fabricated in different technology. The transmitters reported in [16], [17], [18], [19], designed in CMOS technology with different process nodes target for cellular applications and achieve respective output power of 4 dBm, 8 dBm, 5 dBm and 11 dBm. The transmitter reported in [21] is designed for micro UAS in 65 nm CMOS technology but

operates with a frequency of 15 GHz and having power of 13.3 dBm. Only the transmitter reported in [10] which is operating at ADS-B frequencies provides higher power but it is assorted with three different modules in printed circuit board (PCB) and is fabricated with hybrid technology.

1.3. Organization of the Dissertation

Chapter 2 will discuss the high-power and high efficiency carrier signal generation for ADS-B transmitter. In this chapter, the design procedure of obtaining high power and high efficiency from CMOS VCO to be integrated into the ADS-B transmitter will discussed. Chapter

Table 2. Performance of the state-of-the-art transmitter operating around ADS-B frequencies

Application	Frequency of Operation (GHz)	Power (dBm)	Technology	Year References
IEEE WLAN 802.111/b/g Dual Band Tx	2.4-2.483 5.15-5.35	8 6	0.25um CMOS	2005 [15]
GSM/EGSM	0.85 / 0.9	4	0.13um CMOS	2008 [16]
GSM 850 / EGSM 900	0.85 / 0.9	8	90nm CMOS	2009 [17]
Cellular CDMA	0.85	5	65nm CMOS	2010 [18]
ADS-B Tx	0.978 1.09	51	HIC	2012 [14]
Multimode Tx	0.95-2.15	11	40 nm CMOS	2013 [19]
L-Band Tx	1-2	15	0.18um BiCMOS	2014 [19]
IEEE WLAN 802.11abgn/ac Dual Band Tx and Rx	2.4 4.9-5.9	20 18.5	55nm CMOS	2015 [20]
Ku Band RDAR For micro UAV	15	13.3	65nm CMOS	2016 [21]

3 will discuss about the high-power and high gain CMOS power amplifier to be integrated into the transmitter architecture. Chapter 4 will present the integration of ADS-B transmitter into CMOS 0.18 um technology. So, this chapter will discuss about the proposed single-chip CMOS transmitter architecture for ADS-B system. Finally, chapter 5 will summarize the technical contribution of this dissertation and will provide future research direction.

CHAPTER 2. HIGH-POWER AND HIGH-EFFICIENCY SIGNAL GENERATION FOR ADS-B TRANSMITTER

To transmit the information at larger distance high output power is required from the ADS-B transmitter. VCO is an important block for ADS-B transmitter to operate reliably at the ADS-B frequencies. Designing a voltage controlled oscillator (VCO) providing high output power will reduce the driver stages of the power amplifier block of the transmitter and thus will reduce the size and power dissipation of the whole transmitter and will save the cost.

In this chapter, the concept of VCO for local oscillator (LO) signal generation will be presented. Different performance metrics of the VCO such as tuning range, phase noise, output power, DC-to-RF power efficiency will be discussed. The chapter will also discuss the design procedure of CMOS based high-power and high-efficiency cross-coupled VCO for ADS-B transmitter of UAS. Finally, measurement results of the two prototypes of the VCO will be presented.

2.1. A Short Introduction of Voltage Controlled Oscillator

An oscillator is a positive feedback amplifier as shown in Figure 2.1 with no applied input signal (but white noise) and with loop gain equal to 1. The transfer function of the system is given by

$$T(s) = \frac{A(s)}{1 - A(s)H(s)} \tag{2.1}$$

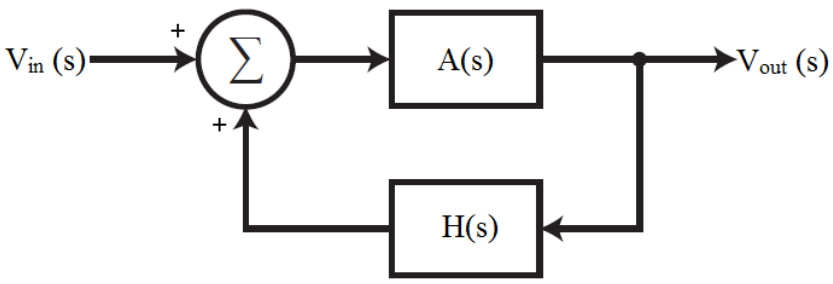

Figure 2.1. The oscillator as a positive feedback amplifier.

The necessary conditions to oscillate, the negative feedback amplifier in Figure 2.1 must follow the Barkhausen's criteria [22] which are

i) Magnitude of the loop gain must be 1, i.e. $|A(s)H(s)|=1$, and

ii) Phase of the loop gain must be 0^0 or an integral multiple of 360^0 i.e. $\angle A(s)H(s) = n\times 360^0$; where n=0,1….

The sufficient condition to start up the oscillation is that the magnitude of the loop gain must be greater than unity. This will allow the system to overcome the losses in the system and to grow the output exponentially. The output amplitude of the oscillator will be limited by the gain compression phenomena due to the nonlinearities in the active device. As Barkhausen's criterion may be met at many frequencies, a resonant tank circuit is used as a filter at the feedback path to set a single frequency of oscillation. So, the oscillator can be considered as a combination of negative resistance generating active part and a passive part of lossy resonant tank tuned to the frequency of oscillation as shown in the Figure 2.2. If the value of negative resistance, -R is larger than the real part of the tank impedance $R_{p,}$ the system will oscillate at the resonant frequency of the tank.

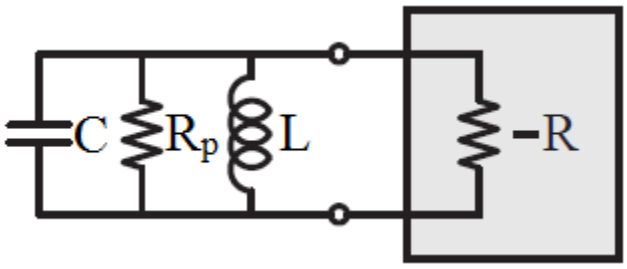

Figure 2.2. The oscillator as a negative resistance generator with passive resonant tank.

2.2. Circuit Design Methodology

To realize the VCO for the ADS-B system, a conventional cross-coupled structure has been considered, as it, being differential in nature, provides better noise performance and even

harmonics cancellation. Two types of VCOs have been implemented. Figure 2.3 and Figure 2.4 shows two types of VCOs with buffer. In the VCO type-1 (Figure 2.3), sources of the cross-coupled transistors pair are connected directly to the ground and gates are biased from outside supply to control the frequency of operation besides the tuning by diode-connected NMOS transistors (TN3 and TN4). This structure can control the output power to some extent by controlling both drain and gate power supply. In the VCO type-2 (Figure 2.4), sources of transistors pair are not connected directly to the ground, but rather through a tail transistor which can steer current through the transistors TN1 and TN2 in the same fashion. In addition, the gate biases of TN1 and TN2 are not controlled from the outside supply but are biased by the DC voltage at the drain of transistors TN1 and TN2. This type of VCO has advantages over the type-2 in terms of higher output power, lower dissipation and lower phase noise. This will be discussed in the following sections and will be showed clearly in the measurement results section 2.3.

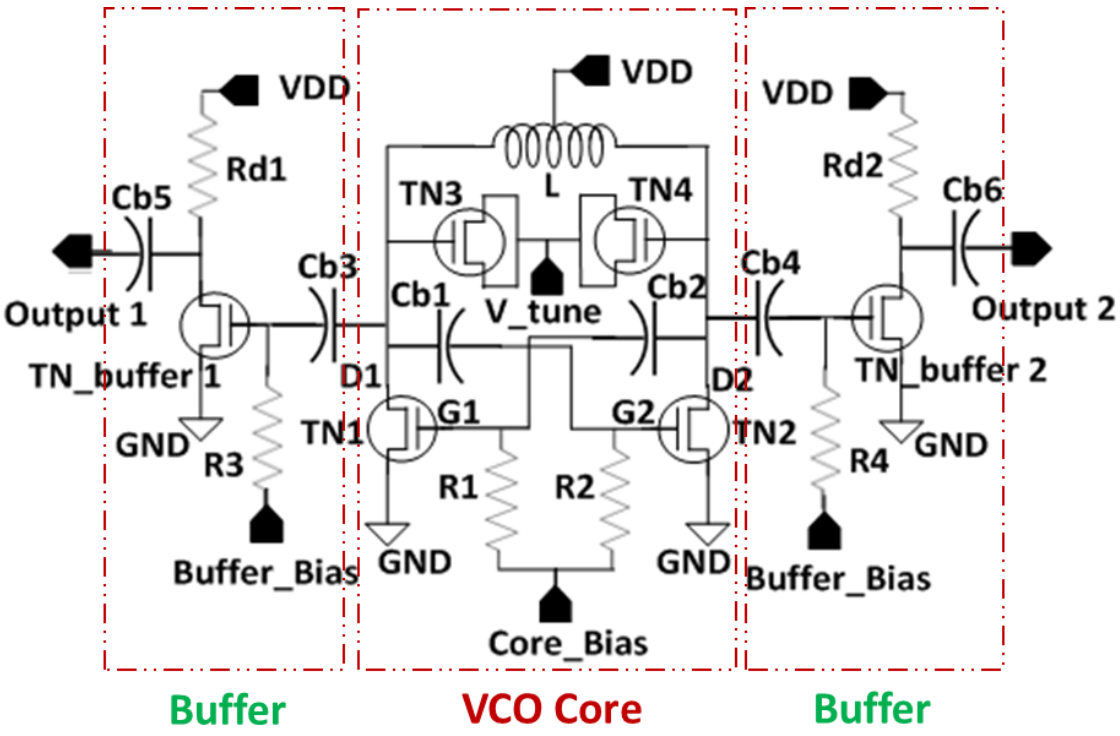

Figure 2.3. The circuit diagram of the VCO type-1 with buffer.

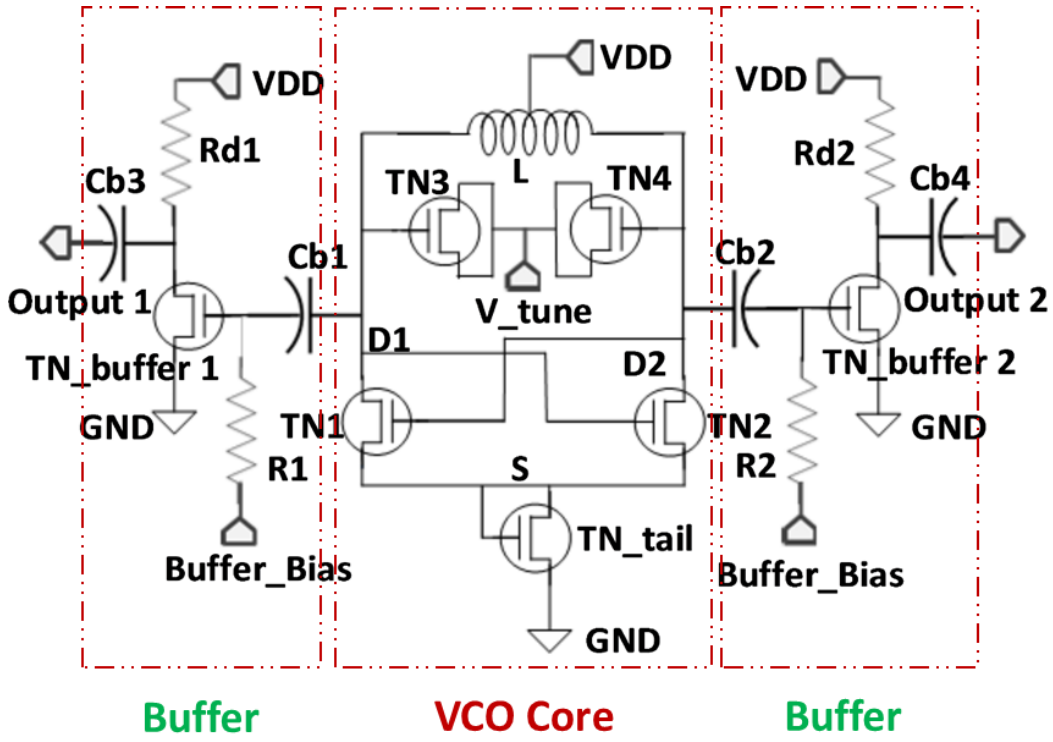

Figure 2.4. The circuit diagram of the VCO type-2 with buffer.

2.2.1. Start-up of VCO

The above VCO core circuit can be represented as two tuned tank amplifiers whose input is the output of the other tuned tank amplifier as shown in the Figure 2.5. The start-up condition

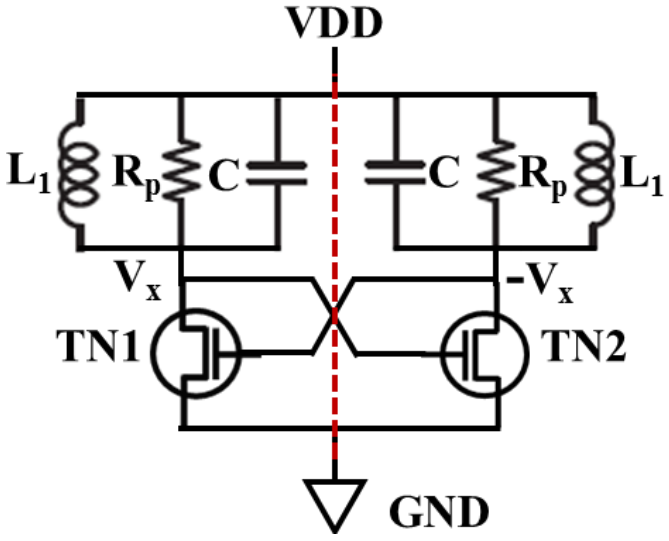

Figure 2.5. The circuit of VCO core in Figure 2.3 and Figure 2.4 after reduction.

can be analysed by considering the half circuit of Figure 2.5. The impedance of the active part of the VCO is parallel to the resonator tank circuit. The impedance of the active part is given by

$$\begin{aligned} I_x &= g_m(-V_x) \\ \Rightarrow Z_x &= \frac{V_x}{I_x} \\ \Rightarrow Z_x &= -\frac{1}{g_m} \end{aligned} \tag{2.2}$$

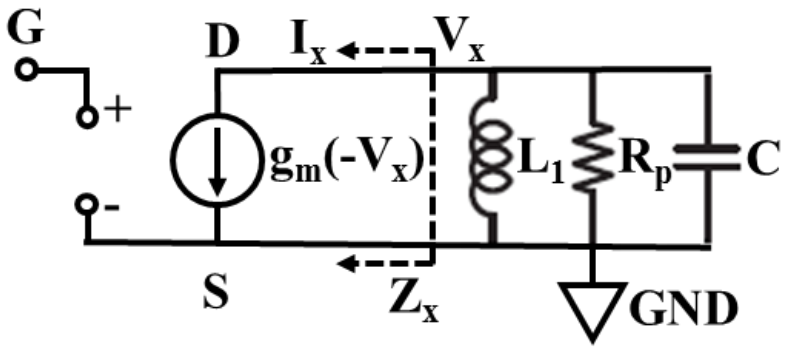

Figure 2.6. Equivalent circuit of one part of two tuned circuits in Figure 2.5.

Now, for the oscillation to occur, the conductance of the active part must be greater than R_p, which is responsible to incur the losses of the tank circuit, i.e.

$$\begin{aligned} |-g_m| &\geq \frac{1}{R_p} \\ \Rightarrow g_m R_p &\geq 1 \end{aligned} \tag{2.3}$$

Another way to get this result is from the Barkhausen's Criterion, i.e., the loop gain of the complete circuit must be greater than unity. The gains of the two half circuits at the resonance are $-g_{m1}R_p$ and $-g_{m2}R_p$. So, the loop gain is given by

$$\begin{aligned} A(\omega = \omega_0) &= (-g_{m1}R_p)(-g_{m2}R_p) \\ &= g_{m1}g_{m2}R_p^2 \\ &= (g_m R_p)^2 \qquad \textit{for} \quad g_{m1} = g_{m2} = g_m \end{aligned} \tag{2.4}$$

For oscillation to occur

$$\left(g_m R_p\right)^2 \geq 1$$
$$\Rightarrow g_m R_p \geq 1 \tag{2.5}$$

2.2.2. Output Amplitude

In the VCO circuit, instead of using a commercial design kit varactor with higher loss, we have used custom designed diode-connected NMOS transistors (TN3 and TN4) as the variable capacitor for tuning the frequency. This arrangement because of its lesser loss and the operation of the VCO at the verge of voltage-limited regime provides a larger DC voltage at the drain of core transistors and consequently helps in extracting high RF output power [23] with high efficiency. Furthermore, the diode-connected tail transistor (TN_tail) which reduces the power dissipation of the core circuit by reducing the current through the core transistors (because it increases the node voltage V_s at S) is also responsible for achieving the high efficiency of the VCO.

To get an idea how the design parameters impact the performance of the output power and efficiency, we have used the Fourier analysis technique [23] to obtain the output power. Figure 2.7 shows the simulated output voltage waveform at the node D1 (G2) and D2 (G1) and simulated current waveform of the transistors TN1 and TN2. During the ON period (T1 for TN1 and T2 for TN2), the transistors operate both in the saturation and triode regions, but they spend most of the ON period in the triode region, and, thus, their conduction current during the ON period can be considered as that of triode region. In the OFF period (T2 for TN1 and T1 for TN2), the transistors pass from the saturation region to cut-off region. As they spend less time in the saturation region than the cut-off region, the conduction of the transistors can be ignored in the OFF period. The relationship between the node voltages (V_{G1} and V_{D2}, V_{G2} and V_{D1}) of the VCO in Figure 2.3 are given by

$$V_{G1} = \frac{V_{D2}}{\left(1+C_{gs1}/C_{b2}\right)\left(1+\omega_1/j\omega\right)} \tag{2.6}$$

$$V_{G2} = \frac{V_{D1}}{\left(1+C_{gs1}/C_{b2}\right)\left(1+\omega_2/j\omega\right)} \tag{2.7}$$

where, $\omega_1=1/R_1(Cgs1 + C_{b2})$ and $\omega_2=1/R_2(C_{gs2} + C_{b1})$, C_{gs1} and C_{gs2} are the gate-to-source capacitances of TN1 and TN2, respectively, and ω is angular frequency of operation. Now, for ω >> both ω_1 and ω_2, and both $C_{b1}>>C_{gs2}$ and $C_{b2} >> C_{gs1}$

$$V_{GS1} = V_{G1} \approx V_{D2} = V_{DS2}, V_{GS2} = V_{G2} \approx V_{D1} = V_{DS1} \tag{2.8}$$

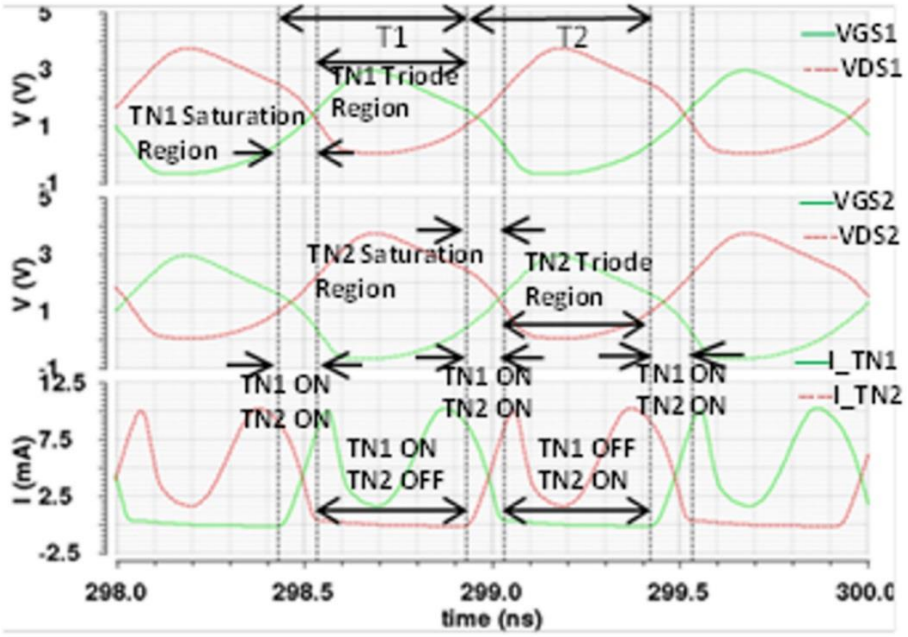

Figure 2.7. Simulated voltage waveforms at the nodes G1 (VGS1), D1 (VDS1), G2 (VGS2), D2 (VDS2), respectively and simulated current waveforms through the transistors TN1 and TN2, respectively.

The drain current through transistor TN1 (for both type of VCOs) during the ON period (neglecting the saturation current) is given by

$$i_{D1} = \mu_n C_{ox} \frac{W}{L_G}\left[\left(V_{GS1}-V_T\right)V_{DS1} - \frac{1}{2}V_{DS1}^2\right] = \beta\left[\left(V_{DS2}-V_T\right)V_{DS1} - \frac{1}{2}V_{DS1}^2\right] \tag{2.9}$$

where, $\beta = \mu_n C_{ox} W/L_G$, V_T is the threshold voltage of the NMOS transistor, μ_n is the electron mobility, W and L_G are the width and the length of the gate, respectively.

Since the i_{D1}, V_{D1} and V_{D2} are periodic, they can be represented by the Fourier series expansion as follows

$$i_{D1} = i_{dc} + \sum_{n=1}^{\infty} i_{e,n} \cos(n\omega t) + \sum_{n=1}^{\infty} i_{o,n} \sin(n\omega t) \tag{2.10}$$

$$V_{D1} = V_{dc} + \sum_{n=1}^{\infty} V_{e,n} \cos(n\omega t) + \sum_{n=1}^{\infty} V_{o,n} \sin(n\omega t) \tag{2.11}$$

$$V_{D2} = V_{dc} + \sum_{n=1}^{\infty} (-1)^n V_{e,n} \cos(n\omega t) + \sum_{n=1}^{\infty} (-1)^n V_{o,n} \sin(n\omega t) \tag{2.12}$$

where, i_{dc} (dc current), $i_{e,n}$, $i_{o,n}$, V_{dc} (dc voltage) , $V_{e,n}$, $V_{o,n}$ are the Fourier series coefficients. The coefficients of the current $i_{e,n}$, $i_{o,n}$ are given by

$$i_{e,n} = \frac{\omega}{\pi}\left[\int_0^{(\pi/\omega)} 0 \cos(n\omega t)dt + \int_0^{(2\pi/\omega)} i_{D1} \cos(n\omega t)dt\right] \tag{2.13}$$

$$i_{o,n} = \frac{\omega}{\pi}\left[\int_0^{(\pi/\omega)} 0 \sin(n\omega t)dt + \int_0^{(2\pi/\omega)} i_{D1} \sin(n\omega t)dt\right] \tag{2.14}$$

As we are interested in the amplitude of the fundamental component of the VCO output, the Eqs. (2.10) - (2.12) reduce to

$$i_{D1} = i_{dc} + i_{e,1} \cos(\omega t) + i_{o,1} \sin(\omega t) \tag{2.15}$$

$$V_{D1} = V_{dc} + V_{e,1} \cos(\omega t) + V_{o,1} \sin(\omega t) \tag{2.16}$$

$$V_{D2} = V_{dc} - V_{e,1} \cos(\omega t) - V_{o,1} \sin(\omega t) \tag{2.17}$$

The output voltage at node D1is equal to

$$V_{D1} = -R_p i_{D1} \tag{2.18}$$

where, R_p, is the equivalent parallel resistance of the inductor's series resistance R_s and, is given by

$$R_p = R_s\left(1 + Q_S^2\right) \qquad \text{and} \qquad Q_S = \frac{\omega L}{R_s} \tag{2.19}$$

Solving Eqs. (2.15) - (2.18) using Eq. (2.9) and Eqs. (2.13) - (2.14) we obtain the Fourier series components of the output voltage as function of Fourier series components of output current as

$$V_{e,1} = -R_p i_{e,1} \tag{2.20}$$

$$V_{o,1} = -R_p i_{o,1} \tag{2.21}$$

The amplitude of the fundamental component of the output voltages V_{D1} and V_{D2} of the VCO is the same and equal to

$$V_f = \sqrt{V_{e,1}^2 + V_{o,1}^2} \tag{2.22}$$

where,

$$V_{e,1} = \sqrt{V_{dc}\left(V_{dc} - 2V_T\right)} \tag{2.23}$$

$$V_{o,1} = \left[\frac{\pi}{4}\left(V_{dc} + V_T\right)\right] - \left[\frac{\pi}{2\beta R_p}\right] \tag{2.24}$$

$$V_{dc} = V_T + \frac{\sqrt{1 + 2\beta R_s\left(V_{DD} - V_T\right)} - 1}{\beta R_s} \tag{2.25}$$

The output voltage of the VCO is given by $20\log\left|V_f\right|$ (in dB). The output power from the buffer will be just V_f multiplied by the gain of the buffer, i.e., $10 + 20\log\left|G.V_f\right|$ (in dBm), where G is the gain of the buffer.

Eq. (2.24) plays an important role in determining the two modes of operation of the VCO: 1) Voltage-limited regime and 2) Current-limited regime [24]. In the current-limited regime, the output amplitude will grow with the bias current until the VCO enters the voltage-limited regime. In the voltage-limited regime, the amplitude of the VCO is limited to a certain voltage, which is determined by the supply voltage and/or the change in the operation of the transistor. If the quantity in the 2nd square bracket of Eq. (2.24) is smaller than the quantity under the 1st square bracket which is the case when β is high or R_p is high (larger inductance gives higher R_p), then the VCO operates in the voltage-limited regime, where $V_{o,1}$ is almost independent of the inductance and frequency. Consequently, the amplitude of the output voltage remains constant with frequency and the inductance of the tank circuit. Whereas for smaller values of the inductance (R_p is smaller) or smaller values of β, $V_{o,1}$ is a stronger function of inductance, frequency, and transistor size, and,

then, the VCO enters the current-limited mode. In the current–limited mode, the amplitude of the output voltage increases with transistor size and the inductance of the tank circuit. But, with the increase of transistor size, the power dissipation increases (as the current through the core transistors increases), and ultimately the efficiency of the VCO reduces. With the increase of inductance in the current-limited regime, the amplitude of the output voltage will increase until the VCO enters the voltage-limited regime. In the voltage-limited regime, output power can be increased by increasing V_{dc}, according to Eqs. (2.22) - (2.24), which in turn can be increased only by reducing R_s, according to Eq. (2.25) [keeping β fixed; if β is reduced to a smaller value to get higher Vdc, the VCO will be no longer in the voltage-limited regime because the quantity in the 2^{nd} square bracket will be higher than that in the 1^{st} square bracket of Eq. (2.24)]. So, to obtain constant output power for the desired frequency tuning range, the VCO must be operated on the borderline of voltage-limited and current-limited regimes avoiding the possibility of 'waste of inductance' and 'waste of power' [24]. To get high RF output power we have reduced series resistance, R_s of the tank circuit by using the inductor of wider spiral width. Moreover, in the VCO circuit, instead of using a design kit varactor, we have used two diode-connected NMOS transistors (TN3 and TN4) as the variable capacitor for tuning the frequency. As the diode connected NMOS transistors are less lossy than the design kit varactor, this arrangement provides larger V_{dc} and hence larger V_f according to the Eqs. (2.22)-(2.25) and consequently helps in obtaining more RF output power from the VCO. Furthermore, we have introduced a diode-connected tail transistor (TN_tail), to the source of core transistors, which increases the voltage at the source node, and which in turn reduces the gate-to-source voltages of TN1 and TN2, and, thus, reduces the current through them. Consequently, the VCO achieves high efficiency in extracting high RF output power.

2.2.3. Frequency of Oscillation

As the transistor nonlinearity has a considerable effect on frequency of oscillation of the VCO, to find out the oscillation frequency, it is necessary to consider the transistor's nonlinear effects. The frequency of oscillation of the cross-coupled LC tank VCO, considering the nonlinear effects of the transistor, is given by [23]

$$f = \frac{1}{\sqrt{LC}\left[2\pi + 4\sin^{-1}\left(\frac{V_{DD} - V_{dc}}{V_f - V_{DD} - V_{dc}}\right)\right]} \tag{2.26}$$

where, $C = C_{eq} + C_{var}$ and C_{eq} is equivalent capacitance at the drain node of the transistor TN1 (or TN2) except the capacitance, C_{var}, and C_{var} is the variable gate capacitance of the NMOS diode, TN3 (or TN4). Eq. (2.26) shows that V_{dc} plays an important role to determine the oscillation frequency. If V_{dc} gets reduced from V_{DD}, the transistor nonlinearity gets increased and the frequency of oscillation gets decreased. If the dc voltage is equal to the supply voltage then the oscillation frequency of Eq. (2.26) becomes

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2.27}$$

Then the frequency of the VCO does not depend on any other factors other than the inductor and equivalent capacitance at the drain node of TN1 or TN2. So, making the dc voltage equal to the supply voltage is a desired design consideration.

2.2.4. Frequency Tuning Range

By using $C = C_{eq} + C_{var}$, Eq. (2.26) can be written as

$$f = \frac{1}{\sqrt{LC_{eq}\left(1 + \frac{C_{\text{var}}}{C_{eq}}\right)}\left[2\pi + 4\sin^{-1}\left(\frac{V_{DD} - V_{dc}}{V_f - V_{DD} - V_{dc}}\right)\right]} \tag{2.28}$$

$$f = \frac{1}{\sqrt{LC_{eq}\left(1+\frac{C_{\text{var}}}{C_{eq}}\right)}\left[2\pi + 4\sin^{-1}\left(\frac{V_{DD}-V_{dc}}{V_f - V_{DD} - V_{dc}}\right)\right]} \tag{2.29}$$

$$f = \frac{\left(1-\frac{C_{\text{var}}}{2C_{eq}}\right)}{\sqrt{LC_{eq}}\left[2\pi + 4\sin^{-1}\left(\frac{V_{DD}-V_{dc}}{V_f - V_{DD} - V_{dc}}\right)\right]} \tag{2.30}$$

$$f = \frac{\left(1-\frac{C_{\text{var}}}{2C_{eq}}\right)}{\sqrt{LC_{eq}}\left[2\pi + 4\sin^{-1}\left(\frac{V_{DD}-V_{dc}}{V_f - V_{DD} - V_{dc}}\right)\right]} \tag{2.31}$$

If the varactor capacitance varies from C_{var1} to C_{var2}, then the tuning range is given by

$$\Delta f = \frac{\left(\frac{C_{\text{var}\,2}-C_{\text{var}\,1}}{2C_{eq}}\right)}{\sqrt{LC_{eq}}\left[2\pi + 4\sin^{-1}\left(\frac{V_{DD}-V_{dc}}{V_f - V_{DD} - V_{dc}}\right)\right]} \tag{2.32}$$

Eq. (2.32) shows that the tuning range also depends on the supply voltage due to the non-linear effects of the device. But this dependency can be avoided by making V_{dc} close to V_{DD}. So, the frequency tuning is performed by varying the capacitance C_{eq}, and this is done by applying the tuning voltage across the NMOS diodes. Figure 2.8 shows the variation of capacitance C_{eq} at the gate of NMOS diodes TN3 and TN4 with tuning voltage. The variation of the capacitance is achieved by choosing their sizes as large as 150 µm and by operating them in the accumulation, depletion and inversion regions over the tuning voltage.

Figure 2.9 shows three different kinds of elements which can be used for tuning the frequency of VCO. The first kind is the design kit varactor diodes which vary capacitance with the

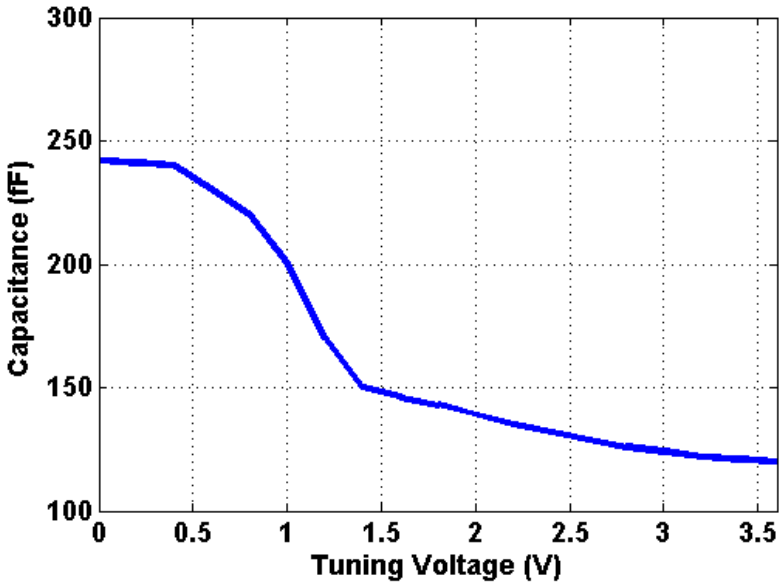

Figure 2.8. Variation of capacitance at the gate of NMOS diodes, TN3 and TN4 with tuning voltage.

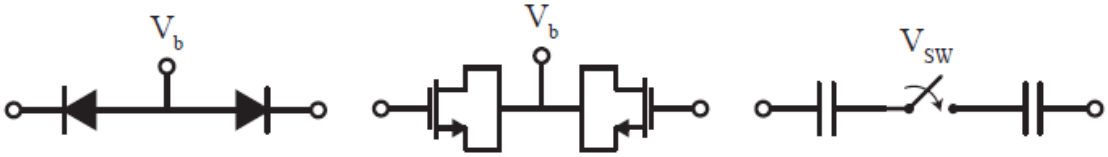

Figure 2.9. Elements for tuning the VCO frequency a) varactor diode b) diode-connected NMOS transistor and c) switched capacitor.

voltage applied at the anode node of the diode. In this case, to turn on the diode, the voltage, V_b must be always positive and in some case, must be greater than the cut-in voltage of 0.35 V or 0.5 V etc. The design kit varactor diodes have different maximum voltage limits depending on the gate oxide thickness and turn-on voltage which depends on the threshold voltage. In any case, availability of low turn-on voltage and larger range of capacitance tuning with larger voltage variation is sometimes impossible in the corresponding technology. In addition, the design kit diodes are lossy. The second kind of capacitance tuning is implemented by using NMOS transistor in the diode connection. Here the applied voltage, V_b may be positive or negative with respect to the gate node. Thus, for diode-connected NMOS tuner, both forward and reverse biased diode capacitance can be utilized. In this kind, larger range of capacitance tuning with larger voltage

variation can be achieved. This kind of arrangement is less lossy than design kit varactor diodes. The third kind of capacitance tuning can be implemented by using a switched capacitor. This arrangement is a discrete type of tuning and needs multiple switches and multiple capacitors to get the whole tuning range compared to the other two types. This is suitable for a narrow tuning range for the same physical areas.

2.2.5. Phase Noise

An ideal oscillator will produce an output of constant amplitude with purely periodic sinusoid at a single frequency without any harmonics as in

$$V_{out}(t) = A\cos(\omega_0 t) \tag{2.33}$$

But, in reality, due to the noise generated within the active devices, the output will differ from its ideal frequency with a time dependent phase, $\phi(t)$ as in

$$V_{out}(t) = A\cos(\omega_0 t + \phi(t)) \tag{2.34}$$

where $\phi(t)$ is the phase noise [25].

The output spectrum of the ideal oscillator will be two impulses at $\pm\omega_0$, but for a real oscillator the output frequency will experience random variations from its ideal frequency ω_0. Consequently, the impulses at $\pm\omega_0$ of the output spectrum get broadened as shown in the Figure 2.10. Phase noise is contributed by three main components: i) conversion of additive noise to phase noise, ii) cyclostationary noise, and iii) time-varying resistance. Open loop Q is a measure of how

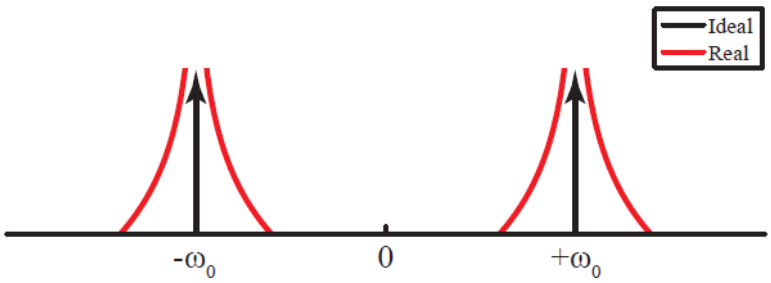

Figure 2.10. Output spectrum of an ideal and real noisy oscillator.

much noise the oscillator is rejecting. But phase noise also depends on how much noise different devices are contributing, the point in time during a cycle when devices are injecting noise, and the output voltage swing (carrier power). Contribution of additive noise to phase noise can be given by Lesson's equation [26] as

$$PN = \frac{1}{4Q^2}\left(\frac{\omega_0}{\omega}\right)^2 \tag{2.35}$$

In this noise calculation, it is assumed that the noise contribution from the devices is constant, but devices in the oscillator performs noise modulation periodically. So, such noise sources are cyclostationary. When both devices are in near equilibrium, they inject maximum noise with a total of two-sided spectral density of $kT\gamma g_m$. But other times such as when a device is OFF, it does not inject any noise, or when it is fully ON, it contributes little noise. In the cyclostationary noise, it is considered that constant conductance is seen between the drains of two devices. But it should be time averaged conductance as it swings between -gm/2 and nearly zero. So, combining the above effects, the phase noise of cross-coupled VCO is be given by

$$PN = \frac{1}{4Q^2}\left(\frac{\omega_0}{\omega}\right)^2\left[\frac{\pi^2}{2}\frac{kT}{I_{ss}^2}\left(\frac{3}{8}\gamma g_m + \frac{2}{R_p}\right)\right] \tag{2.36}$$

where, R_p is the series component converted to parallel given by Eq. (2.19). This R_p is equal to the average resistance at steady state.

The Eq. (2.36) implies that the phase noise can be reduced by increasing the tank open loop Q and I_{SS}. By increasing the tail current, the phase noise declines initially, but, only up to the point where the transistors enter the triode region. Beyond this point, the higher tail current increases the output swing more gradually, but overall tank Q starts to fall, thereby producing no significant improvement in the phase noise.

2.2.6. Figure-of-Merit (FOM)

In the design of the VCO, there are many parameters like frequency of oscillation, tuning range, phase noise, output power, power dissipation etc. to be traded-off with each other. So, to measure the performance of the VCO, it is essential to account for all the VCO parameters. Figure-of-merit (FOM) is such a measure which accounts for all important parameters of the VCO and is given by [27]

$$FOM = PN(\Delta f) - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) - 20\log_{10}\left(\frac{FTR}{10}\right) + 10\log_{10}\left(\frac{P_{DC}}{1mW}\right) \tag{2.37}$$

where, PN (Δf) is the phase noise in dBc/Hz, f_0 is the center frequency, Δf is the frequency offset, FTR is in %, and P_{DC} is power dissipation in mW.

The above Eq. (2.37) takes into account the phase noise, frequency of oscillation, frequency offset, frequency tuning range (FTR), and the power dissipation, but it does not consider the performance of the VCO for generating RF output power and the efficiency of the VCO. Eq. (2.38) is formulated to take account for output power in addition to other parameters in Eq. (2.37) and modified figure-of-merit, FOM_P is given by

$$FOM_P = FOM - 10\log_{10}\left(\frac{P_{out}}{1mW}\right) \tag{2.38}$$

where, P_{out} is RF output power in mW.

When the efficiency of the VCO is taken into account, a new figure-of-merit, FOM_{PE} is obtained and it is given by

$$FOM_{PE} = FOM - 10\log_{10}\left(\frac{P_{out}}{1mW}\right) - 10\log_{10}(\eta) \tag{2.39}$$

where, η is the efficiency is in %, which is defined as the ratio of RF output power to the power dissipation. From Eqs. (2.37)-(2.39), a VCO shows overall better performance if it has lower values of FOM, FOM_P, and FOM_{PE}.

2.3. Measurement Results

Both prototypes of VCO chips are fabricated using a 0.18 µm CMOS process. Figure 2.11(a) and Figure 2.11(b) show the micrograph of the fabricated VCO chips type-1 and type-2, respectively. The dimensions of both types of VCO chips with buffer, considering the bond pad, are 0.738 mm X 0.606 mm and 0.713 mm X 0.638 mm, respectively.

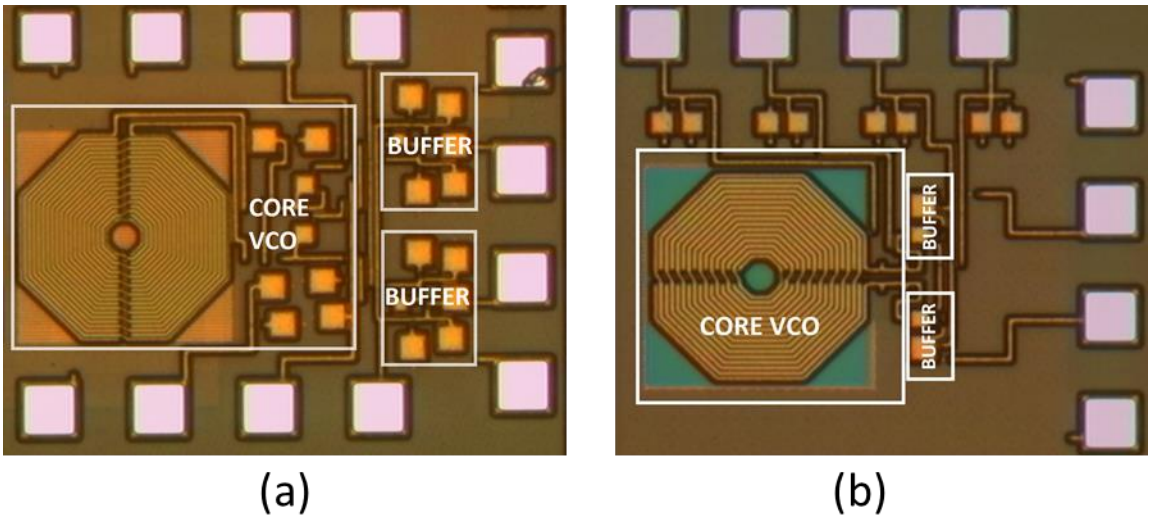

Figure 2.11. Micrograph of (a) 0.738 mm X 0.606 mm (type-1) and (b) 0.713 mm X 0.638 mm (type-2) fabricated VCO chips.

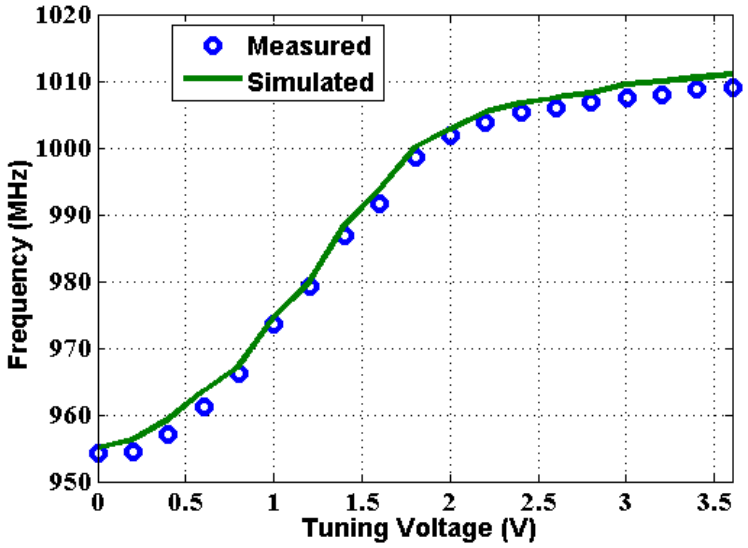

Figure 2.12. Simulated and measured tuning frequency range versus tuning voltage of the VCO type-1.

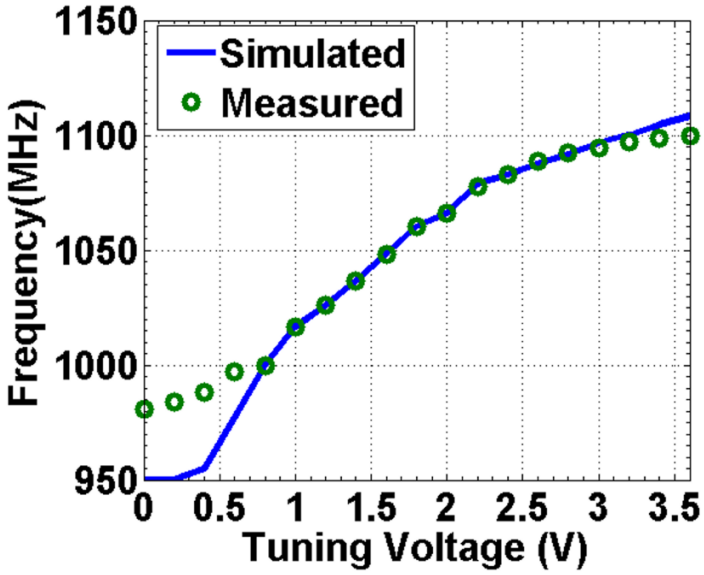

Figure 2.13. Simulated and measured tuning frequency range versus tuning voltage of the VCO type-2.

Figure 2.12 and Figure 2.13 show the respective simulated and measured frequency tuning range of type-1 and type-2 over the tuning voltage from 0 to 3.6V. Excellent agreement between simulation and measurement is achieved in type-1. But there is a small variation of type-2 at the lower tuning voltage. The VCO type-2 has a bandwidth of 120 MHz with the frequency tuning range from 980 MHz to 1100 MHz while the VCO type-1 has a bandwidth of only 55 MHz with the frequency tuning range from 954.3 to 1009.4 MHz.

The single-ended output spectrum of both types of VCO measured with the spectrum analyzer (Tektronix RSA 3408B) are shown in Figure 2.14. The single-ended measured output power of type-1 at 978 MHz is -0.64 dBm and that of type-2 at 980 MHz is 0.62 dBm after de-embedding the cable loss of 1.5 dB. The single-ended peak power for both VCOs were measured to be -0.46 dBm at 1 GHz and 1.4 dBm at the frequency of 1097 MHz, respectively, whereas the differential peak output power from them were 2.54 dBm and 4.4 dBm, respectively. Figure 2.15 shows the simulated and measured output power of VCO type-1 versus tuning voltage. Excellent agreement between simulated and measured results confirms the design accuracy of this VCO. It

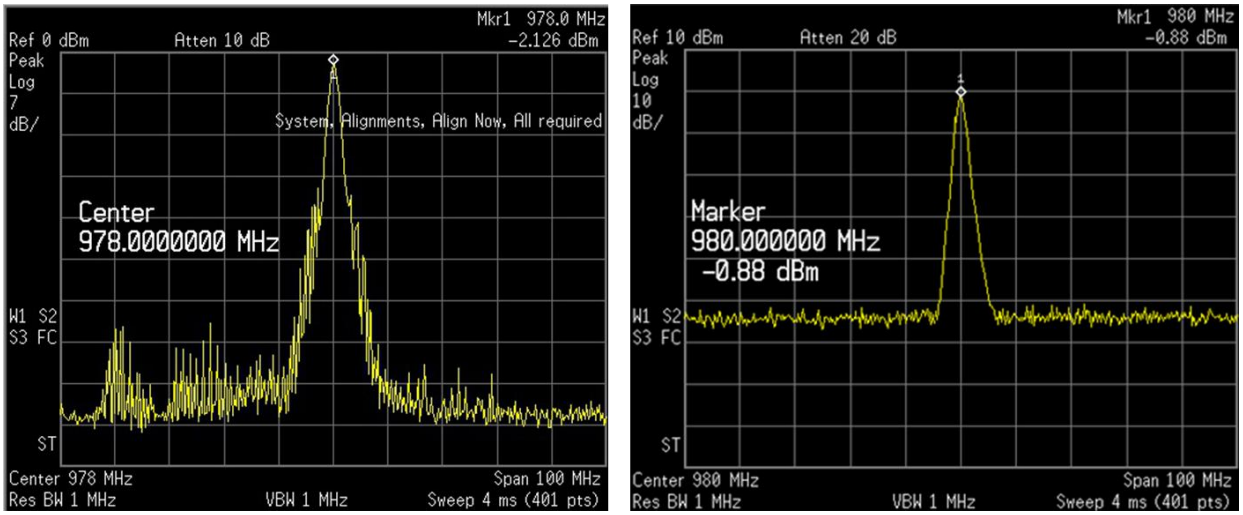

Figure 2.14. Measured output power spectrum of the VCO (a) type-1 at 978 MHz and (b) type-2 at 980 MHz.

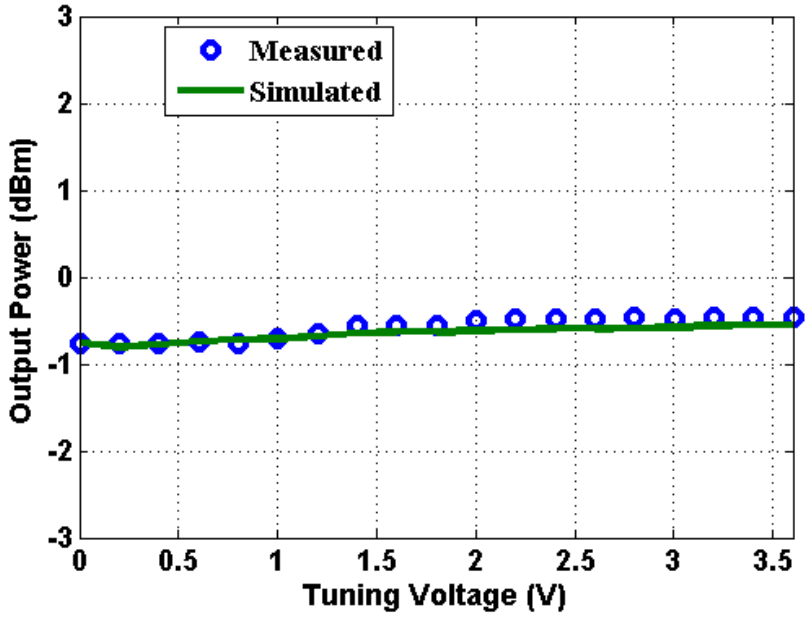

Figure 2.15. Simulated and measured single-ended output power of the VCO type-1 versus frequency.

is clear that the output power is almost constant over the tuning frequency range, which is desirable for the VCO operated in the voltage-limited regime as explained earlier. Figure 2.16 shows the simulated and measured output power and efficiency of VCO type-2 versus frequency. The output power is almost constant over the tuning frequency range as in VCO type-1. Figure 2.16 also shows

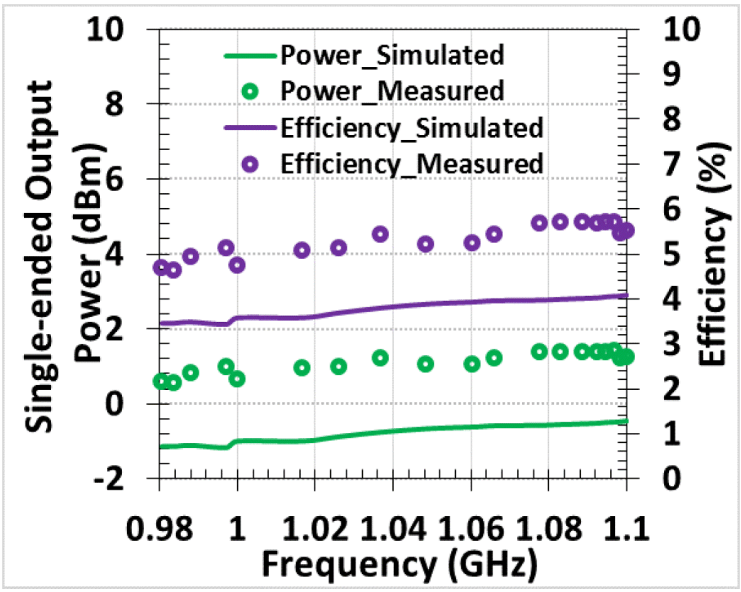

Figure 2.16. Simulated and measured single-ended output power and efficiency of the VCO type-2 versus frequency.

that the variation in efficiency over the frequency range is very low, within 1 %. The VCO core of type-1 consumes 19 mW DC power, whereas the whole chip consumes 35 mW DC power from a 1.8 V DC supply. The core VCO of type-2 consumes 8.5 mW DC power, whereas the whole chip consumes 48 mW from the 1.8 V DC supply. The maximum DC-to-RF power conversion efficiency of type -1 for the whole chip is 5.1% at 1 GHz, whereas the efficiency for the VCO core only is 9.5% (without considering power dissipation of the buffer). The maximum conversion efficiency of type-2 for the whole chip is 5.7% at 1.097 GHz, while that for the VCO core only is 32.5%.

The phase noise of the VCO measured with the spectrum analyzer (Tektronix RSA 3408B) at 1 MHz offset from the center frequency of 978 MHz for VCO type-1 and at 980 MHz for VCO type-2 are shown in Figure 2.17 and Figure 2.18, respectively. The phase noise of the VCO type-2 measured as -125 dBc/Hz is lower than that measured for VCO type-1, which is -109 dBc/Hz. In Figure 2.17 and Figure 2.18, the phase noise at 10 MHz (at 100 MHz) offset are not 20 dB (40 dB) down than at 1 MHz offset because the half of the BW (55 MHz / 2) for VCO type-1 and

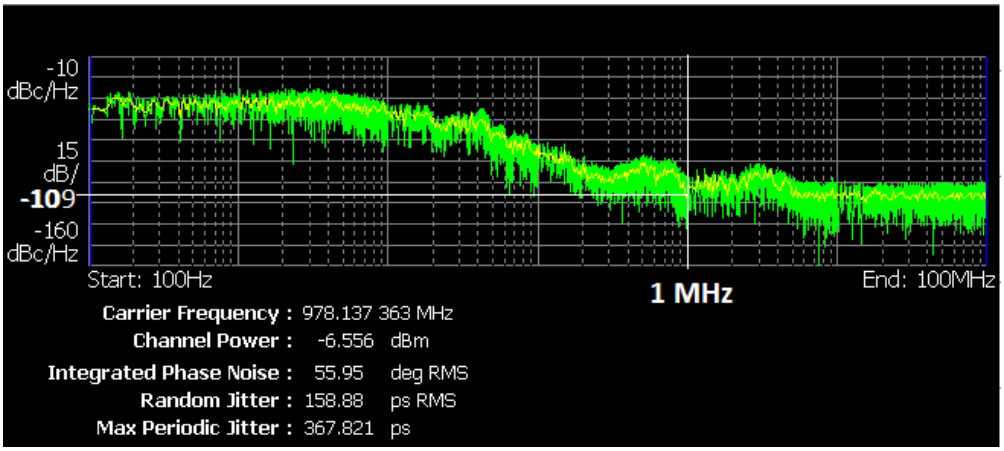

Figure 2.17. Phase noise of the VCO type-1 measured at the center frequency of 978 MHz at an offset of 1 MHz.

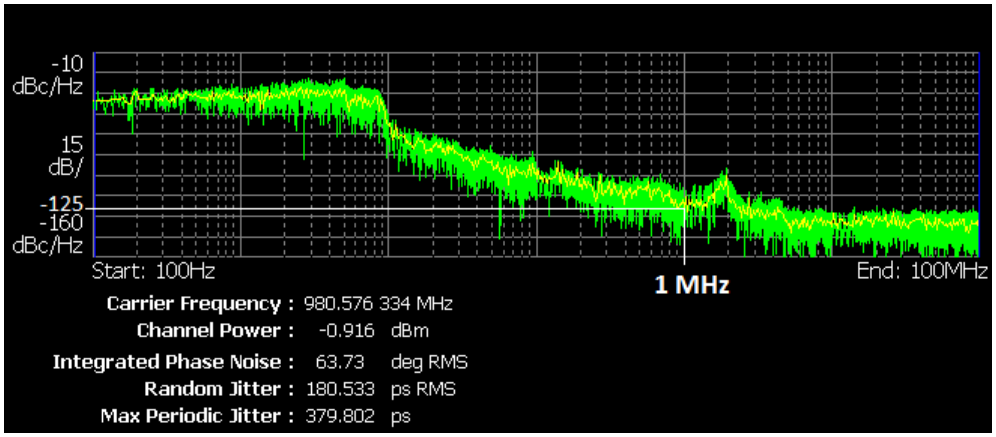

Figure 2.18. Phase noise of the VCO type-2 measured at the center frequency of 980 MHz at an offset of 1 MHz.

(120 MHz / 2) for VCO type-2 is now comparable to or smaller than the frequency offset 10 MHz (100 MHz) which makes the resonator Q term of Lesson's phase noise formula reducing effect or ineffective to the corresponding frequency offset than the other flicker or phase perturbation terms [28]. The variation of phase noise of VCO type-2 with frequency is also shown in Figure 2.19.

The performance of the VCO type-1 and type-2 were measured with four and twenty chips, respectively. Very little offset in the frequency and the output power have been found between the chips for VCO-type-1. For VCO type-2, the frequency tuning range varies across the chips and the respective values of mean, and standard deviation for frequency tuning range are 117.2 MHz and

3.26 MHz, and those for single-ended maximum output power are -0.06 dBm and -8 dBm. The phase noise and FOM_{PE} also varies from chip to chip with the respective mean and standard deviation of -122.63 dBc/Hz @1 MHz and 1.69 dBc/Hz, and -177.1 dBc and 1.79 dBc. However, Figure 2.12 to Figure 2.19 have been presented with the best results of the experiments.

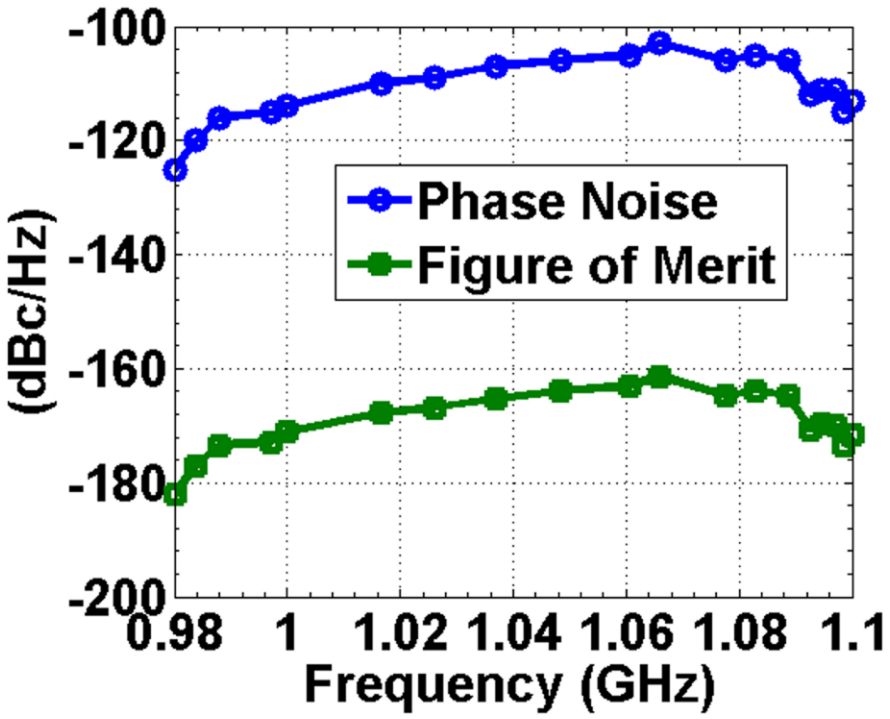

Figure 2.19. Variation of phase noise @ 1-MHz offset and FOM_{PE} with frequency.

To compare the performance of the VCO type-1, FOM_P as in Eq. (2.36) has been considered. The table 3 shows the comparison of the performance of this VCO with state-of-the-art VCO around the frequency of 1 GHz. Although the fabricated VCO type-1 chip shows better phase noise than that of references [29]-[30], [34] only and higher FOM_P than that of references [29]-[31], [34] only, the main achievement of this work is to generate high output power with high efficiency compared to the other VCO chips reported in references [29]-[35], maintaining the other performance parameters within the desirable range.

Table 3. Comparison of the performance of VCO type-1 with the state-of-the-art technology

	This Work	Ref [29]	Ref [30]	Ref [31]	Ref [32]	Ref [33]	Ref [34]	Ref [35]
Technology	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.13um CMOS	65nm CMOS
Frequency (MHz)	978	2900	1670	900	2400	2690	1260	2870
Frequency Tuning Range (MHz)	954.3 ~ 1009.4	500 ~ 3000	500 ~ 2000	834 ~ 997	2150 ~ 2750	2438 ~ 2971	830 ~ 3720	2460 ~ 3020
Voltage Tuning Range (V)	0~3.6	0.3~1.3	0 ~3	0.4~1.2	0~1.8	0~2	0.5~0.87 1 ~ 1.6 -0.5 ~ 1	0~3
Phase Noise (dBc/Hz) (@ 1 MHz offset)	-109	-102	-90.33	-127.8	-121.45	-119.28	-104	-112
Output Power (dBm)	2.54	-20	-20.8	-21	-7.77	-8	-0.9	-13.3
Power Dissipation (mW)	19	28	13.8	37.4	6.98	2.886	13	3.9
Efficiency (%) (VCO Core)	9.46	0.142	0.06	0.021	2.4	5.5	6.25	1.2
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.8	1.5	1.2	1.5
Chip Area (mm^2)	0.447	0.252	0.09*	1.2444	-----	1.278	0.108*	0.2893
FOM_P (dBc/Hz)	-158.56	-142.78	-122.60	-150.1	-172.85	-175.27	-150	-162

*Without bond pad.

To compare the performance of the VCO type-2 chip, FOM_{PE} has been considered. The variation of FOM_{PE} with frequency is shown in Figure 2.19 and the best FOM_{PE} of the whole VCO chip is found at 980 MHz and is equal to -181.5 dBc/Hz (-196.8 dBc/Hz for the VCO core only). Table 4 shows the comparison of the performance of this VCO with state-of-the-art VCOs. An advantage of this VCO chip over the other type is that this VCO type-2 achieves a better tuning range, higher output power, better phase noise, higher efficiency and better overall figure-of-merit,

FOM_{PE}. Although, the VCO type-2 chip better performs than other state-of-the-art VCOs, [29] - [36], in terms of phase noise the main achievement of this VCO is to obtain high RF output power with high efficiency and a high value of FOM_{PE}, at least compared to the other VCO chips in the references [29] - [36] around the operating frequency of 1 GHz.

Table 4. Comparison of the performance of VCO type-2 with the state-of-the-art technology

	This work		Ref [29]	Ref [30]	Ref [34]	Ref [35]	Ref [36]
	VCO type-2	**VCO type-1**					
Technology	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.13um CMOS	65nm CMOS	0.18um CMOS
Frequency (MHz)	980	978	2900	1670	1260	2870	2400
Frequency Tuning Range (MHz)	980 ~ 1100	954.3 ~ 1009.4	500 ~ 3000	500 ~ 2000	830 ~ 3720	2460 ~ 3020	1300 ~ 3800
Phase Noise (dBc/Hz) (@ 1 MHz offset)	-125	-109	-102	-90.33	-104	-112	-94
Single-ended Output Power (dBm)	1.4	-0.46	-20	-20.8	-0.9	-13.3	-10
Power Dissipation (mW)	48 (8.5*)	35 (19*)	28	13.8	28.6 (13*)	3.9	5
Efficiency (%)	5.7 (32.5*)	5.1 (9.5*)	0.142	0.06	2.84 (6.25*)	1.2	2
Chip Area (mm^2)	0.455	0.447	0.252	0.09†	0.108†	0.2893	0.098†
FOM_{PE} (dBc/Hz)	-181.5 (-196.8*)	-165.6 (-168.3*)	-153	-132	-177 (-184*)	-169	-168

*Calculated without considering buffer power consumption. † Without bond pad.

2.4. Conclusion

In this chapter, the concept of differential LO signal generation for an ADS-B transmitter has been discussed. High-power and high-efficiency LC cross-coupled CMOS VCOs are developed to be integrated into an ADS-B transmitter. Two types of VCO prototypes have been

developed. By operating on the borderline of voltage-limited and current-limited mode, and using custom designed diode-connected NMOS transistors as variable capacitors, the VCO type-2 delivers single-ended peak output power of 1.4 dBm and differential peak output power of 4.4 dBm at 1.097 GHz and maintains almost constant output power over the entire frequency tuning range of 120 MHz. Additionally, using diode-connected tail transistor, the VCO achieves a core efficiency of 32.5%, and the whole chip efficiency of 5.7%. The VCO type-1 has an advantage of better control of the frequency of oscillation. On the other hand, the VCO type-2 has several advantages over the other VCOs such as higher output power, better tuning range, lower phase noise, higher efficiency and higher figure-of-merit. The state-of-the-art performance comparison shows this CMOS VCO type-2 delivers the highest reported output power with highest efficiency and highest figure-of-merit around a 1 GHz operating frequency, to the best of author's knowledge, with good phase noise performance and desirable tuning range. This shows the promising applications for realizing a high-power single-chip CMOS based ADS-B transmitter.

CHAPTER 3. HIGH-POWER AND HIGH-GAIN CMOS POWER AMPLIFIER FOR ADS-B TRANSMITTER

3.1. Introduction

Power amplifier (PA) is an essential component in microwave and millimeter wave (MM-wave) systems finding applications in a broad range of areas such as telecommunication, radar [37]-[39], electronic warfare, heating [40]-[41] and medical microwave imaging [42]-[47], just to name a few. With such diverse applications, the specifications of the PA greatly differ in operating, technological and design requirements. Regardless of the applications, the basic functionality of the PA is to increase the power level at the output.

Recently, both cellular and avionics industries are finding low-cost, compact wireless solution for smart phones and unmanned aircraft system (UAS), respectively. A fully integrated transceiver is the best solution for low-cost and small-sized devices. Incorporating a same device for multiple applications is one step more. As mentioned earlier, the ADS-B transmitter is optimized for the manned aircraft system but not for UAS. The power amplifier block is manufactured with GaAs / GaN technology to obtain the required transmitted power. This is costly, bulky and essentially demands a different technology, other than CMOS technology [14], [48] - [49]. So, this is not an appropriate option to use GaAs or GaN PA to the ADS-B transmitter for UAS because it will increase the payload of UAS. On the other hand, a PA with mature CMOS technology will enhance the integration level and ultimately reduce the cost. Many techniques have been followed recently to improve power [50]-[52], power added efficiency [52], and bandwidth [53] of a PA. But most of them suffer from low large signal gain. The gain directly impacts the figure-of-merit of the PA. Additionally, higher gain acts to maximize the PAE as PAE= $\eta(1-1/G)$, where, η is the efficiency and G is the gain. There are many applications which need

input power to be less than -5 dBm and output power higher than 24 dBm from a pre-driver of L-band radars such as 1090 MHz secondary surveillance radar in a lineup for 54 dBm or more [54]. This indicates a driver having higher gain may exclude the requirement of a pre-driver in a lineup for high power. So, in this chapter design of a CMOS PA targeting to achieve high power and high gain with multiple applications such as in avionics and cellular will be discussed. A new method of current combining technique ("resistive current combining" technique) will be introduced to achieve high output power as compared to reactive current combining. Measurement results of a CMOS PA prototype will be presented. As the PA design generally evokes the trade-off between some conflicting parameters such as output power level, power gain, linearity, efficiency, and bandwidth. So before going to PA design to obtain high power, these conflicting parameters are discussed briefly.

3.2. Output Power and Power Gain

The output power, P_{out} of a PA is the average power delivered to the external load (usually a 50 Ω load) at a frequency f and is given by

$$P_{out}(f) = \frac{1}{2}\mathrm{Re}\left\{V_{out}I_{out}^{*}\right\} \tag{3.1}$$

while the input power, P_{in} is the available power at the input of the PA at the same frequency and is given by

$$P_{in}(f) = \frac{1}{2}\mathrm{Re}\left\{V_{in}I_{in}^{*}\right\} \tag{3.2}$$

The power gain, G of the PA is the ratio between output power to the input power, i.e.

$$G(f) = \frac{P_{out}(f)}{P_{in}(f)} \tag{3.3}$$

As the active device behaves nonlinearly with the high input drive level, the power gain due to the nonlinear behavior of the PA depends on the input signal level. The power gain of the PA after a specified point (P_{1dB}, discussed in the next section) gets compressed and is no longer an actual linear power gain of the PA.

3.3. Linearity

3.3.1. P_{1dB}

The PA experiences nonlinearity because of the compressive input-output characteristics of the active device. The output power in the Figure 3.1 linearly increases with the input power and then the device enters the saturation region and the output power increases sub-linearly with the input power. So, the gain remains initially constant with the input power and then drops. One of the measure of nonlinearity of PA is the P_{1dB}, a point where actual output power of the PA is 1 dB below the ideal linear output power (extrapolated line). So, $P_{in,1dB}$ and $P_{out,1dB}$ are the linear input and output power levels respectively beyond which the device gets heavily saturated and the

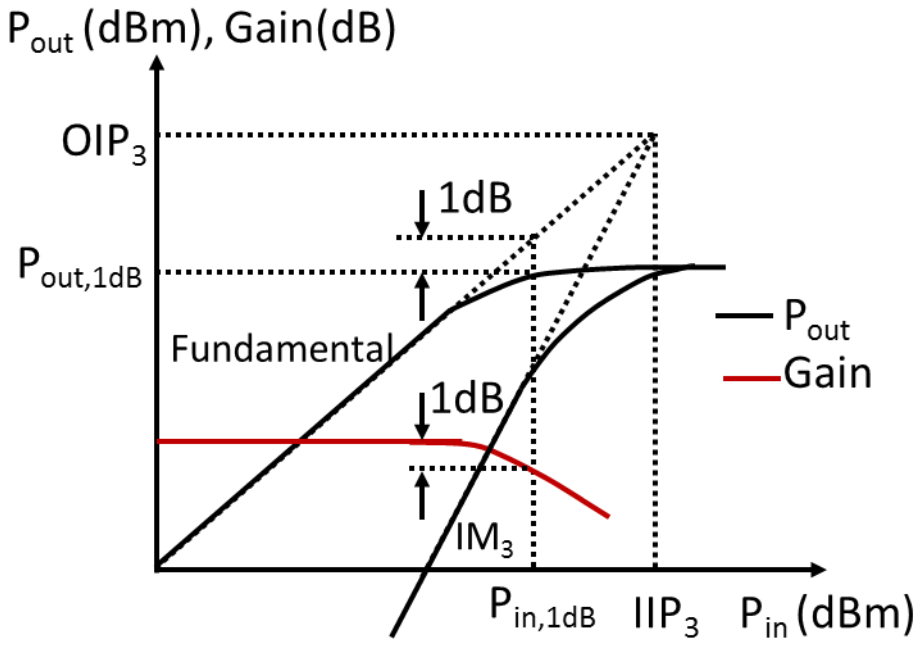

Figure 3.1. Output power and gain versus input power showing P_{1dB} point and IP3 point.

gain gets heavily compressed. The expression of the P_{1dB} can be obtained by considering the device is experiencing the 3rd order nonlinearity. The output, y(t) is given by

$$y(t) = \alpha_1 x(t) + \alpha_2 [x(t)]^2 + \alpha_3 [x(t)]^3 \tag{3.4}$$

Now, considering the input, x(t) = A cos (ωt), the Eq can be written as

$$\begin{aligned} y(t) &= \alpha_1 A\cos(\omega t) + \alpha_2 A^2 \cos^2(\omega t) + \alpha_3 A^3 \cos^3(\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \end{aligned} \tag{3.5}$$

Now, the input P_{1dB} is found by equating the difference between the output power of the fundamental component with compression and the same without compression to -1 dB, i.e.

$$\begin{aligned} &20\log\left|\alpha_1 A_{in,1\,dB} + \frac{3\alpha_3 A_{in,1\,dB}^3}{4}\right| - 20\log\left|\alpha_1 A_{in,1\,dB}\right| = -1dB \\ &\Rightarrow P_{in,1\,dB} = 0.145\left|\frac{\alpha_1}{\alpha_3}\right| \qquad \text{where, } P_{in,1dB} = A_{in,1\,dB}^2 \end{aligned} \tag{3.6}$$

3.3.2. Intermodulation (IM) Product

The output of the PA may show nonlinear effects that may not manifest themselves in gain compression and harmonic distortion [55]. One of the measure of such nonlinear effect is the intercept point, precisely, the third order intercept point (IP3). If two interferers at ω_1 and ω_2 are applied to a nonlinear system, due to mixing of two frequencies the output of the system consists of two components of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, which are called 3rd order intermodulation (IM3) products and are closer to the components of ω_1 and ω_2, and may corrupt the desired output signal. If the transmitter sends the desired signal accompanying with these IM signals, and the power of the IM signals are comparable to the desired signals and/or the power of them are sufficient to desensitize the receiver, it's very hard for the receiver to demodulate the desired signal. The IM3 products can be obtained by expressing the input signal $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$ in Eq. (3.4). So, the output, y(t) is given by

$$
\begin{aligned}
y(t) &= \alpha_1[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)] + \alpha_2[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)]^2 + \alpha_3[A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)]^3 \\
&= [\text{DC Terms}] + \left(\alpha_1 A_1 + \frac{3\alpha_3 A_1^3}{4} + \frac{3\alpha_3 A_1 A_2^2}{2}\right)\cos(\omega_1 t) + \left(\alpha_1 A_2 + \frac{3\alpha_3 A_2^3}{4} + \frac{3\alpha_3 A_2 A_1^2}{2}\right)\cos(\omega_2 t) \\
&+ \frac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_1 - \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_2 - \omega_1)t + \frac{3\alpha_3 A_1 A_2^2}{4}\cos(2\omega_1 + \omega_2)t \\
&+ \frac{3\alpha_3 A_1^2 A_2}{4}\cos(2\omega_2 + \omega_1)t + [2\omega_1, 2\omega_2 \text{components}] + [\omega_1 \pm \omega_2 \text{components}] \\
&+ [3\omega_1, 3\omega_2 \text{components}]
\end{aligned} \tag{3.7}
$$

In the Eq. (3.7) the components of $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ are 3rd order IM products. But, only $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are of our interest as they fall closer to the fundamental components ω_1 and $2\omega_2$. Now the IP3 points are the input and output powers where the fundamental output power intersects the output power of the IM3 products. This point is determined by equating the output power of the fundamental components to that of the IM3 components, i.e.

$$
20\log\left|\frac{3\alpha_3 A_{IIP3}^3}{4}\right| = 20\log\left|\alpha_1 A_{IIP3}\right|, \quad \text{considdering } A_{1,IIP3} = A_{2,IIP3}
$$

$$
\Rightarrow IIP3 = \frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right| \qquad \text{where, } IIP3 = A_{IIP3}^2 \tag{3.8}
$$

$$
\Rightarrow \frac{IIP3}{P_{in,1dB}} = \frac{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} = 9.6\ dB \quad \text{using Eq. (3.6)} \tag{3.9}
$$

where, IIP3 is the 3rd order input intercept power and is given by Eq. (3.8). The relationship between IIP3 and $P_{in,1dB}$ is given the Eq (3.9). The 3rd order output intercept power, OIP3 is given by

$$
OIP3 = IIP3 + G \tag{3.10}
$$

where, G is the linear gain of the PA. A higher value of OIP_3 indicates better linearity performance of the PA. For cascaded amplifier, the equivalent IIP3 is given by the

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{\alpha_1^2}{IIP3_2} + \frac{\alpha_1^2 \alpha_2^2}{IIP3_3} + ... \tag{3.11}$$

where, $IIP3_1$ $IIP3_2$ and $IIP3_3$ are the IIP3 of the 1st, 2nd and 3rd stages, and α_1 and α_2 are the gain of the 1st and 2nd stages. From Eq. (3.11), the IIP3 of cascaded amplifier is lower than a single-stage amplifier.

3.3.3. AM/PM Conversion

When the amplitude of the input of the PA is varying with time (that is the case for dynamic system with memory), the output of the PA experiences nonlinear phenomena both in amplitude and phase. If the input, x(t) is considered as

$$x(t) = A(t)\cos[\omega t + \theta(t)] \tag{3.12}$$

then, the output of the PA can be given as

$$y(t) = G[A(t)]\cos[\omega t + \theta(t) + \Phi[A(t)]] \tag{3.13}$$

The Eq. (3.13) shows that the output amplitude of the PA varies with the time varying input amplitude (i.e., the input drive level) which leads to AM/AM compression effects. Phase of the output also varies with the input drive level leading to the AM/PM conversion.

3.4. Efficiency and Power Added Efficiency

The efficiency, an important performance parameter of a PA, is defined as the ratio of output RF power to the input DC power as in the following equation

$$\eta = \frac{P_{out}}{P_{dc}} \tag{3.14}$$

The Eq. (3.14) shows that the efficiency does not consider the input power contribution to the output power. So, another performance parameter, power added efficiency (PAE), which considers the input power contribution to the output power, plays an important role in designing the PA. The

PAE is the ratio of the power added, P_{add} i.e. net increase in the signal power from the PA to the input DC power and is defined as

$$PAE = \frac{P_{add}}{P_{dc}} = \frac{P_{out} - P_{in}}{P_{dc}} = \eta\left(1 - \frac{1}{G}\right) \tag{3.15}$$

So, for a high gain PA, the PAE is almost the same as the efficiency of the PA.

3.5. Stability of Power Amplifier

The stability of the PA is a major issue in designing a PA. Power amplifier stability is typically verified and ensured by using small signal stability criteria based on Rollet's K factor and the Rollet proviso [56] – [57]. In order to be unconditionally stable, the following condition has to be met [58]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1 \tag{3.16}$$

where, $\Delta = S_{11}S_{22} - S_{12}S_{21}$ (3.17)

combined with one of the following conditions:

$$|\Delta| < 1 \tag{3.18}$$

$$b_1 = \frac{1 - |S_{11}|^2}{|S_{12}||S_{21}|} > 1 \tag{3.19}$$

$$b_2 = \frac{1 - |S_{22}|^2}{|S_{12}||S_{21}|} > 1 \tag{3.20}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \tag{3.21}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 > 0 \tag{3.22}$$

To avoid cumbersome checking of the above two criteria, the Eq. (3.16) and any one of the Eq. (3.18) - Eq. (3.22) together, a single μ-test based on a geometrical parameter is followed [59] and is expressed as

$$\mu_1 = \frac{1-|S_{11}|^2}{|S_{22}-S_{11}^*\Delta|+|S_{12}S_{21}|} > 1 \tag{3.23}$$

$$\mu_2 = \frac{1-|S_{22}|^2}{|S_{11}-S_{22}^*\Delta|+|S_{12}S_{21}|} > 1 \tag{3.24}$$

The above criteria for stability should be fulfilled not only at the desired frequency range but also at other frequencies. This small signal stability test does not ensure the stability for the large signal, but due to the unavailability of a correct approach to check large signal stability or nonlinear stability, it is better to have the value of K-factor or μ as large as possible maintaining the desired gain of the PA. Stability of a multi-stage PA becomes very difficult at microwave and MM-wave frequencies. To make the PA stable, each stage of the PA must be stable. Instability of a PA can be avoided by reducing the gain of the unstable stage or introducing losses in that stage.

3.6. Class of Operation of Power Amplifier

A PA can be classified depending on the bias level regardless of the input drive level. So, depending on the fixed bias point or current conduction angle (CCA) of the active devices, the PAs are generally of four types: i) Class A, ii) Class B, iii) Class AB and iv) Class C. In this class grouping it is assumed that the input of the PA is sinusoidal. Only the CCA varies among different classes of PA. Figure 3.2 shows different classes of operation of a PA. Classes A, B, AB and C have a CCA of 2π, π, $\pi < \phi < 2\pi$, and $\phi < \pi$, respectively. Efficiency has a direct link with the CCA of active devices. With the reducing CCA of the active device, the efficiency increases as the device is dissipating DC power for a shorter period.

More advanced power amplifier classifications can be made depending on the dynamic operating conditions of the active device and the matching network termination. Two broad categories are identified in this classification: i) switching-mode and ii) current-mode. In the switching-mode PA [55], the active device behaves like a switch so that the DC power gets dissipated only during the switching transition of the active device. Thus, the switching PA has very high efficiency, 100% for the ideal switch-mode PA. Depending on the switching duty-cycle

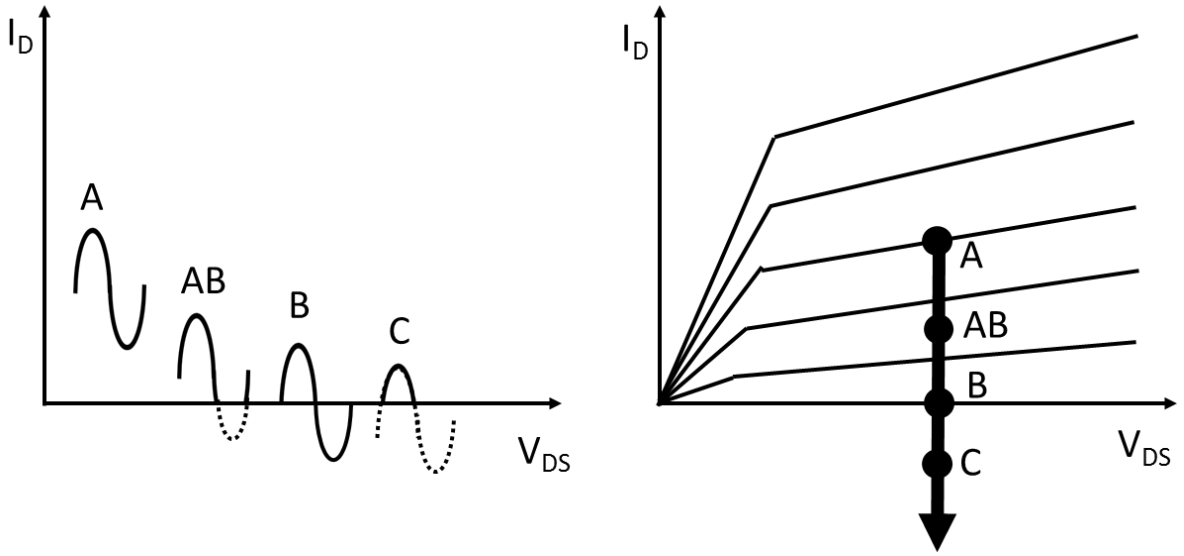

Figure 3.2. Class of operation of power amplifier depending on the output current conduction angle (left) and on the fixed device quiescent point (right).

Table 5. Class of operation and efficiency of PA

Class	Current Conduction Angle (CCA)	Linearity	Theoretical Efficiency
A	360^0	Best	50%
AB	180^0 - 360^0	Good	50-78.5%
B	180^0	Moderate	78.5%
C	< 180^0	Poor	78.5-100%
D, E, F, G, H, S…	0^0	Non-linear	100%

of the active device, switching-mode PAs can be classified into i) Class D, ii) Class E, iii) Class G, iv) Class H, v) Class S…etc. In the current-mode PA, the active device acts like a voltage controlled current source (CMOS) or current controlled current source (BJT). In these PA, harmonic termination (HT) across the active device, i.e. wave-shaping phenomena are being adopted to improve the output power and/or efficiency. Depending on the criteria of wave-shaping adopted, these PA can be classified as i) Class 2nd HT, ii) Class 3rd HT or Class F, iii) Class 2nd HT and 3rd HT… etc. The table 5 shows the class of operation with CCA, theoretical efficiency and linearity. Detail discussion on the classification of the PA is out of scope of this work.

3.7. Challenges in Designing High-Power and High-Gain PA

Designing PA in CMOS technology is a cost-effective solution in current transceiver architecture. But the CMOS solution has its own drawbacks. With the down-scaling of the technology the oxide breakdown voltage goes down which force the PA to operate at lower supply voltages. This makes designing a PA to get high output power a challenging task. To deliver 1 W power to a 50 Ω load, the device plane needs to supply more than 1 W power. If it is considered that the output matching network (OMN) is loss less and a single device is delivering 1 W power, then the peak voltage, V_p across the device having equivalent impedance of R_T is given by

$$\frac{V_p^2}{2R_T} = 1W \tag{3.25}$$

The table 6 shows the peak voltage required across the device for different impedance value of the device to deliver 1 W power to the load. So, for 0.18 um CMOS technology, as the breakdown voltage is 1.8 V, the device output impedance needs to be lowered than 1.6 Ω. So, the impedance transformation ratio becomes 50/1.6 = 31.25. This large impedance transformation is not possible with a single impedance transformer. This will lead to an insertion loss of the OMN.

On the other hand, lossy inductor to be used in the OMN will provide more loss leading the device to generate more power than it is assumed before to deliver 1 W power. Consequently, this will end up with lowering the device plane impedance further of the value lower than 1.6 Ω. The 2-stage OMN consisting of design kit inductor has loss of 2-3 dB. Considering 2 dB loss of OMN, the value of the device plane impedance is required to be 1.6 X $10^{\wedge(-2/10)}$ = 1 Ω. So, for 2 dB loss in the OMN, the efficiency gets reduced by 33.33%. On the other hand, a single device cannot handle a large amount of current of 880 mA to deliver 1 W power with a loss of 2 dB in the OMN. The requirement of this large amount of current will create thermal and reliability issues of the device. So, to obtain high power from the PA without affecting the thermal and reliability issues of the device, it is required to use combining techniques such as current combining, voltage combining or power combining techniques. In the following section 3.8, different combining techniques will be discussed.

Table 6. Peak voltage required across the device for different device plane impedance to deliver 1 W power

R (Ω)	Vp (V)
10	4.47
5	3.16
2	2
1.6	1.8
1	1.4
0.5	1

3.8. Classification of Power Combining Technique

Because of the high-power requirements in different application, a huge number of different combining solutions have been made so far [60]-[62]. So, a unique classification is almost impossible. However, in broad, PA can be classified in two groups: i) spatial-level ii) circuit-level. In spatial-level, the power combining is performed in unbounded [63] or partially bounded [64] region, and is accomplished by transmit/receive radiating elements, i.e. antennas [65]. Such kind of power combiners are grid type [66], patch type [67]-[68] and rectangular waveguide type [69]. On the other hand, in circuit-level combiners, the power is supposed to confined within a finite region, so that the radiation through the combiners are considered as undesirable phenomena and lossy occurrence [60]-[61]. Because of relative dimensions in wavelength, the circuit-level combiners are smaller than spatial-level. Thus, circuit-level combiners are adopted in lower end of microwave and millimeter-wave frequencies, whereas the spatial-level combiners find applications in millimeter-wave frequencies [65], [70]. Circuit-level combiners can be classified in two groups: i) resonant type and ii) non-resonant type combiners. To properly combine the power signals, resonating properties are applied to the combining structures. Example of this kind of power combining are rectangular, cylindrical or radial structures which are used in microwave and millimeter-wave frequencies [71]-[72]. Planar type of resonating power combiners are patches, ring or sector components. Resonating power combiners are generally narrowband type but having high power capabilities, whereas non-resonating combiners are used in broadband applications with low power capabilities. Non-resonating combiners are i) cavities or ii) transmission line (TL) based structures, where metal lines / conductors are used to propagate the waves. TL based combiners can be categorized into two groups: i) N-way combiners and ii) corporate combiners. Example of N-way combiners are Wilkinson combiner (two-way or

generally N-way) [73], hybrid structures (branch-line, rat race, Lang coupler, etc.), planar multiports, bus bar, etc. [55]. In N-way combiners, N input ports are properly combined into an output port in a single step. On the other hand, in corporate combiners a tree-structure of M-way (typically, M=2 or 3) combiners is used to combine a large number of input ports, N (N>M) into output port in S number of cascaded sections such that, $N=M^S$ [74]. As in corporate combiner, many internal loops are generated, their stabilities become bottleneck of the overall stability of the combiner. This issue can be reduced by utilizing the symmetry in binary corporate combiner, i.e. with M=2 [57], [75]-[77].

Power combining techniques can be classified into three groups depending on the type of combining parameters of current, voltage and power [78]:

1) Direct Power Combining Technique [55]
2) Voltage Combining Technique [78], and
3) Current Combining Technique [79]

3.8.1. Direct Power Combining Technique

In this approach, several power devices combine their power with an arbitrary impedance. The combining can be done with many devices in one stage with termination of 50 Ω as in N-way Wilkinson combiner or with many devices in several stages (N stages) with gradual impedance transformation in successive stages such that final stage of the combiners terminates to 50 Ω load as in corporate power combining. So, these kinds of combiners do not need output matching network (OMN). At high frequency of operation, the impedance transformation is achieved by λ/4 transmission lines. So, these types of power combiners suffer from some combining losses at each stage but free from losses incurred in the OMN. Also, the losses due to parasitic at high frequencies become prominent in addition to TL based combining losses. Despite of these losses they are

widely used in III–V microwave and mm-wave PAs. Realizing the impedance transformation section at low frequency near 1 GHz requires the use of lumped capacitor and lossy inductors because, no longer TL based impedance transformation can be used due to the longer wavelength. Thus, at low frequency these types of combiners provide more combining losses at each stage, but losses due to parasitic becomes less prominent. However, the loss in both TL based and element based power-combining networks in combination with its parasitic loss through the conductive silicon substrate limits the output power, efficiency, and bandwidth of power-combined silicon-based PAs. Moreover, power combiners occupy large silicon area, leading to high implementation cost. Nevertheless, in the absence of other viable approaches, this technique is in common use to implement microwave and mm-wave CMOS PAs [80]-[87].

3.8.2. Voltage Combining Technique

In voltage combining topology, as shown in the Figure 3.3, two or more transistors are stacked so that the overall voltage swing is increased with the increase in output impedance [88]-[90], ultimately increasing the output power. Stacking of transistors helps to overcome the low breakdown voltage of scaled CMOS technologies. Several stacked PA designs have been reported so far in the literature where stacking of transistors is performed in three ways: i) stacking a common-source (CS) stage with several common-gate (CG) transistors [91], ii) stacking several CS cells with input transformers [92], and iii) combination of the above two approaches by implementing cells of CS and/or cascode with input transformers used for dc isolation [93]. In the first kind of stacking, the output power is limited by the gate-oxide breakdown voltage, stability issues and the top bypass capacitor whose value approaches to parasitic values. Only a maximum of four transistors have been stacked successfully so far. In the second kind of stacking, the power gain and power-added efficiency (PAE) are the main issues and are usually limited because of the

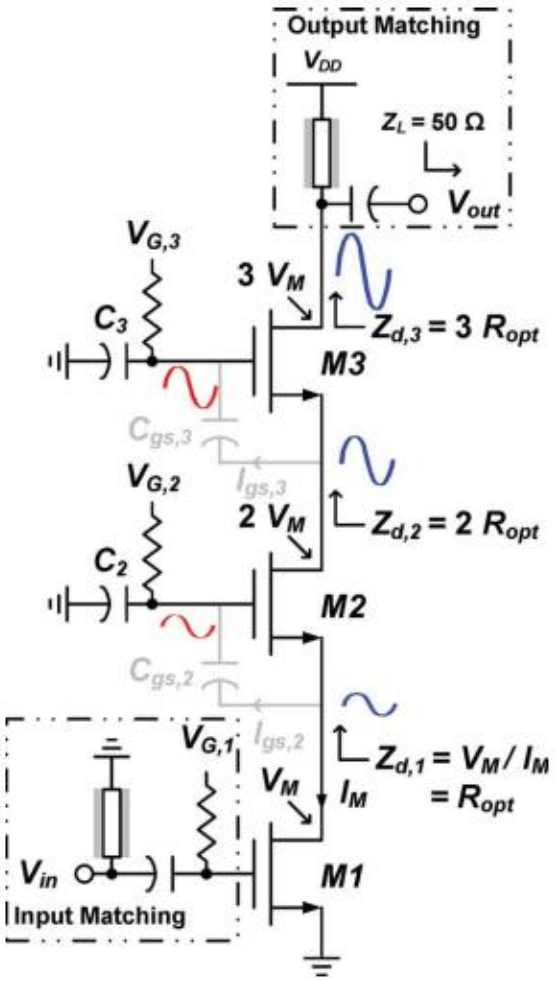

Figure 3.3. Stacked NMOS transistors showing voltage combining phenomena with increased impedance at the output (adapted from [91]).

use of relatively lossy transformer for each CS transistor in the stack. The third approach combines the advantages of the two other approaches by facilitating stacking of more than four transistors (cascode instead of CS stage) through the utilization of input transformers and dynamic biasing of transistors and thus output power, gain, and PAE can be increased. But, still its output power is limited by the voltage combining efficiency. The voltage combining technique has advantages of consuming smaller areas and providing good efficiencies for moderate amount of output power [91]-[93]. One main drawback of the voltage combining technique is the failure of one of the devices in the stack. If one device gets failed due to the breakdown of the gate-oxide or if any of

the devices does not draw any DC current due to the bias problem, no power will be obtained at the output. If it is considered that no such problem is manifested, still the output power and PAE may severely get affected by inefficient voltage combining. If the output voltage from each device is not combined in the same phase and/or in proper amplitude, the overall output swing may not increase, thereby reducing total output power and efficiency. In addition, due to the AM-PM conversion, the output voltage waveform will be distorted affecting the overall linearity of the PA [94]. Also, voltage combining technique demands for requirement of high power supply than other kinds of combining.

3.8.3. Current Combining Technique

In current combining topology, parallel combination of transistors is used to increase the overall output current while the individual transistors are subjected to an identical output voltage equal to the maximum allowable voltage across one device. Thus, the total output power at the device plane gets increased. At low frequency, the N-way current combining technique in M-stages (where $N=2^M$) doesn't not require any impedance transformation network for each current combining section. This technique reduces both input and output impedances and requires OMN to transform the low device plane impedance to the 50 Ω load. OMN, when implemented on a silicon chip, are lossy and degrade the output power, bandwidth, and efficiency of the PA. Because of high impedance transformation ratio, the loss incurred by the OMN may be higher than the losses incurred in impedance transformation network at each stage of the N-way corporate type or N-way Wilkinson power combiners. However, if the number of combining stages becomes more (for $N \geq 2$), the total losses in the latter case of power combiners is more than that in the OMN in current combining technique. In this technique, a high current flowing through a parallel combination of multi-finger transistors has both short and long-term reliability concerns, leading

to thermal runaway and catastrophic failure of the PA [95] if proper number of fingers of the device, power trace, ground plane and other interconnecting traces are not designed to meet both DC and AC current limit. Current combining can be categorized in two ways:

i) Reactive current combining, and

ii) Resistive current combining.

3.8.3.1. Reactive Current Combining Technique

In reactive current combining, as shown in Figure 3.4, the currents from several devices get combined in a phase different from the phase of voltage across the devices. The total current from this kind of combining is given by

$$I_{combined} = |I_1|\angle\theta_1 + |I_2|\angle\theta_2 + \cdots\cdots + |I_n|\angle\theta_n \tag{3.26}$$

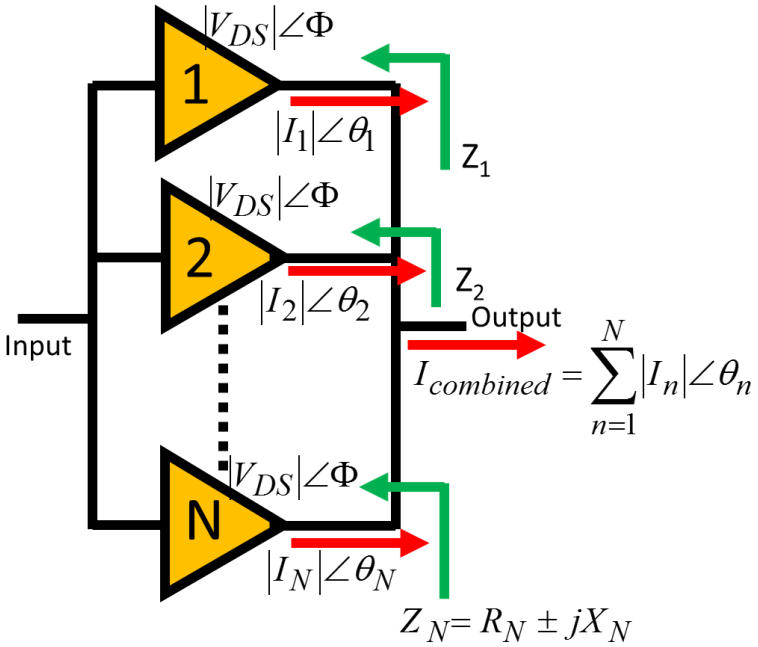

Figure 3.4. N-stage of reactive current combining.

The equivalent device plane impedance is given by

$$\frac{1}{Z_{combined}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \cdots\cdots + \frac{1}{Z_N} \tag{3.27}$$

where, $Z_N = R_N \pm jX_N$ and $\angle(\Phi - \theta_N) = \pm \tan^{-1}\left(\frac{X_N}{R_N}\right)$ (3.28)

The reactive current combining can happen with all the currents get added in same phase to each other. In that case, the impedance looking into each device are same and hence their equivalent device plane impedance is just output impedance of a single device divided by the number of current combiners, i.e. Z_1/N. In reactive current combining, the capacity of total power extraction from fixed number of devices is lesser than the resistive current combining.

3.8.3.2. Resistive Current Combining Technique

In resistive current combining, the currents from several devices are combined with same phase with the voltage across the devices. The total current from this kind of combining is given by

$$I_{combined} = |I_1|\angle\Phi + |I_2|\angle\Phi + \cdots\cdots + |I_n|\angle\Phi \quad (3.29)$$

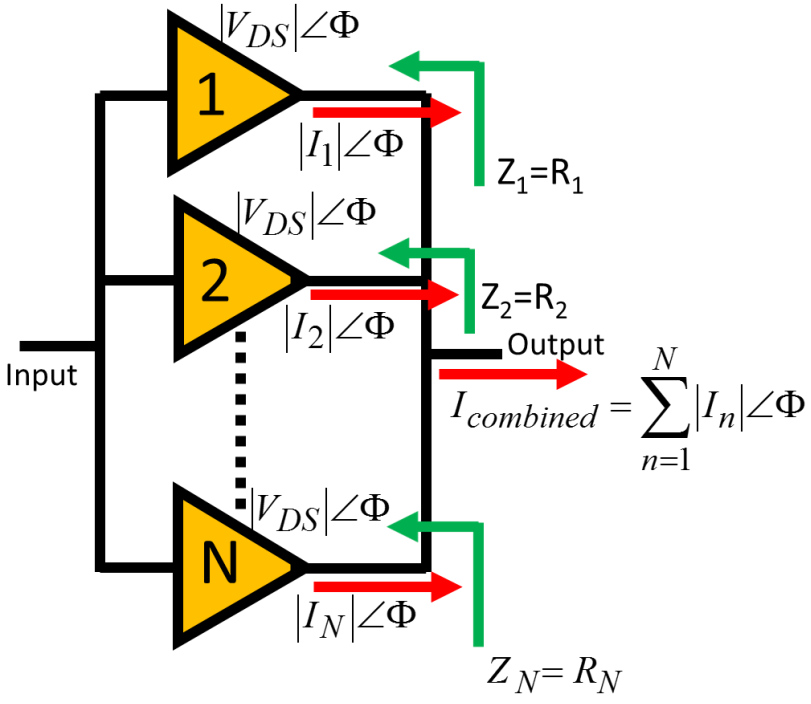

Figure 3.5. N-stage resistive current combining.

The equivalent device plane impedance is given by

$$\frac{1}{R_{combined}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots\cdots + \frac{1}{R_N} \tag{3.30}$$

In this technique, current basically combines at the resonance which occurs with device capacitive impedance and inductive load and thus extract more power from the device than the reactive current combining. Figure 3.5 shows the idea of resistive current combining. In this case, the output impedance from a single device is always resistive and hence the equivalent device plane impedance. When all devices are identical, the equivalent device plane impedance is given by R_1 / N. Details of resistive current combining will be discussed in the circuit design procedure in section 3.10.

3.9. Figure-of-Merit (FOM)

As the performance of a PA has several conflicting parameters such as power, gain, bandwidth, and PAE, the improvement of one parameter over the other does not reflect the overall performance of the PA. So, to account for overall performance of the PA, the figure-of-merit (FOM) is considered and it is given by [53]

$$FOM = P + G + 20\log B + 10\log(PAE) \tag{3.31}$$

where, the output power (P) is in dBm, the power gain (G) is in dB, the bandwidth (B) is in GHz and the PAE is in %.

3.10. Circuit Design Methodology

Figure 3.6 shows the circuit schematic of the proposed power amplifier designed with cascading four stages. The size lineup of the transistors of the successive stages are 90 µm, 420 µm, 2x1.3 mm, 4x2 mm, respectively. High power gain is achieved by using 1st stage, 2nd stage as voltage gain amplifiers, and 3rd stage, 4th stage as power gain amplifiers. Each stage provides required gain to the next stage. The gain of the successive stage is reduced so that the amplified

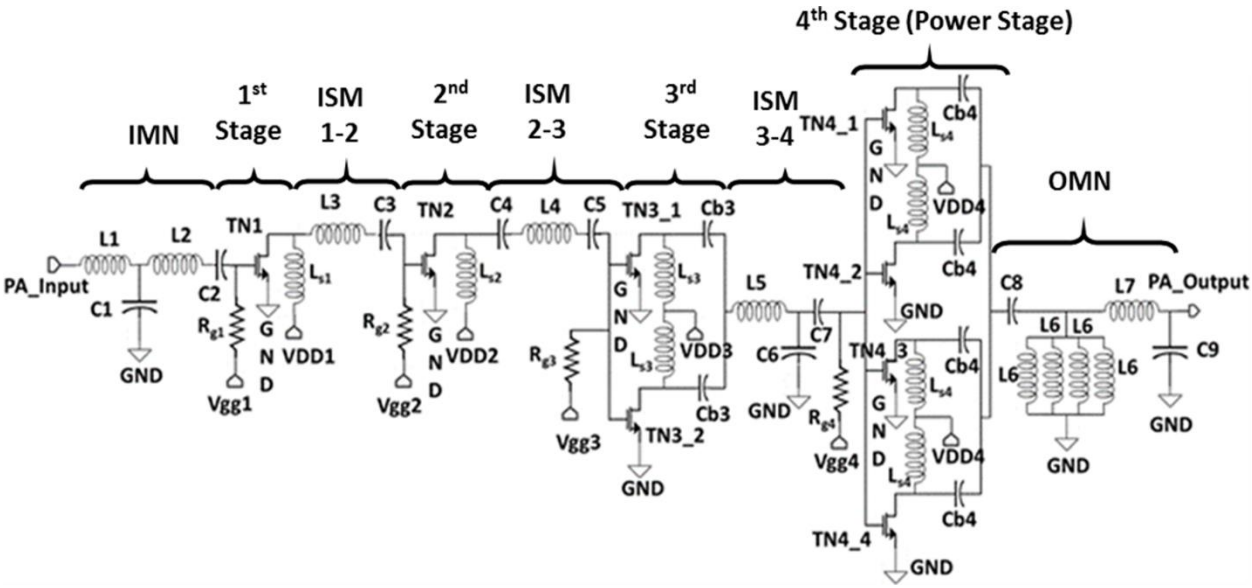

Figure 3.6. Circuit diagram of 4-stage power amplifier with IMN and OMN.

voltage and/or power to the input of the next stage does not heavily saturate the amplifier. Thus, this will avoid the possibility of nonlinearity due to the saturation of the following stages. Due to improper matching between stages the power may be lost at the input of the next stage and the voltage swing across the device may cross the limit of the breakdown voltage. To avoid these possibilities, conjugate matching is followed for inter-stage matching (ISM) between 1st - 2nd stage, 2nd - 3rd stage, and 3rd - 4th stage. The supply inductors of the 1st, and 2nd stages have been used as an element for the 1st - 2nd stage ISM and 2nd - 3rd stage ISM, respectively.

3.10.1. Combining Mechanism

High power gain and large power handling are achieved by adopting resistive current combining technique at the 3rd and 4th stages. Figure 3.7 shows the block diagram of the N-cell (N-way) or M-stage resistive current combining technique. In the first stage, the currents from two devices combine resistively with impedance $R_{eq}/2$, where R_{eq} is the equivalent impedance of 1-cell device. In second stage, four devices combine the current resistively with impedance $R_{eq}/4$. Similarly, in the M-stage, 2^M devices combine the current with the impedance of $R_{eq}/2^M$. If the 1-

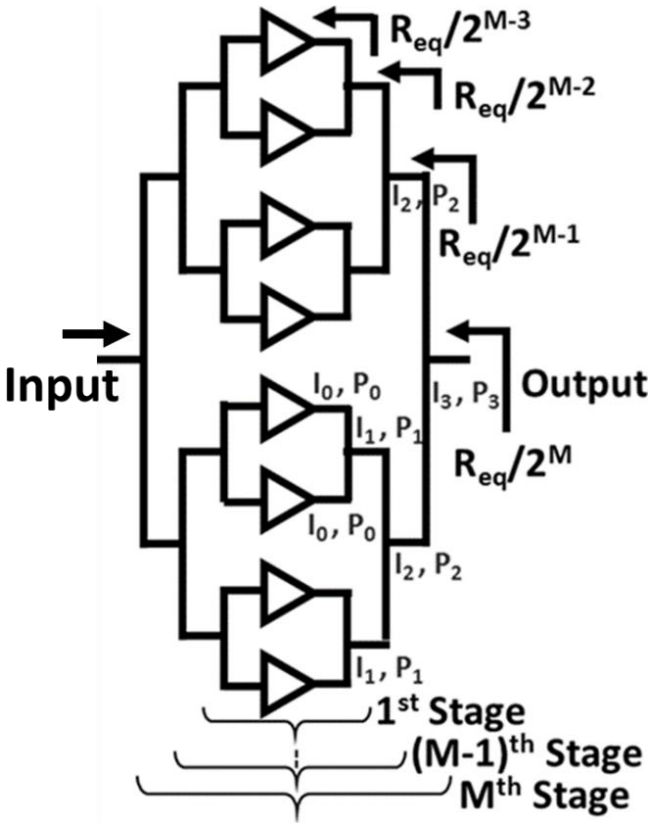

Figure 3.7. M-stage resistive current combining showing the combining mechanism with 1-transistor unit cell.

cell device supplying power P_0 with current I_0, then $P_0 = I_0^2 \times R_{eq}$. If I_1 is the current from 1-stage current combiner, then $I_1=2I_0$ and the power, $P_1 = I_1^2 \times R_{eq}/2=(2I_0)^2 \times R_{eq}/2=2I_0^2 \times R_{eq} = 2P_0$. Similarly, the current and power from the M-stage current combiners are $I_M=2^M \times I_0$ and $P_M = I_M^2 \times R_{eq}/2^M = (2^M \times I_0)^2 \times R_{eq}/2^M =2^M \times I_0^2 \times R_{eq} = 2^M \times P_0$ respectively. Output impedance of 1-cell device is made resistive by resonating out the device equivalent capacitance, C_d with the on-chip supply inductor. At high frequency, the resistive current combining can be achieved by using $\lambda/2$ transmission lines at the output of 1-cell resonator. But, at low frequency, no transmission line is required rather the output ports of N-cell resonators are required to place close enough to avoid both magnitude and phase mismatches between the output current of each cell resonator. Even placing the input ports of N-cell resonators close enough in the layout compared to the wavelength

corresponding to the highest frequency of operation will ensure to avoid odd-mode excitation due to mismatch in phase and magnitude at the inputs. [55].

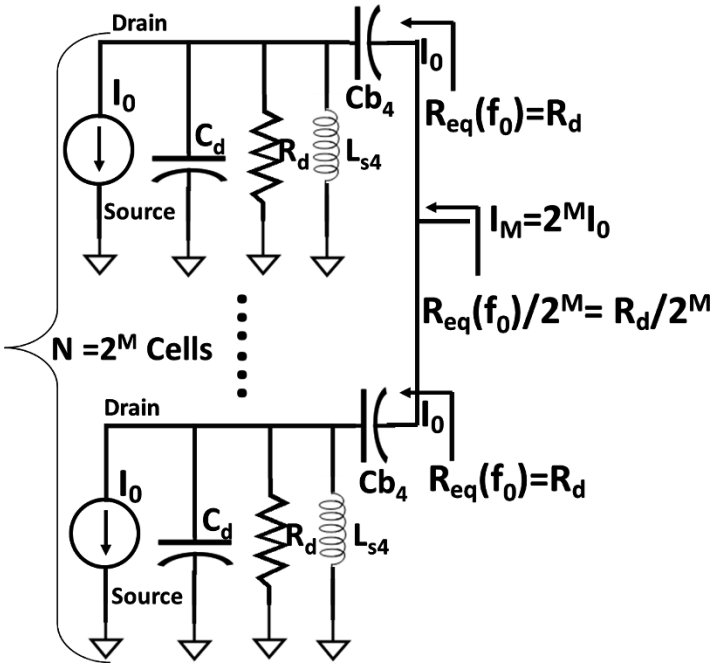

Figure 3.8. AC equivalent circuit for resistive current combining at the 4th stage of the PA.

Figure 3.8 shows AC equivalent circuit of N-cell current combiners (or M-stage current combiners) of the 4th stage formed by device impedance, supply inductor and blocking capacitor so that its impedance is resistive. In this work, 1-stage (2-cell) resistive current combiner for 3rd stage and 2-stage (4-cell) resistive current combiners for 4th stage have been implemented. By using two wider transistors in parallel and supply inductors, L_{s3} at the 3rd stage, and four wider transistors in parallel and supply inductor, L_{s4} at the 4th stage forms the 2-cell and 4-cell current combining resonators, respectively. Thus, the current from each transistor gets combined resistively with optimum load termination of $R'_{eq}/2$ for 3rd stage and $R_{eq}/4$ for 4th stage, where R'_{eq} and R_{eq} are the equivalent resistive component of 1-cell device of 3rd and 4th stage, respectively. The arrangement of absorbing the supply inductor as matching element for resonator cell saves the wastage of power incurred by the lossy on-chip inductor in the case of RF choke, where high value

of inductor is required. Figure 3.9 shows the smith chart of the output impedances of 4th stage for 1-cell resonator, 2-cell resonators (1-stage combining), 4-cell resonators (2-stage combining). Although the output impedance of 1-cell resonator is not purely resistive at lower frequencies, but has very low inductive reactance of 0.2 Ω, whereas the output impedances of 2-cell and 4-cell resonators are purely resistive for the frequencies ranges from 825 MHz to 1115 MHz.

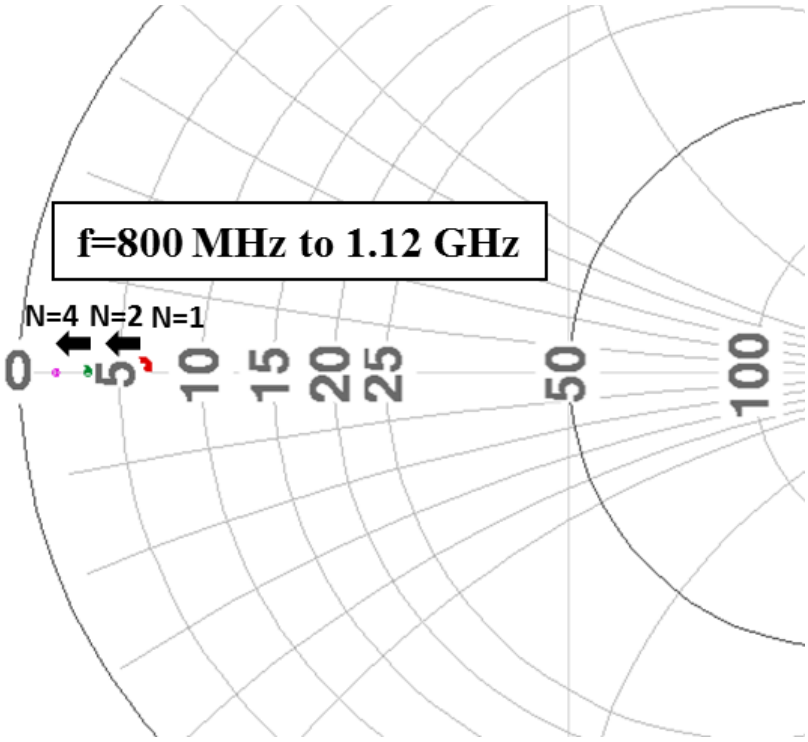

Figure 3.9. Smith chart of output impedance of the 4th stage for 1-cell, 2-cell, and 4-cell resonators.

Now L_{s4} is chosen such that maximum power occurs at the resonant frequency,

$$f_0 = \frac{1}{2\pi\sqrt{L_{s4}C_d}} \tag{3.32}$$

The power from 1-cell resonator is given by

$$P_0(f_0) = I_0{}^2 R_{eq}(f_0) \tag{3.33}$$

The power from N-cell current combiners (M-stage combiners) is given by

$$P_M(f_0) = 2^M I_0{}^2 R_{eq}(f_0) = N I_0{}^2 R_{eq}(f_0) \text{ , where } N = 2^M \tag{3.34}$$

For maximum power transfer, the power is delivered to the optimum load, $R_{opt} = R_{eq}/N$ from N-

cell combiners and the power is given by the following equation

$$P_{opt}(f_0) = \frac{N}{4} I_0{}^2 R_{eq}(f_0) \tag{3.35}$$

where,

$$R_{eq}(f_0) = \frac{R_d \; X_0^2(f_0)}{R_d{}^2 + X_0^2(f_0)} \quad \text{and} \quad X_0(f\;) = (2\pi f L_{s4})\left[1 - \left(f \big/ f_0\right)^2\right]^{-1} \tag{3.36}$$

For resistive current combining technique, $X_0(f_0) = \infty$. So, $R_{eq}(f_0) = R_d$ and

$$P_{opt}(f_0) = \frac{N}{4} I_0{}^2 R_d \tag{3.37}$$

where, R_d is the resistive component of output impedance of a single device.

Now, if different value of supply inductor is chosen such as L'_{s4} and dc blocking capacitor is not very high enough to consider X_{cb4} negligible, the current combining will be reactive. The output power for reactive current combining, considering the optimum load as complex conjugate of output impedance at the device plane, will be:

$$P_{opt}(f_c) = \frac{N}{4} I_0{}^2 R_{eq}(f_c) \tag{3.38}$$

where,

$$R_{eq}(f_c) = \frac{R_d \; X_0^2(f_c\;)}{R_d{}^2 + X_0^2(f_c)} \quad \text{and} \quad X_0(f_c\;) = (2\pi f_c L'_{s4})\left[1 - \left(f_c \big/ f_0\right)^2\right]^{-1} \tag{3.39}$$

As at $f = f_c$, $X_0(f_c)$ has some finite value, $R_{eq}(f_c)$ will be lower than R_d and hence the power, $P_{opt}(f_c)$ will be lower than $P_{opt}(f_0)$. Thus, resistive current combining gives higher output power and hence higher power gain. Now within 3-dB bandwidth the variation of the reactive component of device impedance is low and can be neglected, so the current combining is almost resistive.

In case of current combiner, if any one block in the chain is not working, still there will be output power but with reduced power level, which is not possible in case of voltage combiners in stacked devices. If any device of the stacked devices fails, no output will be obtained. This is one

of the unique advantage of current combining PA. To account for the degradation property of the current combiner, the combining efficiency is considered. It is defined as the ratio of the combiner output power to the combiner input power, i.e.

$$\eta_{comb} = \frac{P_{out,comb}}{P_{in,comb}} \tag{3.40}$$

If the combiner structure is lossless and all the amplifiers are injecting signals into the combiner with proper matching load, then the combining efficiency is unity.

3.10.2. Bandwidth Enhancement

Figure 3.10 shows the output power versus frequency to depict how resistive current combining provides higher bandwidth than reactive current combining. The 3-dB bandwidth for resistive current combining is obtained by finding the two frequencies, ω_L and ω_H, where power become half of the maximum value.

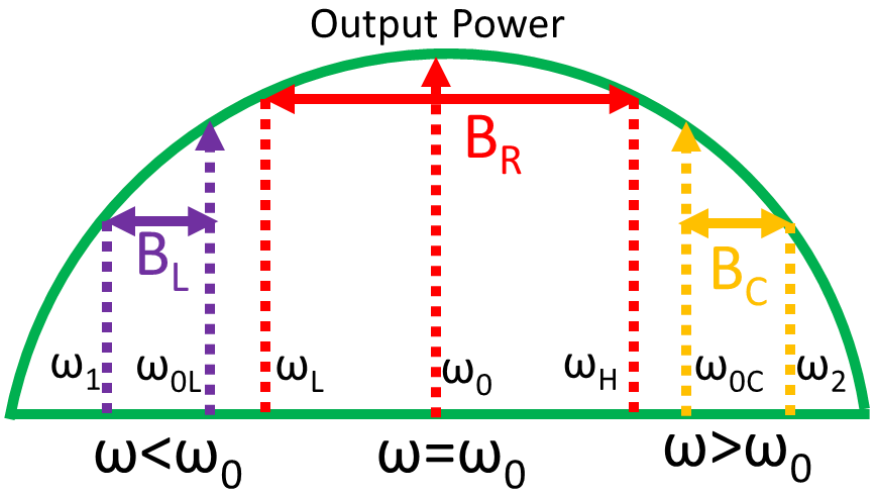

Figure 3.10. Output power versus frequency for resistive and reactive current combining.

From Eq. (3.38), the power at ω_L and ω_H are given by

$$P_{opt}(f_{H,L}) = \frac{N}{4} I_0^2 R_{eq}(f_{H,L}) = \frac{1}{2} P_{opt}(f_0) \tag{3.41}$$

From Eq. (3.37) and Eq. (3.41), $X_0(f_{H,L})$ is given by

$$X_0(f_{H,L}) = R_d \tag{3.42}$$

$$Z_{f_{H,L}} = \sqrt{R_d^2 + X_0^2(f_{H,L})} = \sqrt{2}R_d \tag{3.43}$$

So, these two frequencies, ω_L and ω_H happen at the impedance where reactive part of the impedance becomes R_d so that the magnitude of the impedance at these two frequencies are equal to $\sqrt{2}R_d$. The bandwidth, B_R (= $\omega_H - \omega_L$) is given by L_{s4} / R_d. For reactive current combining, the current combines capacitively for $\omega > \omega_0$ with frequency of operation at ω_{0C} and inductively for $\omega < \omega_0$ with frequency of operation at ω_{0L}. For reactive current combining of capacitive type and inductive type, half-power frequency occur only at single frequency of ω_2 and ω_1, respectively. In any case, the bandwidth B_L (= $\omega_{0L} - \omega_1$) and B_C (= $\omega_2 - \omega_{0C}$) are always less than B_R.

3.10.3. Matching Network

Input matching network (IMN), has been used at the input side of PA to convert the input impedance of the PA to 50 Ω with L-C-L T-network, as shown in the Figure 3.6. To bias the 1st stage of the PA, a DC blocking capacitor is used in series with L at the device side.

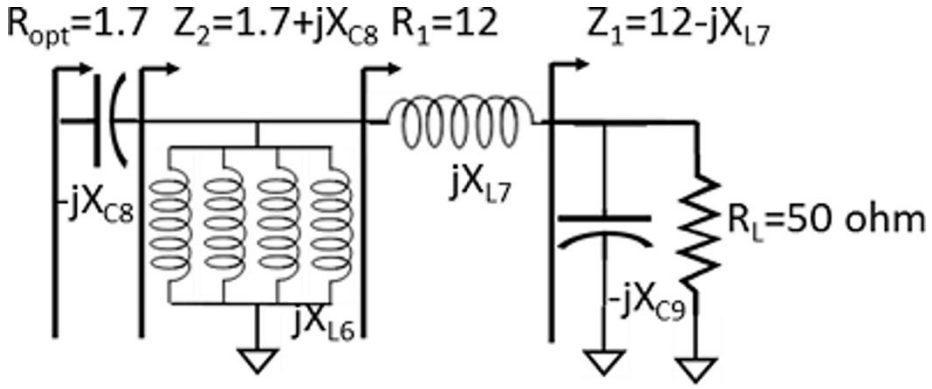

Figure 3.11. Circuit schematic of OMN.

Within the bandwidth the device plane impedance varies from 1.5 Ω at 3-dB frequency to 1.7 Ω at center frequency. An output matching network (OMN) after the device plane is required to transform the output load of 50 Ω to optimum load (R_{opt}) of 1.7 Ω. Two successive impedance

transformation sections, as shown in the Figure 3.11, have been used. In the first section, shunt-C transforms load 50 Ω to 12 Ω and its value is determined by the Eq. (3.44) and excessive capacitive reactance is neutralized by using a series-L and value is determined by Eq. (3.45). In the second section, shunt-L transforms 12 Ω to 1.7 Ω and excessive inductive reactance is neutralized by the series-C and their values are determined by the Eq. (3.46) and Eq. (3.47).

$$X_{C9} = \frac{R_L}{\sqrt{(TR_1 - 1)}} \tag{3.44}$$

where, impedance transformation ratio, $TR_1 = R_L/R_1$

$$X_{L7} = \frac{R_L \times R_1}{X_{C9}} \tag{3.45}$$

$$X_{L6} = \frac{R_1}{\sqrt{(TR_2 - 1)}} \tag{3.46}$$

where, impedance transformation ratio, $TR_2 = R_1/R_{opt}$

$$X_{C8} = \frac{R_1 \times R_{opt}}{X_{L6}} \tag{3.47}$$

Four parallel inductors, are used in the 2nd impedance transformation section, which improves the overall Q and the ac current handling capability. Because of lossy inductors in the OMN, the loss of the OMN is from 2.4 dB to 3 dB within the desired frequency band.

3.10.4. Overall Efficiency of PA

There are many mechanisms that affects the PAE of a PA as described in [96]. Considering the most critical influencing parameters, the overall efficiency of the PA is given by

$$\eta_{overall} = \eta_{class} \times \eta_{comb} \times \eta_{OMN} \tag{3.48}$$

where, η_{class} is the maximum efficiency that can be achieved in a definite bias class of operation for amplification, η_{comb} is the combining efficiency of the current combiners and η_{OMN} is the OMN efficiency. For class A operation, the maximum value for η_{class} is 50%. η_{comb} depends

on the symmetry of the devices, and reliability of the devices at high current condition. η_{comb} can be enhanced by ensuring that every unit cell is operating with symmetric nature, by placing the devices / unit cell close enough, by ensuring that number of fingers, width of the power line trace, ground plane and other interconnecting traces are sufficient to carry large current load so that no thermal instability and catastrophic phenomena doesn't occur.

Non-ideal passive components in the output matching network also degrade the efficiency. For an impedance transformation from R_L to R_{opt}, the Q-factor of the impedance transformation is given by [96]

$$Q_{OMN} = \sqrt{\frac{R_L}{R_{opt}} - 1} \tag{3.49}$$

The combining efficiency, η_{OMN} is given by

$$\eta_{OMN} = \left(\frac{Q_L}{Q_L + Q_{OMN}} \right)^2 \tag{3.50}$$

where, Q_L is the quality factor of the inductor. From this Eq. (3.50), it is clear that combining efficiency improves with the lower impedance transformation ratio.

3.11. Measurement Results

Figure 3.12 shows the micrograph of the 3.63 mm X 0.95 mm fully integrated PA chip fabricated using 0.18 um CMOS process including all bond pads.

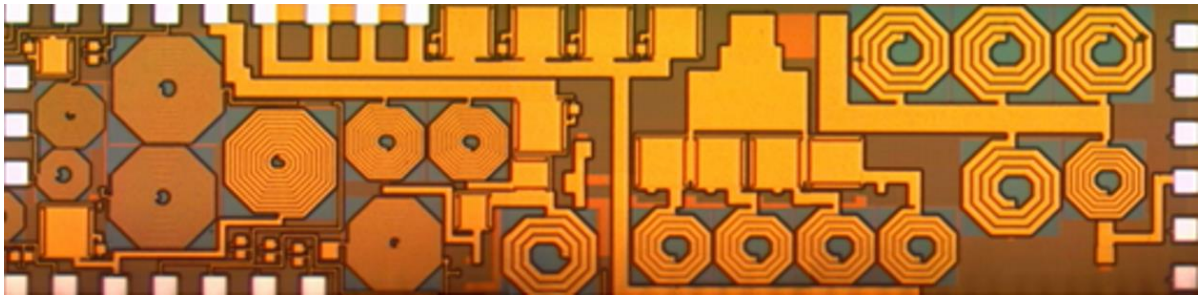

Figure 3.12. Micrograph of a fully integrated 3.63 mm X 0.95 mm fabricated CMOS PA chip.

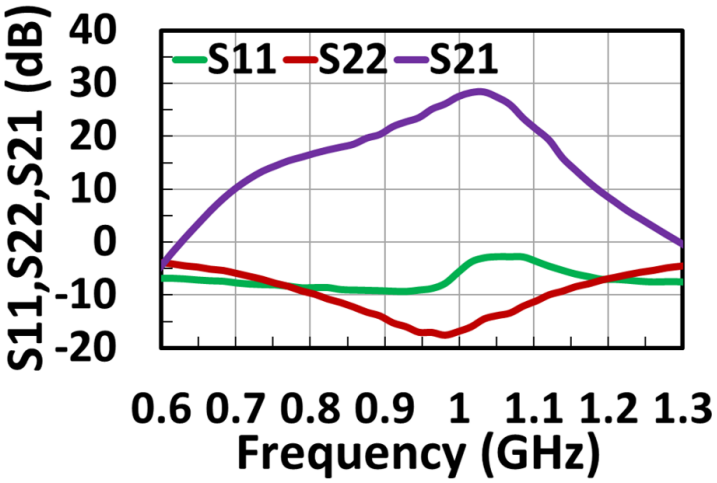

Figure 3.13. Measured S-parameters.

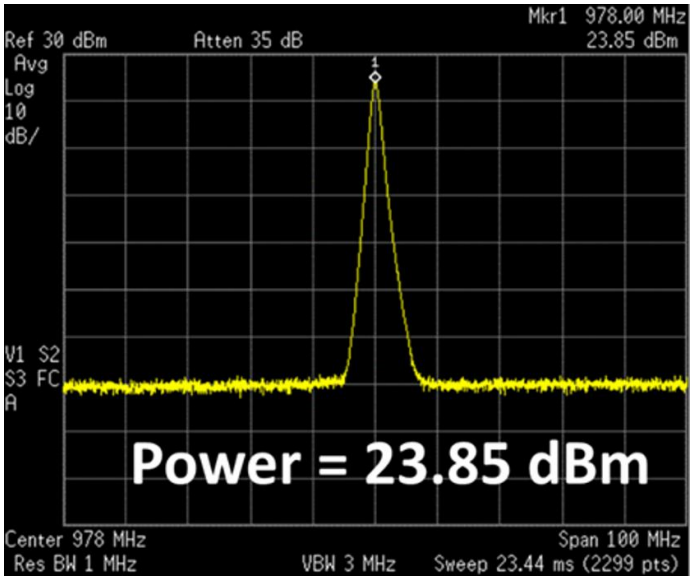

Figure 3.14. Measured single-tone output power of the PA at 978 MHz.

Figure 3.13 shows the measured S-parameters and Figure 3.14 shows the measured single-tone peak output power of 23.85 dBm after de-embedding the cable loss of 3 dB, measured with Tektronix RSA3408B. The modulated output power from the PA has been measured providing modulated input power from Anristsu MG 3700A vector signal generator. Figure 3.15 (a), 3.15 (b), 3.15 (c) and 3.15 (d) show the respective modulated output power of 22.55 dBm, 22.26 dBm, 22.10 dBm, and 21.87 dBm, measured with 25 MHz GMSK, 8PSK, 16QAM and 64QAM baseband signals.

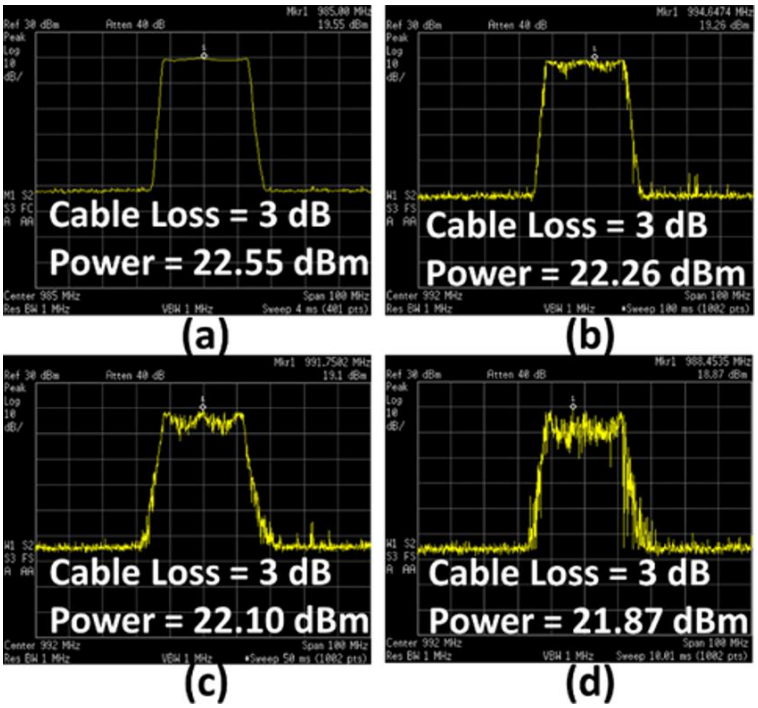

Figure 3.15. Measured modulated output power spectrum of the PA with 25 MHz baseband (a) GMSK, (b) 8PSK, (c) 16QAM, and (d) 64QAM signals.

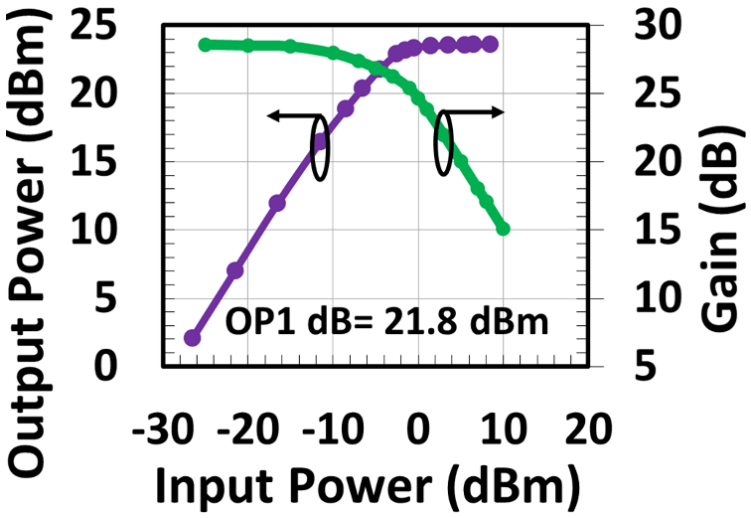

Figure 3.16. Measured output power and gain versus input power.

Figure 3.16 shows the measured output power and the measured power gain at 978 MHz vs input power. The peak power gain of 27 dB within 3-dB band power occurs at input power of -6 dBm. Figure 3.17 shows the output power against the frequency and it shows the 3-dB bandwidth of the PA is 290 MHz. The DC power consumption of the PA is 3.5 W.

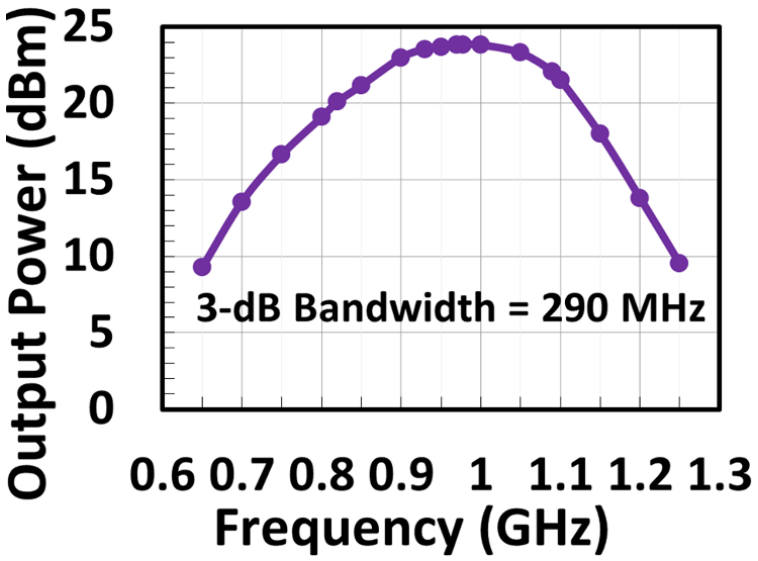

Figure 3.17. Measured saturated output power versus frequency.

The performance of the PA were measured with twenty chips. Some deviations in the S-parameters and output power have been found. The input return loss (S11) shows variation at 978 MHz and 1090 MHz with mean and standard deviation of -6.98 dB and 3.44 dB, and -7.4 dB and 0.993 dB, respectively. The output return loss (S22) shows the variation at 978 MHz and 1090 MHz with mean and standard deviation of -17.2 dB and 1.47 dB, and -11.65 dB and 0.52 dB, respectively. The maximum power gain (S21) varies across the chip with mean and standard deviation of 23.2 dB and 2.3 dB, respectively. The output power has been measured in four experiments with the same chip which shows the best performance for S-parameter measurement. The saturated output power varies across the experiments very little with mean and standard deviation of 23.76 dBm and 0.0876 dBm, respectively. However, Figure 3.13 to Figure 3.17 shows the best results of the experiments.

To compare the overall performance of the PA with the state-of-the-art technology, the FOM is as in Eq. (3.25) is considered. The table 7 shows the comparison of the performance of the proposed PA with the state-of-the-art PA around the frequency of 1 GHz. Although, the proposed PA has lower peak output power than the PAs reported in [50]-[51], the proposed PA

Table 7. Comparison of the performance of state-of-the-art CMOS PAs in the similar frequency range

	This Work	2006 [50]	2012 [51]	2012 [52]	2014 [53]
Frequency of Operation (GHz)	0.825-1.115	0.86-0.96	1.8	1-1.3	1.5-3.6
Peak Power (dBm)	24	27	26	31	17.3
Average Power (dBm)	22	-	23.4	-	-
Peak Power Gain (dB)	27	16	12	13.2	15
Peak PAE (%)	10	28	34	53	25
EVM (%)	8 (QPSK)	-	3.2	-	-
3-dB BW (MHz)	290	100	10	300	2100
Size (mm^2)	3.45	>3.3*	2.42	62**	0.9
FOM (dB)	50	38	14	50	52
Type	4-Stage CS Class-A with Resistive Current Combining	Two-Stage Cascode DAT TL Transformer Based Power Combining	Single-Stage Cascode Envelope Tracking	Two-Stage Inverter Based CS Class-E	Two-Stage Cascode Low-Q Matching
Technology	0.18 um CMOS	0.25 um CMOS	0.18 um CMOS	65 nm CMOS	0.18 um CMOS

*Size of on-chip transformer. So chip size is more than this size.
**PCB Size. Off-chip input and output matching network

achieve higher gain and higher 3-dB bandwidth providing higher FOM. Although the peak power and bandwidth of the PA in [52] are higher, but the gain is 14 dB lower than this work. Also, the IMN and OMN used for the PA in [52] are off-chip, whereas the proposed PA is fully integrated. The bandwidth of the PA in [53] is higher than the PA of this work, but the proposed PA provides higher peak power, higher power gain and comparable FOM. So, this work clearly shows that the proposed PA has highest peak power gain, moderate saturated output power, moderate bandwidth and comparable FOM with respect to the other PAs in the references.

3.12. Conclusion

In this work, a fully integrated 0.18 um CMOS PA with high power gain has been developed using resistive current combining technique. The proposed PA provides peak output power of 24 dBm with maximum gain of 27 dB and bandwidth of 290 MHz maintaining excellent figure-of-merit of 50 dB. The PA supports GMSK (GSM), 8PSK (EDGE), 16QAM (LTE-a) and 64QAM (LTE-a) modulation schemes and covers the LTE-advanced bands from 825 MHz to 915 MHz, ADS-B bands of 978 MHz UAT and 1090 MHz ES modes for UAS with more than 22 dBm of modulated output power. Thus, this PA chip will enable to reduce the size of the state-of-the-art ADS-B transmitter for UAS and hence will reduce the cost of UAS to integrate to the NAS.

CHAPTER 4. HIGH-POWER HIGH-EFFICIENCY FULLY INTEGRATED SINGLE-CHIP CMOS ADS-B TRANSMITTER FOR UAS

4.1. Introduction

As mentioned in the chapter 1, because of huge possibilities of applications, UAS is finding mass production for its commercialization. But before its mass production, technical compatibility to operate in the NAS has to be met. It has to follow operational rules and guidelines, and also FAA mandate [8]. The FAA strictly prohibited to allow operation of small UAS in class A airspace (above 18,000 ft) but allowed operation in class B, C, D, E airspace (from 700 ft to 18000 ft) with ATC permission and allowed operation in G airspace without ATC permission [1]. The FAA mandated all UAS to equip with Automatic dependent Surveillance Broadcast (ADS-B) transmitter by 2020 [8].

Operating with two modes of ADS-B system, 978 MHz UAT (operates below 18,000 ft) and 1090 ES (operates above 18,000 ft) modes, each airplane will communicate wirelessly with its nearby airplanes, or with its nearest ground station. In additon, new datalink for ADS-B for UAS including video data, L-DACS1 (975 -1164 MHz) and L-DACS2 (960-975 MHz) is going to be in effect in near future [9]. ADS-B UAT and 1090 ES braodcasting messages with continuous phase frequency shift keying (CPFSK) modulation scheme of moduation index not less than 0.6 at a rate of 1.041667 Mbps [10]. Both L-DACS1 and L-DASC2 bands are being tested with GMSK, QPSK,16 QAM and 64 QAM and OFDM modulation schemes [9].

The performance of the transmitter depends on the output power and the range of the transmitter. The power required from the transmitter for manned aircraft to get the range upto 12 NM (63,000 ft) is approximately 7 W (38 dBm) [10]-[11], whereas the power required for UAS to

operate below the class A airspace (below 18000 ft, i.e. 3 NM) at 978 MHz is 21~23 dBm (range is calculated using Friis transmission equation according to [12]).

As mentioned earlier that present ADS-B transmitter is fabricated with hybrid integrated circuits (HICs) in three different modules: a Phase Locked Loop (PLL) module, an Up-converter (modulator) module and the Power Amplifier (PA) module [14], [97]-[98] which makes the system very large in size and expensive. In this chapter, ADS-B transmitter for UAS is proposed. Then different blocks of the proposed transmitter will be discussed in the section of circuit design procedure. As VCO, mixer and PA are very an essential blocks of a transmitter, their design procudere need to be discussed in details. VCO and PA are already discussed in chapter 2 and chapter 3. So, an elaborate details of mixer (up-convereter) is discussed in this chapter. Also, design challenges to implement the transmitter in CMOS technology will be discussed. Then, measurement results of the transmitter will be presented with a comparison of proposed ADS-B transmitter with the state-of-the-art transmitters around L, S, C and Ku bands. Finally, the chapter will conclude with the conclusion.

4.2. Proposed ADS-B Transmitter

Figure 4.1 shows the objective of this thesis work. Figure 4.2 shows the proposed ADS-B transmitter, as a part of UBR implemented in a fully integrated single chip using Complementary Metal Oxide Semiconductor (CMOS) process, which is capable of operating in both ADS-B modes 978 MHz UAT and 1090 ES modes, and in a part of future L-DACS1 band (978 -1100 MHz). The chip is capable of operating the UAS below class A airspace. If the UAS needs to operate above this range, this single chip ADS-B transmitter can be interfaced to drive an off-chip high power PA and thus it will reduce the burden of the input power and the gain of the off-chip PA.

The proposed ADS-B transmitter, is a direct conversion type, consists of VCO, buffer, hybrid, up-converter, balun and PA with IMN and OMN. In the block diagram, VCO generates differential local oscillator (LO) signal from 978 MHz to 1.1 GHz providing high power with high efficency.Two hybrids produce quadrature componenets of the LO signals, which are then get up-converted with baseband signals to either lower side band (LSB) or upper side band (USB) by up-converter. Differential outputs of the up-convereter are then converted to single LSB / USB signal to feed to the input of the PA. The LSB / USB signal is then amplified to the desired transmitted output power level by high-power and high-gain power amplifier.

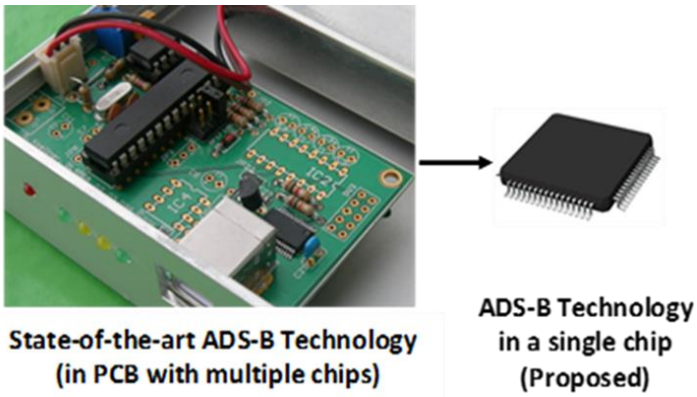

Figure 4.1. Objective of this thesis work.

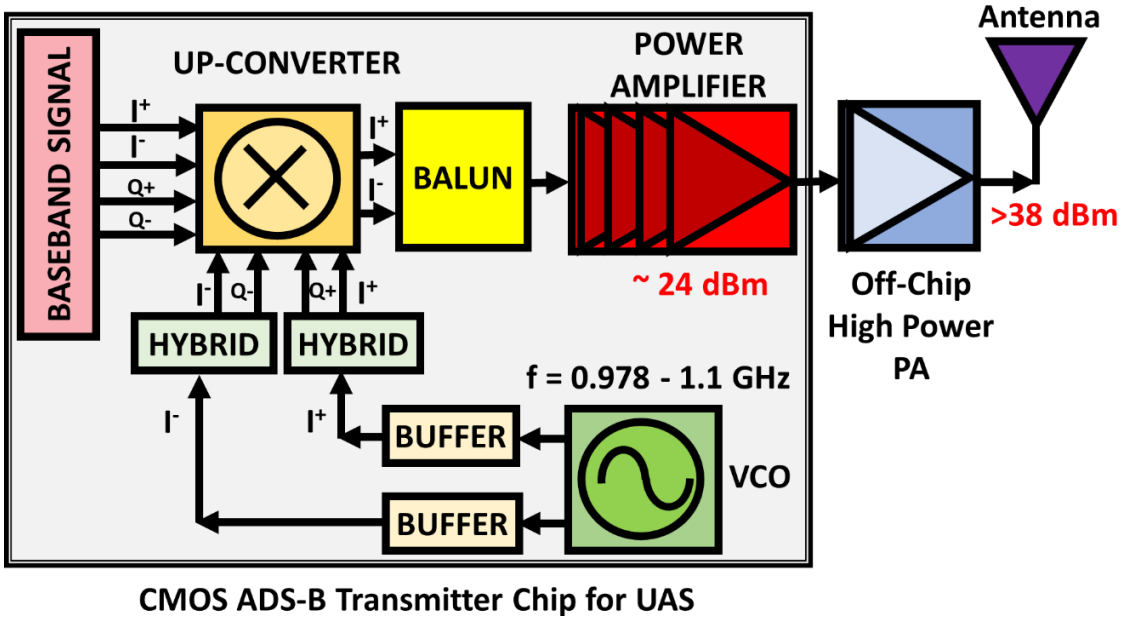

Figure 4.2. Block diagram of proposed CMOS ADS-B transmitter in a single-chip.

4.3.Circuit Design Methodology

4.3.1. VCO and Buffer

A cross-coupled type VCO has been designed to generate carrier frequencies for ADS-B system, as shown in the Figure 4.3, which provides the tuning frequencies from 978 MHz to 1100 MHz. The VCO has been designed to provide high power with high efficiency by operating the VCO in the borderline of voltage-limited and current-limited regime and using custom designed diode-connected NMOS transistors as the variable capacitor for tuning the frequencies instead of using commercial design kit varactor having higher loss [11], [99]-[100]. In addition, the diode-connected tail transistor, which reduces the power dissipation of the core circuit by reducing the current through the core transistors, (because it increases the node voltage of the tail transistor) has been used to enhance the efficiency of the VCO [100]. Details design procedure of the VCO has been discussed in the chapter 2. A buffer of common source configuration is inserted between the

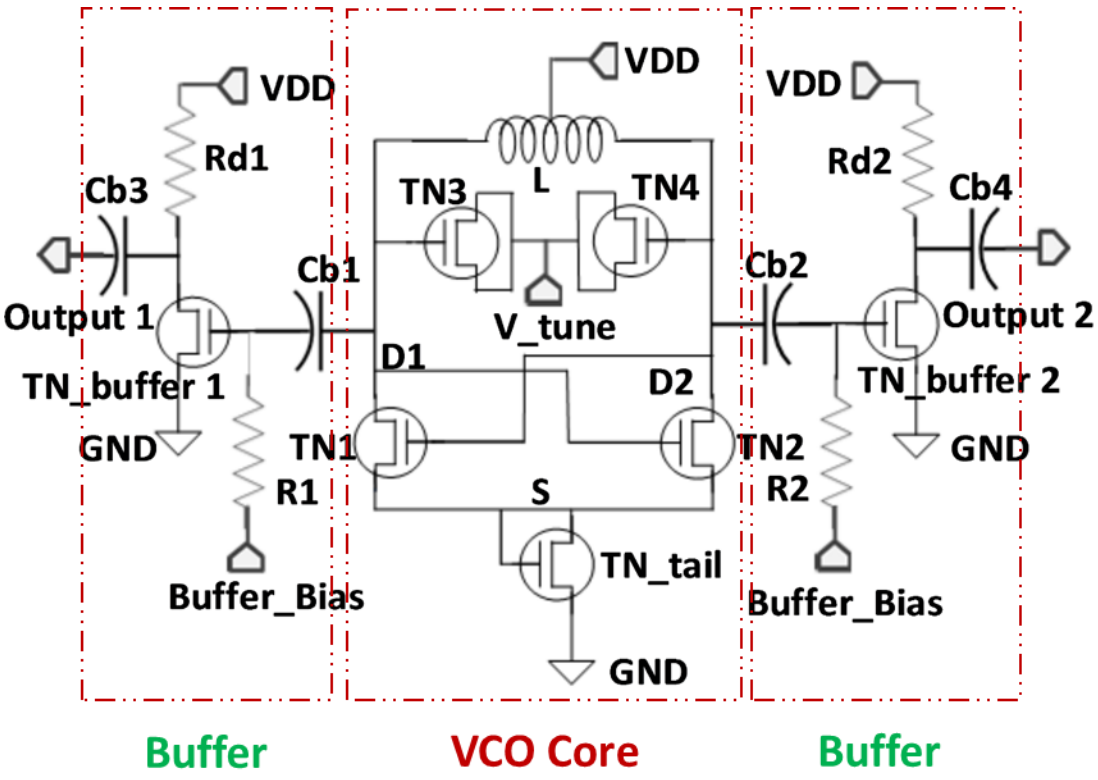

Figure 4.3. The circuit diagram of the VCO with buffer.

VCO and the hybrid to make frequency of the VCO insensitive to the variation of passive elements of the hybrid due to variations of process, voltage and temperature. Using a high-power and high-efficiency VCO with good phase noise is helping towards realizing a high-power and high-efficiency ADS-B transmitter.

4.3.2. Hybrid

Hybrid is designed with RC low-pass filter (LPF) and high-pass filter (HPF) as shown in the Figure 4.4. The output of the in-phase component is taken across the capacitor of LPF and that of the quadrature component across resistor of HPF.

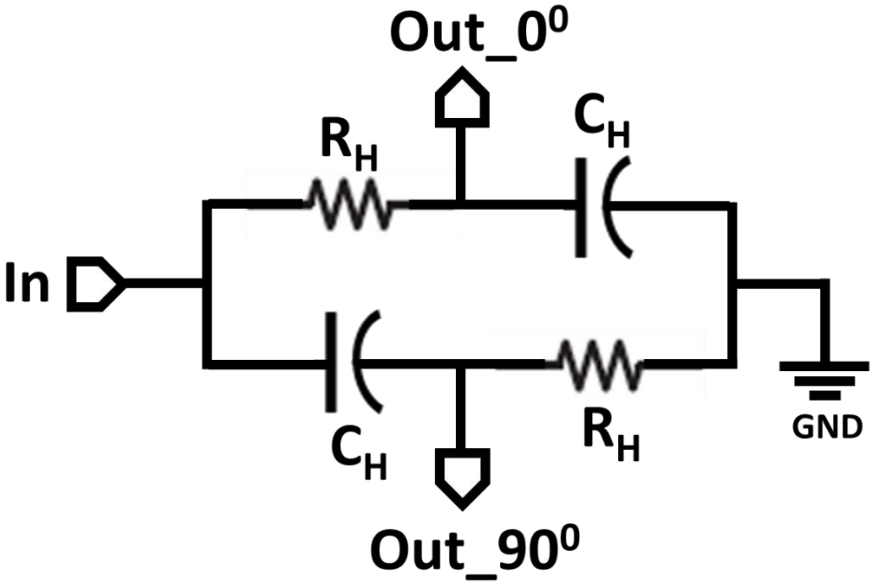

Figure 4.4. Circuit diagram of passive hybrid.

The in-phase output voltage across the capacitor in LPF is given by

$$V_{out\_0^0} = \frac{\frac{1}{j\omega C_H}}{R_H + \frac{1}{j\omega C_H}} V_{in} = \frac{1}{1 + j\omega C_H R_H} V_{in} \tag{4.1}$$

$$\Rightarrow V_{out\_0^0} = \frac{1}{\sqrt{1 + (\omega C_H R_H)^2}} |V_{in}| \angle \left[\theta - \tan^{-1}(\omega C_H R_H) \right] \tag{4.2}$$

$$V_{out\_90^0} = \frac{R_H}{R_H + \frac{1}{j\omega C_H}} V_{in} = \frac{j\omega C_H R_H}{1 + j\omega C_H R_H} V_{in} \tag{4.3}$$

$$\Rightarrow V_{out\_90^0} = \frac{\omega C_H R_H}{\sqrt{1 + (\omega C_H R_H)^2}} |V_{in}| \angle \left[\theta - \tan^{-1}(\omega C_H R_H) + 90^0 \right] \tag{4.4}$$

$$\Rightarrow V_{out\_90^0} = \left| \omega C_H R_H V_{out\_0^0} \right| \angle 90^0 = \left(\frac{\omega}{\omega_0} \right) \left| V_{out\_0^0} \right| \angle 90^0 \tag{4.5}$$

where, $V_{in} = |V_{in}| \angle \theta$ and $\omega_0 = \frac{1}{C_H R_H}$ (4.6)

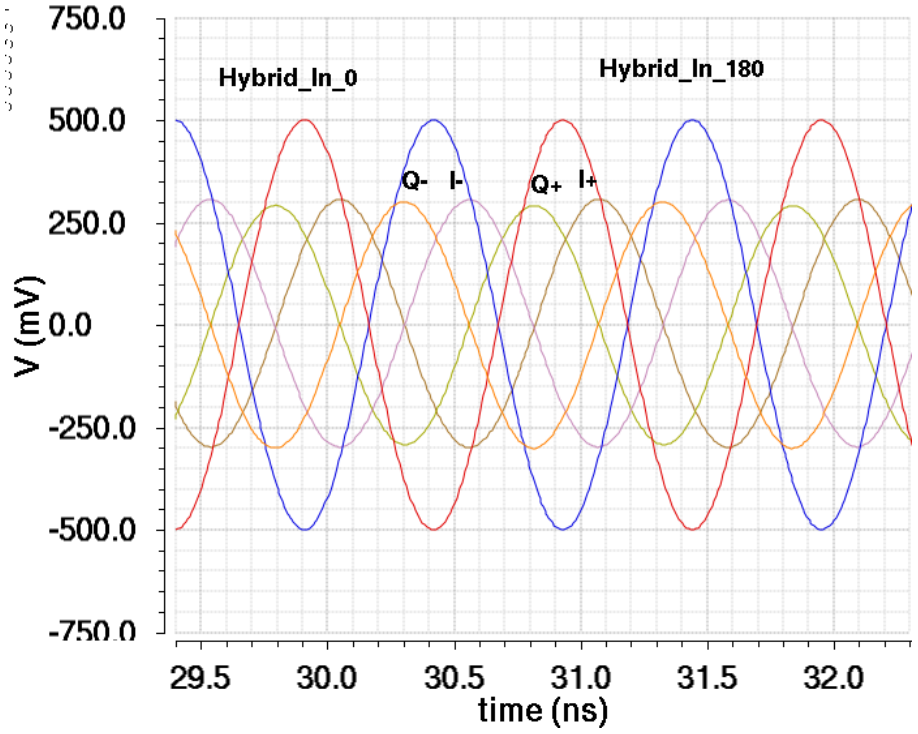

Figure 4.5. Simulated voltage waveforms of differential inputs and outputs of two hybrids.

From the Eq. (4.5), the two outputs always 90^0 out of phase for all frequencies and their magnitudes are equal at the angular frequency, ω_0, but different at any other frequency. So, the hybrid shows ideal phase quadrature. There is no phase mismatch between in-phase and quadrature components. But, there is a gain mismatch between the two components at frequencies other than

reactance component of the hybrid are equal. The value of the resistance is chosen to be $254\sqrt{2}\ \Omega$ so that each arm of the filter makes an impedance of 508 Ω and thus, finally, the input impedance of the hybrid becomes 254 Ω, which is the output impedance of the buffer.

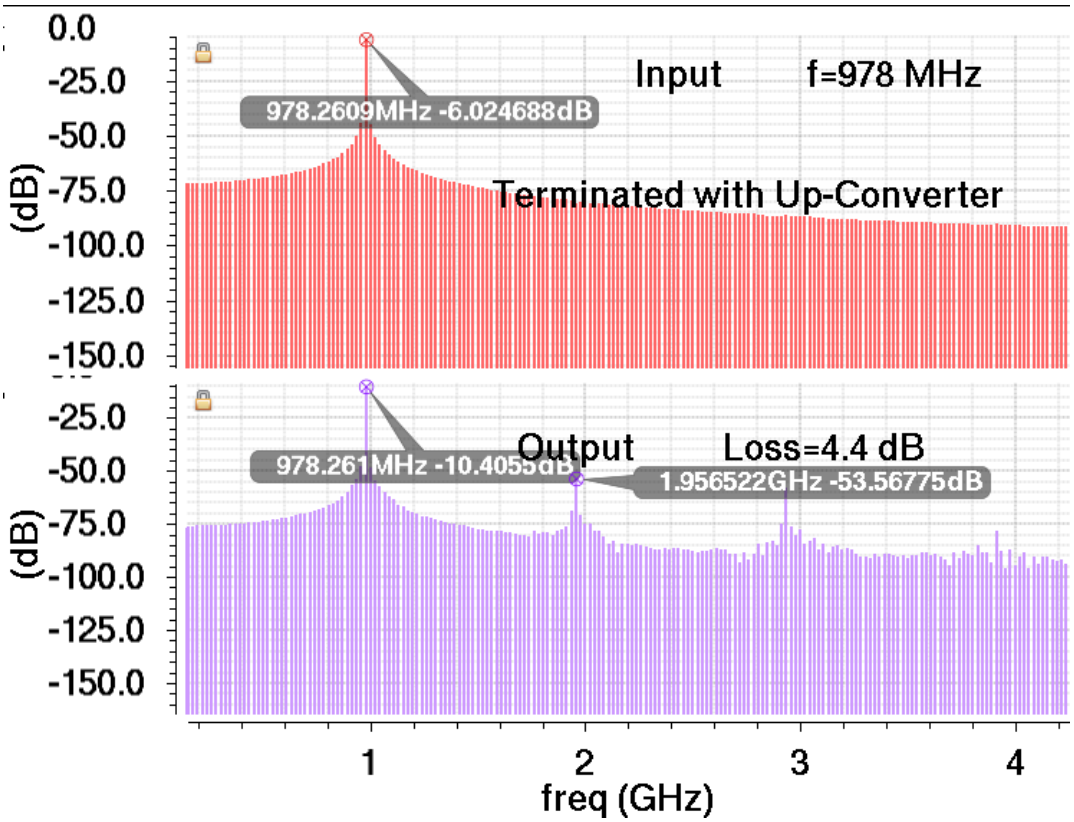

Figure 4.6. Simulated input and output spectrum of the hybrid.

Figure 4.5 shows the simulated input and output voltage waveforms at the cut-off frequency of 978 MHz and it shows that both in-phase components, I^+ and I^- are ideally 90^0 of out of phase with quadrature components, Q^+ and Q^-, respectively. Figure 4.6 shows simulated results of the input / output spectrum of the hybrid. The output voltage at the I+ port is -10.4 dB with an input voltage of -6 dB. This shows that the loss at the I+ port is 4.4 dB. The simulated results of the gain of the hybrid at both I^+ and Q^+ ports with the frequency is shown in the Figure 4.7. The hybrid basically provides a loss of -4.4 dB for in-phase component and a loss of -4.6 dB for quadrature components at 978 MHz. But, the loss for in-phase component increases and for

quadrature component reduces with frequency. So, the mismatch between I-Q components from 950 MHz to 1100 MHz is within 0.72 dB. The performance of the hybrid is shown in the table 8.

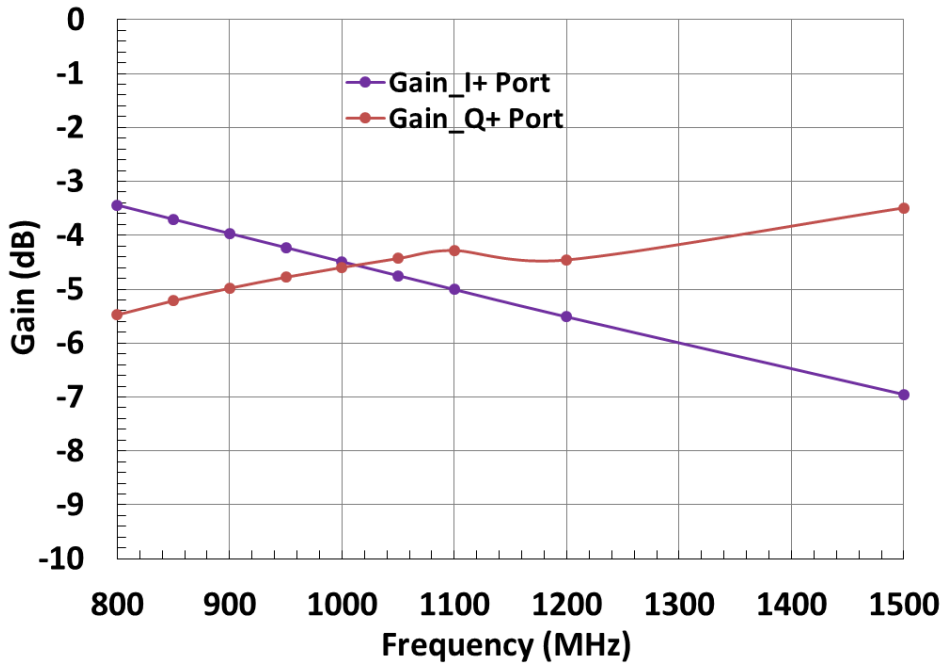

Figure 4.7. The simulated results of the gain of the hybrid at I^+ and Q^+ ports versus the frequency.

Table 8. Performance of the hybrid

Parameter	Value
Frequency Range	900 MHz – 1.2 GHz
Gain	-5.5 to - 4 dB
Phase Mismatch (I^+ - Q^+ and I^- - Q^- ports)	0
Gain Mismatch (I^+ - Q^+ and I^- - Q^- ports)	0.55 to 1 dB

4.3.3. Up-converter

The up-converter performs frequency translation from the baseband frequency to RF frequency by multiplying the signals of LO and baseband frequencies. Up-conversion mixer, as

shown in Figure 4.8 (a), has three distinct ports: LO signal port, baseband signal port and RF signal port. Mixer simply woks like a switch as shown in Figure 4.8 (b), where LO signal, V_{LO} turns the mixer ON/OFF yielding at the output of the mixer, V_{RF} is either 0 or V_{BB}.

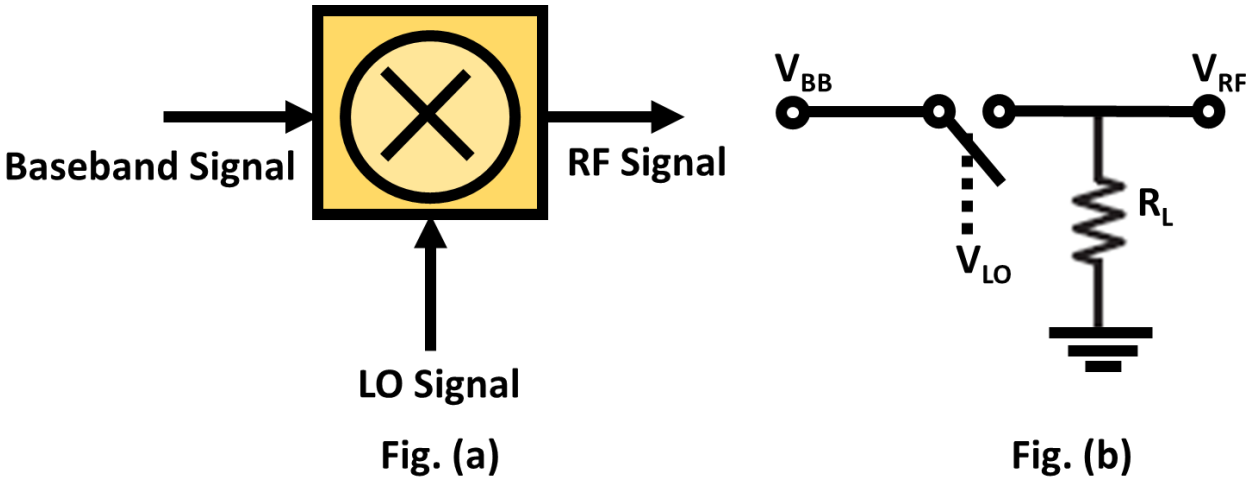

Figure 4.8. (a) Up-conversion mixer, (b) mixer as an ideal switch.

The conversion gain of a mixer is an important parameter. The conversion gain of up-conversion mixer is defined by the ratio of the output signal power at RF frequency to the input signal power at baseband frequency. But, in this design, co-design approach has been followed. So, the input and output of the mixer are matched to the output impedance of the hybrid and input impedance of the balun, respectively, rather than 50 Ω matched. So, the conversion gain is defined as the ratio of the output rms voltage at RF frequency to the input rms voltage at baseband frequency.

The output of the mixer can be given by

$$V_{RF} = V_{BB} \times V_{LO} = V_{BB} \times S(t) \tag{4.7}$$

where, S(t) is the square wave. The Fourier series of square wave is given by

$$S(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{(2n-1)} \sin\left[(2n-1)\omega_{LO} t\right] \tag{4.8}$$

Plugging Eq. (4.8) into Eq. (4.7), the output of the mixer, V_{RF} is

$$V_{RF} = V_{BB} \times \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{(2n-1)} \sin\left[(2n-1)\omega_{LO}t\right] \tag{4.9}$$

For abrupt switching, the operation of the mixer can be considered as multiplication of the baseband signal by the square wave toggling between 0 and 1.

Mixers can be categorized broadly in two kinds: passive mixers and active mixers. The passive mixers do not operate as amplifying devices and hence passive mixers are lossy. On the other hand, active mixers operate with amplifying devices and achieve gain. Passive mixers are classified in four categories:

i) Single-ended Mixer

ii) Single-ended Sampling Mixer

iii) Single-balanced Mixer

iv) Single-balanced Sampling Mixer

v) Double-balanced Mixer

vi) Double-balanced Sampling Mixer

Figure 4.9 (a) and Figure 4.9 (b) show the single-ended mixer and single-ended sampling mixer, respectively. In case of sampling mixer, the capacitor is used at the output rather than using resistor in single-ended mixer, to store the voltage for OFF period. For single-ended mixer, V_{RF} is given by

$$V_{RF} = A_{BB} \cos(\omega_{BB}t) \times \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{1}{(2n-1)} \sin\left[(2n-1)\omega_{LO}t\right] \tag{4.10}$$

Considering only the fundamental component of the square wave, the output voltage of the mixer is given by

$$
\begin{aligned}
V_{RF} &= A_{BB}\cos(\omega_{BB}t)\times\frac{2}{\pi}\sin(\omega_{LO}t) \\
&= A_{BB}\times\frac{1}{\pi}\sin(\omega_{LO}-\omega_{BB})t \\
&= A_{BB}\times\frac{1}{\pi}\sin(\omega_{RF}t)
\end{aligned}
\tag{4.11}
$$

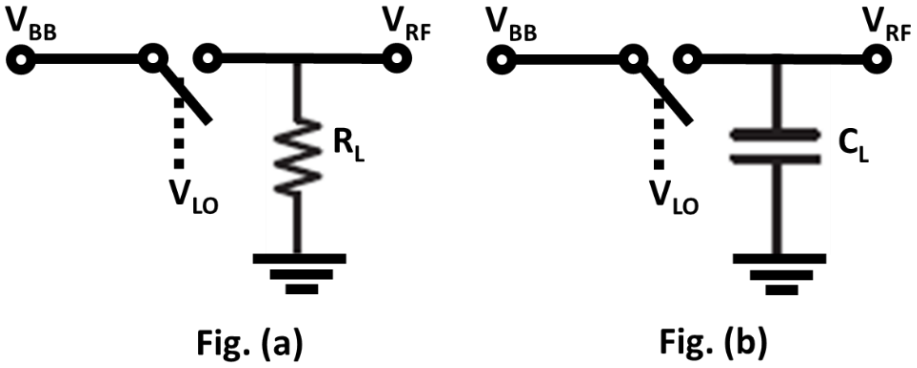

Figure 4.9. Passive (a) single-ended mixer, and (b) single-ended sampling mixer.

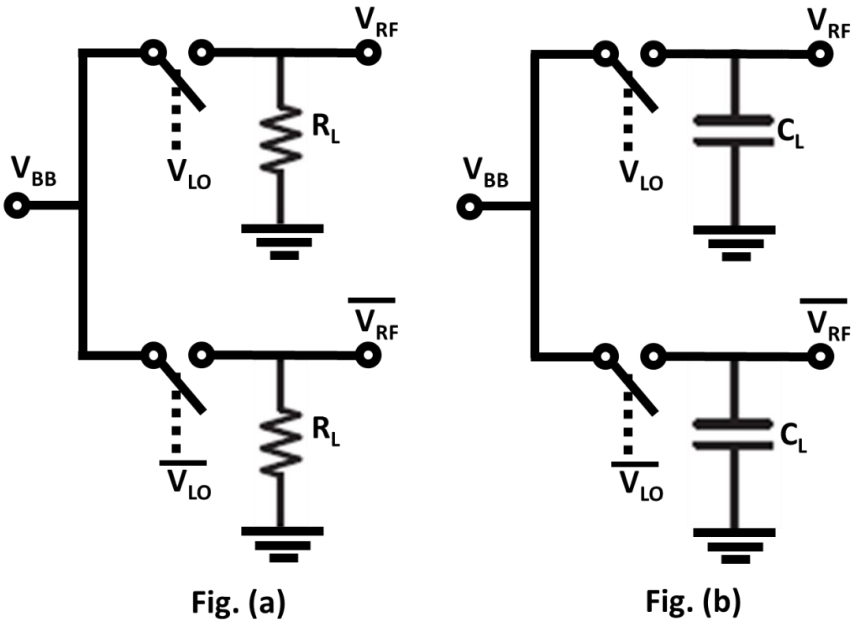

Figure 4.10. Passive (a) single-balanced mixer, and (b) single-balanced sampling mixer.

So, the fundamental gain of the single-ended passive mixer is 1/π. As the ideal square wave toggles between 0 and 1 in single-ended mixer, the output will be zero for half of the LO time period. For single-balanced mixer, as shown in the Figure 4.10 (a), either of the switches will be always ON and the switches are driven by differential LO phases. So, the outputs of a single-

balanced passive mixer will be in differential form and will have twice the gain of single-ended passive mixer, i.e. $2/\pi$. As in the single-ended sampling mixer, output has a capacitor load which acts to store voltage when the switch goes OFF, which is not possible for just single-ended mixer having only resistive load. Hence, total voltage at the output in a LO time period is more than single-ended passive mixer. So, the gain for single-ended sampling mixer is more than single-ended mixer and the value is given by [25]

$$\text{Gain} = \sqrt{\left(\frac{1}{2}\right)^2 + \left(\frac{1}{\pi}\right)^2} \tag{4.12}$$

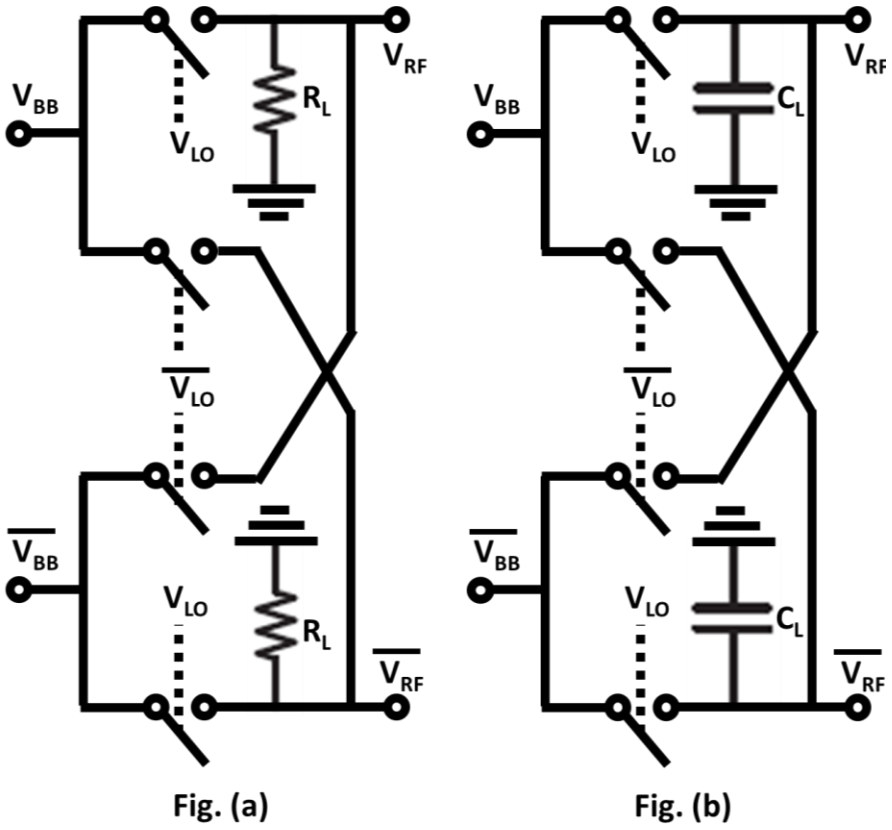

Figure 4.11. Passive (a) double-balanced mixer, and (b) double-balanced sampling mixer.

Similarly, the gain of the single-balanced sampling mixer, as shown in Figure 4.10 (b), is twice as that of the single-ended sampling mixer. One of the advantages of single-balanced mixer over the single-ended mixer is that single-balanced mixer can nullify the LO-BB feedthrough at

LO frequency if the LO-BB paths for both phases are symmetric. Nonetheless, single-balanced mixers suffer from LO-RF feedthrough. Double-balanced mixers can overcome this issue. Figure 4.11 (a) shows the double-balanced mixer, where two single-balanced mixers are connected in such a way that each output contains opposing LO feedthroughs so that their effect cancels out but the signals do not cancel. The circuit, as shown in Figure 4.11 (a), is called double-balanced mixer because it operates with both balanced LO signals and balanced baseband signals. The double-balanced mixers have gain twice that of the single-balanced mixer as each output provides RF signal at each half of LO time period and also it provides differential outputs. The double-balanced sampling mixer, as shown in Figure 4.11 (b), does not have gain twice that of a single-balanced sampling mixer because, the voltage at each output due to the two differential BB inputs are not added. The capacitors don not play any role other than resistors do, as the output in both cases are equal at any given point of time. So, the conversion gain is $2/\pi$. To obtain the advantages of the

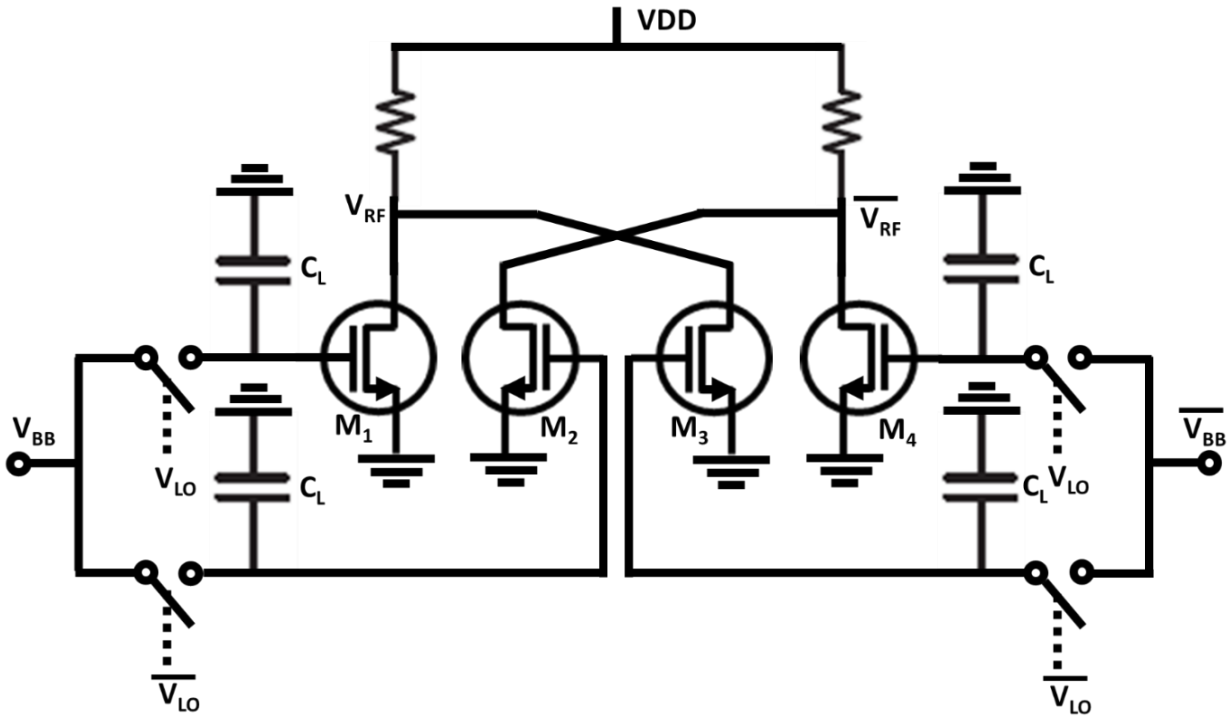

Figure 4.12. Double-balanced passive sampling mixer consisting of two single-balanced mixers connected with the outputs summed in current domain.

double-balanced operation for sampling mixers, two single-balanced sampling mixers are connected in such a way that the outputs of them are summed in the current domain. Figure 4.12 shows the double-balanced sampling mixer consisting of two single-balanced sampling mixers whose outputs are combined in current domain. Thus, the output of the double-balanced sampling mixer become double of the single-balanced mixer doubling the conversion gain, i.e.

$$\text{Gain} = 2\left[\sqrt{\left(\frac{1}{2}\right)^2+\left(\frac{1}{\pi}\right)^2}\right] \tag{4.13}$$

As the passive mixer is lossy, an active mixer is a good choice to be used in the transmitter path to recover the loss incurred (especially in the passive hybrid) up to the input of the mixer. The active mixer generally performs three functions:

i) they convert baseband signal voltage to current

ii) switch the baseband current by the LO signal and

iii) then convert the RF current to RF voltage

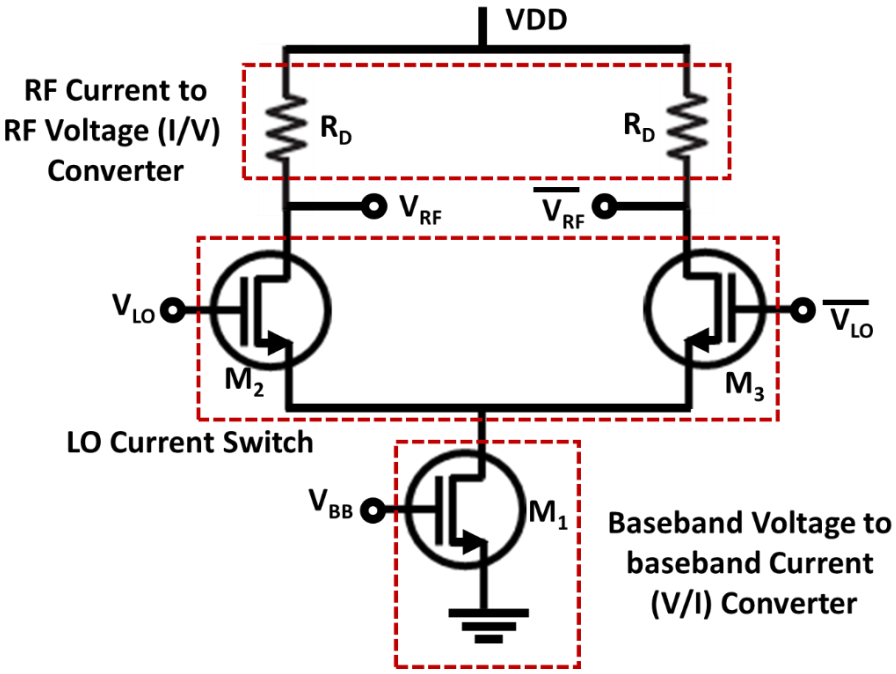

Figure 4.13. Single-balanced active mixer.

Figure 4.13 shows the single-balanced active mixer where the transistor M1 converts the baseband voltage to the baseband current, transistors pairs M2-M3 commutes the RF current by the LO signal and the resistors R1 converts the RF current into the RF voltage. The double-balanced active mixer, as shown in the Figure 4.14, is basically two single-balanced active mixers whose output currents are combined and then combined currents are converted to voltage. This topology is also called as Gilbert cell mixer. Gilbert cell mixer has excellent LO-RF, LO-BB, RF-BB isolation which are not possible in passive mixers.

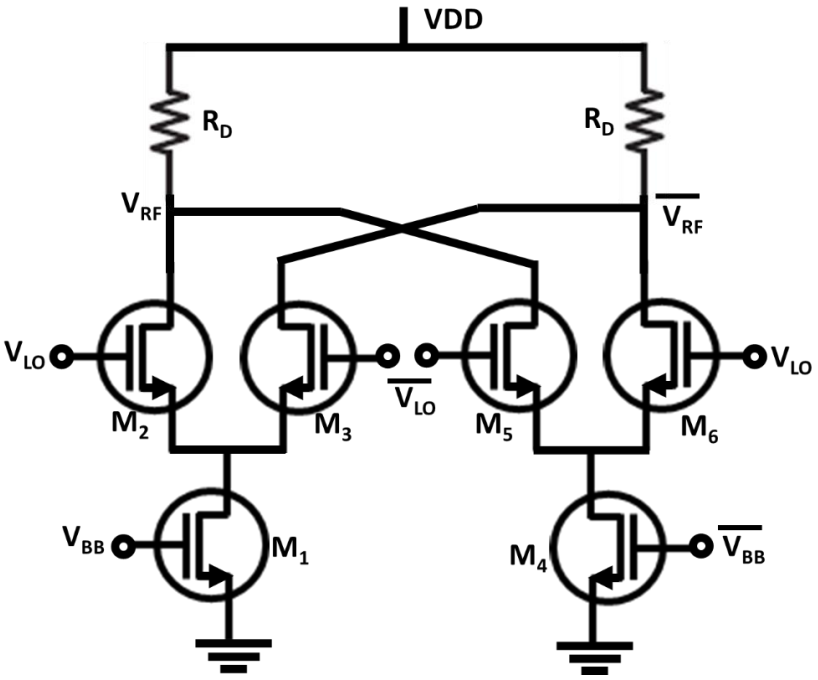

Figure 4.14. Double-balanced active mixer consisting of two single-balanced mixers connected with the outputs summed in current domain.

In the circuit of Figure 4.14, both the transistors M1 and M4 produce small signal baseband current, I_{BB1} and I_{BB2} which are given by

$$I_{BB1} = g_{m1} V_{BB} \tag{4.14}$$

$$I_{BB2} = -g_{m2} V_{BB} \tag{4.15}$$

Now, with abrupt LO switching, the currents I_{BB1} and I_{BB2} get multiplied by square wave S(t) and S(t-T_{LO}/2), respectively, and produce RF currents I_{RF1} and I_{RF2}, respectively. So, they are given by

$$I_{RF1} = I_{BB1}S(t) = g_{m1}V_{BB}S(t) \tag{4.16}$$

$$I_{RF2} = I_{BB2}S(t - T_{LO}/2) = -g_{m2}V_{BB}S(t - T_{LO}/2) \tag{4.17}$$

Now, the resistor converts the RF currents to RF voltages. So

$$V_{RF} = V_{DD} - I_{RF1}R_D = V_{DD} - R_D g_{m1}V_{BB}S(t) \tag{4.18}$$

$$\overline{V_{RF}} = V_{DD} - I_{RF2}R_D = V_{DD} + R_D g_{m2}V_{BB}S(t - T_{LO}/2) \tag{4.19}$$

Now, considering $g_{m1}=g_{m2,}$ the differential RF output voltage is given by

$$V_{RF,diff} = V_{RF} - \overline{V_{RF}} = R_D g_{m1}V_{BB}\left[S(t - T_{LO}/2) - S(t)\right] \tag{4.20}$$

Now, in the Eq. (4.20), S(t) and S(t-T_{LO}/2) are square waves toggling between 0 and 1, but S(t-T_{LO}/2) is delayed by half time-period than S(t). So, when S(t) is 1, then S(t-T_{LO}/2) is 0 and when S(t) is 0, S(t-T_{LO}/2) is 1. So, the difference between S(t) and S(t-T_{LO}/2) will toggle between 1 and -1. The Fourier series of the function S(t)-S(t-T_{LO}/2) can be expressed as

$$S(t - T_{LO}/2) - S(t) = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{(2n-1)}\sin\left[(2n-1)\omega_{LO}t\right] \tag{4.21}$$

From Eq. (4.20) and using baseband voltage, $V_{BB}=A_{BB}\cos(\omega_{BB}t)$, and using only fundamental component of Eq. (4.21), differential voltage is given by

$$\begin{aligned} V_{RF,diff} &= R_D g_{m1}A_{BB}\cos(\omega_{BB}t)\frac{4}{\pi}\sin(\omega_{LO}t) \\ &= \frac{2}{\pi}g_{m1}R_D A_{BB}\sin(\omega_{LO}+\omega_{BB})t + \frac{2}{\pi}g_{m1}R_D A_{BB}\sin(\omega_{LO}-\omega_{BB})t \end{aligned} \tag{4.22}$$

So, the Gilbert cell mixer produces two side bands. One of the sideband can be retained by using a filter. The conversion gain of the both sidebands are same and is given by the ratio of the peak differential RF voltage to the peak baseband voltage, i.e.

$$\text{Coversion Gain} = \frac{V_{RF,diff}(p)}{V_{BB}(p)} = \frac{V_{RF,diff}(p)}{A_{BB}} = \frac{2}{\pi}g_{m1}R_D \tag{4.23}$$

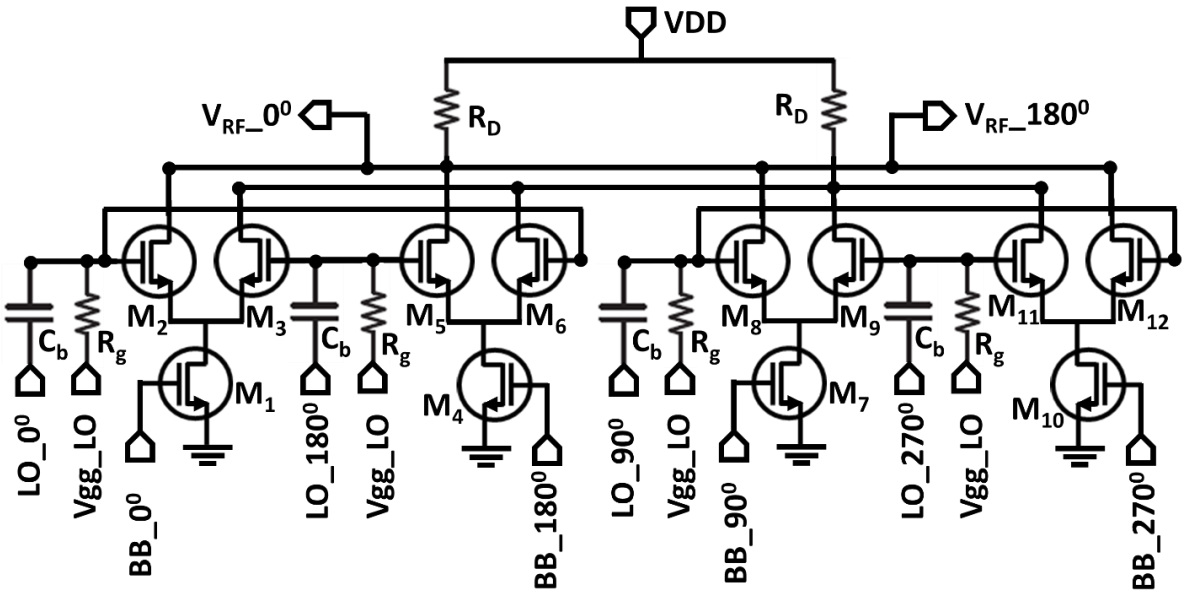

Figure 4.15. I-Q double-balanced active mixer connected with the outputs summed in current domain.

The mixers discussed so far are not free from image frequency of the desired RF frequency. This issue can be nullified by combining the output currents of two double-balanced active mixers (two I-Q Gilbert cell mixers) whose LO and BB signals are in quadrature phase to the corresponding signals of the other Gilbert cell mixer as shown in Figure 4.15. This I-Q Gilbert Cell topology as up-converter can produce carrier suppressed single side band output signal of either lower side band (LSB) frequency, $f_{LSB} = f_{LO} - f_{BB}$ or upper side band (USB) frequency, $f_{USB} = f_{LO} + f_{BB}$, where, f_{LO} and f_{BB} are the LO and baseband frequencies, respectively. If the Figure 4.15 produces LSB signal, the USB signal can be produced by swapping the baseband signals ports BB_90^0 and BB_270^0. One Gilbert cell produces RF outputs with LO switching at 0^0 phase and 180^0 phase ($T_{LO}/2$ time) and the other Gilbert cell produces RF outputs with LO switching at 90^0 ($T_{LO}/4$ time) and 270^0 phase ($3T_{LO}/4$ time). So, the RF output due to I-phase LO switching is given by Eq. (4.22) and the same due to Q-phase LO switching is given by

$$V_{RF,diff\_2} = g_{m1} R_D A_{BB} \cos\left(\omega_{BB} t + 90^0\right)\left[S\left(t - 3T_{LO}/4\right) - S\left(t - T_{LO}/4\right)\right] \qquad (4.24)$$

The function $S(t-T_{LO}/4)- S(t-3T_{LO}/4)$ toggles between 1 and -1 but with a delay of 90^0 phase. The fundamental component of the Eq. (4.24) reduces to

$$V_{RF,diff\_2} == \frac{4}{\pi} A_{BB} g_{m1} R_D \cos\left(\omega_{LO} t + 90^0\right) \sin\left(\omega_{BB} t + 90^0\right) \tag{4.25}$$

So, the total differential RF output is the summation of these two outputs of Eqs. (4.22) and (4.25) and is given by

$$V_{RF,diff} = \frac{4}{\pi} A_{BB} g_{m1} \left[\cos(\omega_{BB} t)\sin(\omega_{LO} t) + \cos\left(\omega_{BB} t \pm 90^0\right)\sin\left(\omega_{LO} t + 90^0\right)\right] \tag{4.26}$$

$$= \frac{4}{\pi} g_{m1} R_D A_{BB} \left[\sin(\omega_{LO} t)\cos(\omega_{BB} t) + \cos(\omega_{LO} t)\{\pm \sin(\omega_{BB} t)\}\right] \tag{4.27}$$

$$= \frac{4}{\pi} g_{m1} R_D A_{BB} \left[\sin(\omega_{LO} t)\cos(\omega_{BB} t) \pm \cos(\omega_{LO} t)\sin(\omega_{BB} t)\right] \tag{4.28}$$

$$= \frac{4}{\pi} g_{m1} R_D A_{BB} \sin(\omega_{LO} + \omega_{BB}) t \qquad \text{[USB]} \tag{4.29}$$

$$= \frac{4}{\pi} g_{m1} R_D A_{BB} \sin(\omega_{LO} - \omega_{BB}) t \qquad \text{[LSB]} \tag{4.30}$$

The '+' sign in the Eq. (4.27) stands for USB and '-' sign for LSB. So, the conversion gain of both the USB and LSB are same and is given by

$$\text{Coversion Gain} = \frac{V_{RF,diff}(p)}{V_{BB}(p)} = \frac{4}{\pi} g_{m1} R_D \tag{4.31}$$

So, in I-Q Gilbert cell, twice the conversion gain can be achieved in addition to nullifying the image frequency w.r.t. single Gilbert cell mixer.

Figure 4.16 and Figure 4.17 show respective simulated RF output voltage waveform and spectrum of the designed I-Q Gilbert cell up-converter. The up-converter is simulated with LO frequency of 978 MHz and BB frequency of 1 MHz producing LSB of 978 MHZ. The baseband power (here it is voltage in dB) is -8.5 dB. The output contains LSB power of -5 dBv and -4.5 dBv at two differential output ports, respectively. The outputs also contain harmonics of LSB frequency and other spurious components. But nearest peak, 3rd harmonics are 18 dB and 15 dB down at the

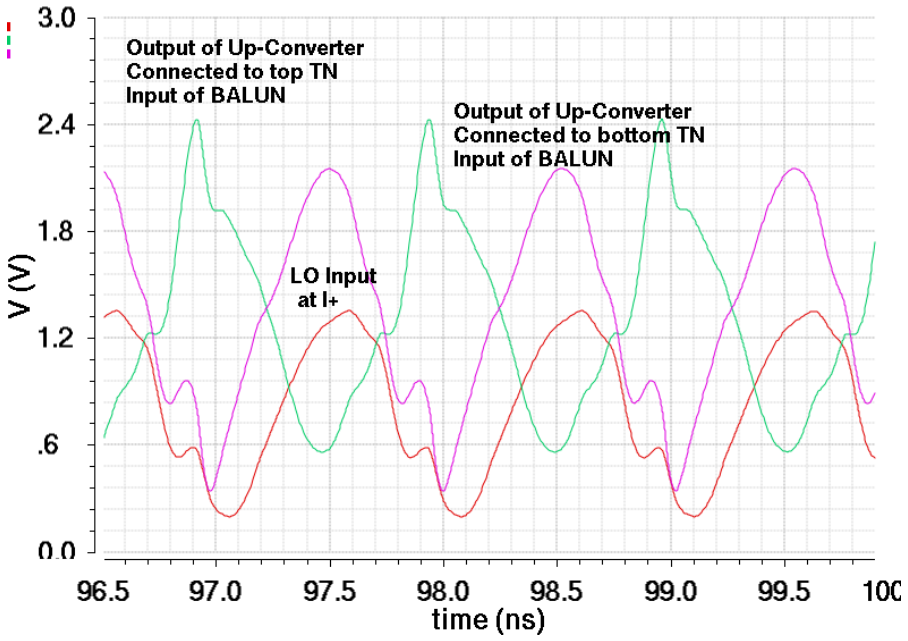

Figure 4.16. Simulated voltage waveforms of input and output of the up-converter in Figure 4.15.

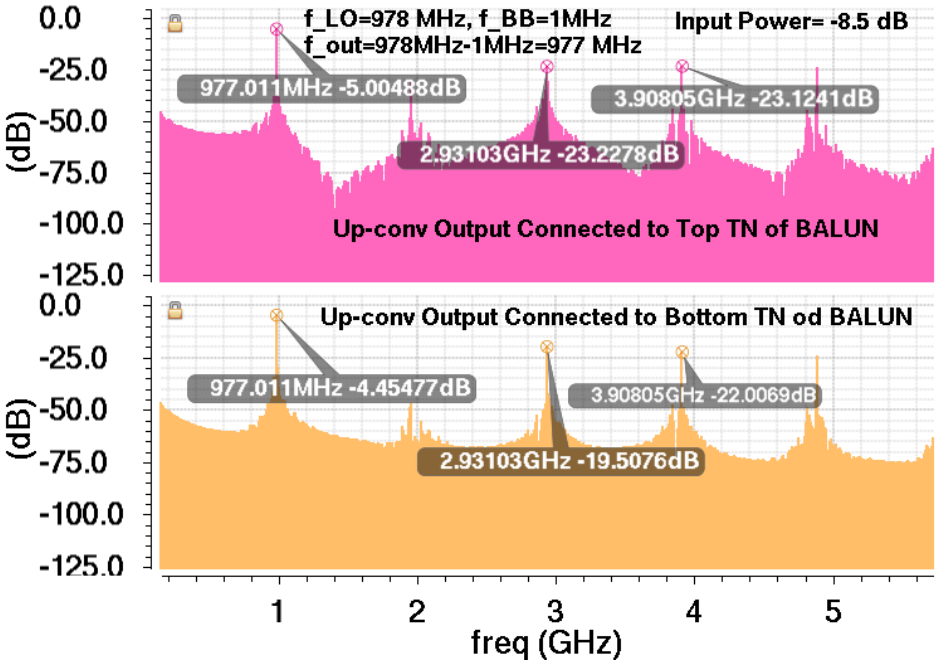

Figure 4.17. Simulated results of input and output spectrum of the up-converter.

two outputs, respectively, and the spurious components are more than 35 dB below the LSB components. As the mixer is differential pair, the odd harmonics are prominent than even order harmonics. Ideally, even order harmonics should disappear or should have very low value. But due

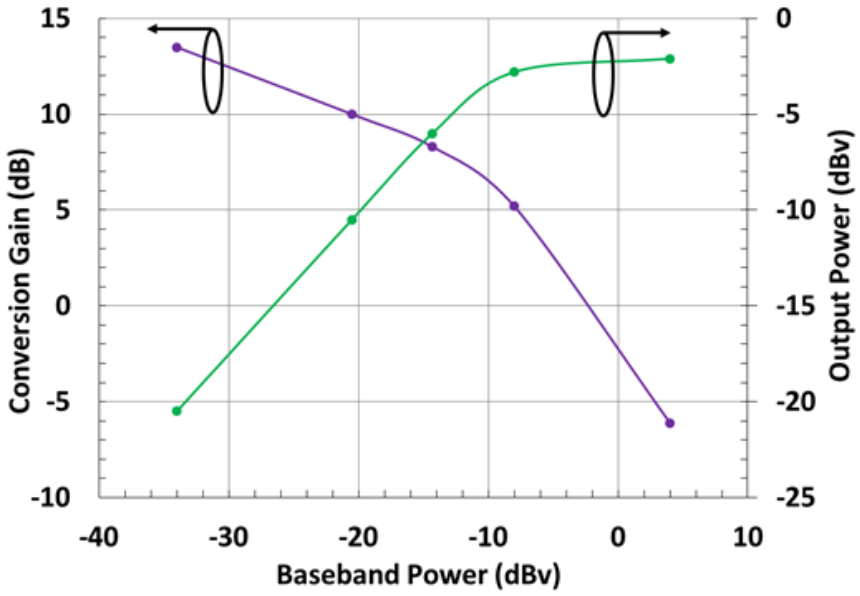

Figure 4.18. Simulated results of output power and conversion gain versus baseband power.

to the mismatch between differential transistor pairs and output impedance variations, even harmonics may present at the outputs. The up-converter in this design sees the two inputs of the active balun where one output of the up-converter is connected to the gate of top transistor and the other to the gate of bottom transistor of two stacked transistors in the balun. But the variation in the output impedance termination of the up-converter are kept low so that the even harmonics have lower values. The 3rd and 4th order harmonics of the LSB appears at the output because of arising nonlinearity at the baseband voltage to current converter, i.e. transistors M1, M4, M7 and M10. As high baseband power of -8.5 dBv is applied, these devices start to saturate and experience nonlinearity. Figure 4.18 shows the simulated results of output power and conversion gain against baseband power at LO frequency of 978 MHz. The up- converter is linear up to the baseband power of -8.5 dBv and its conversion gain at this baseband power is 5 dB. Figure 4.19 shows the conversion gain at LO frequency of 978 MHz versus baseband frequency and it shows the conversion gain varies from 5 dB to 7.6 dB up to the baseband frequency of 100 MHz. So, the up-converter has conversion gain over the bandwidth of 500 MHz. So, the up-converter can overcome

the loss in the hybrid by providing sufficient gain. This up-converter designed for ADS-B transmitter can support both single-tone and modulated signals such as ASK, FSK, PSK (QPSK, 8 PSK), 16 QAM, 64 QAM, GMSK. The table 9 shows the performance of the up-converter and shows the P_{1dB} is -8.5 dB with conversion gain of 8 dB with BB bandwidth of 500 MHz and consumes only 8.3 mW DC power.

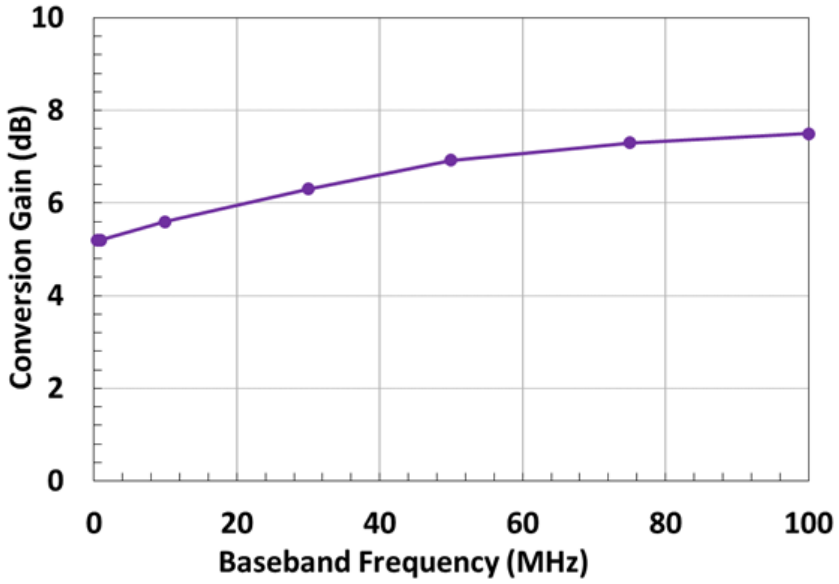

Figure 4.19. Simulated results of the conversion gain of the up-converter versus frequency.

Table 9. Performance of the up-converter

Parameter	Value
Baseband Frequency (MHz)	0-500
Conversion Gain (@ BB Power) (dB)	7 (978 MHz) 6 (1090 MHz)
Conversion Gain (@ BB Frequency) (dB)	4.3-9 (978 MHz) 3-8.8 (1090 MHz)
P_{1dB} (dB)	-8.5
Power Dissipation (mW)	8.3

4.3.4. Balun

The balun for ADS-B transmitter, is an active balun, converts differential inputs to a single-ended output. Two topologies are designed for ADS-B transmitter. Topology-1, as shown in Figure 4.20, is used in the first prototype of the ADS-B transmitter. The second topology, as shown in Figure 4.21, is used for the second prototype of the transmitter. In Figure 4.20, two PMOS transistors are used as the load for two NMOS common source (CS) amplifiers, which amplify two input signals of 180^0 out-of-phase. Among two PMOS load one is used as diode-connected configuration (left) and the other PMOS transistor (right) amplifies the signal amplified by the NMOS transistor (left) with same phase of the input of the NMOS transistor (left). This amplified signal is then added with the same phase to the other amplified signal, which is amplified by the NMOS transistor (right). Thus, balun is designed to provide small signal gain. But it will be lossy if the input signal swing is very large enough to saturate all the transistors. On the other hand, if the input impedance of the power amplifier is not high enough than the output impedance of the balun, then at least one of the two superimposed signals at the Balun_Out port (the signals

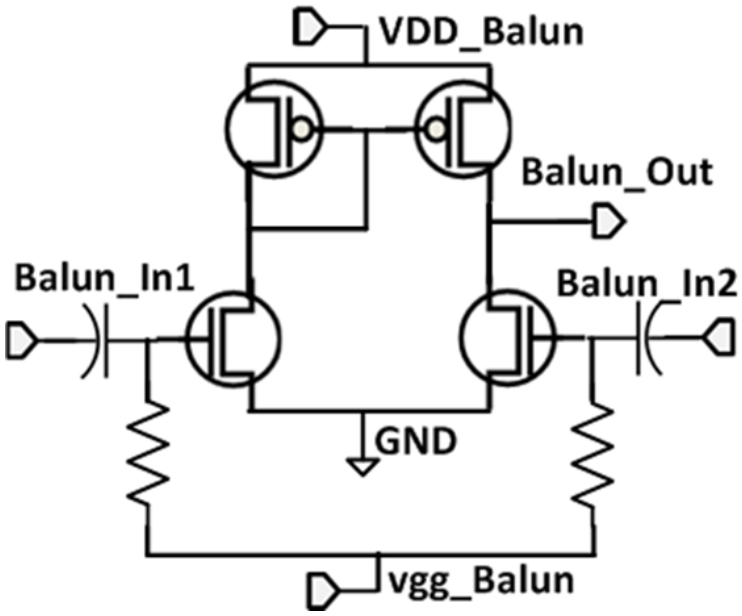

Figure 4.20. Circuit diagram of the balun (topology-1).

amplified by the two NMOS CS amplifier and NMOS CS - PMOS CS amplifier pair) will be amplified with loss and thus the balun would be lossy. So, the design of this kind of topology is very critical.

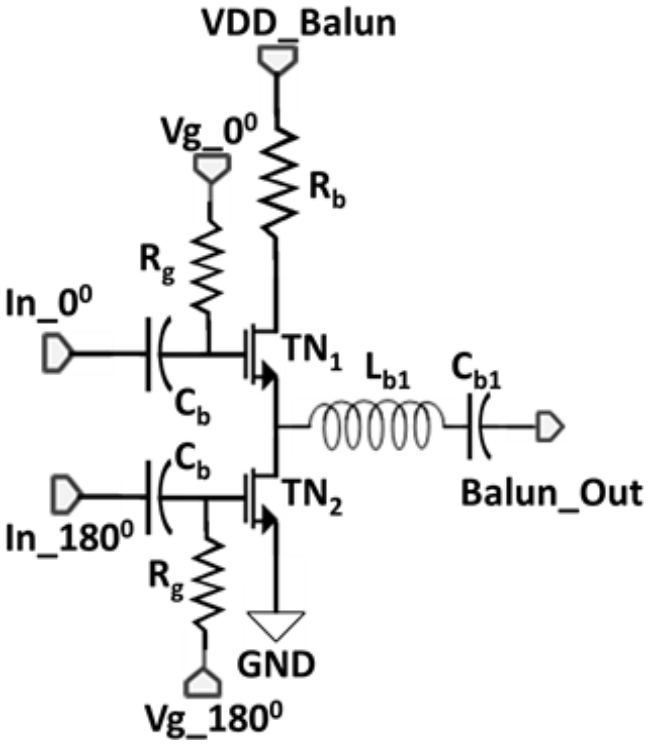

Figure 4.21. Circuit diagram of the balun (topology-2).

The balun in Figure 4.21 is basically a NMOS common source (CS) amplifier whose drain is connected to the source of a NMOS common drain (CD) amplifier. The in-phase signal gets amplified by CD amplifier in same phase, whereas the out-of-phase signal gets amplified by the CS amplifier in opposite phase. The two amplified signals then get added in same phase at the drain of CS amplifier and is then fed to the input of the PA. Both topologies of the balun are designed to have single-ended input to single-ended output gain but, both provides loss from differential input to single-ended output. The choice of second topology over the first is to reduce the loss from differential input to single-ended output. Figure 4.22 and Figure 4.23 show the simulated spectrum of single-ended input / output and single-ended input / differential output

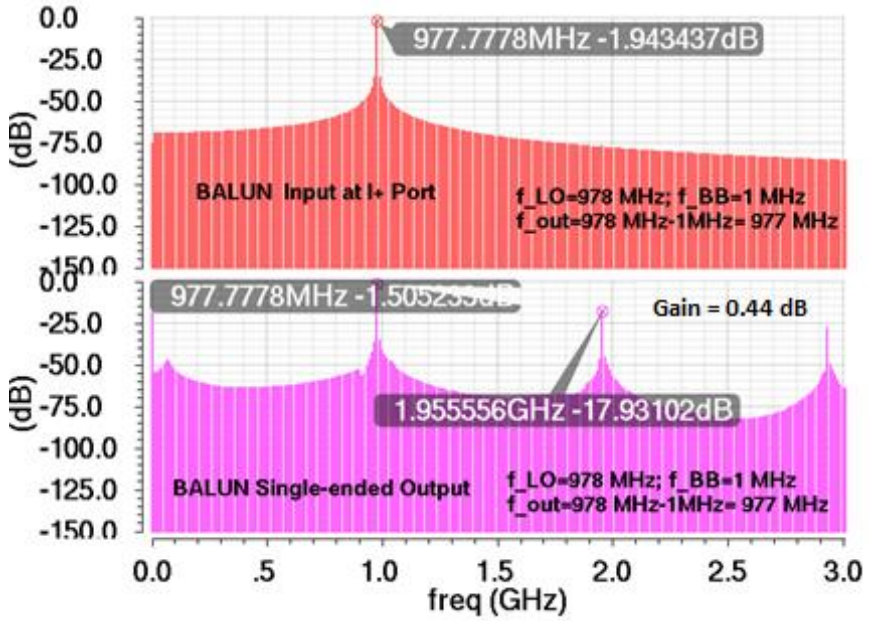

Figure 4.22. Simulated result of frequency spectrum of single-ended input and single-ended output.

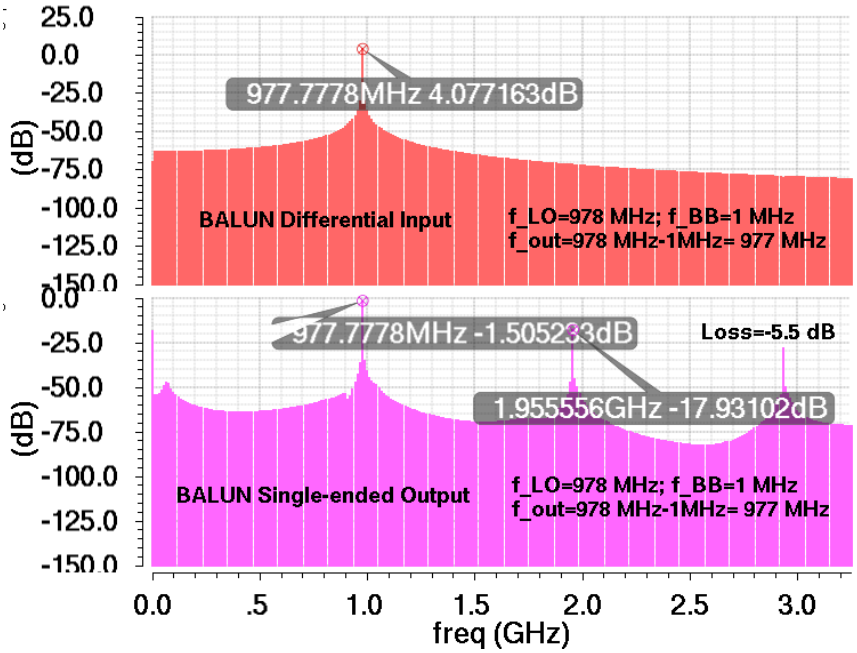

Figure 4.23. Simulated results of the frequency spectrum of differential input and single-ended output.

spectrum, respectively, for the balun topology-2, considering the LO and baseband frequencies of 978 MHz and 1 MHz, respectively. They clearly show the gain from single-ended input to single-ended output of 0.44 dB and the loss from differential input to single-ended output of -5.5 dB.

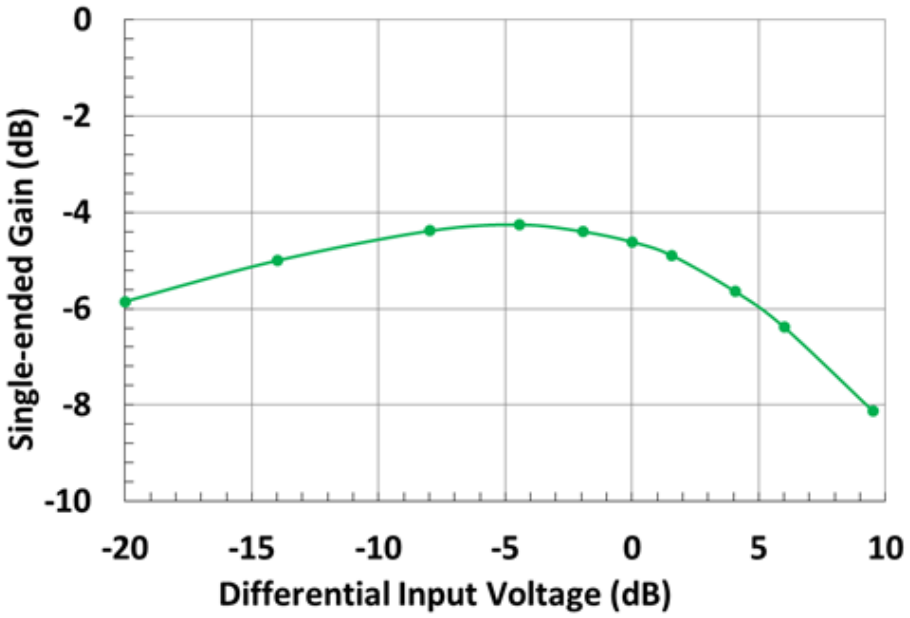

Figure 4.24. Simulated results of the differential input to single-ended output gain versus the differential input voltage.

Table 10. Performance of the balun

Parameter	Value
LSB / USB Frequency (MHz)	100 – 1200
LSB / USB Power (dBv)	-20 ~ 4
Gain (dB) (Single-ended input)	0 ~ 1.3
Gain (dB) (Differential input)	-5.5 ~ -4
Power Dissipation (mW)	13

Figure 4.24 shows simulated results of the differential input to single-ended output gain with the differential input voltage and the loss is minimum at the differential input voltage of -5 dB. So, the balun is operated near to this LSB / USB power. The table 10 shows the performance of the balun, which indicate the balun can operate with frequency range of 100 MHz to 1200 MHz. The LSB /

USB power ranges from -20 dBv to 4 dBv with the gain variation for single-ended input from 0 dB to 1.3 dB and for differential input from -5.5 dB to -4 dB. The power consumption for this balun is 13 mW.

4.3.5. Power Amplifier

To design the PA block for the ADS-B transmitter, two topologies of the PA have been followed, as shown in Figure 2.25 and Figure 4.26. To achieve higher gain, a topology of CS amplifier with four cascade stages has been followed for both PAs. In the first topology, the input impedance of the first stage of the power amplifier is matched to the output impedance of the balun (topology-1) simply by L-C section. A series resistance is used at the input section for reducing the overall gain to ensure the stability of the PA. The size lineup of the transistors of the successive stages are 1x20 µm, 1x100 µm, 1x2 mm, 6x1mm, respectively. The power gain at the power stage (fourth stage) is obtained by current combining technique. By using six wider transistors in parallel at the power stage, the current from each transistor gets combined and channeled through the blocking capacitor to the output matching network. The use of wider transistors in parallel reduces the output device impedance to 2 Ω and, thus, manages the voltage swing across the device plane to reduce below the breakdown voltage of the transistor. The load 50 Ω is converted to device plane impedance of 2 Ω with two successive impedance transformation using series-C and parallel-L passive elements keeping impedance transformation ratio same (here 5) for both sections. First,

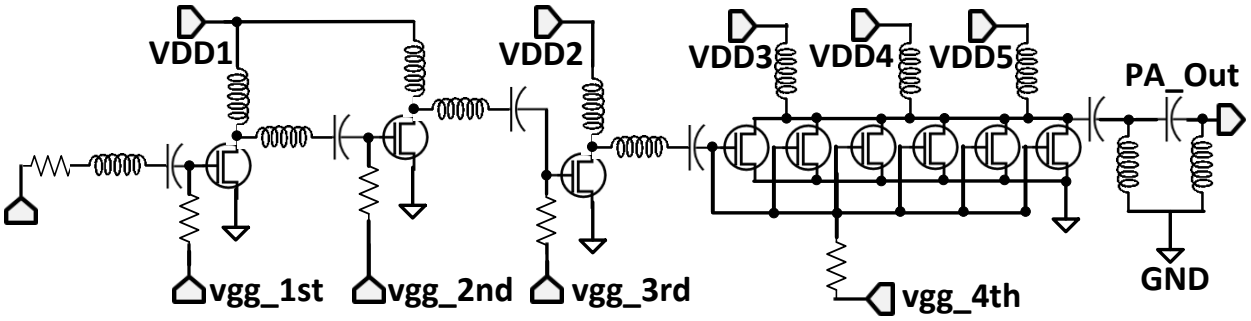

Figure 4.25. Circuit diagram of 4-stage PA which uses current combining technique (topology-1).

50 Ω is converted to 10 Ω by using parallel inductor across 50 Ω and cancelling the excessive inductive reactance with equal capacitive reactance using series capacitor. Similarly, 10 Ω is transformed to 2 Ω using parallel-L and series-C elements. Impedance transformation with two successive stage with same transformation ratio provides better impedance matching. The supply in the fourth stage is divided into three stages to reduce the current load through the supply bond pads. The loss of the OMN in this design was nearly 3-3.3 dB.

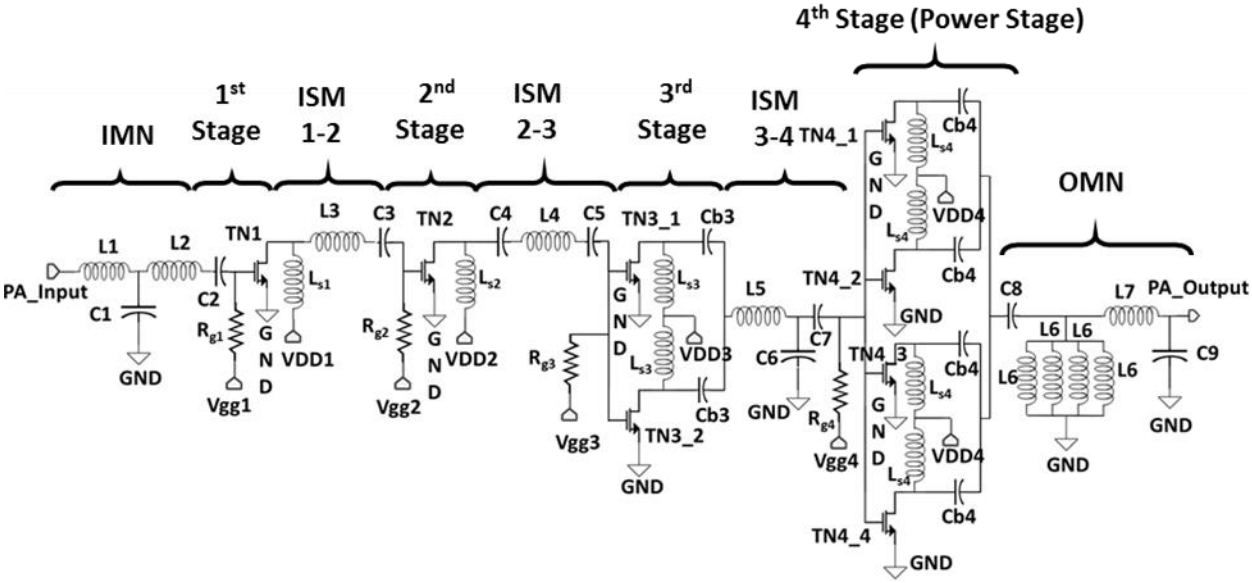

Figure 4.26. Circuit diagram of high-power and high-gain 4-stage PA which uses resistive current combining technique (topology-2).

To improve the output power and the gain, the second topology for PA, as shown in Figure 4.26, is proposed. The size lineup of the transistors of the successive stages are 90 µm, 420 µm, 2x1.3 mm, 4x2 mm, respectively. The key difference in this topology over the other is to use resistive current combining at both third and fourth stages. Another difference is to make the resistive current combining symmetric (binary current combining in a unit cell). Two such unit-cell current combiners have been used in this PA. But to increase power level and current handling capacity from each device, the size of each device is widened to 2 mm. The resistive current combining technique has been discussed in detail in the chapter 3. The size of the devices for the

first and second stage drivers are also increased to handle large current. The input impedance of the first stage of the power amplifier is matched to the output impedance of the balun (topology-2) with the input matching network of T section (L-C-L). Due to improper matching between stages the power may be lost at the input of the next stage and the swing across the device may cross the limit of breakdown voltage. To avoid this possibility, conjugate matching is followed for inter-stage matching (ISM) between 1^{st} - 2^{nd} stage, 2^{nd}- 3^{rd} stage and 3^{rd}- 4^{th} stage. The supply inductors of the 1^{st}, 2^{nd}, 3^{rd} stages have been used as an element for the 1^{st} - 2^{nd} stage ISM, 2^{nd} - 3^{rd} stage ISM and 3^{rd} - 4^{th} stage ISM respectively. As the resistive current combining will provide maximum power only at the optimum resistive load termination, the output power from the device is transferred to the 50 Ω load by using output matching network (OMN). As mentioned earlier, the current combining technique provides lower power loss over power combining technique at low frequency (around 1 GHz). In the power-combining technique successive impedance transformation (Wilkinson combiner, corporate tree combiner) is needed to transfer the power from low device plane impedance to 50 Ω. Moreover, at this low frequency, λ/4 transmission line (TL) based impedance transformation is not feasible. So, several lossy inductors are needed for several impedance transformation sections for power combining technique and, thus, will reduce significant portion of the total output power. On the other hand, in the current combining technique, there is no power loss for each current combiner section. In the current combining technique, the output impedance at the current combiner becomes very low which sometimes makes the design of OMN difficult to achieve low loss unless transformer based OMN is used. In the current combining technique, the use of smaller number of impedance transformation sections can minimize the loss of the OMN consisting of lumped lossy inductors. The supply inductor, L_{s4} at the power stage is no longer ideal choke (for ideal choke large inductance is required and at larger

inductance, Q of the inductor drops and the choke becomes very lossy) rather it has been absorbed as an element to make each device output impedance resistive so that resistive current combining follows between four parallel current combiners. As the resistive current combiners are resonator comprising the device capacitance and supply inductor, the entire power stage can be viewed as N-parallel combination of a current source with a shunt resistor and, thus, the overall device plane impedance is just resistive of R_d/N. The AC equivalent circuit of the fourth stage of the PA can be represented as in the Figure 4.27. The proper current combining and hence maximum power transfer to the load will be at the optimum output load termination. To know the optimum load and the maximum power transferred to the load, the Figure 4.28 will be considered, which shows one current source and a shunt resistor converted to the Thevenin voltage with series resistance and other N-1 stages as N-1 shunt resistors (considering one stage is supplying current and the other stages just act as load and then applying the same to all the other stages and applying superposition to find out the total load current).

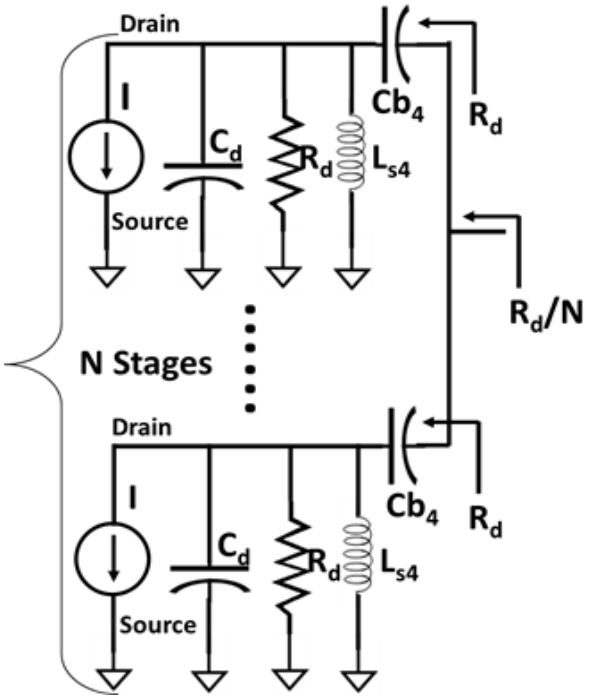

Figure 4.27. AC equivalent circuit of the power stage.

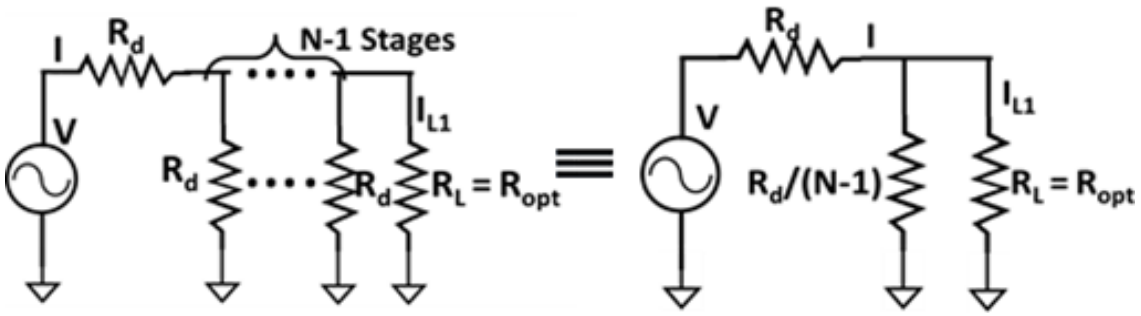

Figure 4.28. Equivalent circuit of the power stage considering one device unit as generator and other N-1 stages as load.

The current generated by one device can be expressed in terms of the voltage across the device (V), device resistance (R_d) and optimum load (R_{opt}) as

$$I = \frac{V}{R_d + \left[\left(\frac{R_d}{N-1}\right) \| R_{opt}\right]} \tag{4.32}$$

Now, the current through the load is given by

$$I_{L1} = \left[\frac{\frac{R_d}{(N-1)}}{\frac{R_d}{(N-1)} + R_{opt}}\right] I \tag{4.33}$$

Now, considering all other device units are behaving in a similar way and finding the load current for each device unit considering it as generator and then applying superposition for current, the total load current is

$$I_L = I_{L1} + I_{L2} + ... + I_{LN} = N I_{L1} \quad \text{as} \quad I_{L1} = I_{L2} = ... = I_{LN} \tag{4.34}$$

The power transferred to the load is given by

$$P_{L,C} = {I_L}^2 R_{opt} = N^2 {I_{L1}}^2 R_{opt} \tag{4.35}$$

Now, from Eqs. (4.32) - (4.35), power at the load can be written as

$$P_{L,C} = \frac{R_{opt}}{\left(R_{opt} + \frac{R_d}{N}\right)^2} V^2 \tag{4.36}$$

and, P_d, the maximum power delivered by one device unit with optimized load of R_d, is given by

$$P_d = I^2 R_d = \frac{V^2}{R_d} \tag{4.37}$$

Now, for maximum power $\frac{dP_{L,C}}{dR_{opt}} = 0$. From Eq. (4.36), this leads to the R_{opt} to be

$$R_{opt} = \frac{R_d}{N} \tag{4.38}$$

and the maximum power becomes

$$P_{L,C} = \frac{N}{4}\frac{V^2}{R_d} = \frac{N}{4} P_d \tag{4.39}$$

Now, for optimum impedance for one device, i.e. R_d = 6.8 ohm and for four parallel stages (i.e. N=4) the overall optimum impedance for maximum power transfer according to the Eq. (4.38) is approximately 1.7 ohm and the maximum power obtainable is given by the Eq. (4.39).

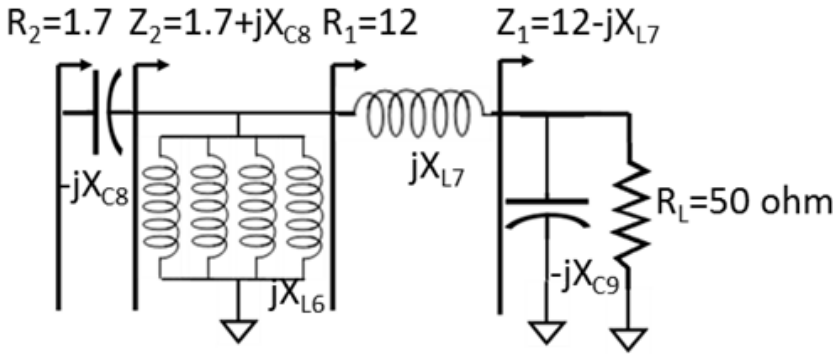

Figure 4.29. Circuit schematic of OMN.

As the optimum load for maximum power transfer is 1.7 Ω, an OMN after the device plane is required to transform the load 50 Ω to 1.7 Ω. Two successive impedance transformation sections have been used to transform from 50 Ωohm to 12 Ωohm and then from 12 Ω to 1.7 Ω. Figure 4.29 shows the circuit schematic of the OMN showing how the 50 Ω ohm load has been transformed into 1.7 Ω. As mentioned in the previous chapter, the two sections are a shunt C - series L and shunt L - series C from load to device side. Here, total shunt L in the 2nd impedance transformation section is used by four parallel inductors to improve the Q of the inductor and to divide the AC

current handling capability through the inductor. So, the OMN of topology-2 is different than that of topology-1. Because of lossy inductors in the OMN, the loss of the OMN is from 2.4 dB to 3 dB within the desired frequency band, whereas the OMN in topology-1 has loss of 3 dB to 3.3 dB in the frequency band.

4.4. Design Challenges

Optimum performance of the whole transmitter can be achieved with the co-design approach where each block is designed with input matching to the output impedance of the previous stage and output matching to the input impedance of the next stage. Design with 50 Ω input / output matching kills the capability to deliver the output power from each block. But, co-design approach sometimes becomes very critical when matching needed from very high impedance to very low impedance or vice versa. The overall performance of the whole ADS-B transmitter depends on three most critical blocks: the VCO, the up-converter, and the PA. In this work, co-design methodology between blocks in the transmitter architecture chain has been followed. In this approach, no longer input and output of a block is designed to 50 Ω termination rather it's input is matched with output impedance of the previous stage and the output is matched with the input impedance of the next stage. This approach saves unnecessary power loss between the blocks due to 50 Ω matching, thereby increasing the efficiency of the whole transmitter chain. To obtain better performance of the VCO, it is better to insert a buffer between the VCO and the hybrid so that operating frequencies from the VCO remains unaffected by the passive components of the hybrid. This will make the system robust. In addition, designing a high-power VCO makes the oscillator pulling by high power PA less significant, which is a critical issue of a direct conversion transmitter. In direct conversion transmitter, there may be a possibility of feedback from output of the PA through the silicon substrate to inject current into the oscillator and, thus,

creates frequency shifting and affects the phase noise. High-power VCO produces higher LO voltage and current swings, which make low amplitude noise current injection less effective to alter the high amplitude of oscillator current swing. Thus, high-power VCO helps to reduce oscillator pulling and retains its actual phase noise after integrating into the transmitter chain. Another important block, the PA block, needs to be designed carefully to provide high power. The design of a PA at high frequencies is somewhat relaxed because the impedance matching can be done by using quarter-wave (λ/4) transmission line and the size of the passive components precisely inductor is low (smaller inductance value for higher frequency). Moreover, because of lower inductance value, high-Q inductor is available. On the other hand, design at the L band, λ/4 transmission line for impedance matching is not possible due to the longer wavelength at these frequencies (λ=30 cm at 1 GHz). In addition, the inductor is very lossy at high inductance value. For the power stage of the PA, the supply inductor is required to be ideal choke and to make ideal choke higher inductance value of 70-100 nH is required at 978 MHz and 1090 MHz frequencies. But at this higher value of inductance, it is very lossy. A high-Q inductor has series resistance of 5 to 6 ohm at this value of inductance at 1 GHz. If the current drawn through each supply inductor is 0.4 A, the power loss is about 0.8 Watt. If the power stage has four current combiners, the overall power loss is 3.2 Watt. This wastage of power can be avoided by using the low value of supply inductor (rather than using ideal choke) and absorbing this inductor as an element in the output matching network.

4.5. Measurement Results

Figure 4.30 and Figure 4.31 show the micrograph of the fully integrated single-chip transmitters of type-1 and type-2, respectively, fabricated using 0.18 um CMOS process. The size of the chips of the type-1 and type-2 are 1.9 mm X 0.84 mm and 4.38 mm X 0.95 mm, respectively,

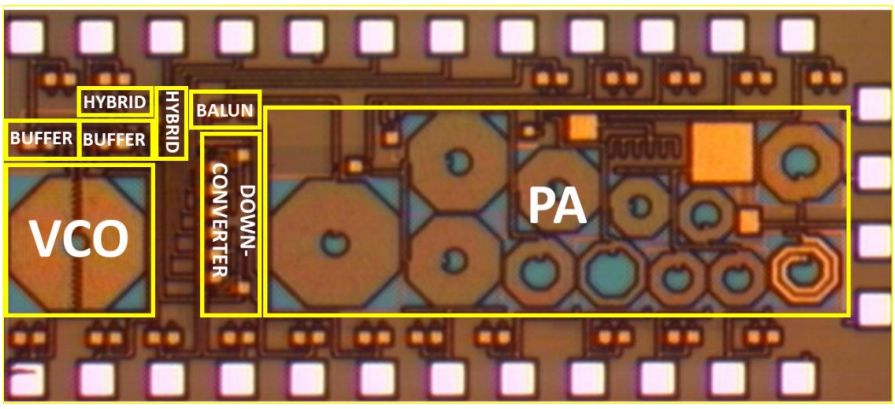

Figure 4.30. Micrograph of a fully integrated 1.9 mm X 0.84 mm fabricated CMOS ADS-B transmitter chip for UAS (type-1).

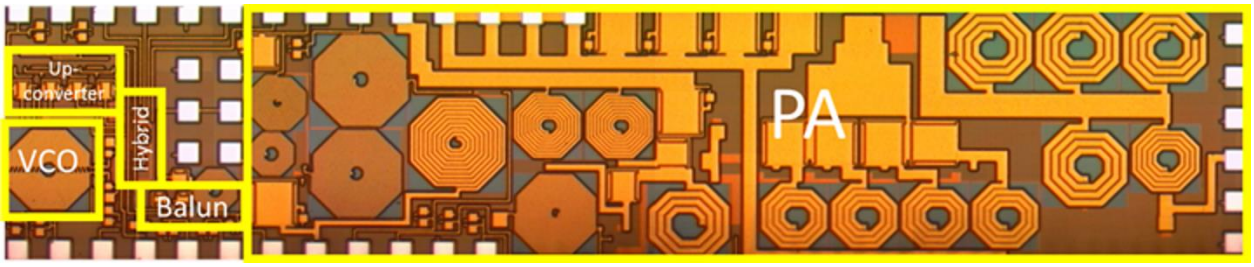

Figure 4.31. Micrograph of a fully integrated 4.38 mm X 0.95 mm fabricated CMOS ADS-B transmitter chip for UAS (type-2).

considering all bond pads. The size of the second prototype is increased because, the PA in second prototype is improved for high-power and high-gain and, thus, consumes more space. The VCO (type-2) with buffer has been measured as a standalone test block and the same VCO is used for the both prototypes of the transmitter chips. As mentioned in the chapter 2, the VCO provides frequency tuning range from 978 MHz to 1100 MHz with tuning voltage from 0 to 3.6V and, thus, covering ADS-B frequency band and a part of the L-DACS2 band. The single-ended output power from VCO at the frequency of 980 MHz is measured to be 0.62 dBm (after de-embedding the cable loss of 1.5 dB) and the single-ended peak output power is measured at 1097 MHZ to be 1.4 dBm. The phase noise of the VCO is measured at 1 MHz offset from the center frequency of 980 MHz and the value is -125 dBc/Hz [12]. The DC power consumption of the VCO core is 8.5 mW and the buffer is 39.5 mW.

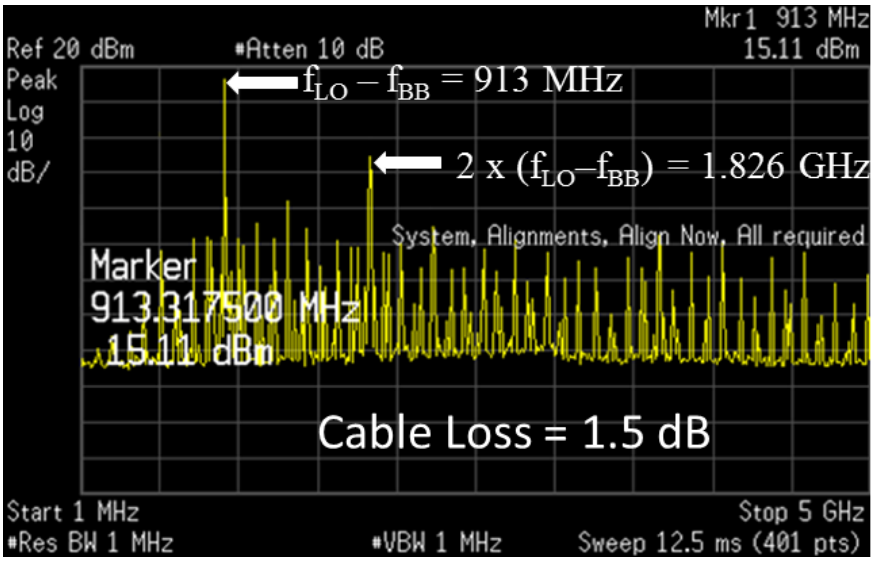

Figure 4.32. Measured single-tone CW output power spectrum of the transmitter (type-1) with carrier frequency of 978 MHz and baseband frequency of 65 MHz giving LSB signal of 913 MHz.

Figure 4.32 shows the measured single-tone continuous-wave (CW) output power spectrum (measured with Tektronix RSA3408B) of the integrated transmitter of prototype-1. With the VCO operating at 978 MHz and the baseband signal of 65 MHz (externally fed at the baseband ports), the transmitter produces LSB signal of 913 MHz and shows the CW output power of 15.11 dBm including 1.5 dB cable loss. So, the maximum single-tone output power from this prototype is 16.6 dBm. The second higher peak at 1.826 GHz is the second harmonic of the LSB signal, which arises due to the nonlinearity of the power amplifier, and it is almost 20 dB down from highest (desirable) peak.

Figure 4.33 (a), Figure 4.33 (b), Figure 4.33 (c) and the Figure 4.33 (d) show the modulated output power spectrum (measured with Tektronix RSA3408B) of the ADS-B transmitter of prototype-2 measured with 25 MHz GSM, 8PSK, 16QAM, and GMSK baseband signals, respectively. The transmitter provides modulated output power of 22.55 dBm, 22.26 dBm, 22.03 dBm, and 22.18 dBm for GSM, 8PSK, 16QAM and GMSK baseband signals, respectively, after de-embedding the cable loss of 3 dB. Figure 4.34 shows the modulated output power against the

frequency of operation of the transmitter and it shows the 3-dB bandwidth of the transmitter is 102 MHz. The DC power consumption of the VCO, the up-converter, the balun, the power amplifier and the whole transmitter chip are 48 mW, 7.5 mW, 30 mW, 4333 mW, and 4418 mW, respectively.

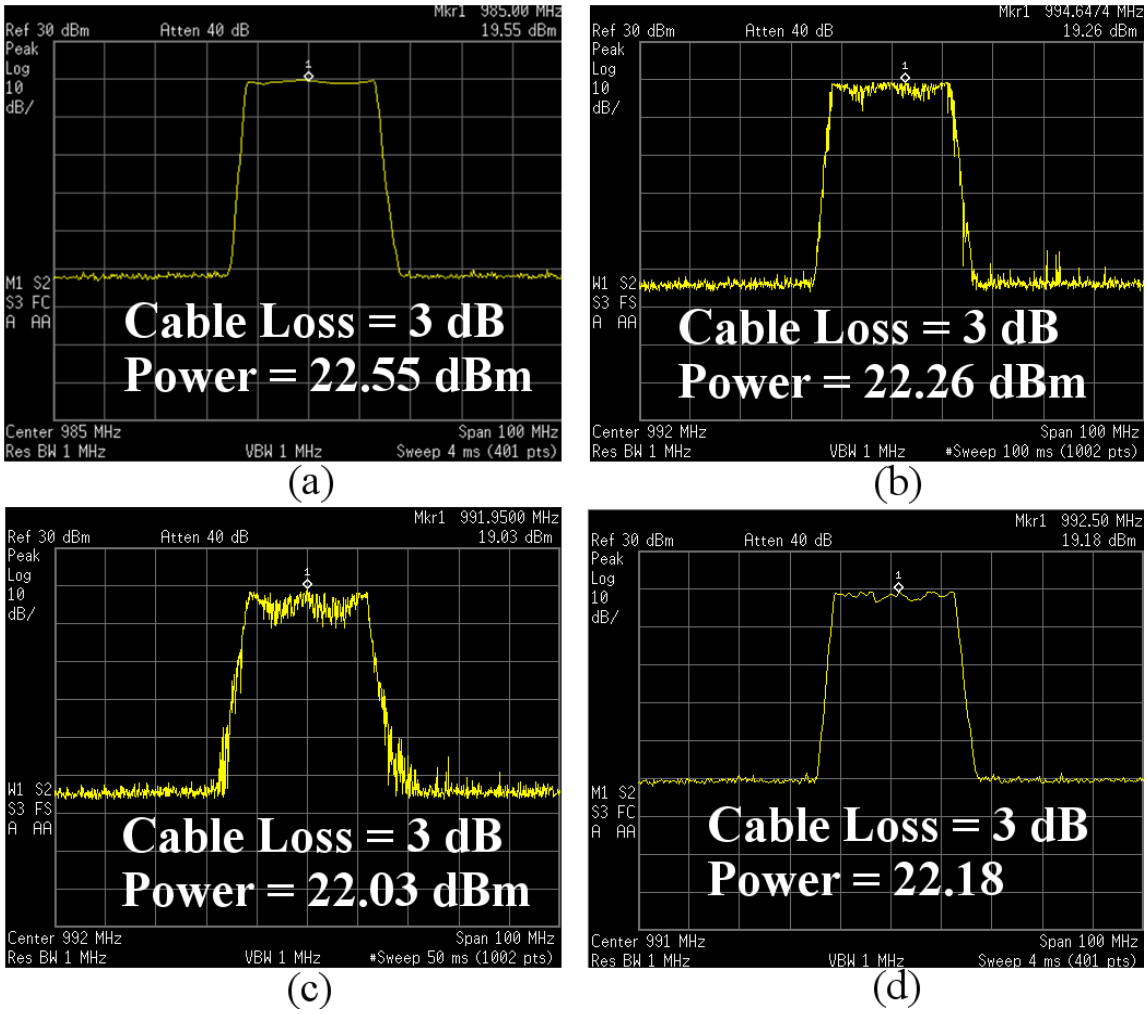

Figure 4.33. Measured modulated output power spectrum of the transmitter (type-2) with 25 MHz baseband a) GSM b) 8PSK c) 16QAM and d) GMSK signals.

The performance of the TX type-1 and type-2 were measured with five and four chips, respectively. The output power from the transmitters show some variations across the chips although overall pattern of the output power versus frequency was similar. Three experiments have been done with a chip which shows the best performance. The output power varies across the

experiments very little with mean and standard deviation of 22.33 dBm and 0.15 dBm, respectively. However, Figure 4.32 to Figure 4.33 shows the best results of the experiments.

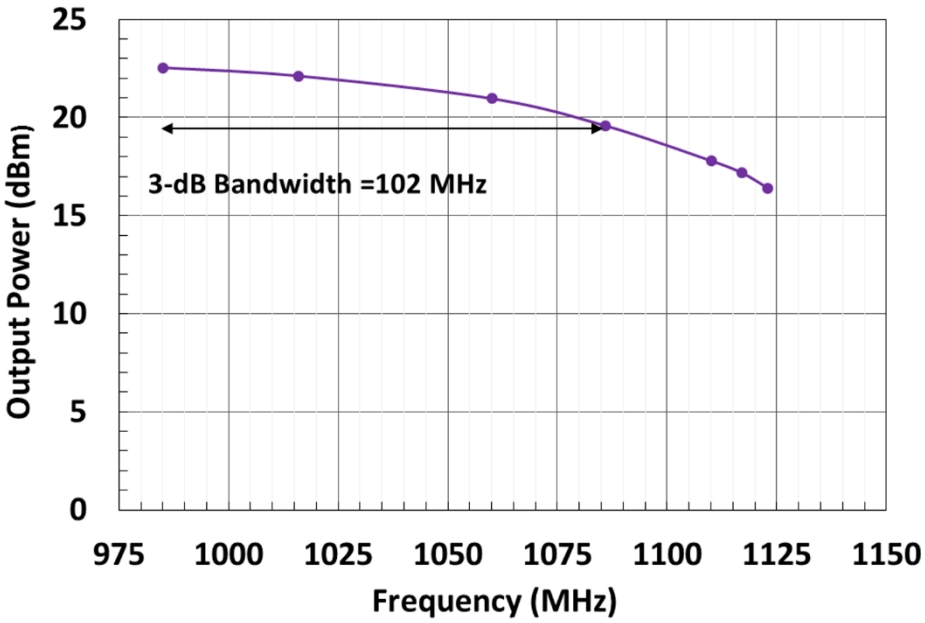

Figure 4.34. Measured frequency characteristics of modulated output power of the transmitter of type-2.

The overall performance of the integrated transmitter chip is shown in the table 11. The table 12 shows the comparison of the output power from this transmitter with the state-of-the art transmitters including their target applications around the ADS-B frequencies and in other S, C, and Ku bands. The transmitters reported in [20], [102]-[103] show the average output power of 20-21.6 dBm whose areas are comparable to this work but their target applications are for IEEE WLAN. The transmitter reported in [101] operating in L-band (frequency of operation is closer to this work) has lower power and higher chip area, and is fabricated in different technology. Whereas, among the transmitters reported in [16]-[19] targeting for cellular applications, [17]-[19] having lower chip area but all of them provide lower power than this work. The transmitter in [21] is designed for micro UAS has lower power and comparable chip area than this work but is operating in different frequency other than ADS-B frequencies (978 MHz and 1090 MHz). Only

the transmitter in [14] which is operating at ADS-B frequencies provides higher power but it is assorted with three different modules in printed circuit board (PCB) and, thus, it consumes very large area. So, from all references, it is clear that to obtain high power from the transmitter, large areas need to be sacrificed. However, this work shows high power ADS-B transmitter with smaller chip area compared to conventional ADS-B transmitter or with comparable chip area compared to other transmitters operating near ADS-B frequencies.

Table 11. Overall performance of integrated ADS-B transmitter

	VCO	Hybrid	Up-converter	Balun	PA	Integrated Transmitter
Frequency (MHz)	978-1100	-	-	-	978-1100	978-1100
Gain (dB)	-	-4.5	5	-4	27	-
Output Power (dBm) (Single-ended)	1.4	-	-	-	24 (Modulated)	23 (GSM)
Return Loss (dB)	-	-	-	-	< -15	< -15
Phase Noise (dBc/Hz) (@ 1 MHz offset)	-125	-	-	-	-	-
Power Consumption (mW)	48 (8.5*)	-	7.5	30	4333	4418
3-dB BW (MHz)	-	-	-	-	275	102

*Calculated without considering the buffer power consumption.

4.6.Conclusion

In this chapter the integration of the ADS-B transmitter has been discussed. The state-of-the-art technology of the ADS-B transmitter is consisting of three different modules (PLL, Up-converter, and PA) in PCB and is fabricated in hybrid IC (HIC) that makes the system to be bulky and expensive. Thus, the state-of-the-art ADS-B transmitter is not suitable for UAS. So, in this

Table 12. Comparison of the performance of the state-of-the-art transmitters in L, S, C, and Ku bands

Application	Frequency of Operation (GHz)	Power (dBm)	Area (mm^2)	Technology	Year References
UAS Tx (ADS-B)	0.978-1.1	23	4.16	0.18 um CMOS	**This Work**
Ku Band RDAR (Micro-UAV Tx)	15	13.3	4.06	65 nm CMOS	2016 [21]
IEEE WLAN 802.11abgn/ac (Dual Band Tx and Rx)	2.4 4.9-5.9	20 18.5	3.4	55 nm CMOS	2015 [20]
L-Band Tx	1-2	15	9.92	0.18 um BiCMOS	2014 [101]
Multimode Tx	0.95- 2.15	11	1.6	40 nm CMOS	2013 [19]
IEEE WLAN 802.11abgn/ac (Dual Band Tx and Rx)	2.4 5	20.5 17.3	3.83	45 nm CMOS	2013 [102]
ADS-B Tx	0.978 1.09	51	- (PCB area)	HIC	2012 [14]
IEEE WLAN 802.11a/g/n (Dual Band Tx & Rx)	2.4 5	21.6 20.5	25	90 nm CMOS	2010 [103]
Cellular CDMA	0.85	5	1	65 nm CMOS	2010 [18]
GSM 850 / EGSM 900	0.85 / 0.9	8	3.8	90 nm CMOS	2009 [17]
GSM 850 / EGSM 900	0.85 / 0.9	4	14.7	0.13 um CMOS	2008 [16]
IEEE WLAN 802.111/b/g (Dual Band Tx)	2.4-2.483 5.15-5.35	8 6	2.6	0.25 um CMOS	2005 [15]

chapter, a single-chip architecture for ADS-B transmitter has been proposed. Two designs of ADS-B transmitter, implemented in CMOS 0.18 µm technology are discussed. Both designs are experimentally verified with measurements and characterizations. In the both prototypes, high-power and high-efficiency CMOS VCO has been used as LO frequency generation for ADS-B

bands. But, ADS-B transmitter of type-2 shows higher modulated output power level than type-1 because of integrating modified balun of lower loss and modified PA with high-power and high-gain in the transmitter chain of type-2. Thus, the high output power (1.4 dBm) from the VCO is maintained at the input of the PA. The modulated output power from the transmitter of the type-2 is 23 dBm and, thus, giving a vertical range of 3 NM for UAS to be operated up to class-A airspace without considering any antenna gain (considering cable loss for both transmitter and receiver side to be 1.5 dB). Considering the antenna gain of 3 dB for both transmitter and receiver, this range can be increased up to 5 NM. Moreover, this ADS-B transmitter chip can drive an off-chip high-power PA to operate the UAS above 5 NM or to meet the performance of the ADS-B system installed in manned aircraft system. Additionally, covering a part of future L-DACS1 (978-1100 MHz) band will enable this single-chip transmitter architecture to have multiple functionalities. Thus, this single-chip CMOS implementation of ADS-B transmitter shows a potential replacement of the state-of-the-art technology by significantly reducing the size and the overall cost of the whole ADS-B system.

CHAPTER 5. CONCLUSIONS AND FUTURE WORKS

5.1. Technical Contributions

- This work first time reported a high-power, high-efficiency and highest FOM CMOS VCO around 1 GHz frequency. By using custom designed diode-connected NMOS transistors as varactor diode for frequency tuning instead of using higher loss design kit varactor diode, and by operating the VCO in the borderline of the voltage-limited and current-limited regime, VCO delivers single-ended output of 1.4 dBm and differential output of 4.4 dBm. In addition, using diode-connected tail transistor, the VCO achieves core efficiency of 32.5% and efficiency of 5.7% for whole chip.
- This work first time reported a high-power and high-gain CMOS power amplifier using resistive current combining technique. The chip provides 23 dBm modulated output power and 27 dB gain with moderate bandwidth of 290 MHz covering LTE-advanced bands from 825 MHz to 915 MHz, ADS-B bands of 978 MHz UAT and 1090 MHz ES modes for UAS and, thus, providing FOM of 50 dB.
- This thesis first time demonstrated to integrate whole ADS-B transmitter blocks into a single-chip for UAS covering both 978 UAT and 1090 ES modes, and a part of future data link L-DACS1 (978-1100 MHz) for UAS. High output power is achieved by using high-power VCO and high-power PA. Using the co-design approach having no unnecessary power losses between blocks and using complex conjugate impedance matching between inter-stages of PA maintains the overall efficiency and ensures the whole transmitter chain to be efficient. In addition, designing high-power VCO makes oscillator pulling by high power PA less significant and, thus, retains its actual phase noise after integrating it into the transmitter chain. Implementing the whole blocks of the transmitter in CMOS 01.8 µm technology significantly

reduce the size and the cost of ADS-B transmitter. Finally, the concept of miniaturization is verified experimentally by measurement / characterization. The chip provides the modulated output power of 23 dBm at LO frequency of 978 MHz with baseband signals of GMSK, QPSK, 8PSK and 16QAM modulated waveforms and, thus, enabling the UAS to operate up to the range of 3 NM (below the class-A airspace) without any antenna gain (considering cable loss for both transmitter and receiver side to be 1.5 dB). But considering antenna gain for both transmitter and receiver to be 3 dB, this range can be increased up to 5 NM. The same chip can be interfaced to drive an off-chip high-power PA chip to operate the UAS above that range, if needed, and / or to operate the manned aircrafts reducing the burden of the off-chip PA. Thus, this work will significantly reduce the size and the cost of the state-of-the-art technology of ADS-B transmitter for UAS. To best of my knowledge, this work is first time to realize the whole ADS-B transmitter into a single-chip.

5.2. Future Works

As ADS-B transmitter is a part of the UAT beacon radio and it has many blocks such as UAT receiver, GNSS receiver, microcontroller, and power supply unit. So, immediate future work will be to integrate both UAT Tx and UAT Rx blocks to a single-chip. Then next work will be to integrate the power supply unit and control the supply intelligently to the PA block to enhance the efficiency of the PA and, thus, to save the battery power. As the microcontroller unit is a digital circuitry, integrating the microcontroller unit is a subject to RF mixed signal integrity issue and possibly would be a good future research work. Thus, integrating the whole UAT radio into a single-chip would be a valuable future research work. In addition, with the same transmitter and added receiver blocks designed in Ka/ku band would find application in sense and avoid radar system. Additionally, the high-power and high-efficiency VCO can be applied in cellular

technology to generate LO signal for GSM cellular handset. Also, the technique of resistive current combining can be applied to any linear PA to obtain high power and large bandwidth.

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APPENDIX A. RELATED PUBLICATIONS

[1] **P. Roy** and D. Dawn, "Fully Integrated CMOS Power Amplifier Using Resistive Current Combining Technique", in *IET Microwaves, Antennas & Propagation* (Accepted on November 29, 2017).

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