HIGH-POWER-DENSITY CONVERTER FOR RENEWABLE ENERGY APPLICATION

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Xiaofeng Lyu

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Title

HIGH-POWER-DENSITY CONVERTER FOR RENEWABLE ENERGY APPLICATION

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The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

DOCTOR OF PHILOSOPHY

SUPERVISORY COMMITTEE:

Dong Cao
Chair

Rajesh Kavasseri

Jinhui Wang

Zhibin Lin

Approved:

11/09/2017
Date

Benjamin Braaten
Department Chair

ABSTRACT

Due to the energy crisis and environmental pollution, renewable sources are more and more important. Power electronics technology is widely applied in these emerging applications and its function is to make the power conversion. The efficiency of power converters is very important and also the size of power converters is more and more concerned. Therefore, high efficiency and high power density with little power loss and light weight are a trend for power converters.

In this research work, light-emitting diode (LED) drivers are first investigated and advanced concaved current control is applied in AC-DC linear LED drivers, which can achieve high power density and high efficiency for indoor applications.

Also, high-power-density single-phase DC-AC inverter with power decoupling function is a very hot topic in Photovoltaic (PV) applications. The research proposed an in-series and in-parallel power decoupling method to minimize the passive dc-link capacitance. Furthermore, an instantaneous pulse power compensator (IPPC) is proposed. When compared with the existing methods, it can achieve higher system power density. Besides, grid-tied controller is designed and tested.

What's more, three-phase inverter is investigated for the segmented motor in electric vehicle (EV) and hybrid electric vehicle (HEV) applications. Interleaved control methods are applied with different control schemes. High-power-density and high-efficiency three-phase inverter systems are compared.

Finally, DC-DC switched-tank resonant converter is studied for 48V data center application. The proposed converter can achieve ultra-high efficiency and high power density. The planar inductor is designed and simulated with Maxwell software. The prototype is made and tested.

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LIST OF ABBREVIATIONS

DC.....direct current.

AC.....alternating current.

PE.....power electronics.

LED.....light-emitting diode.

LCD.....liquid crystal display.

PF.....power factor.

PFC.....power factor correction.

PV.....photovoltaic.

EV.....electric vehicle.

V2G.....vehicle to grid.

HEV.....hybrid electric vehicle.

UPS.....uninterruptible power supply.

SiC.....silicon carbide.

GaN.....gallium nitride.

IPPC.....instantaneous pulse power compensator.

PWM.....pulse width modulation.

PCB.....printed circuit board.

DSP.....digital signal processing.

MMSCC.....multilevel modular switched-capacitor.

ZCS.....zero current switching.

ZVS.....zero voltage switching.

kHz.....kilo hertz.

nH.....nano Henry.

uF.....micro Farad.

1. INTRODUCTION AND MOTIVATION

Due to the energy crisis and environmental pollution, renewable sources, for example, wind energy [1] and photovoltaic (PV) [2]-[3] are widely used. Electric vehicle (EV) and hybrid electric vehicle (HEV) are more and more popular as the oil will be run out in the future. Also light-emitting diodes (LEDs) are taken to replace the traditional light source to achieve more efficiency. Power electronics technology is widely applied in these emerging applications and its function is to make the power conversion. The efficiency of power converters are very important and also the size of power converters are more and more concerned. High efficiency and high power density with little power loss and light weight are a trend for power converters shown in Fig.1.1.

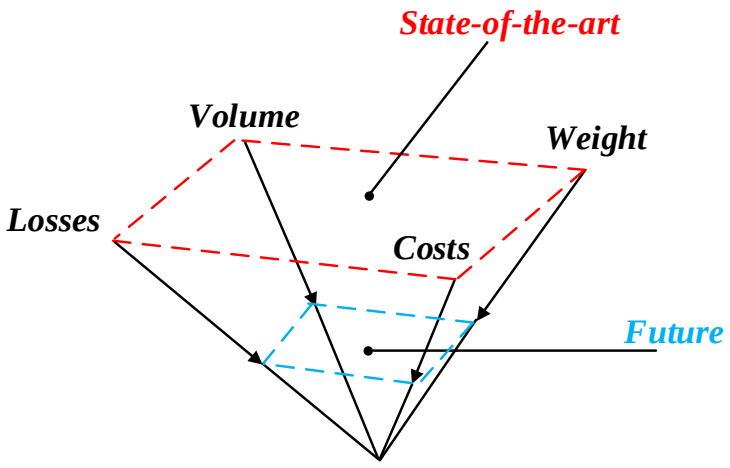

Figure 1.1. State-of-the-art and future of power electronics

1.1. Background

Power electronics technology is widely used in different applications shown in Fig.1.2. For LED applications, LEDs are driven with constant current from the grid power. The power converter is to achieve the function to transfer alternating current (AC) to direct current (DC). Similarly, power converters can make DC power back to grid AC power for PV and wind turbine applications. For EV and HEV applications, power converters can make the battery DC to drive

AC motors. Also data center applications, DC to DC converters are widely used to generate different level of DC voltages. Google Inc. held a high-power-density single-phase inverter competition named Little Box in 2015. The award 1 million dollars encouraged the college and industry to make high-power-density and high-efficiency inverters. Fig.1.3 shows an overview of power density and efficiency relationship for Little Box Competition. To achieve power density more than 50W/inch^3 and efficiency higher than 95%, many college and industry teams did a good job. Normally, the power density and efficiency have a tradeoff relationship shown in Fig.1.3. This is mainly because in order to achieve high power density, usually additional circuits are needed. As a result, power loss will be increased in these applications. However, wide bandgap (WBG) device, such as Silicon Carbide (SiC) device and Gallium Nitride (GaN) device, are more and more popular. This is mainly because they can achieve high switching frequency to make passive filter small and they have lower conduct loss and switching loss compared with traditional Silicon (Si) device. So this dissertation is focused on high-power-density applications with WBG device.

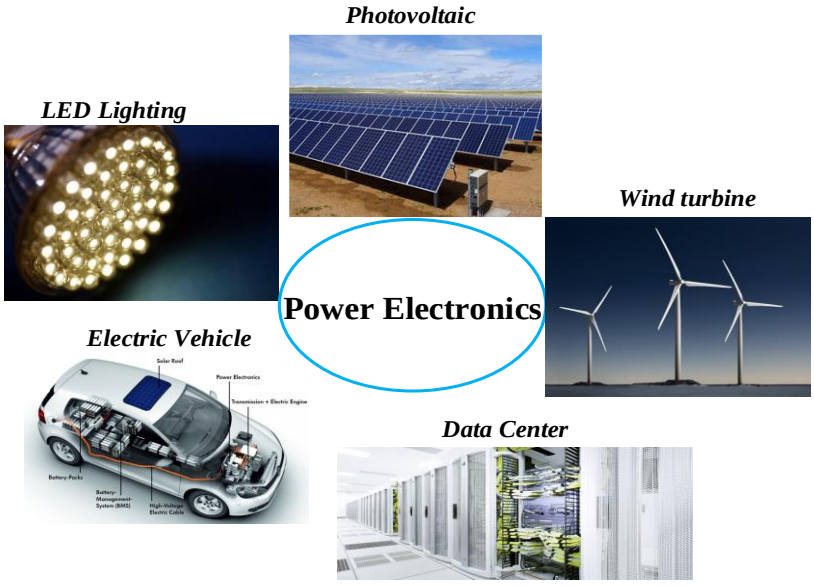

Figure 1.2. Applications of power electronics

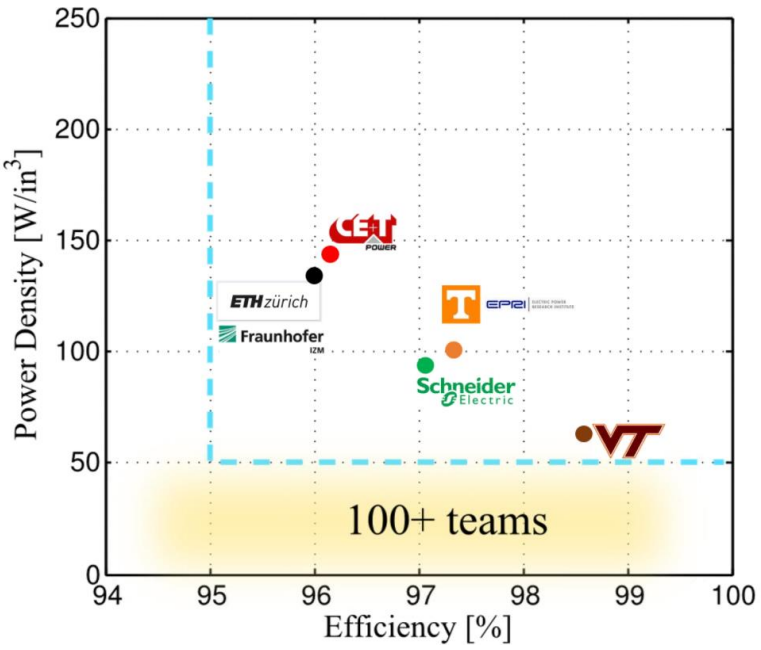

Figure 1.3. An overview of power-density and efficiency for little box challenge

1.2. High-Power-Density for Renewable Energy Application

This section will give a briefly introduction on renewable energy applications, including light-emitting diode (LED) lighting application, photovoltaic (PV) application, electric vehicle (EV) /hybrid electric vehicle (HEV) application and data center application. The existing problems and importance of high-power-density and high-efficiency are briefly introduced, respectively.

1.2.1. LED Application

One typical application for renewable energy application is LED lighting application. Nowadays, LED is more and more popular due to its improved luminance efficacy, long life time and high reliability, when compared with the traditional lighting source. Thanks to these fine characteristics, LEDs are widely used in liquid crystal display (LCD) backlighting, automobiles, automotive headlights and street lighting. Furthermore, LEDs are gradually accepted in residential application instead of traditional fluorescent lighting [1] for energy saving these years. The LED driver is the key component of the LED system since the brightness of LEDs is related to the

driver-controlled-current through the LEDs. The design criterion for the LED driver are high efficiency, high power factor (PF) and low total harmonic distortion (THD). Besides, there is a trend to integrate the LED driver inside the LED package to achieve small size and low cost.

1.2.2. PV Application

Nowadays, photovoltaic (PV) energy has become more and more popular sustainable energy. Because of cost reduction and government incentives, grid-integrated PV system has increased rapidly in the last few years. Normally, there is a large-size dc-link capacitor used in PV applications. For the dc-link side, the large electrolytic capacitor is used to absorb the pulsating power at twice the fundamental frequency. The large electrolytic capacitors could contribute to a short system lifetime and a large prototype volume. Thus, how to reduce this large-size dc-link capacitor is a hot topic recently. With small dc-link capacitor, the system can achieve high-power-density and long lifetime.

1.2.3. EV/HEV Application

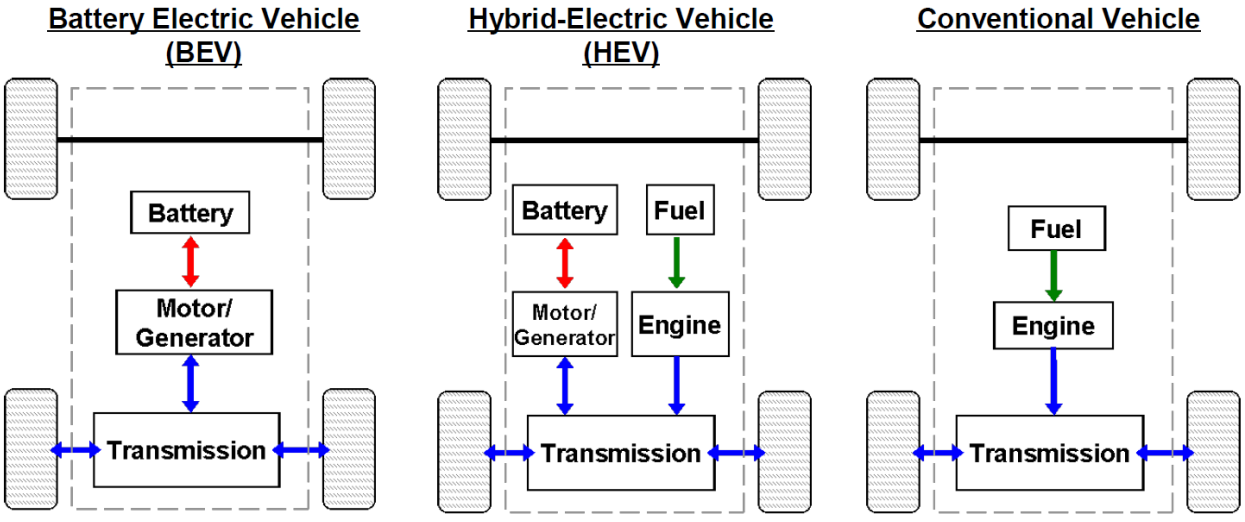

Figure 1.4. Comparison of different vehicles' structure

Electric vehicle is a vehicle that is powered by electricity stored on the vehicle in a battery through the use of one or more electric motors. Hybrid electric vehicle is somehow combined

conventional vehicle and electric vehicle, which use the fuel and battery at different conditions. The structure of conventional vehicle, hybrid electric vehicle and electric vehicle are shown in Fig.1.4. The DC-DC converter boost the dc battery to a high voltage, called dc bus voltage. And three-phase DC-AC inverter drives the motor by transmitting dc bus voltage to AC voltage. Between these two stages, there is a large-size dc-link capacitor applied in the power train system. Unlike the single-phase inverter problem applied in PV applications, for 3-phase inverter system, they have no 2^{nd} harmonic or even low frequency harmonics issue. However, there is still a large volume capacitor selected, because of bus-bar stray inductance and device spike existing in the real system, what is worse, even several large capacitors are in parallel in order to prevent their self-heating, because of the equivalent series resistance (ESR). As a result, the root-mean-square (RMS) value of the dc-link ripple current is of great importance as reducing this value means high power density and long life time for the whole system.

1.2.4. Data Center Application

Data Center is a centralized repository for the storage, management and dissemination of data and information organized around a particular body of knowledge. Power is the largest recurring cost to the user of a data center. Meanwhile, the size of the whole data center is huge, which takes lots of room. Energy use is a central issue for data centers. Power draw for data centers ranges from a few kW for a rack of servers in a closet to several tens of MW for large facilities. Some facilities have power densities more than 100 times that of a typical office building. For higher power density facilities, electricity costs are a dominant operating expense and account for over 10% of the total cost of ownership (TCO) of a data center. By 2012 the cost of power for the data center is expected to exceed the cost of the original capital investment. As a result, the whole system efficiency and high power density with small size is very important.

1.3. Scope of Dissertation

As described above, the scope of dissertation is to solve these issues mentioned above. For different applications, power density is more and more concerned in common. The key point of this dissertation is to solve power density issue with wide bandgap device and different ideas to make the converter or inverter system size become small and also keep the efficiency high. The goal of this research is to develop high power density, high efficiency converters for LED application and to develop high-level technology power decoupling method to solve the size problem in PV application and EV/HEV application, to develop a high efficiency and high power density DC-DC converter used in Data Center application.

1.4. Outline of Dissertation

The outline of this dissertation is as follows,

Chapter 2: firstly, introduction of LED driver application will be summarized. Beyond the state of the art, linear LED driver will be fully introduced for low power application. Single-string LED structure and multi-string LED structure will be compared with the traditional structures. Both the advantages and disadvantages are introduced. Theoretical analysis for single-string structure with different current shape control methods will be shown and the simulation and experimental results will be provided to verify the proposed method. Furthermore, the detailed design consideration is given for the real case. For multi-string linear LED driver, how to configure each string number is usually a different problem. Based on genetic algorithm, a novel configuration method is proposed and finally simulation results verify the proposed idea very well.

Chapter 3: power decoupling methods are widely used to achieve the system high power density for PV application. A state-of-the-art of the traditional power decoupling methods will be compared. Then, a novel in-series and –parallel power decoupling method will be proposed. The

circuit description and operating principle will be further discussed. The theoretical analysis and system design will be conducted. Finally, the simulation and experiments will be shown to verify the proposed idea.

Chapter 4: for power decoupling method applied in the single-phase inverter system, a novel advanced pulse injection power decoupling method is proposed in this chapter. Traditional 2^{nd} order method is fully investigated and the problems of the traditional methods are analyzed. Finally, the IPPC method is proposed and simulation results and experimental results verify the proposed idea very well.

Chapter 5: for PV application, grid-tied inverter with GaN device will be introduced. The detailed controller design is presented for grid-tied function. For detailed problem, this part is to investigate the relay issue before grid-connected. Simulation and experimental results are provided to verify the proposed idea. Furthermore, how to connect to the grid is used PLECS simulation tool and conducted with experiments. Finally, a prototype can be achieved the grid-tied function.

Chapter 6: unlike single-phase inverter system, three-phase inverter system has no low-frequency issues on the dc-link side. However, there is still a large-size dc-link capacitor on the dc-link side. This chapter is focused on system interleaving level to minimize the dc-link capacitor. The theoretical analysis will be derived in this chapter both in the time domain and frequency domain. N-module paralleled method is proposed and simulations are conducted. Finally, the prototype is made to verify the proposed method.

Chapter 7: a novel switched tank converter (STC) is proposed for 48V data center application. Without any large-size inductor, this topology can achieve high-efficiency and high-power-density compared with the existing proposals. 6X single-wing DC-DC converter and system structure will be first introduced in this chapter. The basic operation principle and control

scheme will be shown. Furthermore, the modeling of the proposed circuit is investigated. Simulation results and experimental results are consistent with the proposal. Composite modular power delivery architecture is proposed in this chapter. This novel architecture can be applied AC-DC, DC-DC, DC-AC and AC-AC applications. The total device power stress is extremely low when compared with other topologies. The architecture is presented and some simulation results are shown. Also some future works are given in this chapter.

Chapter 8: conclusion of the dissertation. Finally, contributions are summarized and suggestions for future work are provided in this chapter.

2. LINEAR LED APPLICATION

2.1. Introduction

Nowadays, LED is more and more popular due to its improved luminance efficacy, long life time and high reliability, when compared with the traditional lighting source. Thanks to these fine characteristics shown in Fig.2.1, LEDs are widely used in liquid crystal display (LCD) backlighting, automobiles, automotive headlights and street lighting. Furthermore, LEDs are gradually accepted in residential application instead of traditional fluorescent lighting [4] for energy saving these years. All the typical applications are shown in Fig.2.2.

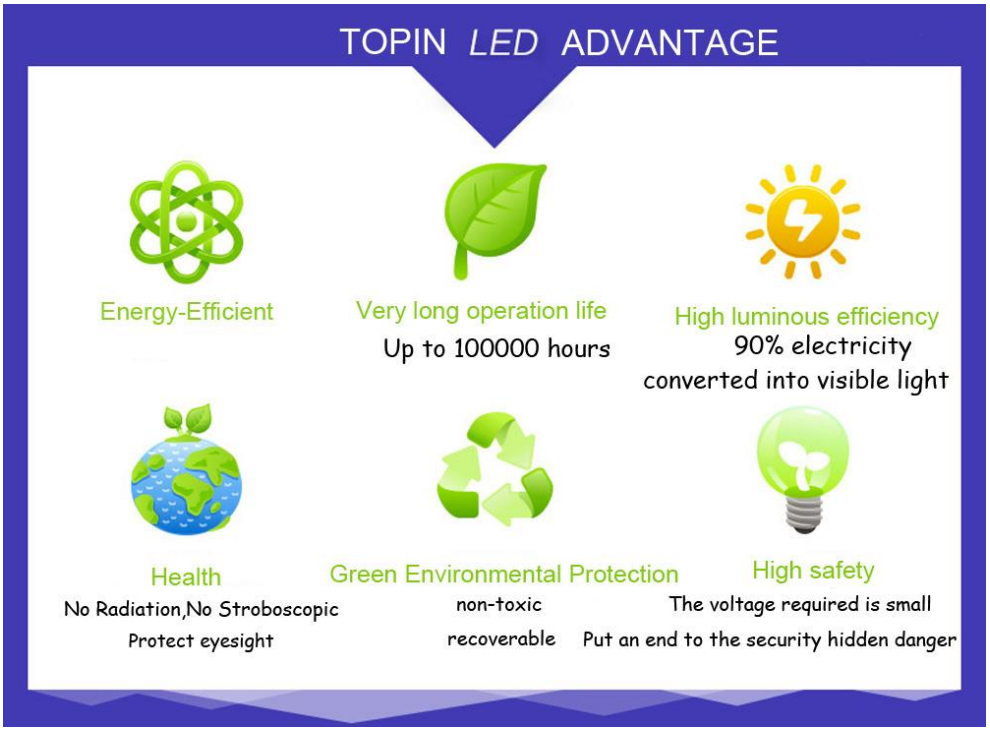

Figure 2.1. Advanced characteristics of LED lighting

The LED driver is the key component of the LED system since the brightness of LEDs is related to the driver-controlled-current through the LEDs. The design criterion for the LED driver are high efficiency, high power factor (PF) and low total harmonic distortion (THD). Various topologies are adopted for the LED driver in different applications [5]. Usually, buck-boost

converter [6], [7] is used for non-isolated application, flyback converter [8] is used for isolated application, and LLC converter [9] is used in high power application. Some other topologies are also applied in LED driver to pursue an improved performance [10]. Many papers are focused on how to drive LEDs in parallel [11]-[16], because how to share and balance the current among different strings is a big issue [17]-[19]. Also some papers pay close attention to dimmable LED driver [20]-[24], as LED luminance is very sensitive to the current through it.

Figure 2.2. Typical applications of LED lighting

2.2. High-Power-Density Linear LED Driver

Compared with topologies introduced above, the linear LED driver has many advantages, such as simple structure, no passive components, easy control and few EMI problems. These advantages bring benefits of low cost and long life time. The linear LED drivers can be divided into single string structure and multi-string structure as shown in Fig.2.3 and Fig.2.4. For multi-string linear LED driver' application, paper [25] reported a method to make a high efficiency and high PF circuit for the LED array. An improved control method is proposed for lighting the LED

array step by step and shaping the output current in proportion to the input voltage. However, it has complex structure and large number of devices. Furthermore, LEDs of the last few rows have low utilization, because they are conducted for a short time during the peak value of the input voltage. On the other hand, paper [26] gives a three-string in series linear LED driver control method. It could make the system power factor high, however, it also needs several switch device and the last few LEDs have low utilization because they are turned on for quite a short time.

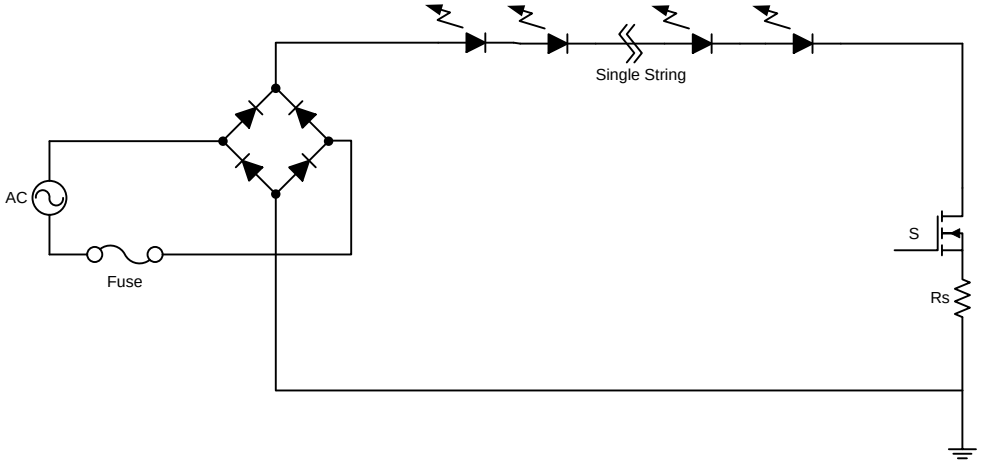

Figure 2.3. Single-string linear LED driver system block

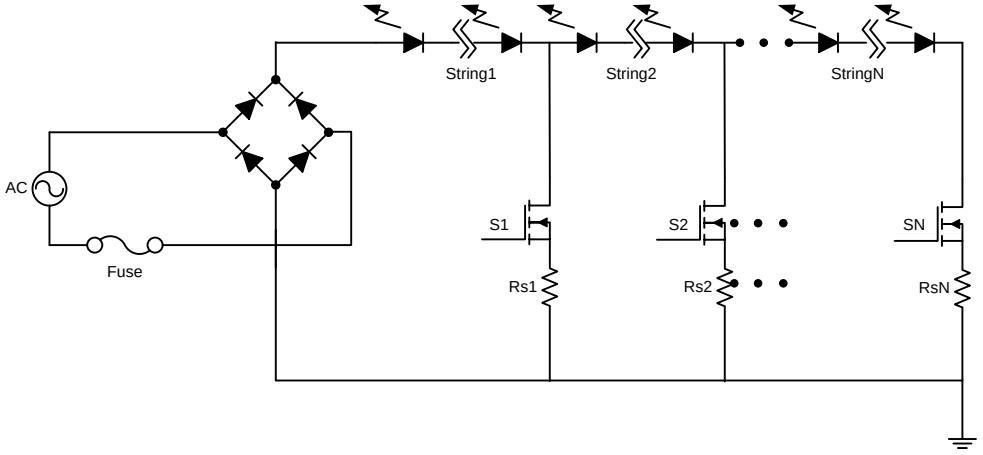

Figure 2.4. Multi-string linear LED driver system block

Paper [27] also comes up with the novel method that by inserting the switching LED module, the linear LED driver could achieve high efficiency without reducing PF. It makes some LEDs lighting even when the input voltage is low through some switching module. However, this method also has complex structure and large number of devices, which has little advantage in low power application.

In additional, in some low power applications, especially in residential application, the efficiency is very important while the high PF is not always required. For example, DoE Energy Star requires that power factor is higher than 0.7 when the power is above 5W and it is not required under 5W power factor [28].

On the other hand, the research on aspects of the single string structure is less. As introduced above, single string structure without much requirement on PF has less device and lower cost than multi-string one, which is more popular in the low power application. However, the efficiency of single string structure is lower than multi-string one. So how to improve the efficiency of the single string structure is a big issue. So this paper is focused on improving the efficiency of the single string structure by altering the input current shape. Also an adaptive current control method is proposed to guarantee the high efficiency under universal input voltage operation.

2.3. Theoretical Analysis

If the number of LEDs in series is given and the output power is constant, changing the input current shape could reduce the input power although power factor could be sacrificed. That means different input current shapes can have different input power under the same input voltage. Power factor and system efficiency need to be traded off when the input current shape is changed. Fig.2.5 gives three input current shapes working in single string structure shown in Fig.2.3. V_{LED} is the total voltage of the LEDs in series. So when the input voltage achieves V_{LED}, LEDs will be

turned on. Different current shapes can be controlled by switching device when $\theta_0 < \theta < \pi - \theta_0$ shown in Fig.2.5.

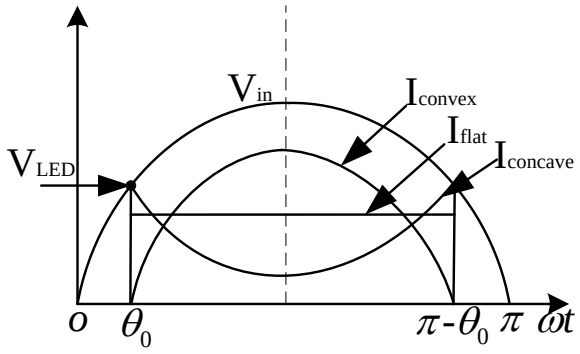

Figure 2.5. Three shapes of the input current

Assuming that the voltage and the average current of LEDs under three different current shape conditions are the same, the output power is equal according to the formula (Eq. 2.1).

$$P_o = V_{LED} I_{av} \qquad \text{(Eq. 2.1)}$$

I_{av} is the average current through the LEDs. When the input voltage reaches the point of V_{LED} shown in Fig.2.5, the LEDs will be turned on at this point, which is defined as shown as (Eq. 2.2).

$$\theta_0 = a\sin(\frac{V_{LED}}{\sqrt{2}V_{in}}) \qquad \text{(Eq. 2.2)}$$

The general current equation could be defined as (Eq. 2.3) shown as follows. I stands for the DC bias value, V_{in} is RMS of the input voltage and k is the coefficient, which affects the peak point of current curve.

$$I(\theta) = I \pm \frac{kV_{in}\sin\theta}{110} \qquad \text{(Eq. 2.3)}$$

Fig.2.5 shows the flat current waveform when $I = I_0$, $k = 0$, the convex current waveform when $I = I_1$, $k = k_1 > 0$ and the concave current waveform when $I = I_2$, $k = k_2 > 0$. Then the three different current shapes' equations are defined as follows (Eq. 2.4) to (Eq. 2.6),

$$I_{flat}(\theta) = I_0 \quad \text{(Eq. 2.4)}$$

$$I_{convex}(\theta) = I_1 + \frac{k_1 V_{in} \sin\theta}{110} \quad \text{(Eq. 2.5)}$$

$$I_{concave}(\theta) = I_2 - \frac{k_2 V_{in} \sin\theta}{110} \quad \text{(Eq. 2.6)}$$

The θ in three equations has the same interval where $\theta_0 < \theta < \pi - \theta_0$ shown in Fig.2.5.

As the average input current is assumed to be equal, then (Eq. 2.7) can be obtained as follow,

$$I_{av} = \frac{\int_0^{\pi} I(\theta) d\theta}{\pi} = const \quad \text{(Eq. 2.7)}$$

Also the input power can be expressed as (Eq. 2.8),

$$P_{in} = \frac{\int_0^{\pi} I(\theta)\sqrt{2}V_{in} \sin\theta d\theta}{\pi} \quad \text{(Eq. 2.8)}$$

The input power of three different current shapes could be compared under same condition. Since the output power is equal, a high efficiency is obtained for a low input power is high according to (Eq. 2.9).

$$\eta = \frac{P_o}{P_{\text{in}}} \quad \text{(Eq. 2.9)}$$

Based on (Eq. 2.7) and (Eq. 2.8), the input power of convex current and flat current conditions are compared as follows,

$$P_{in\_convex}\text{-}P_{in\_flat} = \frac{\sqrt{2}k_1 V_{in}^2}{110} \times [\frac{1}{2}(\pi - 2\theta_0) + \frac{1}{2}\sin 2\theta_0 - \frac{4\cos^2\theta_0}{\pi - 2\theta_0}] \quad \text{(Eq. 2.10)}$$

Also the input power of flat current and concave current conditions are compared as follows,

$$P_{in\_flat}\text{-}P_{in\_concave} = \frac{\sqrt{2}k_2 V_{in}^2}{110} \times [\frac{1}{2}(\pi - 2\theta_0) + \frac{1}{2}\sin 2\theta_0 - \frac{4\cos^2\theta_0}{\pi - 2\theta_0}] \quad \text{(Eq. 2.11)}$$

(Eq. 2.10) and (Eq. 2.11) have the same factor defined as and the values of $f(\theta_0)$ are plotted in Fig.2.6.

$$f(\theta_0) = \frac{1}{2}(\pi - 2\theta_0) + \frac{1}{2}\sin 2\theta_0 - \frac{4\cos^2\theta_0}{\pi - 2\theta_0} \quad \text{(Eq. 2.12)}$$

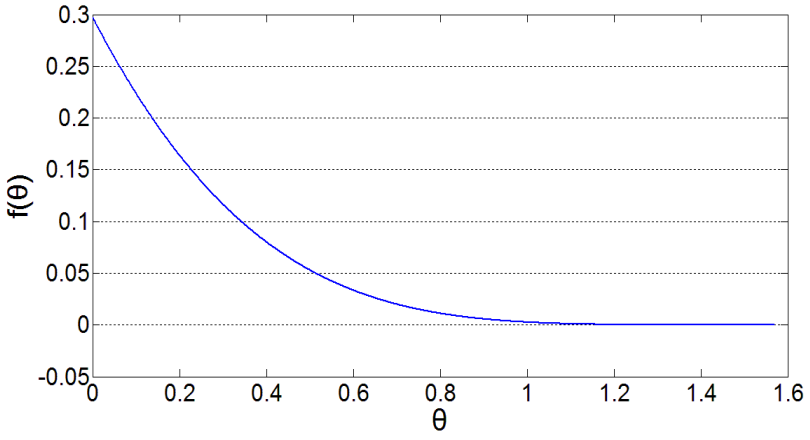

Figure 2.6. The curve of the same factor in formula

The value $f(\theta_0)$ is positive when $0 < \theta_0 < \pi/2$, which is verified shown in Fig.2.6. As $k_1 > 0$ and $k_2 > 0$, $P_{in\_convex} > P_{in\_flat} > P_{in\_concave}$ will be derived from (Eq. 2.10) and (Eq. 2.11). Based on the (Eq. 2.12), under the same condition, the best efficiency is depend on the current shape and it has nothing to do with the input voltage. So this method is valid under universal input voltage condition from 85V to 265V.

In conclusion, different current shapes could affect the system efficiency in single string linear LED circuit. For three current shapes, namely, concave current shape, flat current shape and convex current shape, the efficiency are compared under the same condition of LEDs' voltage and average current $\eta_{in\_concave} > \eta_{in\_flat} > \eta_{in\_convex}$. The concave current shape has the best efficiency among the three current shapes in theory analysis.

2.4. Adaptive Current Control and Design Consideration

The converter with the concave current shape can have higher efficiency than the flat one and convex one. In this part, the factors that affect the efficiency of concave current shape will be further discussed. The bump coefficient is introduced, which means let $k_2 = sI_2$ and the coefficient reflects the concave level. Then (Eq. 2.13) is derived as follow,

$$I(\theta) = I_2 - \frac{sI_2V_{in}\sin\theta}{110} \quad \text{(Eq. 2.13)}$$

The concave current is determined by the coefficient s, the DC current I_2 and the input voltage RMS V_{in}. To guarantee that the current is above zero at $\pi/2$, (Eq. 2.14) could be obtained.

$$sV_{in} < 110 \quad \text{(Eq. 2.14)}$$

As shown in Fig.2.5, when is high, it means the current value at $\pi/2$ and an increased efficiency. However, the power factor (PF) decreases at the same time. Meanwhile, at the conduction point θ_0, the peak current will be high as well. As a result, this method can be used in low power application, when the average current is not very high and PF requirement is not strict.

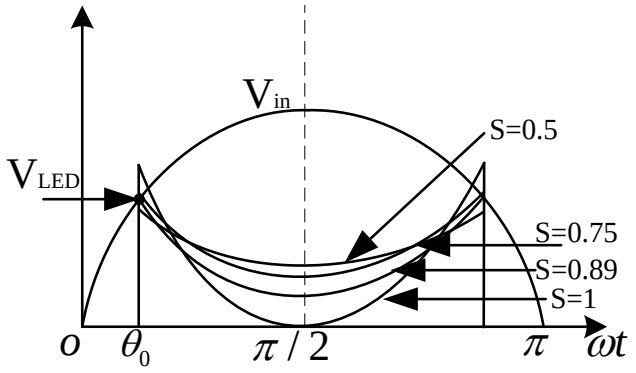

Figure 2.7. Concave current curves under different s

Table 2.1. Efficiency, PF and THD values under different s

s	Concave Current Shape				
	η	PF	THD	I(θ₀)/mA	I(π/2)/mA
0.25	74.0%	0.91	45.5%	65.4	48.2
0.375	75.3%	0.874	55.5%	82	39.6
0.445	77.2%	0.80	74.4%	106	27.3
0.50	81.6%	0.62	126.6%	150	0

Under the condition of $V_{in} = 220V$, $V_{LED} = 200V$ and $I_{av} = 30mA$, the efficiency, power factor, THD and the current values at the point of θ_0 and $\pi / 2$ have been calculated as shown in Table.2.1. With an increasing bump coefficient s, the system efficiency will be increased, however, the power factor and THD will be decreased.

In conclusion, it has to be traded off between the efficiency and power factor when s is adaptively used in concave current shape. In the low power application where power factor is not needed very high, increasing the whole system efficiency with this method has the obvious advantages. Also, if the bump coefficient s could be adaptive under universal input voltage operation, which means sV_{in} becomes high when V_{in} is low. Then a high system efficiency could be obtained under universal input voltage operation conditions.

Although the efficiency of the linear LED driver could be improved by using concave current shape, some practical design factors should be considered. The detailed design consideration should be taken that the peak current at the conduction point could not be too high. So a limit current could be added in the actual circuit shown in Fig.2.8, which is easily implemented by the current limit circuit. And another point is that the current at the point of $\pi/2$ would not be zero. If the current is too low, it may cause the light flickering, which is problematic to the visual comfort, especially in residential application. $I_{off\text{-}set}$ shown in Fig.2.8 is the minimum DC component current, which is determined by the different types of LED lamps. Also in the theoretical analysis, this parameter has already been considered. I_2 in (Eq. 2.13) is represented the DC component to prevent the system flicking happening. The input voltage is varied from 99V to 121V, the LED voltage is set as $V_{LED} = 70V$, the average current is set as $I_{av} = 60mA$ and the cut-top current is assumed as $I_{\text{limit}} = 150mA$.

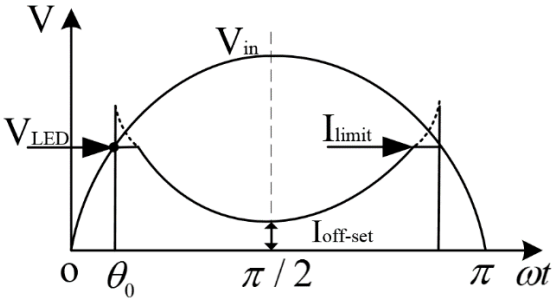

Figure 2.8. The cut-top current waveform

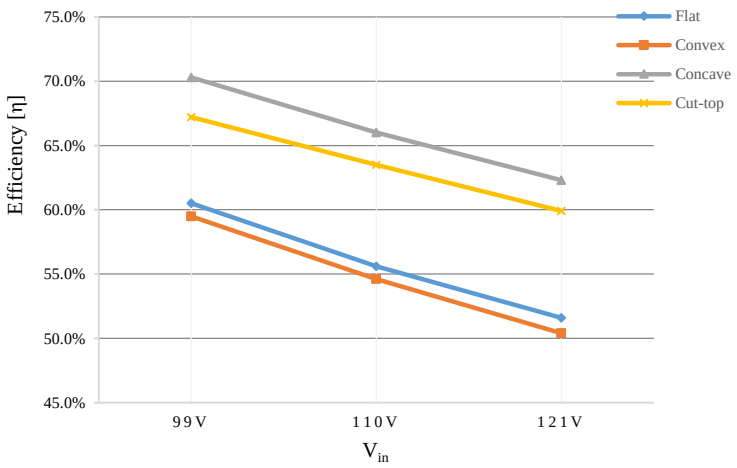

Figure 2.9. Comparison of four current shapes efficiency

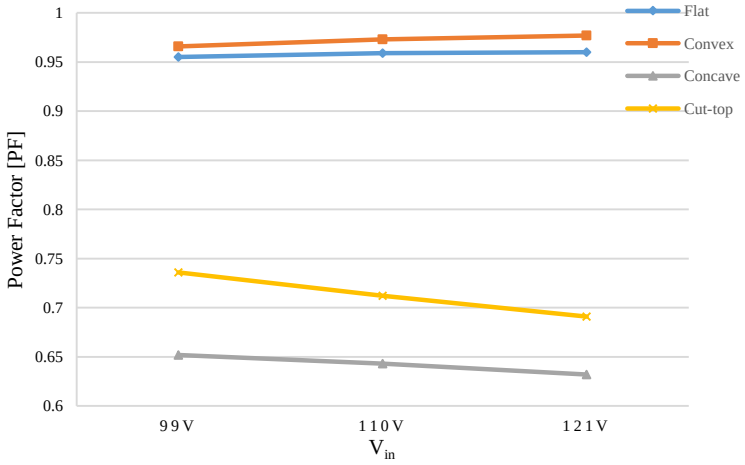

Figure 2.10. Comparison of four current shapes power factor

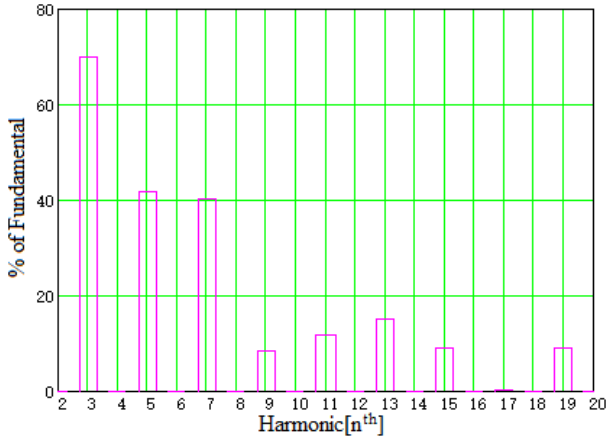

Figure 2.11. Harmonic characteristics of cut-top current

Four different current shapes, namely, flat current shape, convex current shape, concave current shape and cut-top current shape, have been taken into consideration. For these four different current shapes, the efficiency and power factors are calculated based on the equations in section II. The calculations are based on the same condition of the same average current and output power. The results of efficiency and power factors are shown in Fig.2.9 and Fig.2.10, respectively. Fig.2.9 shows that the concave current shape is the most efficient one among the four different current shapes. On the other hand, Fig.2.10 shows that the power factor is the worst for the concave current shape.

It has been discussed before that the peak current at the conduction point should not be too high. In order to reduce the current peak of the concave current shape, a limit current is added as an improved version, namely, cut-top current shape. Fig.2.9 and Fig.2.10 show that the efficiency of cut-top current shape only has a decrease of 2% when compared with that of concave current shape, while the power factor increases a lot (0.1). When compared with the flat and convex current shapes, the efficiency of cut-top current shape is improved by 7%. In conclusion, under the low power condition, especially the power factor is not requested higher than 0.6, the cut-top current shape improved from concave shape is more attractive than the traditional convex current shape and the flat current shape.

The harmonic characteristics of the cut-top current have been analyzed under the assuming condition. THD of the cut-top current under this condition is about 96% and the power factor in this situation is about 0.72. The 3^{rd}, 5^{th}, 7^{th} order harmonic shown in Fig.2.11 are respectively 69.8%, 41.9%, 40.1% of fundamental harmonic, which are not low. This is mainly because the current shape is the concave. In conclusion, it is the trade-off between efficiency and PF, THD.

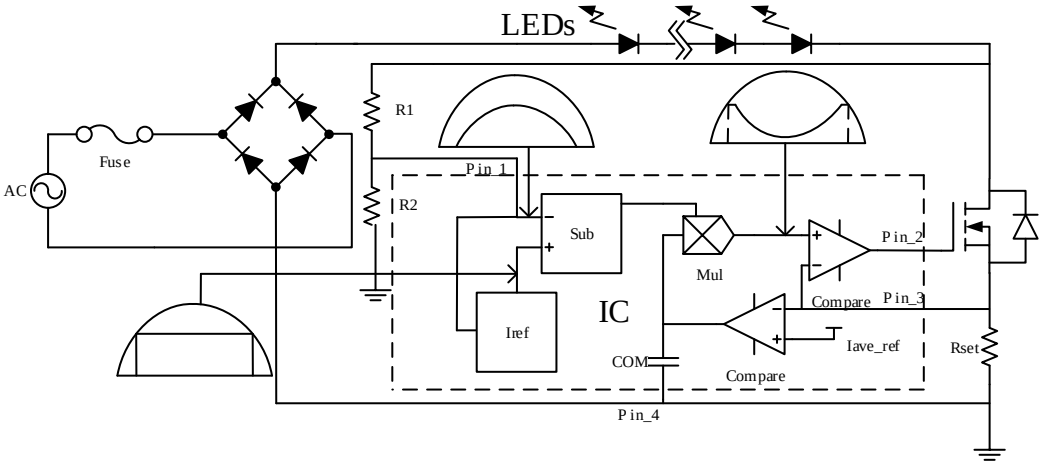

Figure 2.12. System block of concave current waveform control

The system block of concave current waveform control for single-string linear LED drivers is shown in Fig.2.12. A simple structure IC chip is designed to achieve a high efficiency under this low power application. The convex current shape is obtained from the device's voltage as shown in Fig.2.12. And concave current shape is obtained by reversing the convex shape. As a result, the control reference can be achieved. What's more important, the main circuit does not contain any passive components such as capacitor and inductor, which is of great benefits in consideration for a higher reliability and lower cost.

2.5. Simulation and Experimental Results

Simulations with Saber and experiments also have been made to verify the theory analysis of the adaptive current control method. The same conditions are used for the simulations and experiments. The input voltage is varied from 99V to 121V, the voltage of LED is set as $V_{LED} = 70V$, the average current is set as $I_{av} = 60mA$ and the cut-top current is assumed as $I_{\text{limit}} = 150mA$. Fig.2.13-Fig.2.16 show the simulation results with the four different current controls under the input voltage of 110V. Input voltages and the MOSFET's voltages for these four current controls

are shown in the figures. The current waveforms are also shown in Fig.2.13-Fig.2.16, which have the same average current of about 60mA.

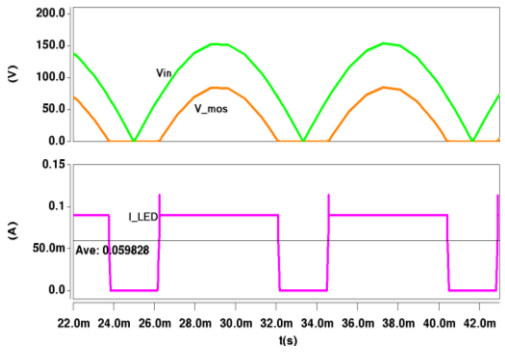

Figure 2.13. Input voltage, MOS voltage and flat current waveform

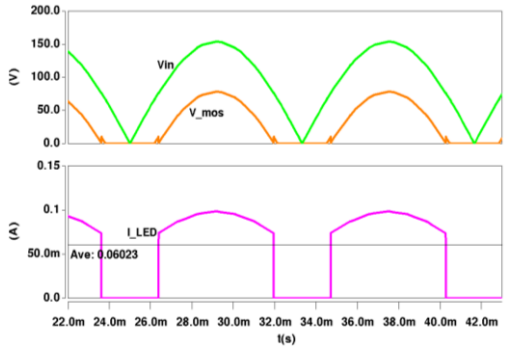

Figure 2.14. Input voltage, MOS voltage and convex current waveform

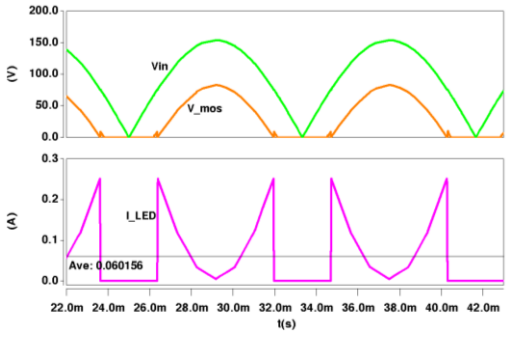

Figure 2.15. Input voltage, MOS voltage and concave current

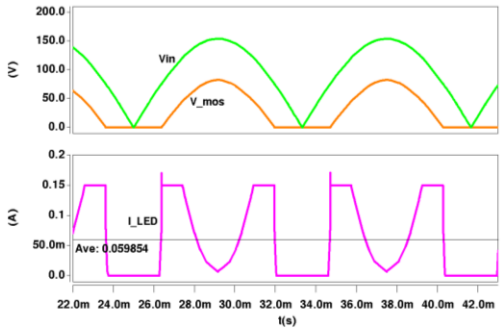

Figure 2.16. Input voltage, MOS voltage and cut-top current waveform

Fig.2.17-Fig.2.20 show the experimental results at the input voltage of 110V for four different current shape conditions, where Fig.2.17 is for flat current shape, Fig.2.18 is for convex current shape, Fig.2.19 is for concave current shape and Fig.2.20 is for cut-top current shape. The input voltage and current waveforms have been measured for these four conditions. It is the same with the simulation that the four current waveforms have the same average current. For the concave current shape as shown in Fig.2.18 there is a peak current of ~240mA at the conduction point. This peak current would lead to a sudden flash of the LED. For the cut-top limit current as shown in Fig.2.20, the peak current is reduced to ~ 150mA. Also, the DC off-set current has been considered to prevent the LED flickering and the off-set value of the concave and cut-top current is both set 15mA during the time pi/2. In the experiment, the practical average current is 68mA, which is a little higher than the theoretical value. This is mainly because that the practical current shape has the rising and falling time, which makes both average current and power factor a little higher than those in the theoretical analysis. Under this condition, the output power increases while the input power is almost the constant. Then the experimental efficiency is higher than the calculation one. Also, the rising and falling time waveform has more abundant harmonic components than the ideal calculation one with no slope. As a result, when compared with the theoretical calculation results in Fig.2.9 and Fig.2.10, the efficiency and power factors are both increased in the experiment. Fig.2.21 and Fig.2.22 show the experiment results of the system efficiency and power factor for

different input voltages. From Fig.2.21, the concave current shape could achieve 10% higher in efficiency than the convex one under universal input voltage operation. And the practical cut-top current adaptive control could achieve 5% higher than the convex one in efficiency. On the other hand, the power factor of cut-top could be higher than 0.7, which could meet the usual power factor requirement in low power application. As a result, the cut-top current shape obtains a better trade-off between the system efficiency and power factor. It achieves a system efficiency improvement for the single string LED driver than traditional methods, while obtaining a sufficient power factor for low power applications at the same time.

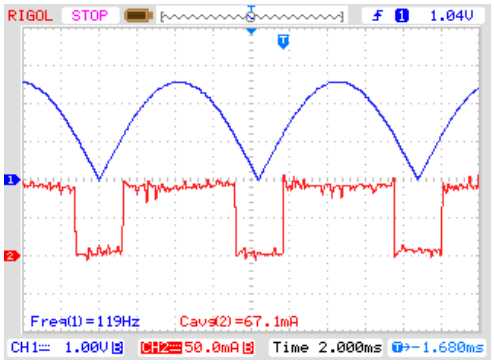

Figure 2.17. Flat current (50mV/div) and sampled input voltage (1V/div), time scale: 2ms/div

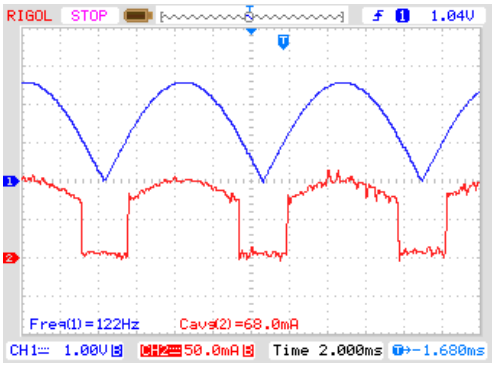

Figure 2.18. Convex current (50mV/div) and sampled input voltage (1V/div), time scale: 2ms/div

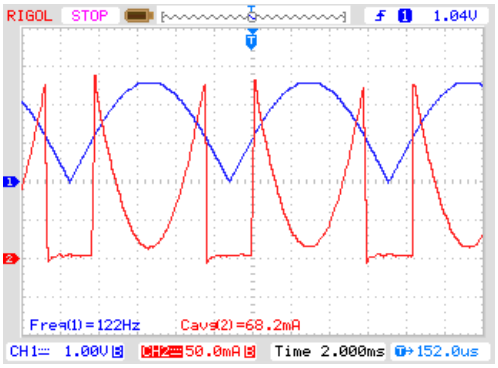

Figure 2.19. Concave current (50mV/div) and sampled input voltage (1V/div), time scale:2ms/div

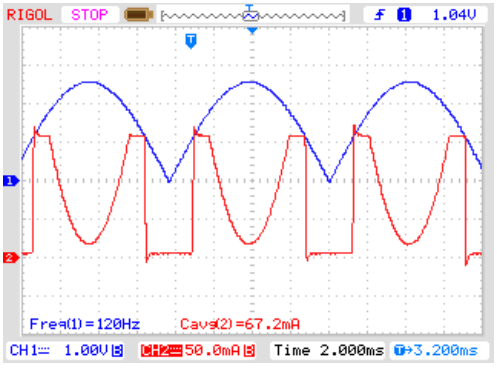

Figure 2.20. Cut-top current (50mA/div) and sampled input voltage (1V/div), time scale: 2ms/div

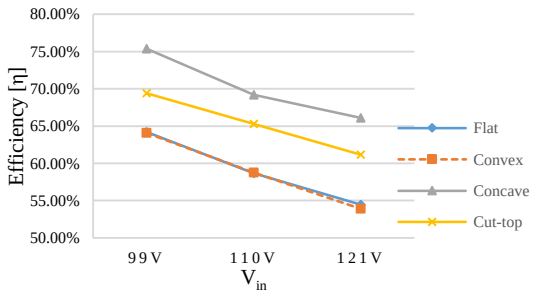

Figure 2.21. Experiments of four current shapes efficiency

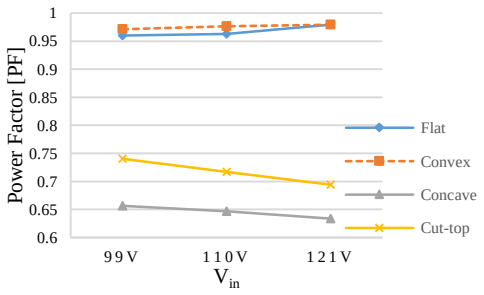

Figure 2.22. Experiments of four current shapes power factor

2.6. High-Power-Density Multi-String Linear LED Driver

2.6.1. System Structure

The linear LED drivers can be divided into single-string structure and multi-string structure shown in Fig.2.3 and Fig.2.4. [1]-[2] focused on the high efficiency single-string structure LED driver. The concave current control method is proposed to make the whole system high efficiency. However, this method satisfied the power factor to achieve high efficiency. Compared with the single-string structure, multi-string structure has better efficiency and power factor. For multi-string linear LED driver application, paper [3] reported a method to make a high efficiency and high PF circuit for the LED array. An improved control method is proposed for lighting the LED array step by step and shaping the output current in proportion to the input voltage. On the other hand, paper [4] gives a three-string in series linear LED driver control method. It can make the system power factor high, however, it also needs several switch device and the last few LEDs have low utilization because they are turned on for quite a short time. Paper [5] also comes up with the novel method that by inserting the switching LED module, the linear LED driver can achieve high efficiency without reducing PF. It makes some LEDs lighting even when the input voltage is low through some switching module. However, this method also has complex structure and large number of devices, which has little advantage in low power application. Furthermore, how to configure the LED number of each string is less. Because of multi-string structure, different number of each string can achieve different efficiency for the same system. So this paper is focused on how to configure the number for each LED string to achieve high efficiency for the whole system based on genetic algorithm.

For multiple string LED drivers, for example, four-string LED structure, its key waveform is shown in Fig.2. The input voltage is positive sinusoidal waveform after rectifier. The operating

principle for linear multi-string LEDs is very simple shown in Fig.2.23. When the input voltage achieve the first string voltage, the first string LEDs become on. Then when the input voltage value achieve the first string plus the second string voltage, both the first and second string are on. When the input voltage achieve all the fourth string voltage threshold, four string LEDs are all on. In practical, for different string mode, a different current is set up for each mode. Table.2.2 shows under different enabled LED string, different current value is chosen. I_{ref} is the reference current and in practical each string mode can multiply one coefficient based on this reference.

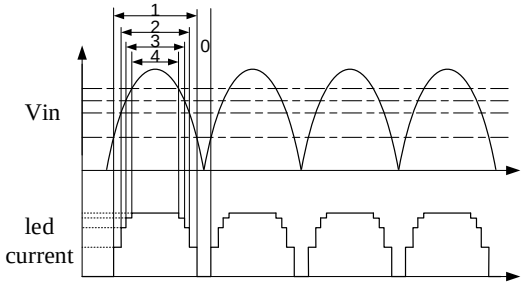

Figure 2.23. Example for 4-string linear LED driver key waveform

Table 2.2. Current setup with Enabled LED String

Enabled LED string	Current Setup
1st	*8 X* I_{ref}
1st & 2nd	*10 X* I_{ref}
1st & 2nd & 3rd	*11 X* I_{ref}
1st & 2nd & 3rd& 4th	*12 X* I_{ref}

When the input voltage reaches the point of θ_n shown in Fig.2.23, the LEDs will be turned on at this point, which is defined as shown as (Eq. 2.15),

$$\theta_n = a\sin(\frac{V_{str\_n}}{\sqrt{2}*V_{in}}) \qquad \text{(Eq. 2.15)}$$

V_{in} is the root-mean-square (RMS) value of the input voltage and V_{str_n} stands for n-string LED voltage value, which is determined by how many LEDs are in-series. Based on this equation, each period for different string mode time can be calculated. Then the output power for multi-string LEDs can be easily got by (Eq. 2.16).

$$P_o = \frac{1}{T}\sum^{n} V_{str\_n} \times I_{str\_n} \times \Delta t_n \quad \text{(Eq. 2.16)}$$

Then based on (Eq. 2.16), the whole system efficiency is easily got.

$$\eta = \frac{P_o}{P_{\text{in}}} \quad \text{(Eq. 2.17)}$$

Based on the analysis above, it is obviously to see the whole system efficiency is depend on different string voltage threshold and reference current configuration. For example, four-string LEDs structure, there are four string voltage set-up and one reference current set-up. Lots of input parameters are related with the final efficiency. Therefore, according to this situation, an optimal configuration method with genetic algorithm is introduced in the next part.

2.6.2. Genetic Algorithm

Genetic algorithm is the advance algorithm to find the best solution based on evolution theory. For industry application, it is widely used to get the optimum solution under various input parameters. Fig.2.24 shows the basic flowchart of genetic algorithm. The algorithm has a fitness function for evaluation of the system solution. For this multi-string LEDs configuration, the fitness function is the whole system efficiency. First of all, a preliminary population are needed to set up. For this example, the preliminary population is the four LED voltage threshold and the reference current. Then an evaluation of the solution is given. Specially, the efficiency is the target for the fitness function. After selection, crossover and mutation, an improved population is created and then make a new evaluation for this improved population in order to get a better efficiency

configuration. After several hundred population, the best or the approximately best solution will be finally got.

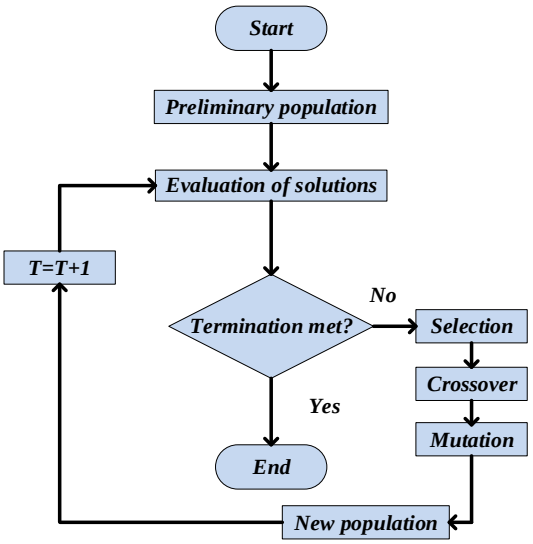

Figure 2.24. Flowchart for genetic algorithm

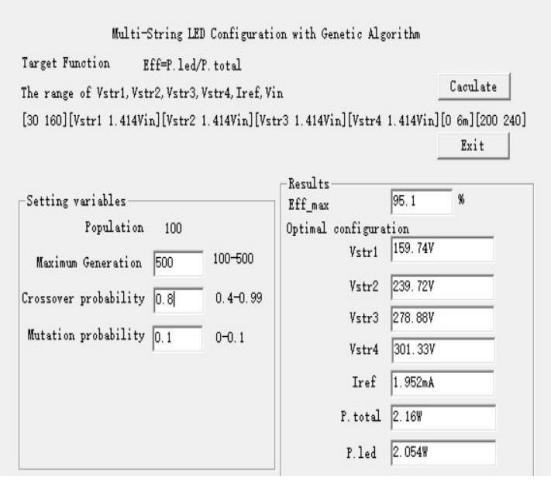

Figure 2.25. Genetic algorithm interface with C++ code for multi-string configuration

Based on this genetic algorithm, interface program with C++ Code is written to get the best configuration for different applications. Fig.2.25 shows the GA interface for 4-string LED configuration. Here the current reference is set up with a range from 0 to 6mA and each string follows the relationship shown as Table 2.3. Also current reference and different string current coefficient as other values, which means for different low power applications. After GA program,

a best configuration is set up with the first string voltage threshold is ~160V, the second string voltage is ~240V, the third one is 279V and the fourth one is ~301V under input voltage 220V. Also the reference current is set up at ~2mA with 16mA, 20mA, 22mA, 24mA for the 1st string, 2nd string, 3rd string and 4th string, respectively. The total power is 2.16W and the efficiency can achieve at 95.1% for low power application.

Table 2.3. Different configurations set up for 4-string LEDs structure

Configuration	String 1 Voltage	String 2 Voltage	String 3 Voltage	String 4 Voltage
1	100	240	279	301
2	200	240	279	301
GA	160	240	279	301
3	160	180	240	260
4	100	180	240	260

2.6.3. Simulation Results

Fig.2.26-Fig.2.30 show the simulation results with saber at the input voltage of ~220V for four-string linear LED driver applications. The four-string voltage threshold is set up based on the genetic algorithm method. The red line stands for the input voltage and the blue line stands for the input current waveform. Fig.2.26-Fig.2.30 show all the configuration's input voltage and input current waveform for one cycle from 50ms to 60ms. As a result, the whole system efficiency can achieve ~95% by genetic algorithm shown in Fig.2.28. Table 2.3 shows some other configuration randomly under the same reference current condition. Fig.2.31 shows these different configuration's efficiency comparison. From Fig.2.31, we can see the solution based on genetic algorithm is the best solution. In conclusion, based on the proposed method, to find a high efficiency LED configuration for multi-string structure is easy to operate instead of complex calculation and simulations.

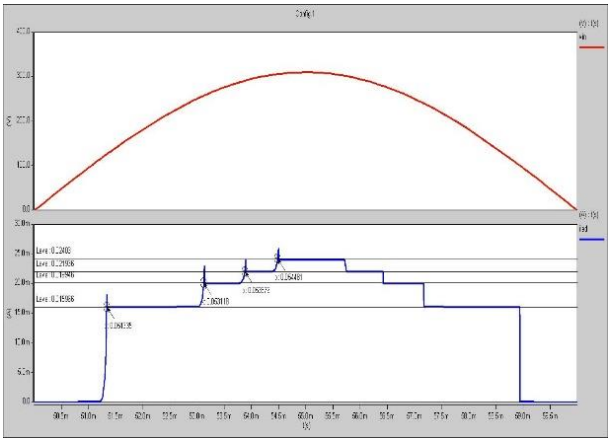

Figure 2.26. Config.1 current and input voltage waveform

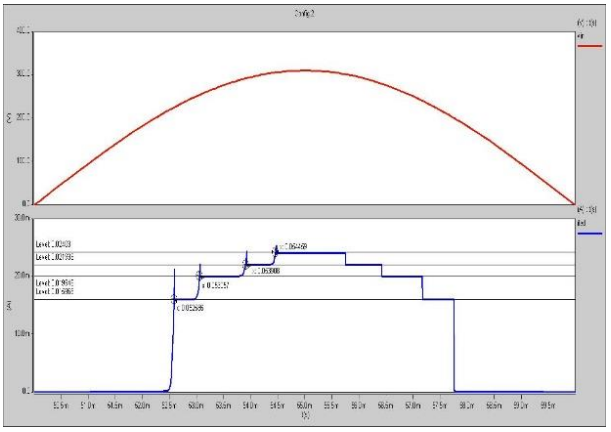

Figure 2.27. Config.2 current and input voltage waveform

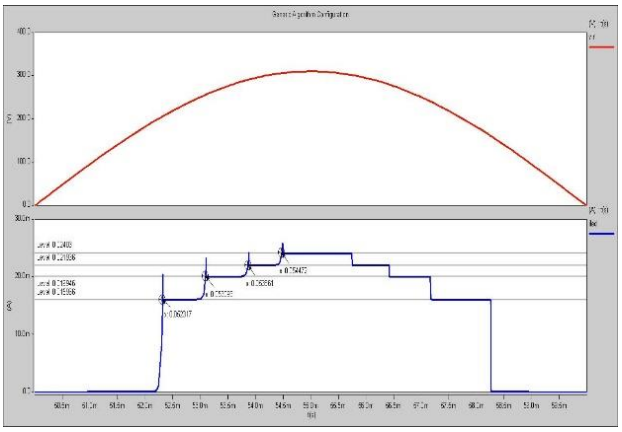

Figure 2.28. GA current and input voltage waveform

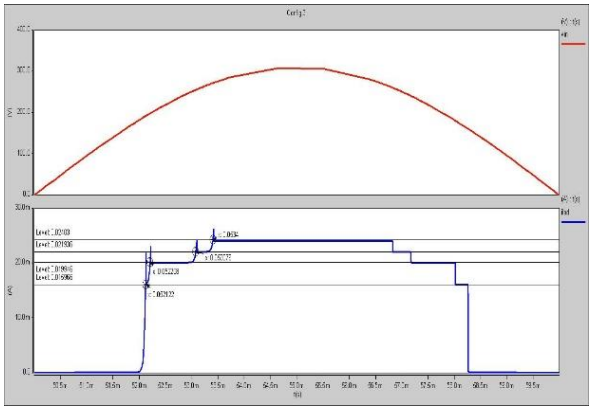

Figure 2.29. Config.3 current and input voltage waveform

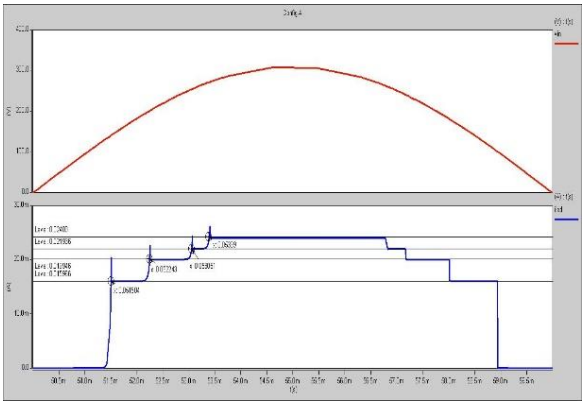

Figure 2.30. Config.4 current and input voltage waveform

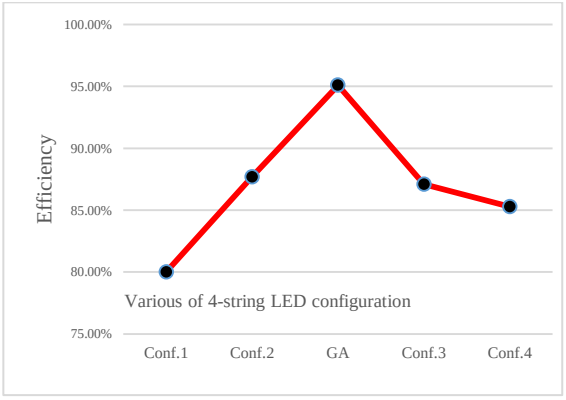

Figure 2.31. Comparison of different configuration system efficiency

2.7. Conclusion

This chapter proposed the concave current control method used in single string linear LED driver for low power applications. Compared with the traditional convex current control and flat

current control, the proposed concave current control method could achieve high efficiency. The operating principles and design considerations of the proposed current control method have been provided. Furthermore, the cut-top current control method is presented in order to limit the peak current of the concave current for practical considerations. A 5% improvement of the efficiency can be achieved by the revised cut-top current than flat and convex current control methods and its power factor could achieve 0.7. The simulation with Saber has verified the proposal. The prototype has been designed, built and tested to verify the proposed current control method. The experimental system efficiency of concave current shape improves 10% higher than that of the convex one under same condition. Meanwhile, this chapter proposed the different string LEDs configuration for multiple string LED structure. Based on the genetic algorithm, a convenient configuration to achieve the high efficiency configuration method is given. With the theoretical analysis and genetic algorithm code, the optimal configuration is proposed. Furthermore, the optimal configuration's efficiency is compared with some other typical configurations. It is shown that based on genetic algorithm method the best optimal configuration for LED number can be fast found. Finally, the simulation results verify the proposed idea very well.

3. HIGH-POWER-DENSITY SINGLE-PHASE INVERTER IN PHOTOVOLTAIC

3.1. Introduction

Single-phase inverter is widely used in many applications, such as uninterruptible power supply (UPS), photovoltaics (PV) and vehicle to grid (V2G) technology. In order to achieve high power density for single-phase inverter, output filter and DC-link capacitor are the two passive parts to be considered to reduce the volume.

Increasing the switching frequency can reduce the filter size. However, the switching loss is increased and very fast switching is also a challenge for Si based device. Silicon Carbide (SiC) [29]-[30] has been identified as a material with the potential to replace Si devices in the near term because of its superior performances such as high thermal conductivity and high critical breakdown field strength [31]-[32]. These advantages could make SiC devices attractive in high voltage, high frequency and high temperature applications.

For the DC-link side, a large electrolytic capacitor is used to absorb the pulsating power at twice the fundamental frequency shown in Fig.3.1. The large electrolytic capacitors could contribute to a short system lifetime and a large prototype volume.

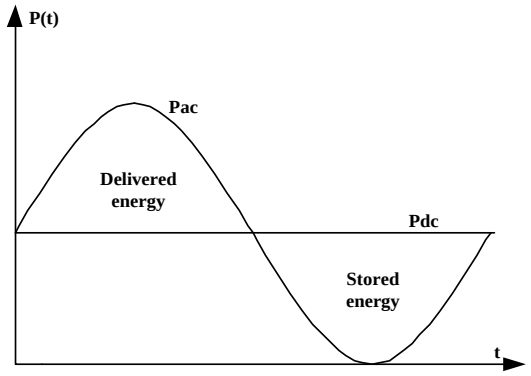

Figure 3.1. Comparison of DC side power and AC side power

3.2. Power Decoupling Method in Single-Phase Inverter

In order to reduce the DC-link capacitors, many power decoupling methods have been proposed and summarized [33]-[35]. In a word, these methods could be divided into two categories.

One kind of method is to use control method in cascade-connection circuits, such as in DC-DC together with DC-AC circuit [36]. The DC-link capacitor current is reduced by sophisticated control [37]. This method has disadvantages of system circuit dependency and inapplicability for single DC-AC circuits.

The active power decoupling methods can be divided into DC-side method and AC third-port method. The DC-side methods contain in-parallel and in-series methods. [38]-[40] showed the DC-side in-parallel method. They introduce buck-boost circuit to store the ripple power to reduce the DC-link capacitors shown in Fig.3.2. Another inverter circuit in parallel was introduced in [41]. 45 degree is shifted to balance the bus line energy. The value of the extra capacitor is very small but its power switching device has high voltage stress. [42] proposed a novel control method to share one inverter leg and one inductor to transfer the second instantaneous power to the AC side. It could achieve lower cost when compared with [40]. However, under the same condition, the extra capacitor value is still large because its switching frequency is dependent on inverter itself. Similarly, [43] used two capacitors on the AC side where each phase leg has a capacitor. [44] also proposed a novel control method without adding extra switching devices to reduce the second-harmonic and the switch current stress. A new current injection method was proposed in [45] to decouple the instantaneous power. A small voltage ripple could be achieved by the AC current injection on the inverter DC side.

A novel in-series method was shown in [46]. As shown in Fig.3.3, there is a compensation voltage source in series in the DC-link line. Usually, this voltage source could be applied with a

full-bridge topology. The additional power device and decoupling capacitor for in-parallel method usually have high voltage stress. The size and package for high voltage stress are normally larger size and high cost. So compared with in-parallel method, for in-series method the extra switching device and decoupling capacitor can have lower voltage stress and the extra capacitors can be easily placed by film capacitors. This is because in-series decoupling circuit only handles the ripple voltage and reactive power flow in the dc-link. However, the value of its additional capacitor is still too large. Although the voltage rating is low, electrolytic capacitors are usually used. Similarly, another in-series topology with this method was proposed in [47] for the current source inverter.

The AC third-port method includes three-leg method and six-switch method. Their typical topologies are shown in Fig.3.4 and Fig.3.5, respectively. The principle of this method is to transfer the ripple power to the third-port on the AC-side. As the third-port is drawn into the single-phase circuit, the three-phase control method could be used in this application. [48]-[51] introduced the three-leg methods. [52]-[54] showed the six-switch method. The space-vector control is often used in this application. The control of AC-side method is flexible. However, the value of extra capacitor or inductor is not obviously reduced compared with that in-parallel DC-side method.

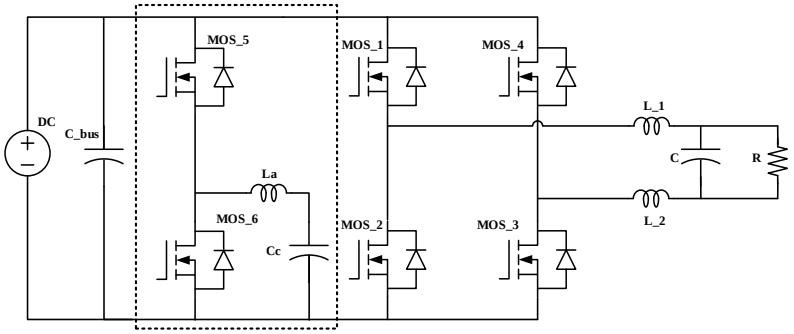

Figure 3.2. DC-side in parallel method

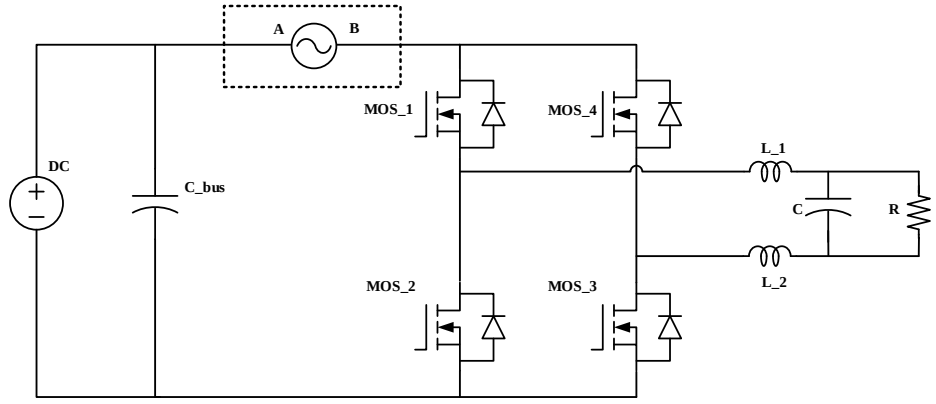

Figure 3.3. DC-side in series method

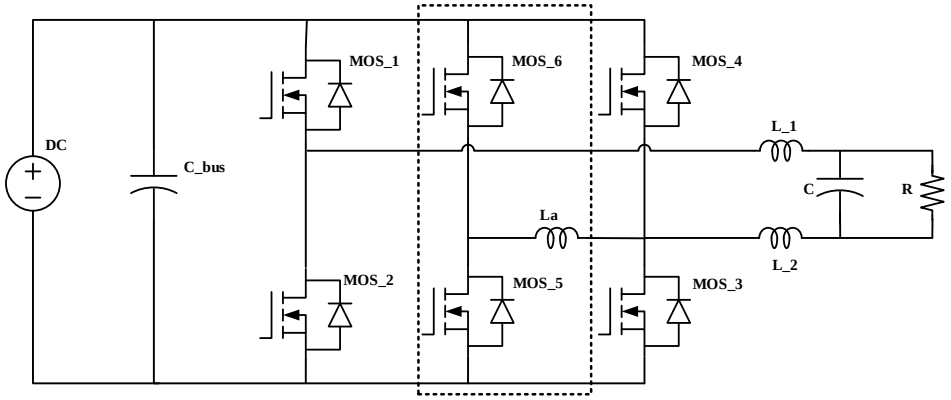

Figure 3.4. AC-side third-port method

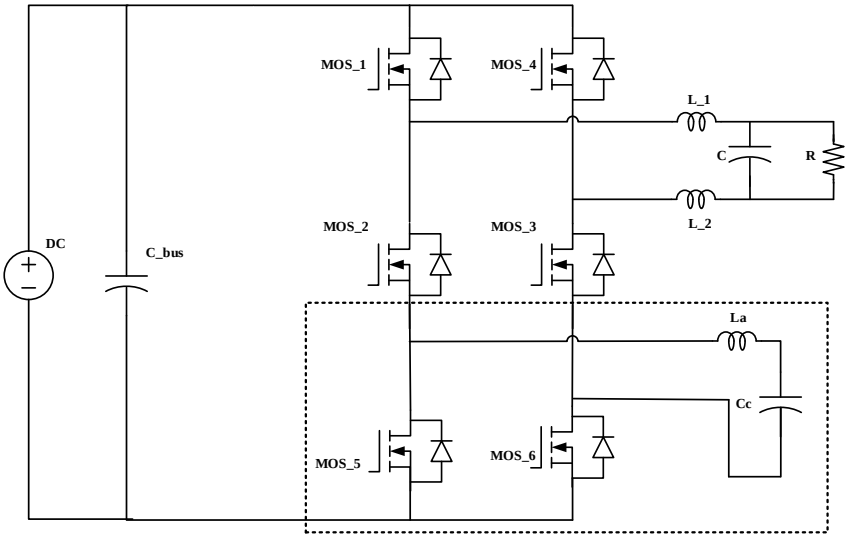

Figure 3.5. AC-side six-switch method

3.3. In-Series and In–Parallel Power Decoupling Method and Theoretical Analysis

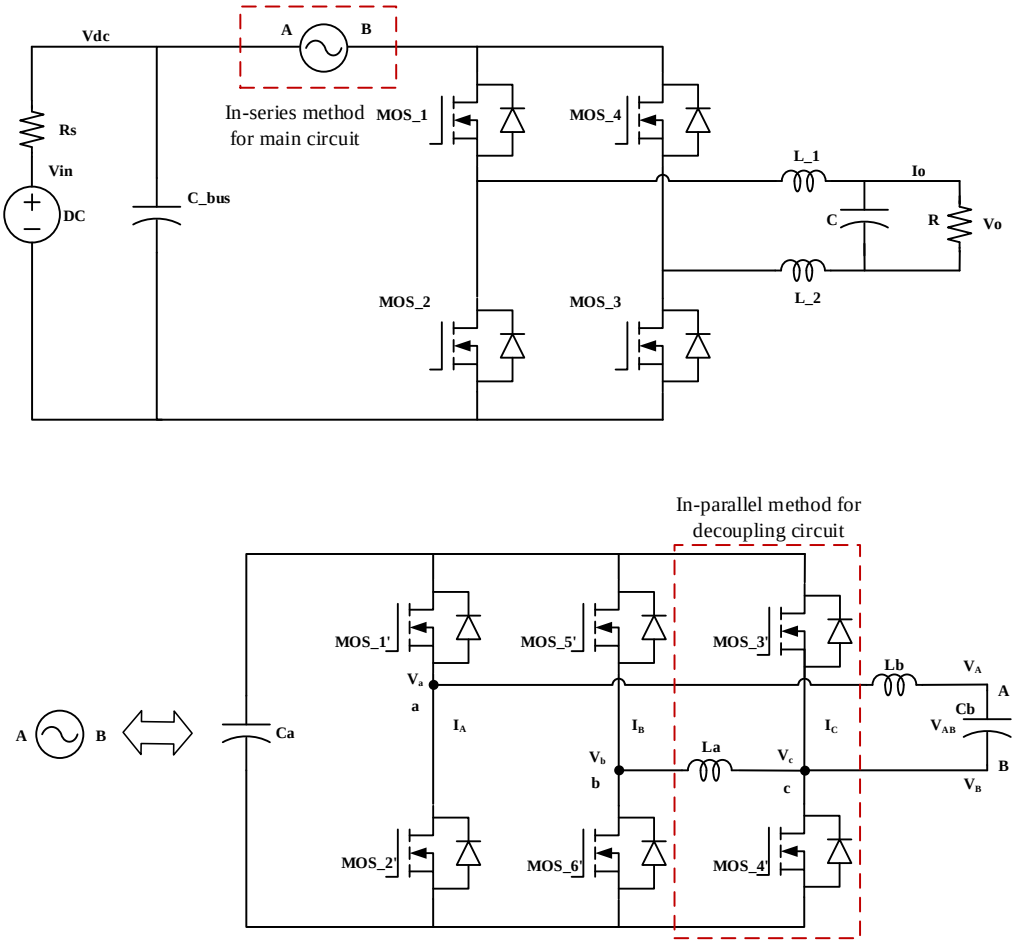

Figure 3.6. The proposed in-series and -parallel power decoupling circuit

Fig.3.6 illustrates the proposed in-series and -parallel circuit to reduce the DC-link capacitor and the extra capacitor. In the single-phase inverter system, the output AC voltage and current are given by (Eq. 3.1) and (Eq. 3.2).

$$v_{ac}(t) = V \sin \omega t \qquad \text{(Eq. 3.1)}$$

$$i_{ac}(t) = I \sin(\omega t + \varphi) \qquad \text{(Eq. 3.2)}$$

where V and I are the magnitudes of the load voltage and the current supplied by the single phase inverter, ω is the angular frequency of the ac system, φ is the power factor angle.

Then the instantaneous power flow is given by (Eq. 3.3)

$$P_{ac}(t) = v_{ac} \times i_{ac} = \frac{V \times I}{2}\cos\varphi - \frac{V \times I}{2}\cos(2\omega t + \varphi) \quad \text{(Eq. 3.3)}$$

The DC-link capacitance can be derived as (Eq. 3.4)

$$C_{dc} = \frac{P_{dc}}{\omega V_{dc} \Delta V_{dc}} \quad \text{(Eq. 3.4)}$$

where P_{dc} is the power rating of the system, V_{dc} is the DC-link voltage and ΔV_{dc} is the ripple of the dc-link voltage.

Since the DC-link voltage ripple is caused by the double-frequency item in equation (Eq. 3.3), a large DC capacitor is always needed to reduce this voltage ripple. In [37], an in-series method is proposed to generate an AC voltage between A point and B point shown in Fig.3.1 to eliminate the DC-link voltage ripple. The voltage and current of AB are defined by (Eq. 3.5) and (Eq. 3.6), respectively, assuming that the phase is the same to the DC-link voltage ripple.

$$v_{AB}(t) = V_{AB}\sin 2\omega t \quad \text{(Eq. 3.5)}$$

$$i_{AB}(t) = I_{AB}\sin(2\omega t + \varphi_{AB}) \quad \text{(Eq. 3.6)}$$

where V_{AB} and I_{AB} are the magnitudes of the in-series voltage and current. As the DC-link voltage ripple is 2nd harmonic order, V_{AB} has the same angular frequency. For in-series voltage source, with a load of only one capacitor C_b, the current I_{AB} could be derived by (Eq. 3.7).

$$i_{AB}(t) = 2\omega C_b V_{AB}\sin(2\omega t + \pi/2) \quad \text{(Eq. 3.7)}$$

So the instantaneous power provided by the extra circuit is given by (Eq. 3.8)

$$P_{AB}(t) = \omega C_b V_{AB}^2 \sin 4\omega t \quad \text{(Eq. 3.8)}$$

Based on equation (Eq. 3.8), the extra circuit instantaneous power does not have active power in a period. The extra capacitor C_a only absorbs the reactive power of the main circuit.

Similar with the DC-link capacitor design method, the extra capacitor is also affected by power rating and ripple voltage. Based on equation (Eq. 3.8), the extra DC-link also has the 4th harmonic order voltage ripple. Furthermore, as switching devices are not ideal and some parasitic parameters in both filter inductor and capacitor exist, there could be DC component in capacitor C_b and other higher order harmonic components injected in the compensation voltage and current. They can also be analyzed using equations above based on Fourier analysis. If there is a little DC component injected in V_{AB}, V_{AB} can be defined as follows,

$$v_{AB}(t) = V_{AB}\sin 2\omega t + V_{dc\_bias} \quad \text{(Eq. 3.9)}$$

where V_{dc_bias} is the DC component, which is a small value. Then the instantaneous power is changed as follows,

$$P_{AB}(t) = \omega C_b V_{AB}^2 \sin 4\omega t + 2\omega C_b V_{AB} V_{dc\_bias} \sin(2\omega t + \pi/2) \quad \text{(Eq. 3.10)}$$

Based on equation (Eq. 3.10), the extra capacitor has both 2nd harmonic order and 4th harmonic order voltage ripple. And the magnitude of the 4nd harmonic order is much larger than the 2nd harmonic order.

As the theory analysis above, although the extra capacitor's voltage could be low based on [37], its value can be very large in order to get a low voltage ripple. Due to the 4th harmonic order voltage ripple across the extra circuit, the third port in-parallel method is introduced to further reduce this extra capacitor C_a. And the power density can be further improved with the proposed method.

For the extra circuit, the voltage and current equations are assumed as follows,

$$\begin{cases} v_a(t) = v_{AB}(t) = V_{AB}\sin 2\omega t \\ v_b(t) = V_b \sin(2\omega t + \varphi_{vb}) \\ v_c(t) = 0 \end{cases} \quad \text{(Eq. 3.11)}$$

$$\begin{cases} i_a(t) = i_{AB}(t) = 2\omega C_b V_{AB} \sin(2\omega t + \pi/2) \\ i_b(t) = I_b \sin(2\omega t + \varphi_{ib}) \\ i_c = -i_a - i_b \end{cases} \quad \text{(Eq. 3.12)}$$

The total instantaneous power of the extra circuit with third-port method could be expressed as (Eq. 3.13) based on space vector method calculation.

$$P(t) = \frac{1}{2}[2\omega C_b V_{AB}^2 \cos(4\omega t + \pi/2) + V_b \frac{V_b}{2\omega L_b} \cos(4\omega t + \varphi_{vb} + \varphi_{ib})] = 0 \quad \text{(Eq. 3.13)}$$

To reduce the extra capacitor, the 4nd harmonic order voltage ripple is transferred from the extra capacitor to the inductor, which means that the equation above is equal to zero. Then based on the relationship between the voltage and current across the inductor, the key value could be calculated with equation (Eq. 3.14),

$$V_b = 2\omega V_{AB} \sqrt{L_b C_b} \quad \text{(Eq. 3.14)}$$

$$\varphi_{vb} = \pi \quad \text{(Eq. 3.15)}$$

As the power rating is low and the frequency is twice as high as that of traditional in-parallel method, the extra inductor can be quite small.

3.4. Operating Principle and Control Strategy

The idealized operating waveforms for the proposed in-series and –parallel method are shown in Fig.3.4. The filter inductance, conduction loss and switching loss in the circuit are all ignored here. It is clear that the power decoupling circuit can provide the second harmonic voltage ripple, which can cancel the fluctuating power from the AC side. The output voltage and current waveforms of the power decoupling circuit are also shown in the figure based on the equations.

As the theory and equations are analyzed above, for extra power decoupling control, the reference voltages are known for each phase leg. Assuming that is the voltage reference for the

extra circuit output voltage and the reference for the voltage applied to the auxiliary inductor L_b shown in Fig.3.3. The modulation functions for the upper switches in each phase leg are given by

$$m_{ap} = \frac{1 + v_a / V_{in}}{2} \quad \text{(Eq. 3.16)}$$

$$m_{bp} = \frac{v_b}{V_{in}} + \frac{1 - v_a / V_{in}}{2} \quad \text{(Eq. 3.17)}$$

$$m_{cp} = \frac{1 - v_a / V_{in}}{2} \quad \text{(Eq. 3.18)}$$

Based on the modulation strategy, the system control block diagram is shown in Fig.3.7. Firstly, the main circuit DC-link voltage V_{dc} shown in Fig.3.3 is sampled and then its ripple voltage is calculated. Based on this ripple voltage and the parallel modulation functions, the detailed control structure can be got. Finally, the PWM control signals of the switching device could be generated according to this control block diagram.

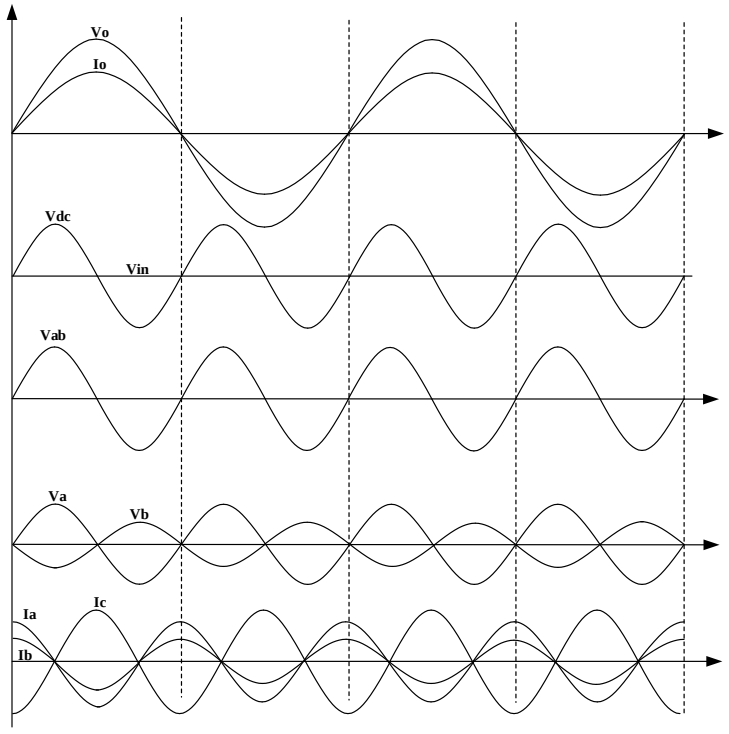

Figure 3.7. Idealized operating waveforms for the proposed in -series and –parallel method

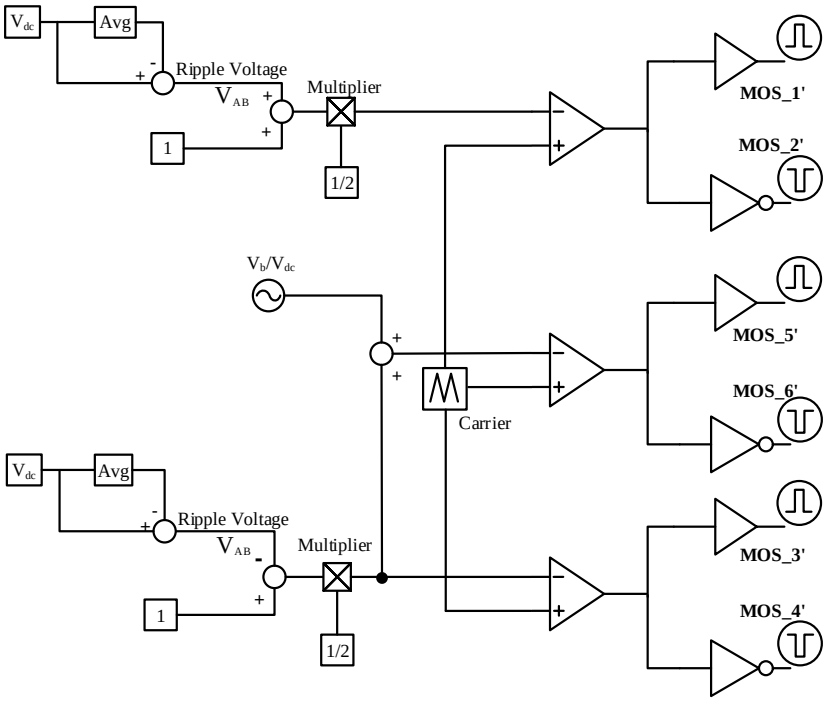

Figure 3.8. Control block diagram for in-series and -parallel power decoupling method

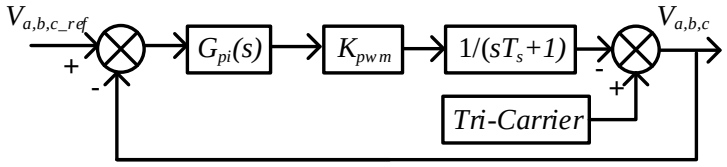

Figure 3.9. In-series and parallel power decoupling control scheme

As the reference of each phase leg is given, simple PI controller could be applied to achieve closed-loop control. Fig.3.8 shows the basic PI control for power decoupling circuit.

Besides the power decoupling circuit controller, the control system block of the single-phase inverter is briefly shown in Fig.3.9. The output filter is designed as LC filter here. Based on the control system block, P and I parameters could be easily designed.

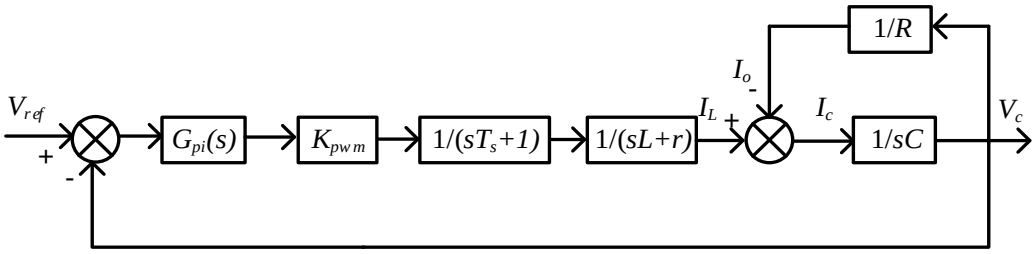

Figure 3.10. Basic control block diagram for the main circuit of single-phase inverter

The open-loop transfer function is shown as follow,

$$G(s) = \frac{1}{LCs^2 + (\frac{L}{R} + rC)s + 1 + \frac{r}{R}} \times \frac{K_{pwm}}{T_s s + 1} \qquad \text{(Eq. 3.19)}$$

L and C are LC filter parameters. R is the load and r is parasitic parameter of the inductor. G_{pi} is the PI controller and K_{pwm} is the ratio between output voltage and dc-link voltage. T_s is the sampling time of the digital system. The detailed design of parameters and system will be introduced next part.

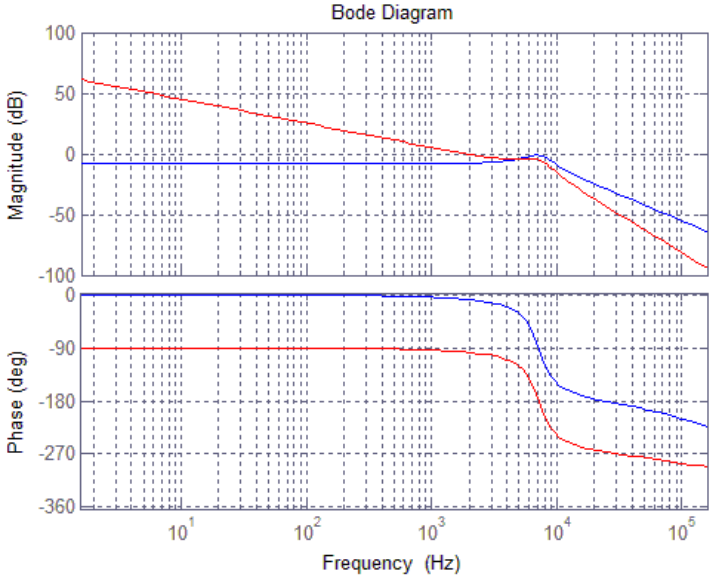

Figure 3.11. Bode plot for the main circuit of single-phase inverter

The open-loop and closed-loop bode analysis are shown in Fig.3.11. It is shown that the magnitude margin and the phase margin of the open-loop are 28.3dB and infinite, respectively. After PI compensation, the closed-loop phase margin is 82.5°. Thus, the whole system has good steady and dynamic performance.

3.5. System Design with SiC Device

The design configuration is shown in Table.3.1. The input is a 450V DC source with a 10Ω resistor in series. And power rating is 2kW with a AC output voltage of 240V. The dc-link voltage ripple is 3%. SiC MOSFET (SCT2120AF) device from ROHM is chosen here. Both conduction and switching loss for body diodes and SiC MOSFET devices together with GaN MOSFET devices are analyzed at different switching frequency and the results are shown in Fig.3.8. It is shown that the switching loss of SiC MOSFET device dominates the total power loss and will increase rapidly with an increasing switching frequency. On the other hand, higher frequency will benefit the output filter reduction. Therefore, a trade-off between the power density and efficiency should be considered. GaN devices are also compared here. Compared with SiC MOSFET, GaN can achieve higher switching frequency under the same condition. However, the characteristics of GaN devices vary a lot with high temperature. Also, its gate driver is hard to design.

Table 3.1. Key parameters in the proposed circuit

Parameters	Value	Parameters	Value	Parameters	Value
V_{in}	450V	R_s	10Ω	$C_{\_bus}$	100uF
V_o	240V	V_{ripple}	3%	P_o	2kW
L_f	240uH	C_f	1uF	*MOS*	STC2120AF

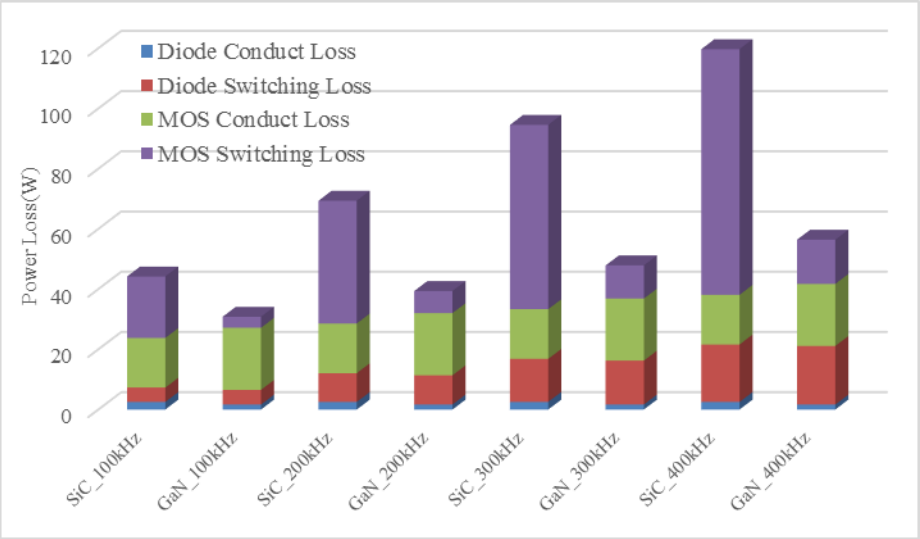

Figure 3.12. 2kW single phase inverter power loss vs switching frequency analysis with SiC/GaN device

If the filter Inductor loss and other loss are considered, the efficiency of the system is shown in Fig.3.13. It gives both SiC based efficiency curve and GaN device based curve to make a comparison here. For high efficiency and system design consideration, 100kHz switching frequency based on SiC device is chosen here. Based on the switching frequency, the AC output filter could be easily designed as shown in Table.3.1.

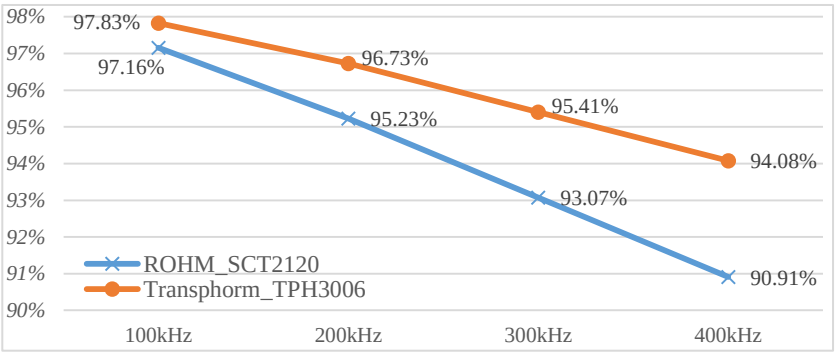

Figure 3.13. 2kW inverter efficiency vs. switching frequency with SiC (SCT2120AF) and GaN (TPH3006)

Similarly, when the extra power decoupling circuit is introduced, efficiency has to be sacrificed to achieve a high system power density. The power loss of the proposed power

decoupling circuit will be analyzed in this section. For power decoupling circuit, the loss for phase A is analyzed as follows,

$$i_a(n) = 2\omega C_b V_{AB} \sin(\frac{n}{N_{cycle}} \times 2\pi + \pi/2) \quad \text{(Eq. 3.20)}$$

$$P_{mos\_con} = 2 f_o \sum_{n=1}^{N_{cycle}} (2 i_a^2(n) \times R_{ds\_on} \times T_s) \quad \text{(Eq. 3.21)}$$

$$P_{mos\_sw} = 2(f_s E_{on} + f_s E_{off}) \quad \text{(Eq. 3.22)}$$

Ignoring the loss of MOS body diode and capacitor ESR loss, the power decoupling circuit losses are composed of MOS conduction loss, switching loss, inductor loss and other loss. The detailed parameters used in the circuit are shown in Table.3.2. Conduction loss and switching loss for phase A can be calculated by (Eq. 3.21) to (Eq. 3.22). Other two phase legs can be analyzed as well. Therefore, the total power loss of power decoupling circuit can be evaluated by the approximate calculation.

Table 3.2. Key parameters of power decoupling circuit

Parameters	Value	Parameters	Value
C_a	300uF	f_s	20kHz
C_b	0.5uF	L_b	500uH
MOS	FDD86102	L_3	500uH

3.6. Simulation Results

The detailed PLECS model is built to verify the theoretical analysis above. The input is a DC voltage source of 450V with a 10Ω resistor in series and the output voltage is 240V. Both Fig.3.10 and Fig.3.11 show the voltage and current waveforms of the main power inverter circuit. The current through the filter inductor and capacitor are also shown in the figures. Fig.3.12 shows the output AC voltage and DC-link voltage ripple for traditional inverter without power decoupling method, in-series method and the proposed power decoupling method. Under the same condition

of a 100uF valued capacitor used in the circuit, both the in-series and the proposed methods can achieve a reduction of DC-link voltage ripple from 87.5V to 10.5V when compared to the traditional without power decoupling method. Both the in-series method and the proposed method could reduce the DC-link capacitor about 89%. The voltage ripple 10.5V over the average dc voltage could achieve the ripple 3%.

On the other hand, for the comparison between the in-series and the proposed methods, the voltage ripples of extra circuit's capacitors are shown in Fig.3.13. It is shown that, when compared to the in-series method, the voltage ripple of extra circuit's capacitor for the proposed method can be significantly reduced from 5.38V to 1.72V. The extra voltage ripple can be reduced 68%.

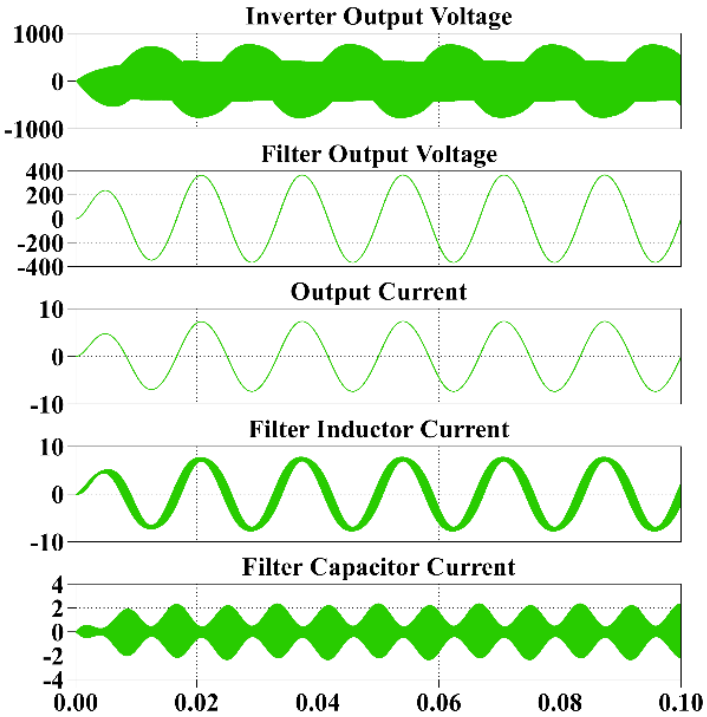

Figure 3.14. Waveforms of main single phase inverter

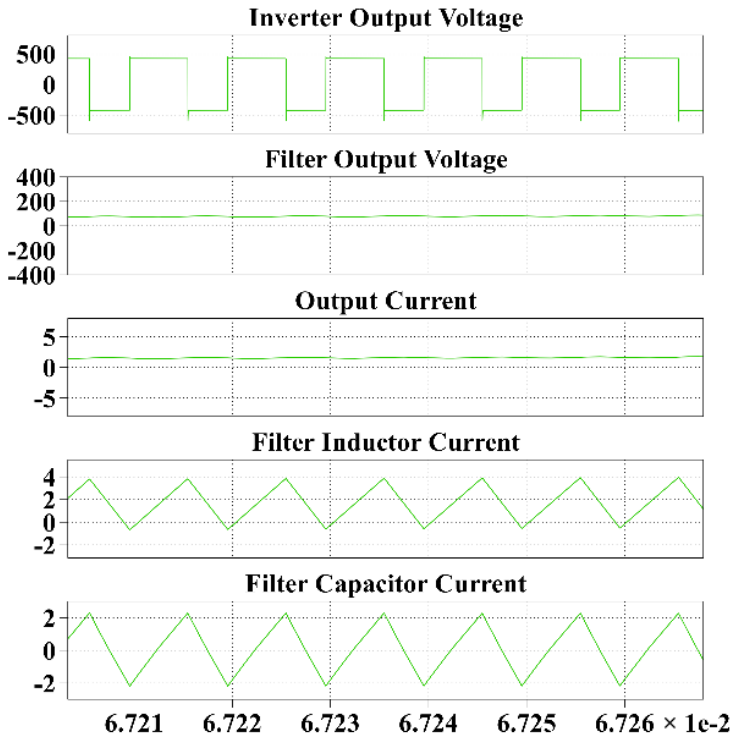

Figure 3.15. Zoom in waveforms of main single phase inverter

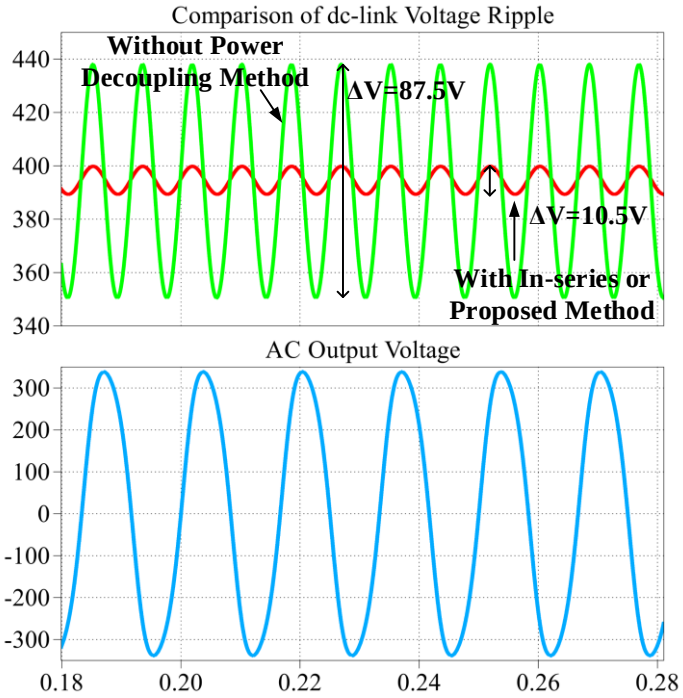

Figure 3.16. Comparison of different methods DC-link voltage ripple

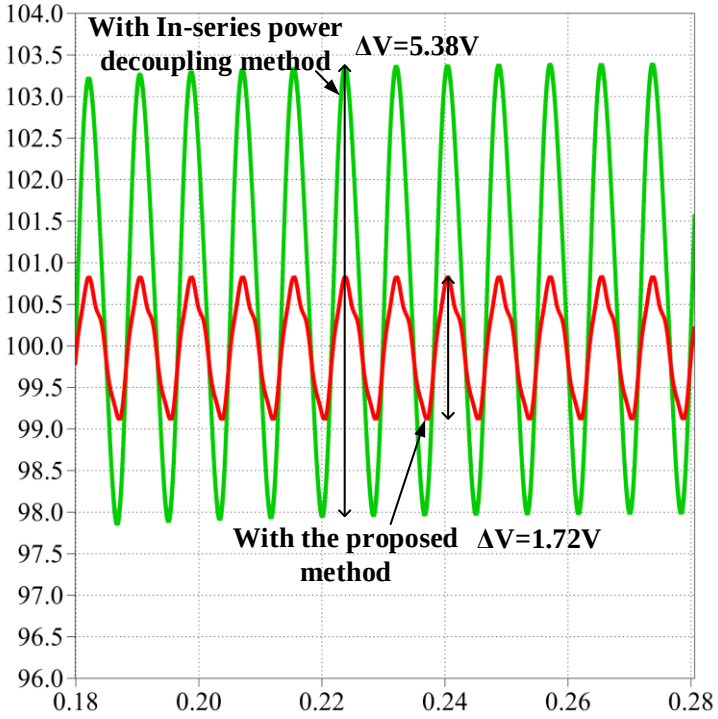

Figure 3.17. Comparison of extra circuits' capacitor voltage ripple

For the theory calculation, under the same voltage ripple around 3%, the dc-link capacitor for the traditional inverter is about 920uF. For the in-series power decoupling method, it just needs about 100uF under the same conditional. The detail capacitor values are summarized and compared in Table.3.3. It is shown that, both the in-series method in [18] and the proposed method in this paper can achieve an 89% reduction of the DC bus capacitance when compared to the traditional SiC based inverter. Furthermore, the proposed method is superior to the in-series method in [18] with a more than 60% reduction of the extra circuit's capacitance. And this result is obtained without any performance penalty. Fig.3.18 shows the spectrum comparison between the in-series method in [18] and the proposed method for the extra power decoupling capacitor. The 2^{nd} harmonic and 4^{th} harmonic voltage components are decreased from 2.59 to 0.79 and from 0.28 to 0.1, respectively. This is result from that the energy of the extra capacitor is transferred to the extra inductor.

Table 3.3. Comparison of capacitor values under the same condition

Parameters	Traditional	Method in [18]	Proposed
$C_{\_bus}$	920uF	100uF	100uF
C_a	-	1000uF	320uF

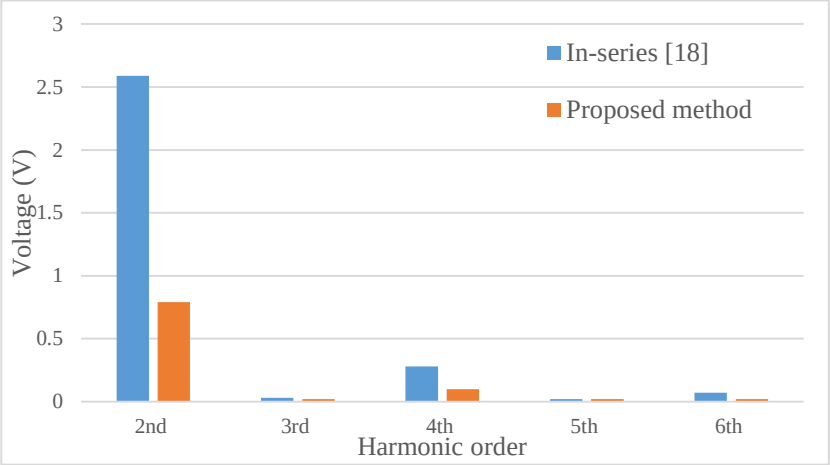

Figure 3.18. Comparison of spectral analysis for extra capacitor voltage

3.7. Prototype and Experimental Results

A 2kW prototype is developed in this paper based on the theoretical analysis. The 3-D prototype model is shown in Fig.3.15. Its size is 7.25×3.6×1.4 inch^3 and the power density of the prototype is about 55W/ inch^3. The test bench is shown in Fig.3.20. Fig.3.21 shows the gate drive waveform of SiC MOSFET device for the main circuit. The DC-link voltage ripples are shown in Fig.3.22 and Fig.3. 23 for the conditions without and with the proposed power decoupling method, respectively. It is shown that, the average DC-link voltage is about 390V due to the effect of the series-connected resistor, and the voltage ripple is more than 12% for traditional inverter. On the other hand, with the proposed power decoupling method, most of the 2nd order harmonic ripple can be eliminated. The dc-link voltage ripple is almost eliminated and the voltage ripple is less than 3% shown in Fig.3.24.

Fig.3.24 shows the comparison of the voltage ripple for the extra power decoupling capacitors between conditions without and with the proposed power decoupling method. It is shown that the ripple of the proposed method (10V) is 64% lower than that of the in-series method (28V). The results are matched with the simulations. As a result, under the same ripple requirement condition, the extra capacitance can be reduced about 64% for the proposed power decoupling method.

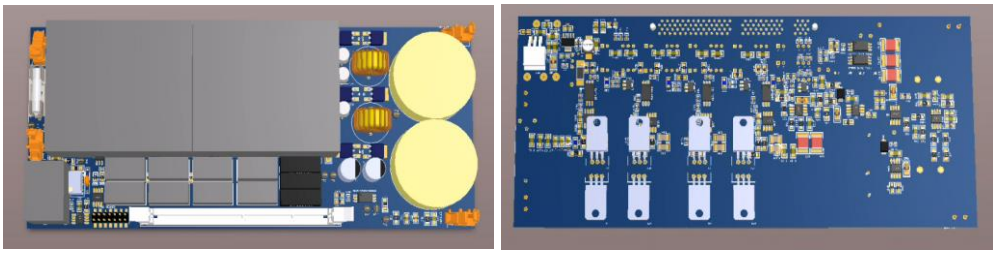

Figure 3.19. 2kW inverter prototype of the proposed method

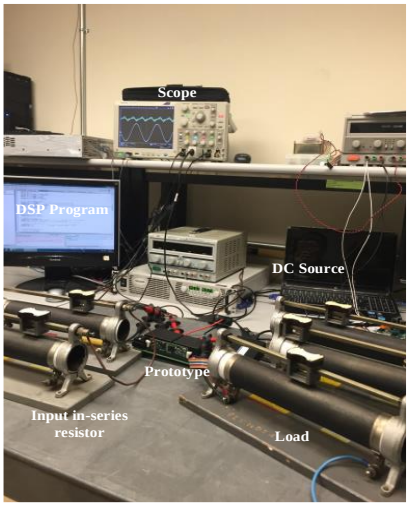

Figure 3.20. Overview of the test bench

The efficiency of the proposed method and in-series method [46] with SiC based inverter are estimated and calculated under the same condition and shown in Fig.3.25. The figure shows that the efficiency for the proposed method is decreased a little compared with that in-series method [18] since the power decoupling circuit consumes some power for extra one-phase leg

device and inductor. Fig.3.26 shows the comparison of the estimated and experimental results. There is very little difference, less than 0.5%, between estimated and experimental results, as there are some auxiliary circuits' and parameter's power consume not considered for estimation. As a result, there is a trade-off between the power density and efficiency of the system. However, with the proposed method, the efficiency is still higher than 95% and less than 0.7% lower than in-series method [46] at the full power rating.

In summary, compared with in-parallel method [40] and in-series method [46], the proposed method has lower voltage rating component than those in-parallel method. However, its device number is the largest, 2 more compared with that in-series method. The power loss is high as it takes in-series method for the main circuit, so the current going through the device should be higher than that in-parallel method. SiC device have low power loss compared with Si, so the efficiency of the proposed method can achieve more than 95%. The lifetime is best because for the decoupling circuit, it takes extra small inductor to store the energy from the decoupling capacitor. As a result, the decoupling capacitor value is much smaller than that in-series method.

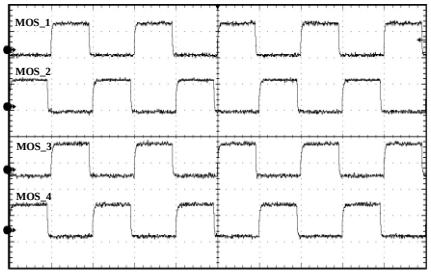

Figure 3.21. SiC MOSFET Gate drive waveform under 100 kHz (20V/div), time scale: 5us/div

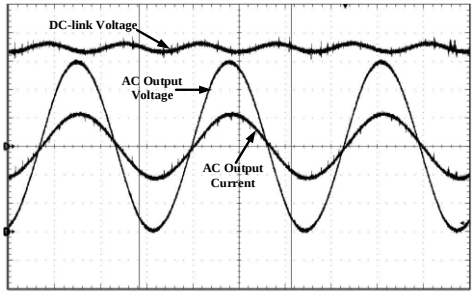

Figure 3.22. DC-link voltage (60V/div) and output AC voltage (120V/div) and current (10A/div) without power decoupling method, time scale: 5ms/div

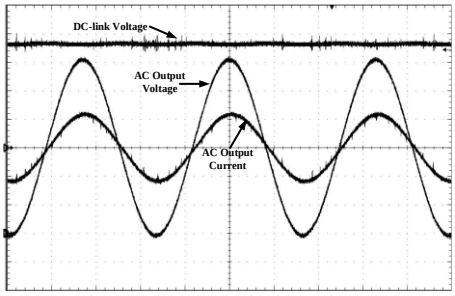

Figure 3.23. DC-link voltage (60V/div) and output AC voltage (120V/div) and current (10A/div) with power decoupling method, time scale: 5ms/div

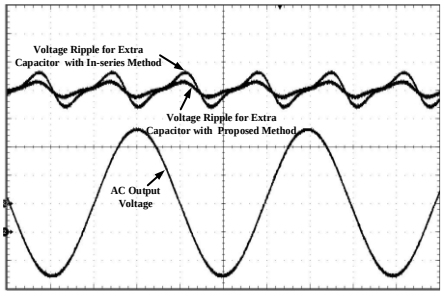

Figure 3.24. Comparison of extra capacitor voltage (20V/div) and AC output voltage (140V/div), time scale: 4ms/div

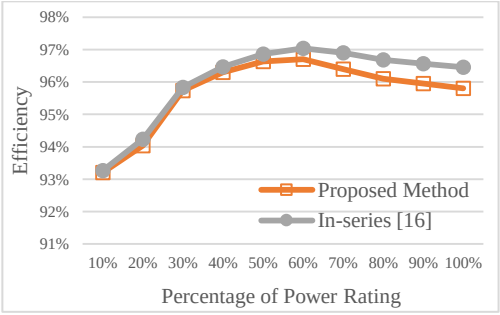

Figure 3.25. 2kW estimated efficiency for proposed method and in-series method

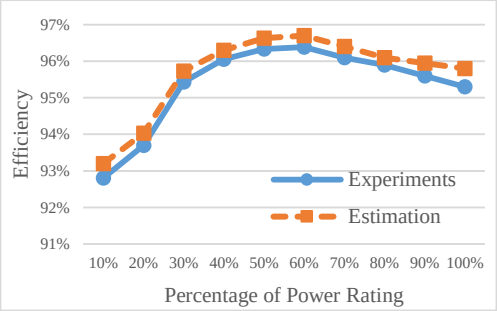

Figure 3.26. Comparison of estimated and experimental efficiency for the proposed method

3.8. Conclusion

This chapter presents an in–series and in–parallel combination power decoupling method for the single-phase inverter. With basic power equation derivation, the proposed method is analyzed and compared with other methods in theory. Based on the theoretical analysis, the proposed method can reduce the DC-link capacitance and the extra circuit's capacitance significantly when compared to the traditional SiC based inverter.

Then, the operating principles and control strategy are introduced. PI control is used for the power decoupling circuit to ensure good steady-state and dynamic-state performances for the whole system. And the output filter is designed as LC filter. The circuit parameters are designed in details and power losses are evaluated for the circuit. Conduction and switching losses for diodes and SiC MOSFET devices are analyzed at different switching frequency. The switching loss of SiC MOSFET device dominates the total power loss and is increased with an increasing switching frequency. On the other hand, higher frequency will benefit the output filter reduction. Therefore, a trade-off between the power density and efficiency should be considered.

To verify the theoretical analysis, a PLECS simulation model is built. The input is a DC voltage source of 450V with a 10Ω resistor in series and the output voltage is 240V. Based on the simulation results, both the proposed method in this paper and the in-series method can achieve a 89% reduction of the DC-link capacitance when compared to the traditional SiC based inverter.

Furthermore, the proposed method is superior to the in-series method with a more than 68% reduction of the extra circuit's capacitance.

A 2kW prototype with a size of 7.25×3.6×1.4 $inch^3$ is developed. It has a power density of about 55W/$inch^3$. When compared to the in-series method, the extra capacitance can be reduced about 64% for the proposed power decoupling method. The experimental results are consistent with the simulation results. The efficiency for the proposed method is higher than 95%.

4. INSTANTANEOUS PULSE POWER COMPENSATOR FOR HIGH-POWER-DENSITY SINGLE-PHASE INVERTER

4.1. Introduction

This chapter presents an instantaneous pulse power compensator (IPPC) concept to achieve ultra-high density power conversion with zero voltage ripple and zero dc-link capacitor. Only high frequency ceramic capacitor is needed on the dc-link to minimize the voltage overshoot during the device turn-off. A single-phase inverter example has been studied using the proposed concept. Compared with the traditional 2nd order power decoupling method with limited dc-link capacitor reduction capability, the proposed IPPC concept could compensate all the order power harmonics on the dc-link thus leading to zero capacitor design. A 2kW Silicon Carbide (SiC) based single-phase inverter and an IPPC have been built. Experimental results have been provided to verify the proposed idea. The proposed IPPC application to achieve zero capacitor design for three-phase inverter and other converters are also discussed. High frequency features of wide band-gap devices could be fully utilized by using the proposed IPPC concept for future high density power conversion.

To verify the theoretical analysis, a PLECS simulation model is built. The input is a DC voltage source of 450V with a 10Ω resistor in series and the output voltage is 240V. Based on the simulation results, both the proposed method in this paper and the in-series method can achieve a 89% reduction of the DC-link capacitance when compared to the traditional SiC based inverter. Furthermore, the proposed method is superior to the in-series method with a more than 68% reduction of the extra circuit's capacitance.

Single-phase inverter is widely used in many applications, such as uninterruptible power supply (UPS), photovoltaics (PV), vehicle to grid (V2G) technology and solid-state transformer

(SST) [59]-[60]. SiC [61]-[62] devices can be applied to increase the system switching frequency to achieve high-power-density and high efficiency. However, there is still a large electrolytic capacitor needed on the dc-link side for single-phase inverters to absorb the pulsating power at twice the fundamental frequency. This large electrolytic capacitor not only makes the system lifetime short but also contributes to a large volume.

In order to reduce large-size dc-link capacitors, many power decoupling methods have already been proposed [63]-[65]. [66]-[67] dealed with control methods from system level to reduce dc-link capacitor. Except special control methods, active power decoupling methods for single-phase inverters are widely used. They can be briefly classified into dc-side methods and ac-side methods. The dc-side methods contain in-parallel and in-series structures. [68]-[70] show dc-side in-parallel decoupling structure. They introduce buck/boost circuit to store the ripple power to reduce dc-link capacitance. Another inverter circuit in-parallel is introduced in [71]. 45 degree is shifted to balance the bus line instantaneous power. This method offers advantage of small value for the extra capacitor, but its power switching device suffers high voltage stress. A novel in-series method is proposed in [72]. The extra devices for power decoupling circuit have lower voltage stress than those paralleled structures. However, the value of its extra capacitor is still too large, because of its low voltage stress. Electrolytic capacitors are normally used in this method. [73] proposed an in-series and in-parallel combination method based on in-series structure to further reduce extra capacitance with a small-size inductor. The efficiency of this method is lower because of high in-series current and extra inductor. [74] also show structure in-parallel on the dc-side. Unlike [72] voltage compensation, it generates 2^{nd} current ripple to reduce dc-link capacitance. The ac-side method includes three-leg method and six-switch method. The principle of this kind of methods is to transfer the ripple power to the third-port on the ac-side. As the third-port is drawn

into single-phase circuits, three-phase control methods can be used in this application. [75]-[77] introduced three-leg methods. Based on basic power equations, control scheme can be easily got. Papers [78]-[80] show six-switch method or variable-capacitor method. The space-vector control is often taken in this application. The control of ac-side method is usually flexible. However, the value of extra capacitor or inductor in ac-side third-port method is not obviously reduced compared with those methods in dc-side. [81] proposed a symmetrical half-bridge method, which introduced another port with capacitors reused for half-bridge topology. Furthermore, paper [82] proposed a novel control method to share one inverter leg and one inductor to transfer the second instantaneous power to ac side. It can achieve low cost compared with other ac-side methods, however, under the same condition, the extra capacitance is still large. Besides, [83] proposed an interleaved power decoupling method with combinational six-switch and coupled inductor. The control of this method is complex and coupled inductor size is still large.

In general, from a comprehensive understanding for all these power decoupling methods, traditional active power decoupling methods only consider pulsating power at twice the fundamental frequency. 2^{nd} order reactive power is transferred from dc-link capacitors to other extra inductors and capacitors via different topologies and controls. This is mainly because 2nd order harmonic is the dominated component and its theoretical analysis is easy to achieve. Therefore, most of papers proposed another port, namely, third port on dc-side or ac-side to absorb 2^{nd} reactive power. However, few papers investigated other higher harmonics effect on the dc-link capacitor and how they affect the dc-link voltage ripple. Actually, papers [84]-[85] already explain dc-link current spectrum in theory. Besides 2^{nd} harmonic, there are still lots of higher-order harmonic components in the dc-link line. State-of-the-art power decoupling methods for single-phase inverter concern 2^{nd} order without other harmonics consideration, mainly because pulse

frequency is high and decoupling circuit efficiency is low with traditional silicon device. However, wide bandgap devices are suitable for this special high-frequency and high-efficiency pulse application. As a result, unlike traditional topology improvement with 2nd harmonic power decoupling method, instantaneous pulse power compensator (IPPC) concept proposed in this paper can lead to new power decoupling methods with various novel pulse topologies and controls.

4.2. Traditional 2nd order Method and Their Issues

For single-phase inverter system, the output AC voltage and current are given by (Eq. 4.1) and (Eq. 4.2)

$$v_{ac}(t) = V \sin \omega t \tag{Eq. 4.1}$$

$$i_{ac}(t) = I \sin(\omega t + \varphi) \tag{Eq. 4.2}$$

where V and I are magnitudes of the load voltage and the current supplied by the single phase inverter, ω is the angular frequency of the ac system, φ is the power factor angle.

Then the instantaneous power flow is derived by (Eq. 4.3)

$$P_{ac}(t) = P_{dc} - P_{ac} = \frac{V \times I}{2} \cos \varphi - \frac{V \times I}{2} \cos(2\omega t + \varphi) \tag{Eq. 4.3}$$

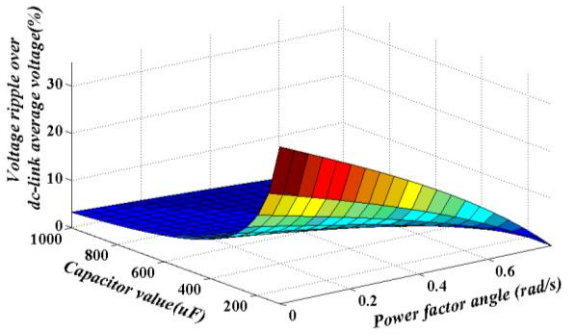

Figure 4.1. 3D plot for voltage ripple with capacitance and PF

The dc-link capacitance is normally evaluated as (Eq. 4.4). The 3-D plot for voltage ripple's relationship with capacitance and power factor is presented in Fig.4.1.

$$\Delta V_{dc} = \frac{P_{dc}}{\omega V_{dc} C_{dc}} * \frac{\sin(\frac{\pi}{2}+\varphi) - \sin\varphi}{\cos\varphi} \quad \text{(Eq. 4.4)}$$

where P_{dc} is power rating of the system, V_{dc} is the dc-link voltage and ΔV_{dc} is the ripple of dc-link voltage.

$$E_{store} = \frac{P_{dc}}{2\pi f_{line}} \quad \text{(Eq. 4.5)}$$

Fig.4.2 shows the basic schematic of single-phase inverter and key waveforms for traditional 2nd order harmonic analysis and one typical 2nd decoupling method [41]. At the output side, the blue line stands for dc-side average power and red line represents the instantaneous power, assuming that the power factor is unity. Except the dc-average power, the dc-link capacitor function is to store and release the AC power to make power balance. (Eq. 4.5) shows the relationship between the DC power and the stored energy. So for traditional power decoupling method, capacitance is calculated by (Eq. 4.4) and stored energy is evaluated by (Eq. 4.5).

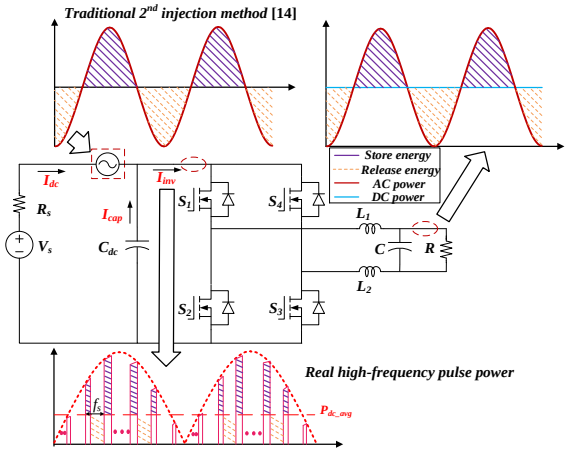

Figure 4.2. Waveforms for 2nd order injection method and real pulse power

As shown in Fig.4.2, traditional power decoupling method [80] deals with 2nd order power. Actually, at dc-side near inverter line, the power is high-frequency pulse power and the current I_{inv} is pulse current. The relationship between dc-link voltage ripple and dc-link capacitance is further

investigated when dc-link capacitance varies. Fig.4.3 shows comparison among traditional calculation in theory with (Eq. 4.4), simulation results and pulse power analysis introduced in the next part. From Fig.4.3, it shows that when dc-link capacitance becomes small, traditional dc-link voltage ripple is quite different from the real case. The comparison shows that (Eq. 4.4) is just a quick evaluation for large-size dc-link capacitor selection without any power decoupling consideration. However, power decoupling application usually takes small dc-link capacitance. As a result, traditional 2nd order theoretical method is not accurate and not suitable for small-capacitance power decoupling evaluation.

The schematic of simulation curve is shown in Fig.4.2 without any decoupling method. An in-series resistor is connected with DC source in order to amplify the voltage ripple on the dc-link line. The DC source is assumed just to pump out current and the current cannot inject back into the DC source. The simulation without any power decoupling method is conducted with the parameters shown in Table.4.1 Closed-loop control is taken to guarantee the output voltage is 240V and power rating is 2kW. The ordinate value is the ratio, which is defined as voltage ripple over dc-link average voltage. Fig.4.4 shows the detailed voltage ripple waveforms with PLECS under 1000uF, 100uF and 10uF, respectively. The voltage ratio is matched with Fig.4.3.

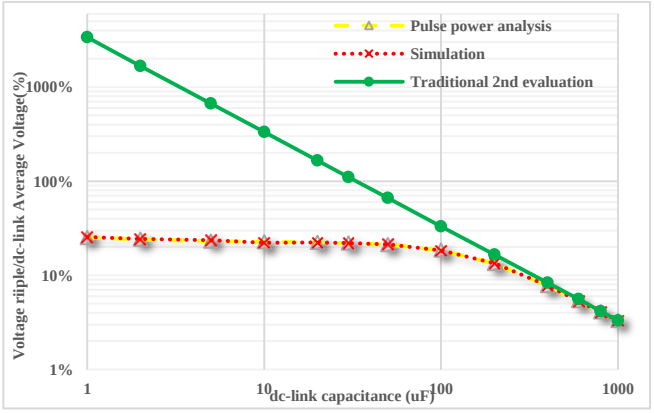

Figure 4.3. Comparison of traditional theoretical calculation, IPPC theoretical calculation and simulation (log scale)

In conclusion, for power decoupling method with small-size dc-link capacitor, traditional dc-link voltage ripple equations have little consideration in details.

4.3. Theoretical Analysis

Traditional 2nd order harmonic method only considers the current is continuous with a low-pass filter, which is applied for ac output. It is true, but not accurate for dc-link voltage ripple evaluation. This is because in the real case, dc-link current near inverter side is the pulse current. The dc-link capacitor ideally deals with pulse current and pulse power shown in Fig.4.5. Pulse power analysis shown in this part removes that virtual low-pass filter and directly deals with the pulse waveform. The pulse current with double Fourier analysis [85] contains many other high-frequency harmonics. Traditional theoretical method without considering these components will prevent further reduce of the dc-link capacitance. That's why paper [72] with traditional 2nd power decoupling method still needs ~120uF extra dc-link capacitor there. The function of dc-link capacitor in the 2nd decoupling methods is to filter the high-frequency components. These high-frequency components actually will have effect on dc-link voltage ripple when the dc-link capacitance becomes small.

Fig.4.4 shows the key waveforms for pulse power analysis. The current on the dc-link side near switches is pulse current and dc-link voltage is 2nd harmonic plus average voltage. Here, it is assumed that the load is resistive load, modulation control is sinusoidal pulse-width modulation (SPWM) with device conduction loss and filter parasitic resistor ignored. The purple line is pulse current and red line is pulse power. The ideal equations to describe pulse current are shown in (Eq. 4.6) to (Eq. 4.9)

$$i_{inv}(t)=\begin{cases}\left|i_o \sin(\omega t+\varphi)\bullet s(t)\right|,(0+k\pi,\varphi+k\pi)\\ -\left|i_o \sin(\omega t+\varphi)\bullet s(t)\right|,(\varphi+k\pi,\pi+k\pi)\end{cases} \quad \text{(Eq. 4.6)}$$

Table 4.1. Key parameters in the single-phase inverter circuit

Symbol	DESCRIPTION	Value
V_{in}	input voltage	450V
R_s	in-series resistor	10 Ω
P_o	power rating	2kW
V_o	output voltage	240V
f_o	fundamental frequency	60Hz
f_s	switching frequency	100kHz
C_{bus}	dc-link capacitor	100uF
L_n	output filter inductor	230uH
C	output filter capacitor	550nF
R	resistor load	28.8 Ω

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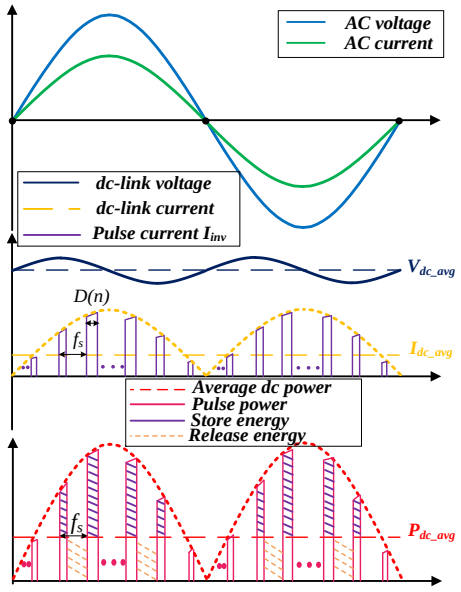


Figure 4.4. Key waveforms for pulse current analysis

k=0,1,2…; φ is the power factor angle. The switching function *s(t)* and every duty cycle *D(n)* is defined as follows,

$$s(t)=\begin{cases}0,(0+kT_S,\frac{T_S-D(n)}{2}+kT_S)\,||\,(\frac{T_S+D(n)}{2}+kT_S,T_S+kT_S)\\1,(\frac{T_S-D(n)}{2}+kT_S,\frac{T_S+D(n)}{2}+kT_S)\end{cases} \quad \text{(Eq. 4.7)}$$

$$D(n)=\left|\frac{\sqrt{2}V_O\sin(\frac{2\pi n}{N})*T_S}{V_{dc}}\right|;n=1...N \quad \text{(Eq. 4.8)}$$

$$N=\frac{f_S}{f_O} \quad \text{(Eq. 4.9)}$$

Where I_{inv} is inverter dc-side current defined in Fig.4.2. *N* means the number of ideal pulse, which is related with output fundamental frequency f_o and switching frequency f_s; i_o is sinusoid output current. T_s is switching period and *D(n)* is the turn-on time of each pulse current, which can be calculated with (Eq. 4.7). It can be derived based on triangle relationship assuming that sinusoid value during this short time is linearly constant ignoring high-frequency ripple.

$$i_{dc}=i_c+i_{inv} \quad \text{(Eq. 4.10)}$$

$$i_{dc}(t)=\frac{V_s-V_{dc}(t)}{Z_{in}} \quad \text{(Eq. 4.11)}$$

$$V_{dc}(t)=\int\frac{i_c}{C_{dc}}dt \quad \text{(Eq. 4.12)}$$

$$\Delta V_{dc}=V_{dc\max}-V_{dc\min} \quad \text{(Eq. 4.13)}$$

Equations (Eq. 4.10) to (Eq. 4.13) are some basic equations to get dc-link voltage ripple. Based on (Eq. 4.5) to (Eq. 4.13), the time domain dc-link voltage can be calculated. It can be seen that dc-link voltage ripple is related with inverter input current i_{inv} according to (Eq. 4.13) and Z_{in}, which is the input impedance, here it is equal to *Rs* (10Ω) followed by Google Little Box's parameters. Fig.4.3 shows dc-link voltage ripple evaluation with both traditional 2nd order analysis

(Eq. 4.4) and pulse power analysis as well as PLECS simulations under the same condition. The results verify that pulse power analysis are more consistent with simulation results and more accurate than traditional method, especially under small dc-link capacitance for power decoupling applications.

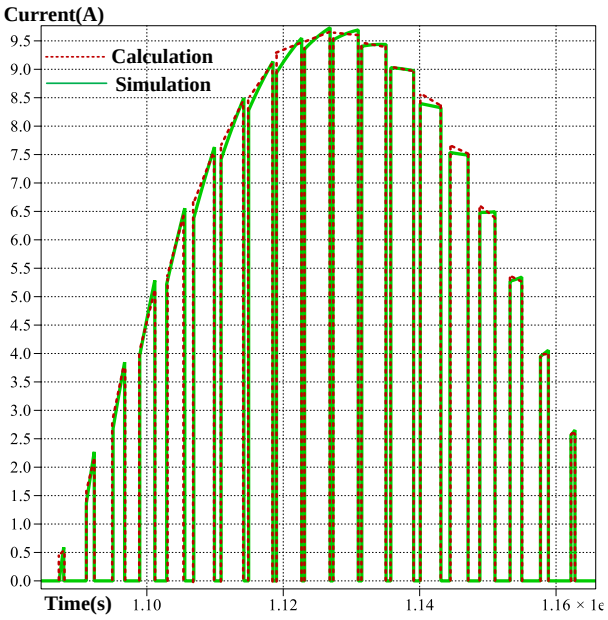


Figure 4.5. Comparison for calculation with equations and simulation results

Fig.4.5 shows comparison for pulse power analysis by (Eq. 4.5) - (Eq. 4.13) and simulation results with PLECS assuming that power factor is unity. Pulse current data can be got with Matlab code. The algorithm is written based on (Eq. 4.5) - (Eq. 4.13). The green line stands for simulation results for dc-link pulse current I_{inv} and red line presents pulse power analysis. The switching frequency here is set as 1.2 kHz for a clear comparison each pulse waveform. The other key parameters are set the same as Table.4.1. The calculation is almost matched with simulation results without high-frequency ripple consideration.

Since the real case is the pulse current waveform, which contains higher order harmonic components, pulse power analysis considers more details when compared to the traditional 2nd

order method. This is very necessary to be considered in the power decoupling method for these high-order harmonic components. Because these high-order components in the pulse waveform can cause large voltage ripple, especially, when dc-link capacitance becomes small. The dc-link capacitor at least needs to provide enough energy for one switching cycle. As a result, whatever 2nd order power decoupling method is taken, they usually need one large capacitor to support one cycle energy.

The inverter-side pulse power equation is shown as follow. The dc-link capacitor pulse power is equal to this power minus dc input power, ignoring the power on the input resistor.

$$P_{inv} = V_{dc}(t) \times i_{inv}(t) \qquad \text{(Eq. 4.14)}$$

The detailed shape of the instantaneous pulse power is shown in Fig.4.6. In conclusion, pulse power analysis can reflect how inverter input pulse current affects dc-link voltage ripple. It has a full consideration of the switching frequency, input impendence and high-order components' effect compared with traditional 2nd order theoretical analysis.

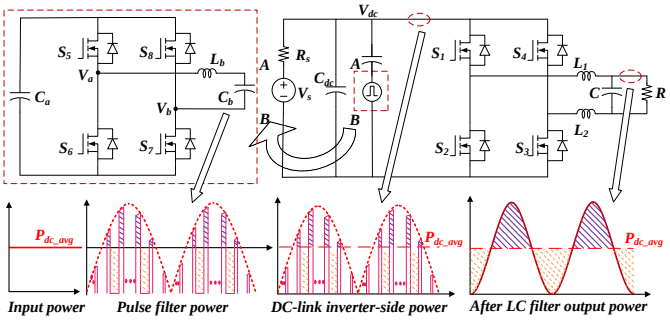


Figure 4. 6. One typical IPPC method with full-bridge topology

4.4. IPPC Control Method

As analyzed above, dc-side instantaneous power actually is the pulse power. Therefore, an instantaneous pulse power compensator (IPPC) concept is proposed in this paper. Unlike low frequency power compensator, IPPC considers directly high-frequency pulse power with pulse

compensation. This concept can be applied in many high density power conversions, which will be further discussed in the last part.

For single-phase inverter power decoupling application, if pulse current can be generated followed by i_{inv} minus dc input average current, there is no need for dc-link capacitors at all, which can achieve dc-link zero-capacitance in theory.

The decoupling circuit can be any circuit, which can achieve pulse function. One typical IPPC method is proposed with full-bridge as shown in Fig.4.6. The current injection function part AB is to inject pulse current directly following the inverter current I_{inv}. Traditional 2nd order decoupling method and IPPC decoupling method for single-phase inverter are both analyzed and simulated to make a comparison. Furthermore, in practical, in-series 2nd method [83] and full-bridge decoupling circuit with IPPC method shown in Fig.4.7 are compared. Fig.4.9 shows detailed comparison waveforms of traditional 2nd order power decoupling method and IPPC decoupling method. The comparison is under a capacitance of 100uF without decoupling method and 100uF, 10uF, 1uF with decoupling method, respectively. At first, there is no decoupling method. The voltage ripple is 76.5V and average dc-link voltage is 413.5V. The percentage of ripple over average value is equal to 18.5% under dc capacitance 100uF, which is matched with Fig.4.3.

Under the same condition, with traditional 2nd order method [80], the ripple is decreased to 14V. The advanced pulse injection method can reduce it to 3V under dc-link capacitance of 100uF. Ideally, both methods can reduce the ripple to 0V shown in green straight line when capacitance is 100uF. When the capacitance is changed from 100uF to 10uF, 10 times smaller, the traditional method decreases voltage ripple to 34.2V and IPPC injection method can achieve 6.2V. The simulation actually still has some 2nd order component, because dc bias is hard to totally be

cancelled out. Ideally, at dc-link capacitance 10uF, the ripple is only 12V without any 2nd order component. When dc-link capacitance is further reduced to 1uF, 2nd order method cannot work. This is mainly because when the capacitance is reduced, the dc-side works from continuous mode to discontinuous mode, which will be further introduced in next part. The energy in the dc-link capacitor cannot support the energy during one switching cycle. In this condition, traditional 2nd order power decoupling method is limited. On the other hand, IPPC injection method can be still applied. The voltage ripple can still achieve 3% under extreme-small capacitance of 1uF.

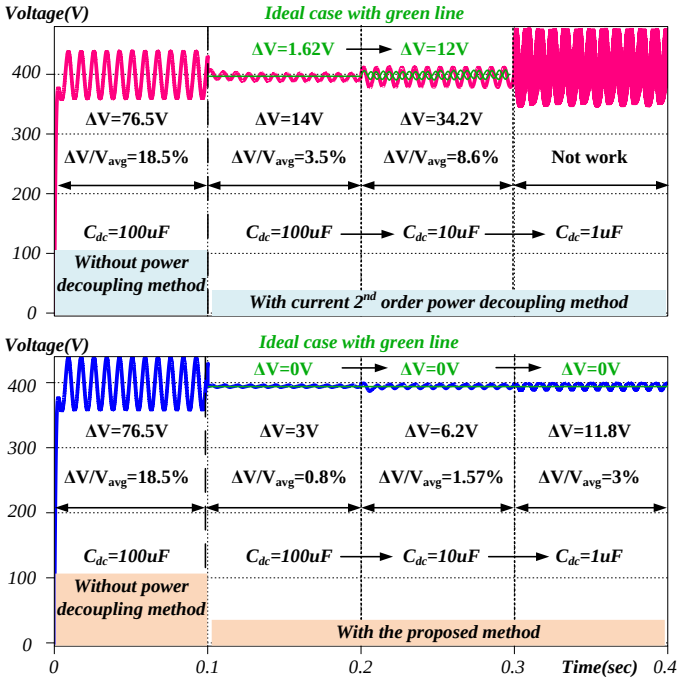


Figure 4.7. Comparison of traditional 2nd order method [84] (pink line) and proposed method (blue line) under dc-link capacitance 100uF, 10uF and 1uF, respectively.

Ideally, the ripple should be zero with IPPC method at the whole range, the practical control contains some high-frequency ripple there. IPPC can achieve theoretical zero dc-link capacitance. As in the practical design, some ceramic capacitors are usually taken to avoid some turn-off shoot of devices. So the capacitance here is only decreased to 1uF, which is already quite small.

With (Eq. 4.5) - (Eq. 4.13), ideal case with 2nd order injection and IPPC injection methods can be conducted with Matlab code. Fig.4.8 shows the flowchart of the algorithm.

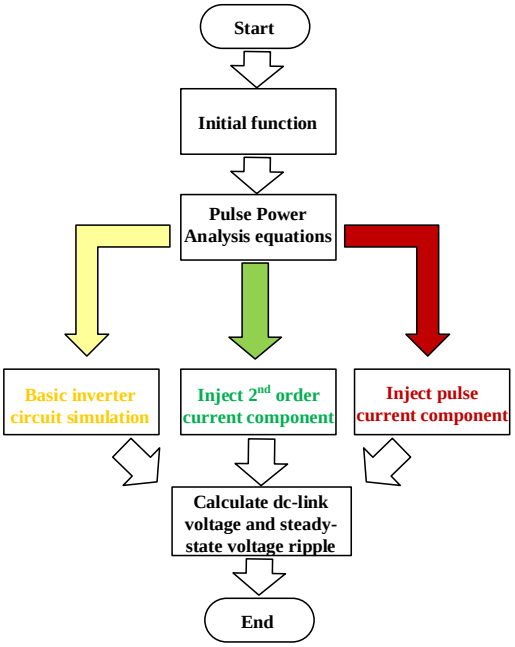


Figure 4.8. DC-link voltage ripple calculation flowchart with MATLAB C language

Fig.4.9 shows limit curves for pulse power analysis without any power decoupling (yellow line), with theoretical 2nd order traditional method (green line) and with theoretical IPPC injection method (red line). The y axis stands for dc-link voltage ripple over dc-link average voltage and the x axis stands for different values of dc-link capacitors. The main parameters are followed in Table.1. As the equivalent series resistance (ESR) is considered here, dc-link capacitor is assumed polypropylene (PP) film capacitor with dc voltage 600V from Kemet. 1uF with ESR 7.7mΩ is assumed. The dissipation factor (DF), which reflects the relationship between ESR and capacitance is defined as follow,

$$DF = ESR / X_C \qquad \text{(Eq. 4.15)}$$

X_C is the impendence of dc-link capacitor at twice fundamental frequency. DF value can be checked with datasheet from manufactory. Based on Vishay mkp1848 datasheet, 1uF to 15uF

capacitors have $85*10^{-4}$ dissipation factor @10k Hz. 20uF to 40uF have $140*10^{-4}$. 40uF to 100uF have $280*10^{-4}$.

The area between the curve without power decoupling method (yellow line) and with 2nd order traditional method (green line) reflects the voltage ripple reduction, which can be only achieved by 2nd order method. The area between 2nd method (green line) and IPPC injection method (red line) can show that the other higher order harmonics, except 2nd order component, totally contribute to voltage ripple. And with IPPC injection method, ideally it can achieve zero voltage ripple in theory no matter how dc-link capacitance is reduced.

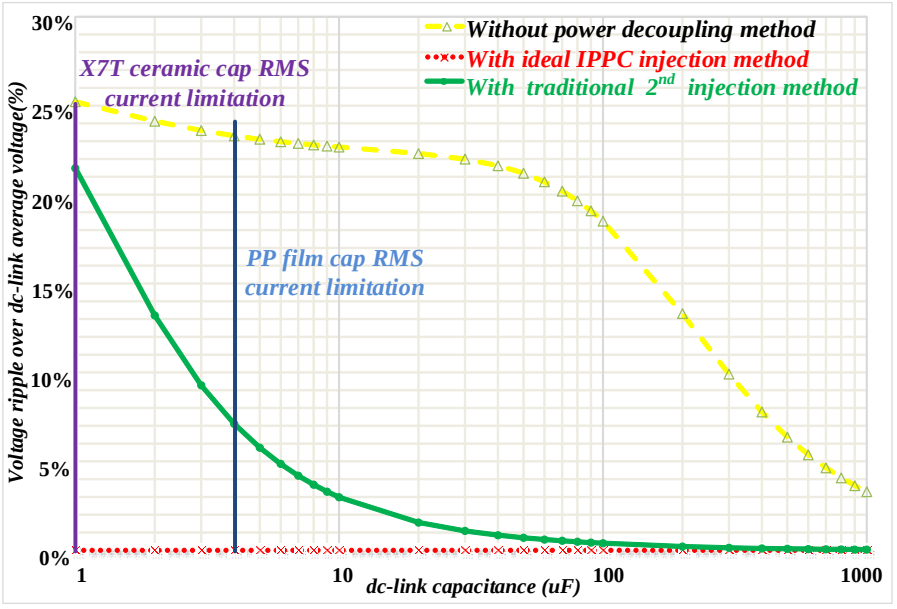


Figure 4.9. Power decoupling limit curves of traditional 2nd injection method, IPPC injection method

By considering rms current limitation, both typical film capacitors and ceramic capacitors are investigated. The film capacitors are taken Vishay dc-link metallized polypropylene (PP) film capacitor. The ceramic capacitors are taken Murata X7T ceramic capacitors. The rms current for dc-link capacitor is ~4.17A. Based on the information from the website, the film capacitance is limited at 5uF with ~5A rms current. For ceramic capacitors, they can be extended to 1uF.

4.5. Case Study with IPPC Concept and Simulation Results

As theoretically analyzed above, IPPC concept is verified with one typical full-bridge topology for particular case study in this section. In fact, the decoupling topology can be any bi-directional decoupling circuits, which can achieve pulse injection control function. Unlike low-frequency 2nd order power decoupling control method, this paper directly considers high-frequency pulsating power with pulse compensation. As a result, the power density can be further improved, however, power loss will also be increased. Both advantages and disadvantages of IPPC are introduced in this section.

Fig.4.10 shows the schematic and control scheme of one typical IPPC case study for high-density single-phase inverter. As the injected current is not twice-line-frequency sinusoidal, the control scheme is totally different here. With decoupling function, the input current is constant. The current i_{inv} shown in Fig.4.10 actually is a sequence of pulse current. Traditional 2nd decoupling control methods normally add a low-pass filter for dc inverter-side current i_{inv} in order to get twice-line-frequency sinusoidal reference. In contrast, pulse injection control with IPPC concept removes that virtual low-pass filter and directly compensate pulse components in this application.

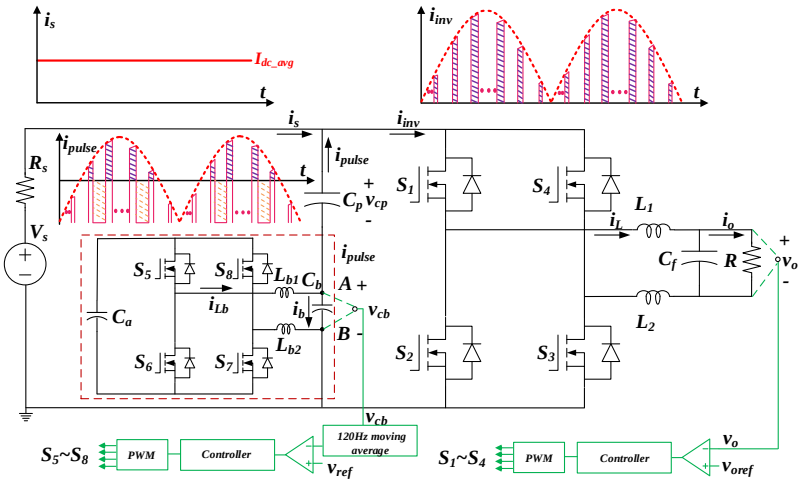


Figure 4.10. Continuous mode and discontinuous mode current waveforms

Actually, it is not easy to fully track high-frequency pulse current directly. The special solution here is to control the capacitor C_b voltage and make capacitor C_p indirectly inject pulse current without dc bias. The capacitor C_p and capacitor C_b have the opposite voltage ripple in order to cancel voltage ripple each other. The voltage on the capacitor C_b can be easily controlled. As a result, if the voltage ripple on the capacitor C_b contains the pulse information. The capacitor C_p can generate high-frequency pulse current instead. The voltage reference on C_b can be got as follow;

$$v_{ref}(n) = v_{ref}(n-1) + \int \frac{1}{C_b} i_{pulse}(n)dt \qquad \text{(Eq. 4.16)}$$

where $V_{ref}(n)$ stands for each cycle voltage reference.

The control voltage references for twice-line-frequency (2^{nd} order) control and IPPC are compared and shown in Fig.4.11. As it is shown, the IPPC reference contains high-frequency pulse information.

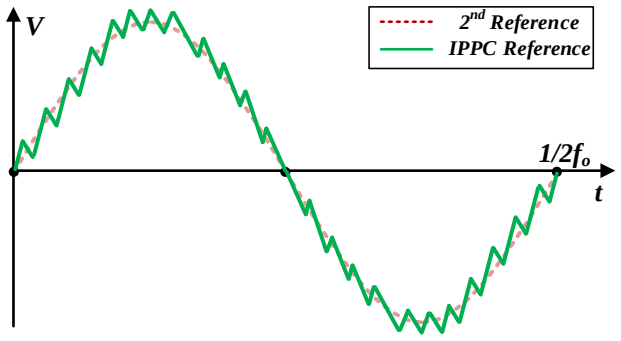


Figure 4.11. Comparison on control reference between traditional 2^{nd} order and IPPC method

Fig.4.12 shows the basic control block for the main inverter circuit (a) and decoupling circuit (b), respectively. There is no resistive load in the decoupling circuit when compared with the main inverter control. Instead, the forward pulse current i_{pulse} can be easily got by equation (Eq. 4.16) and the pulse theoretical equations. The voltage reference can be got by (Eq. 4.16). Finally, the voltage of C_b can be controlled.

$$i_{pulse}(n) = i_{inv}(n) - i_s \quad \text{(Eq. 4.17)}$$

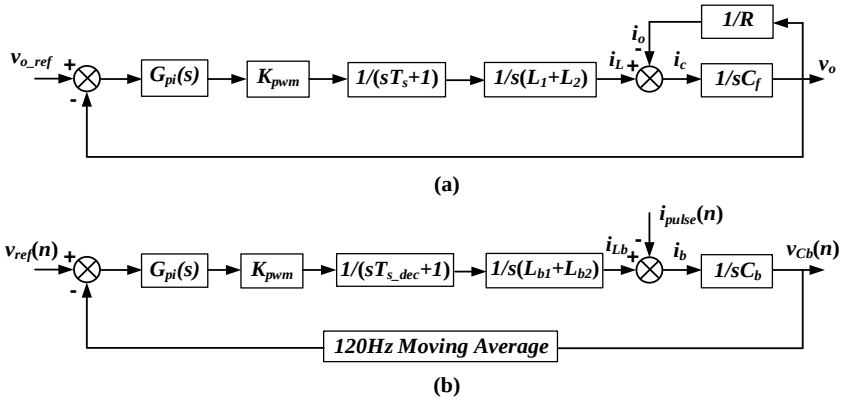


Figure 4.12. (a) Inverter main circuit control system block (b) decoupling full-bridge circuit control system block

Where T_s and T_{s_dec} stand for sampling frequency for main circuit and decoupling circuit, respectively. $G_{pi}(s)$ is the PI controller. Other parameters are all marked in the Fig.4.10. Actually, the capacitor V_{cb} has dc bias in the real case, so it needs to remove 120Hz average voltage for the control scheme. Unlike 2nd component compensation, the decoupling capacitor C_a is evaluated by the pulse power instead of continuous 2nd order power shown in (Eq. 4.17).

$$E_a = C_a V_{avg} \Delta V_a \quad \text{(Eq. 4.18)}$$

where V_{avg} stands for the dc bias voltage across the capacitor C_a. ΔV_a represents the voltage ripple C_a. V_{dc} is the dc-link voltage. E_a is the store energy in the capacitor C_a. It can be got in (Eq. 4.18).

For the decoupling filter value, it can be similar got as the traditional inverter filter design. The inductor design is based on the current ripple.

$$f_c = \frac{1}{2\pi\sqrt{L_b C_b}} \quad \text{(Eq. 4.19)}$$

Where f_c is the cut-off frequency. For each pulse duty cycle, electric charge quantity of the capacitor C_p has to be sufficient to support the pulse current. So C_p can be expressed as follow;

$$C_p \geq \frac{i_{pulse} dt}{dv_{cp}} \qquad \text{(Eq. 4.20)}$$

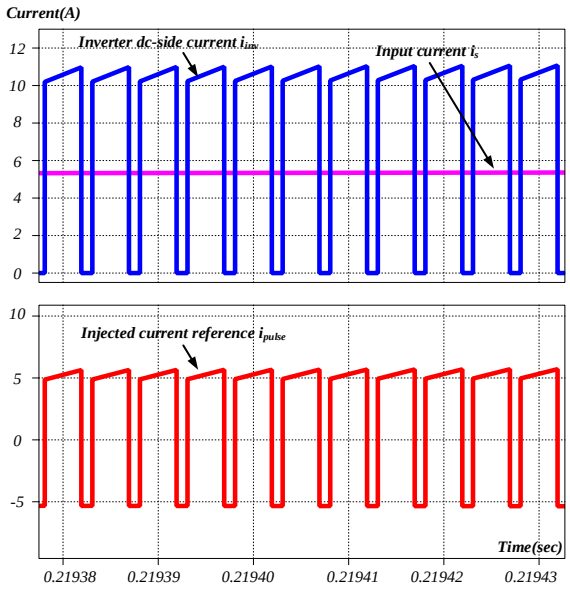


Figure 4.13. Inverter-side, dc input and injected current

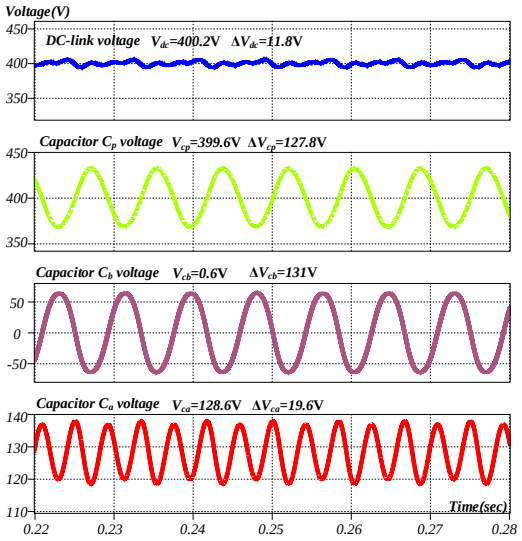


Figure 4.14. Key waveforms for decoupling circuit and dc-link voltage

Simulation with PLECS is conducted to verify the IPPC control method. The parameters are followed in Table.4.1. Fig.4.13 presents the key waveforms of inverter-side current i_{inv}, dc input current is and injected current i_{pulse}, respectively. The capacitor C_p and C_b have the opposite

ripple to cancel each other. The decoupling capacitor Ca has average voltage 128.6V with ripple 19.6V shown in Fig.4.14.

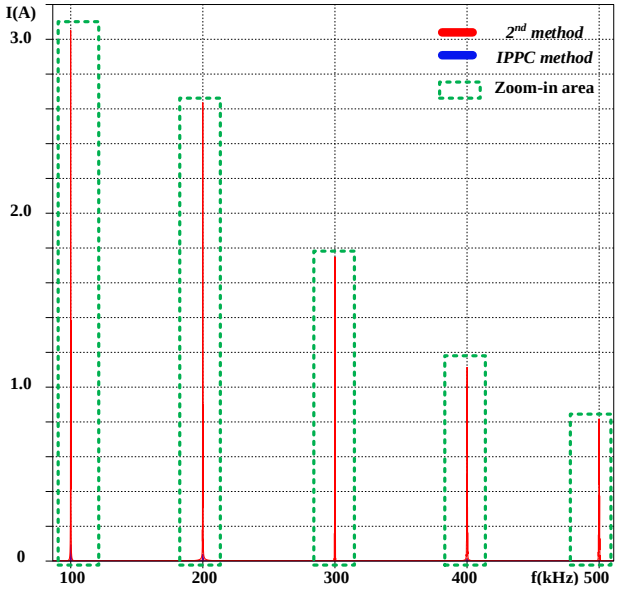


Figure 4.15. Double Fourier Spectrum for dc input current

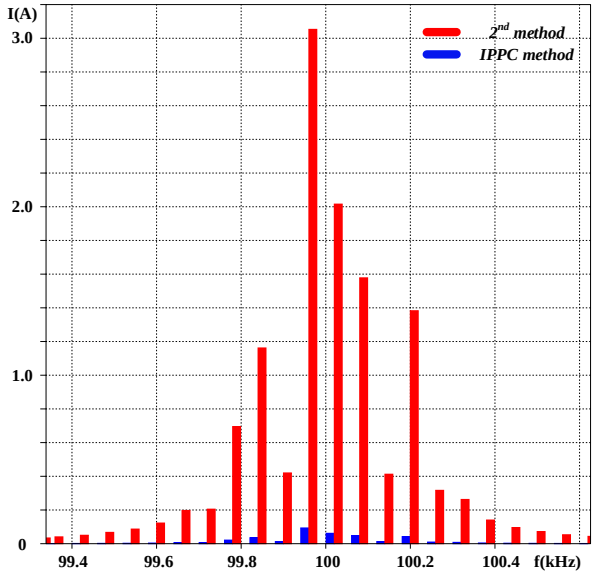


Figure 4.16. Zoom-in with side-band components at 100kHz

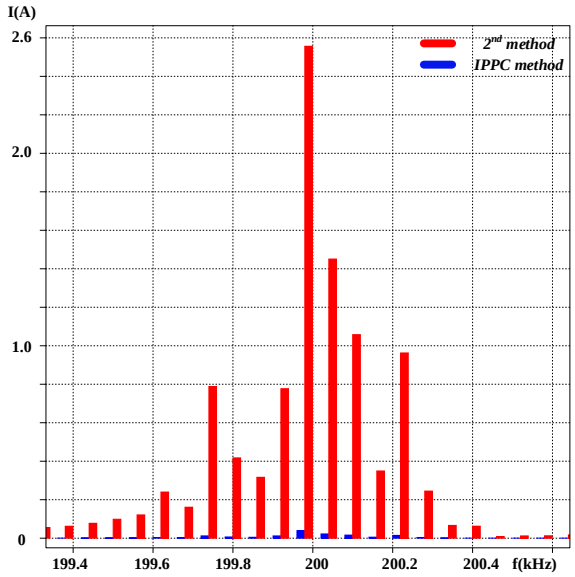


Figure 4.17. Zoom-in with side-band components at 200kHz

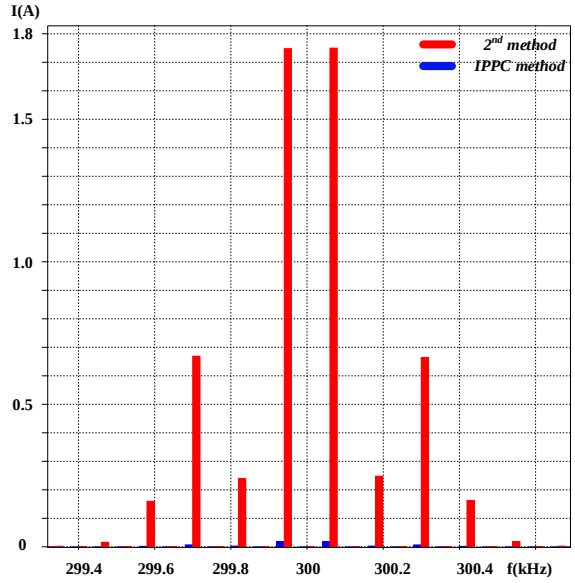


Figure 4.18. Zoom-in with side-band components at 300kHz

Furthermore, the spectrum for dc input current are compared when only 2nd order component is injected and pulse current is injected with IPPC method, respectively. Double Fourier analysis is conducted and compared in Fig.4.15. Besides low-frequency components, the dc input current still has N times switching frequency components and their side-band components based on double Fourier analysis. IPPC control method can not only cancel the low frequency 2nd

order component, similar with traditional 2nd order method, but also compensate those high-frequency components. Fig.4.16 shows at ~100 kHz switching frequency the magnitude with IPPC method are quite low, however, the magnitude with 2nd method are higher. On the other points, such as ~200 kHz shown in Fig.4.17, ~300kHz shown in Fig.4.18 and so on, still IPPC method has lower magnitude when compared with 2nd order method. The detailed influence on dc-link voltage ripple by these high-frequency components is investigated and shown in Fig.4.9.

The simulations for both 2nd order method and IPPC method are conducted under dc-link capacitance 100uF. Fig.4.19 shows without any decoupling method, the voltage ripple are both 76.5V. With just 2nd order method (the red line), 20 voltage ripple can be achieved. On the contrary, to compensate high-order harmonic components, 11.8V can be achieved with IPPC method. Assuming both methods reach the voltage ripple 20V, the dc-link capacitor size for both methods can be compared. With IPPC control method, only 60uF capacitance is needed based on the (Eq. 4.21).

$$C_{dc}=i_c(t)*\frac{dV_{dc}(t)}{dt} \qquad \text{(Eq. 4.21)}$$

Ceramic capacitors C5750X6S2W225K250KA from TDK are taken here to make apple to apple comparison. At the dc bias 400V, this ceramic value can be 0.431uF each. The package is 2220 with 5.7mm*5.0mm*2.5mm each. For 2nd order method, it needs 232 in total and for IPPC, it only needs 139 in total. Thus, the total dc-link capacitor size can be evaluated and compared shown in Fig.4.20. For traditional 2nd order method, it needs 16.53 cm^3, however, for IPPC method, it only needs 9.9 cm^3, which can be reduced 40% at the same condition.

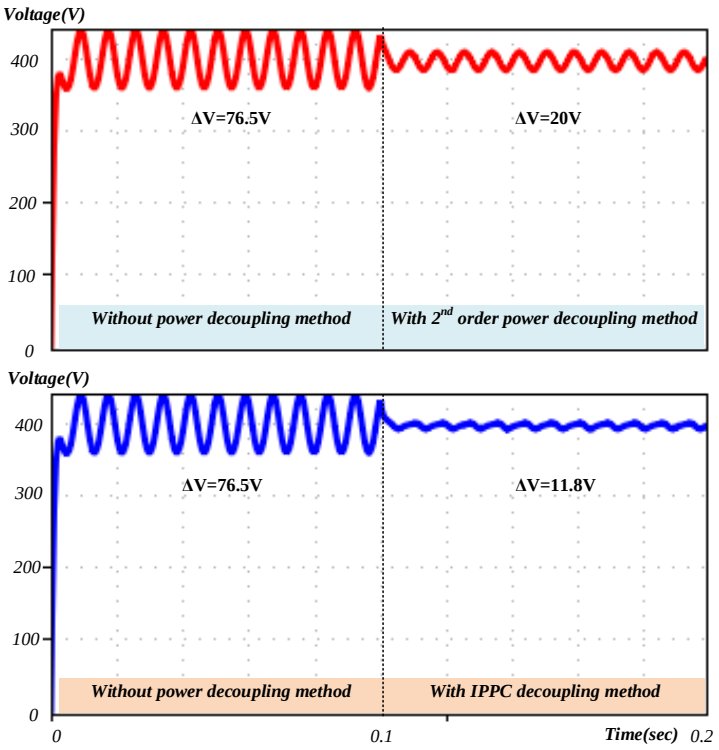


Figure 4.19. Comparison of traditional 2nd order method (red line) and advanced pulse injection method (blue line) under 100uF

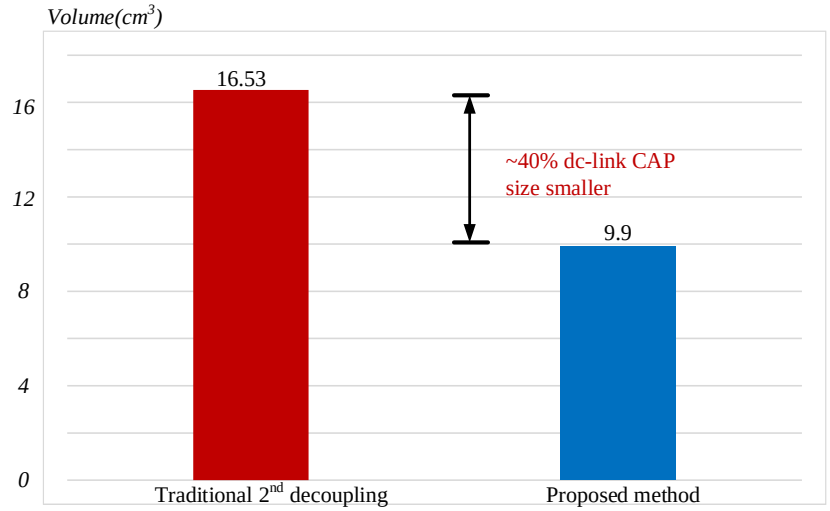


Figure 4.20. DC-link capacitor size comparison under the same voltage ripple condition

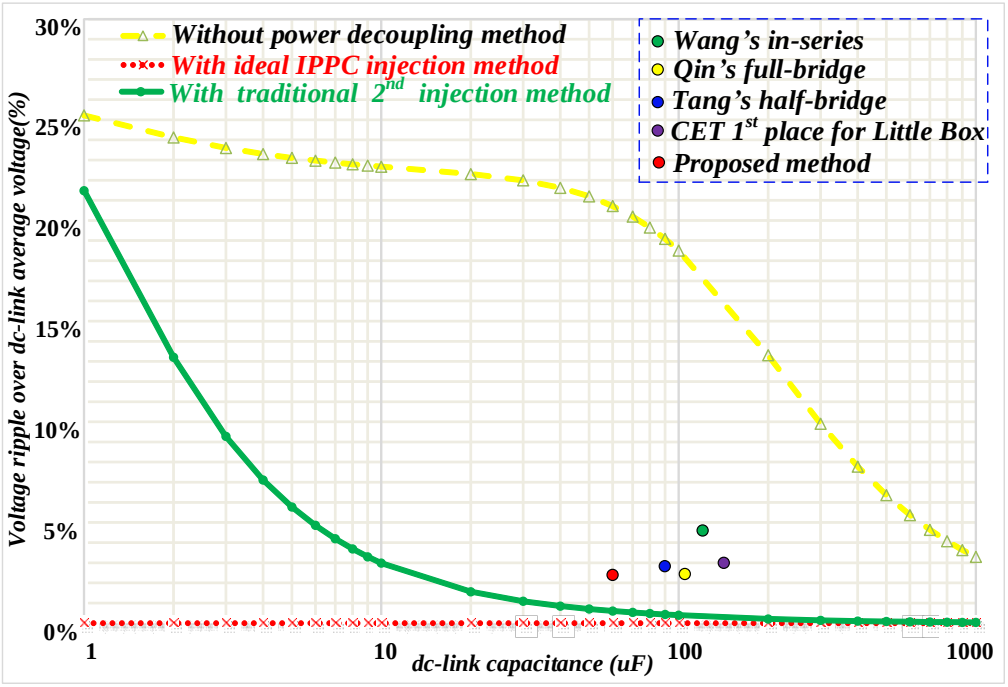


Figure 4.21. Comparison of IPPC injection method and state-of-the-art methods

Furthermore, the state-of-the-art methods for minimized dc-link capacitance are summarized in Fig.4.21 to make a comparison. The comparison is just based on dc-link capacitance and voltage ripple, not on power density. It is not easy to give a standard power density comparison, because of different power rating, different power decoupling topologies and different PCB layout. From the comparison, the proposed pulse method can overcome 2nd order limit curve and achieve extreme-small dc-link capacitance. Ceramic capacitor is a trend for dc-link capacitor application now. The value of ceramic capacitor is normally small and the value also decreases at high voltage stress. With IPPC injection method, package of ceramic capacitors can be reduced significantly.

To verify the controller performance, Fig.4.22 shows transient waveforms from 2kW full-power rating to 1kW half-power rating. The dc-link average voltage is increased from 400.2V with the ripple 11.8V to 426.6V the ripple 5.7V. This is because the input dc current is decreased when the output current is changed half and the voltage drop on the in-series 10Ω resistor is decreased.

As a result, the dc-link voltage V_{dc} is increased. The closed-loop control is followed Fig.4.12. Inverter output voltage is controlled and the output ac voltage rms value is 240V with output current rms value 8.3A (full-power rating) to 4.16A (half-power rating). The transient point happens at t=0.25s and decoupling circuit transient time is ~0.03s.

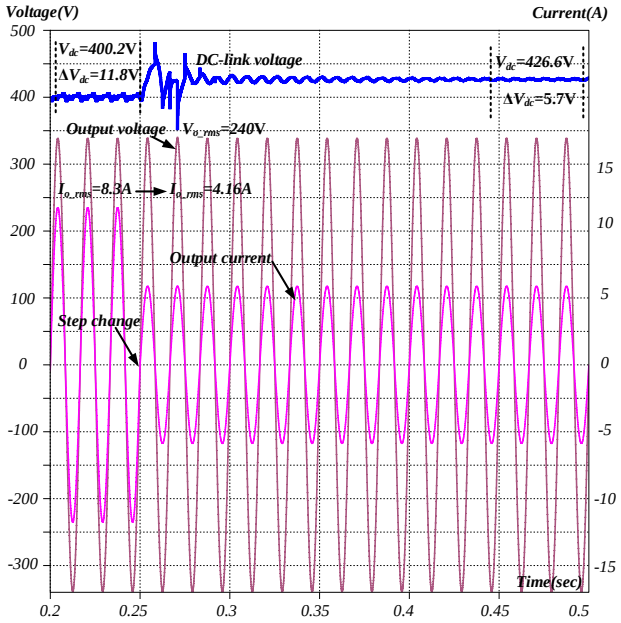


Figure 4.22. Transient waveform from full-power to half-power

When compared with traditional 2nd order decoupling method, IPPC needs higher switching devices. The switching loss of buffer circuit devices with IPPC method is much higher as this decoupling circuit has to track the pulse current. However, the whole system efficiency cannot be affected too much because the buffer circuit only deals with the pulsating power. So the efficiency can be evaluated in (Eq. 4.22).

$$\eta = \eta_{main} - \frac{2}{\pi}(1-\eta_{buffer}) \bullet k \qquad \text{(Eq. 4.22)}$$

where η stands for the whole system efficiency with IPPC control method and η_{main} stands for the inverter itself efficiency. η_{buffer} stands for decoupling circuit efficiency and k is the ratio between the processing power and main output power. When compared with traditional 2^{nd} order

decoupling method, IPPC needs higher switching devices. The switching loss of buffer circuit devices with IPPC method is much higher as this decoupling circuit has to track the pulse current. However, the whole system efficiency cannot be affected too much because the buffer circuit only deals with the pulsating power. So the efficiency can be evaluated in Fig.4.23.

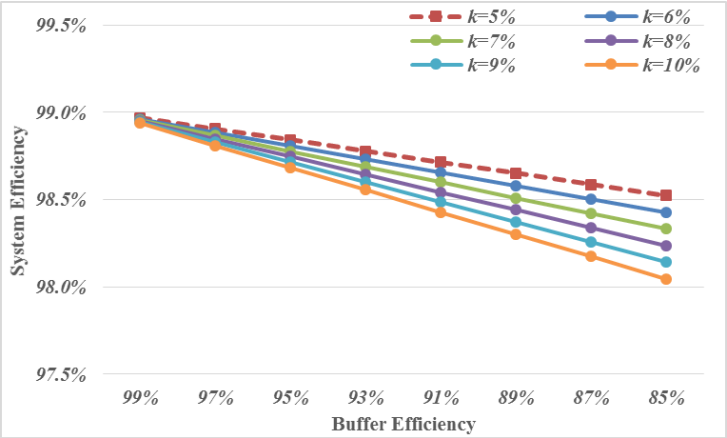


Figure 4.23. Relationship among system efficiency, buffer efficiency and ratio k

Assuming that the main inverter can achieve 99% efficiency, if the buffer efficiency drops from 99% to 85%, the whole system efficiency still can achieve above 98%. Here the ratio k normally is no larger than 10% of the main inverter power rating. As a result, although the decoupling circuit with IPPC method has more efficiency penalty than 2nd order injection method, however, for the whole inverter system, the total efficiency can have less than 1% drop.

4.6. Investigation on Pulse Current Effect with Different DC-Link Capacitances

Based on double Fourier analysis [84], the current going through dc-link capacitor is shown by (Eq. 4.22), which proves that there are still other order harmonic components going through the capacitor. It is shown that besides low frequency components based on fundamental frequency, there are also lots of higher order harmonic components based on both output frequency, carrier frequency and their side-band parts. For three-phase inverter systems, low frequency component can be easily cancelled by the phase leg angle. However, for single-phase inverter systems, low

frequency components, especially 2nd component, make the domain contribution and other components still exist.

$$i_c(t) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty}[A_{0n}\cos(n\omega_o t) + B_{0n}\sin(n\omega_o t)] + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}[A_{mn}\cos(m\omega_c t + n\omega_o t) + B_{mn}\sin(m\omega_c t + n\omega_o t)]$$

(Eq. 4.23)

$$V_{dc} = \sum I(\omega)\bullet[1/\omega C + ESR] \quad \text{(Eq. 4.24)}$$

(Eq. 4.24) shows the relationship between the current components and dc-link voltage ripple. Based on (Eq. 4.24), when dc-link capacitance is large and high-frequency ω is large compared with 2nd order, high-frequency components caused voltage ripple can be ignored. However, if dc-link capacitance is decreased significantly to achieve high power density, the other harmonic components should also be considered, not just 2nd order harmonic. This is because reducing capacitance means extremely amplifying different kinds of harmonics' contribution to the voltage ripple. So how much contribution on dc-link voltage ripple by other current harmonics, besides 2nd component, is presented in Fig.4.24.

From Fig.4.2, dc current from dc source is defined as I_{dc}. The current from dc-link capacitor is defined as I_{cap} and the current through dc-link side going into inverter defined as I_{inv}, respectively. Fig.4.24 shows I_{dc}, I_{cap} and I_{inv} waveforms, under continuous mode (C_{dc}=100uF) and discontinuous mode (C_{dc}=1uF), respectively, under the condition shown in Table.1. I_{inv} is just related with the output parameters and switching frequency. So I_{inv} for two modes are the same based on equation (Eq. 4.23). However, as dc-link capacitance decreases, the energy from dc-link capacitor cannot support the enough energy for one cycle (one switching period). So the current from the dc-link capacitor turns from continuous mode to discontinuous operation mode, which is totally different from large dc-link capacitor's situation. Also, as the capacitance is small, the charge and discharge

time is quite short. So compared with the current I_{dc} straight line in the continuous mode, the current I_{dc} in the discontinuous mode, shown in Fig.4.24, becomes pulse waveform.

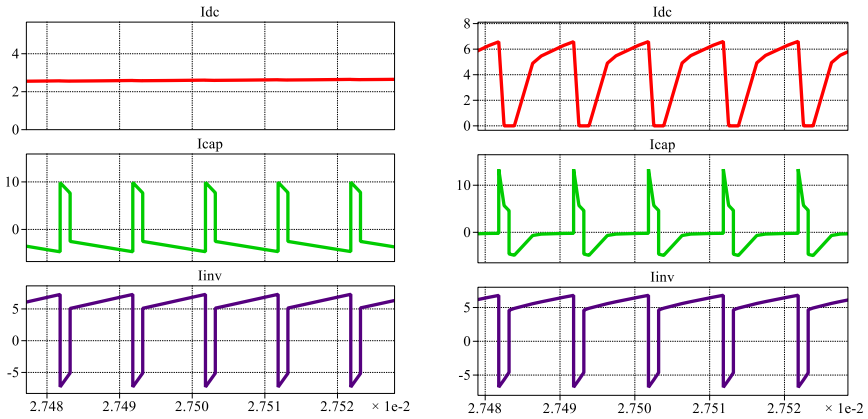


Figure 4.24. Continuous mode and discontinuous mode current waveforms

The spectrum of double Fourier analysis for the dc-link capacitor current is both given in Fig.4.25 and Fig.4.26, respectively for continuous mode and discontinuous mode. Both figures show the amplitude of the current I_{cap} ranging from 1Hz to 1MHz. For continuous mode, the capacitor can support one-cycle energy. The domain component is 2^{nd} order harmonic component and 4^{th} order harmonic is quite small, which is 4% of 2^{nd} order harmonic component. For higher frequency components, such as N times switching frequency and their side-band component, the voltage ripple is affected little by these components based on (Eq. 4.23), because the capacitance is large. On the other side, for discontinuous mode, 2^{nd} order harmonic component is not dominated component any more. 4^{th} order harmonic is 96% of 2^{nd} order harmonic component and 6^{th}, 8^{th} are 35%, 68% of 2^{nd} order harmonic component, respectively. Other components except 2^{nd} order harmonic take much larger proportion compared with those in continuous operation mode. Furthermore, the higher order components, which are related with switching frequency, take larger proportion compared with low frequency components. They also make contributions on dc-link voltage ripple. Finally, time domain dc-link voltage ripple waveforms for both continuous

operation mode and discontinuous operation mode are shown in Fig.4.24 when the capacitance is 1uF. For continuous mode, 2nd order harmonic of current takes domain and it reflects 2nd order voltage ripple waveform. However, for discontinuous mode, other orders harmonic components also make contributions to the voltage ripple.

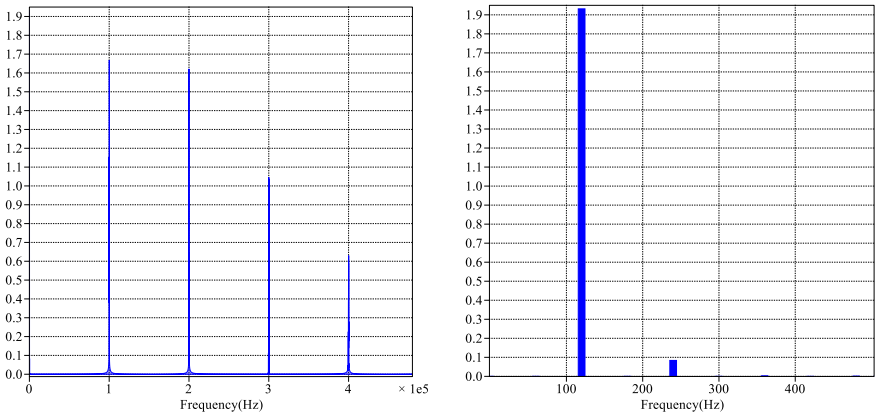


Figure 4.25. Double Fourier analysis for cap current under continuous mode and its zoom-in low-frequency components

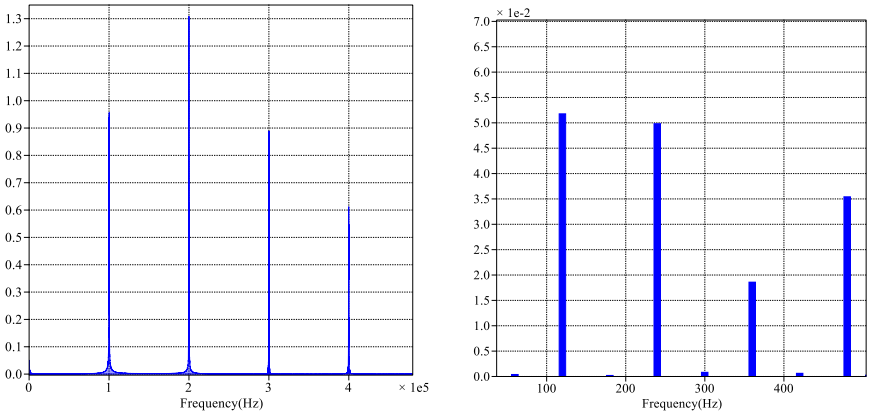


Figure 4.26. Double Fourier analysis for cap current under discontinuous mode and its zoom-in low-frequency components

As a result, the voltage ripple is composed of different-order harmonic components. The voltage ripple, which is shown in Fig.4.21 when the capacitance is 1uF for discontinuous mode, is totally changed. The voltage ripple does not follow 2nd order harmonic. The traditional 2nd

harmonic power decoupling method is very limited for this condition, as other-order harmonics should also be considered.

The detailed current waveforms and operation principles of discontinuous mode are shown in Fig.4.27. For discontinuous mode operation, it can be divided into five stages. During one switching period cycle ($t=1/f_s$), stage (a) shows both dc side and inverter side charge the capacitor together; until dc side current decreases to 0, the inverter current charges the capacitor in stage (b); then the capacitor current discharges into inverter side shown in stage (c). As the energy in capacitor is small, in stage (d), both dc side and capacitor current go into inverter side. Until the capacitor current becomes zero, just the dc side current goes into inverter side in stage (e).

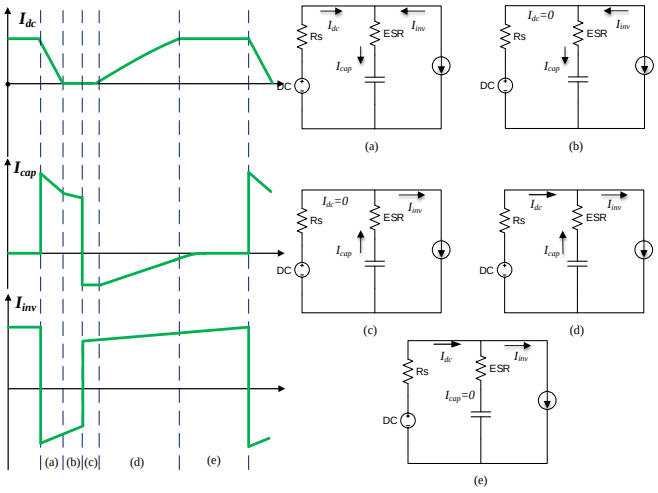


Figure 4.27. Key current waveforms and operation modes of dc-link capacitor under discontinue mode

What's more, Fig.13 shows voltage ripple under different capacitance and different switching frequency under the same condition shown in Table.4.1. When dc-link capacitance is reduced to one particular value, dc-link capacitor cannot support the energy for one switching cycle. The operation mode is changed from continuous mode to discontinuous mode. For discontinuous mode, traditional 2nd order power decoupling method is not suitable at all because

2nd order harmonic is not the domain component any more. Actually, before it comes into discontinuous mode, traditional 2nd method has some limit already shown in Fig.4.9. However, IPPC injection method is still suitable for the whole area. So the whole area can be divided into two modes when power decoupling method is considered. Under extremely small dc-link capacitance with discontinuous mode, increasing switching frequency can reduce the dc-link voltage ripple by a little amount as shown in Fig.4.28.

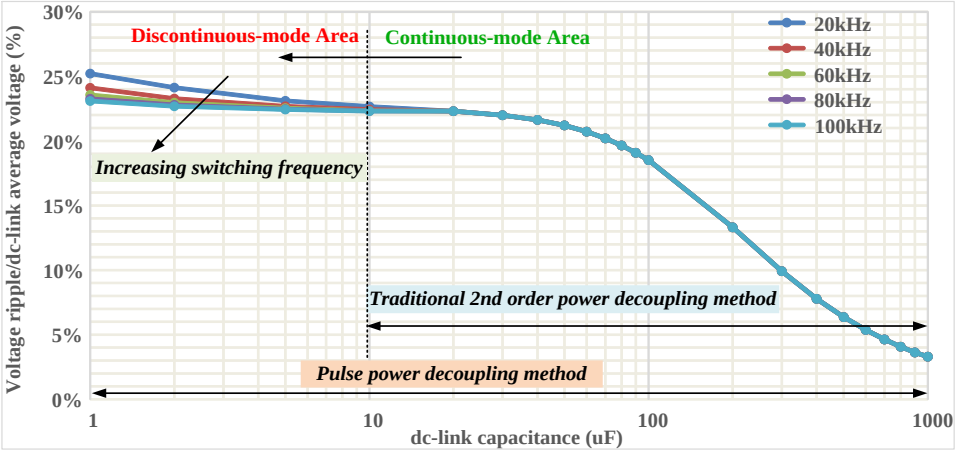


Figure 4.28. Comparison of voltage ripple under different cap values and different switching frequency

4.7. Experimental Results

A 2kW prototype is developed in this paper based on the IPPC concept. Its size is 7.25 inch ×3.6 inch ×1.4 inch and the power density of prototype is about 55W/inch^3. Another similar prototype is applied for pulse current injection with forward control. The test bench is shown in Fig. 4.29. Fig. 4.30 shows the gate drive waveform of SiC MOSFET device for the main circuit with bipolar SPWM control. SiC MOSFET (SCT2120AF) device from ROHM is chosen here. The gate voltage is positive 15V and negative 5V. Fig. 4.31 shows the current waveforms of I_{inv} and I_{inj}, which stands for the inverter side pulse current and injected current with forward control.

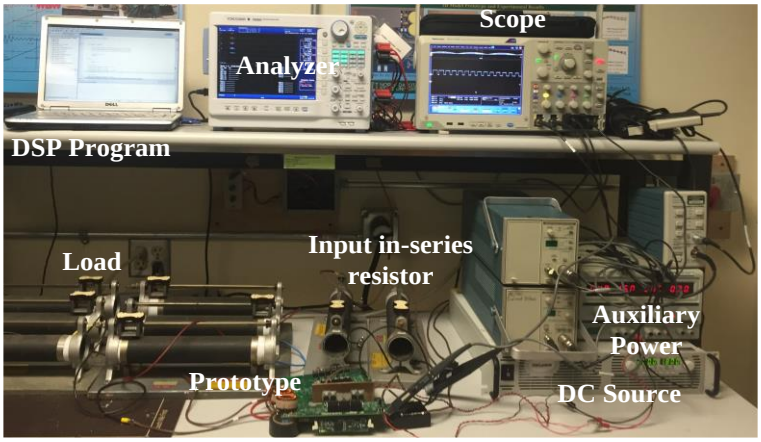


Figure 4.29. Overview of test bench and 2kW prototype

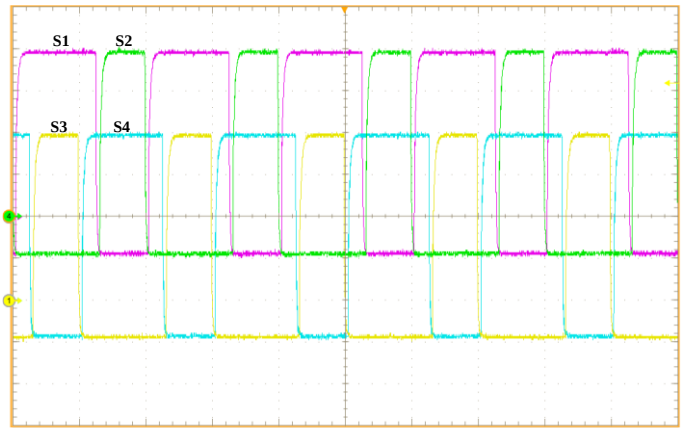


Figure 4.30. 100k Hz SPWM gate driver signals (5V/div), time scale: 5us/div

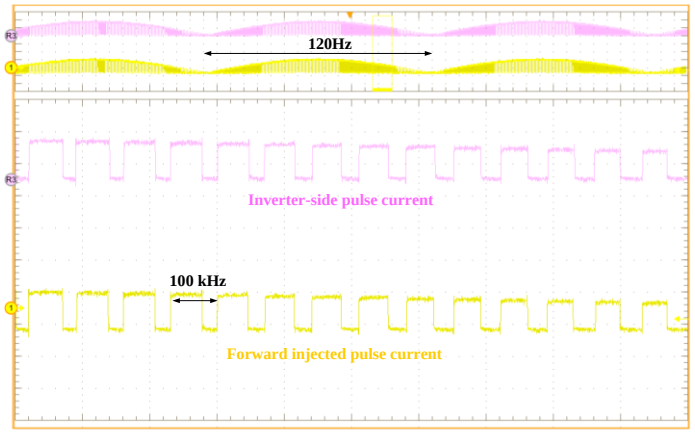


Figure 4.31. Inverter-side pulse current and injected current (2A/div), time scale: 15us/div

The dc-link voltage ripples are shown in Fig.4.32 and Fig.4.33 for the conditions without and with the proposed power decoupling method, respectively.

It is shown that, the average dc-link voltage is set about 190V here due to the effect of the series-connected resistor, and the voltage ripple is ~45V for traditional inverter. The percentage is about 23.7% under 10uF dc-link capacitance. On the other hand, with the proposed power decoupling method, most of the 2nd order harmonic ripple can be eliminated. Pulse injected current waveform and inverter-side dc current I_{inv} are shown in Fig.4.34.

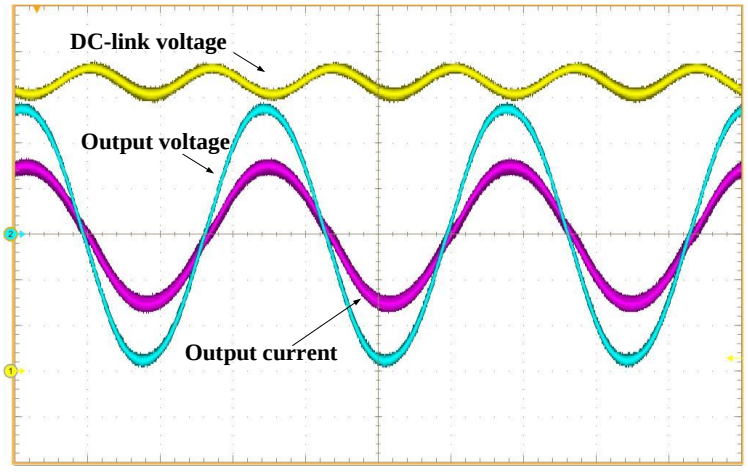


Figure 4.32. Before pulse injection, DC-link voltage (100V/div), output voltage (50V/div) and output current (2A/div), time scale: 10ms/div

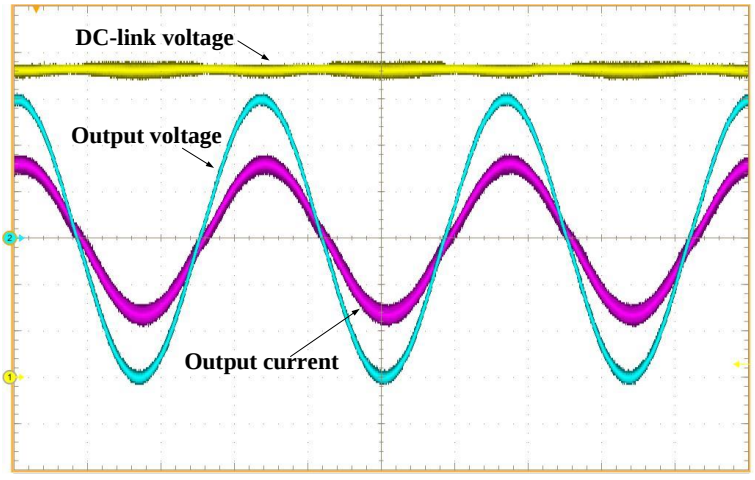


Figure 4.33. After pulse injection, DC-link voltage (100V/div), output voltage (50V/div) and output current (2A/div), time scale: 10ms/div

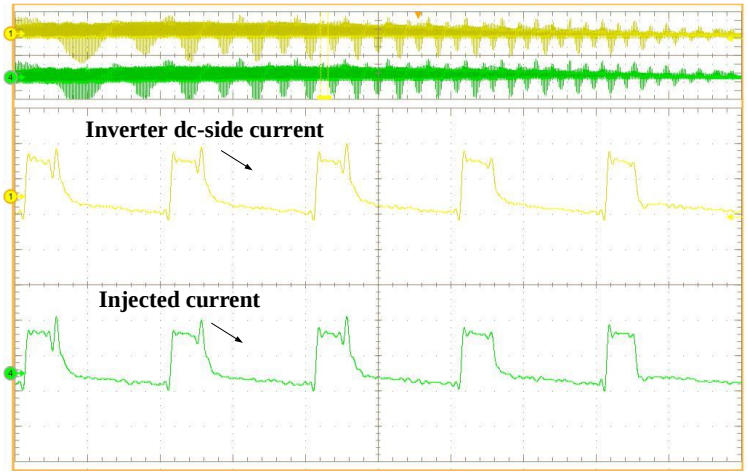


Figure 4.34. DC-link voltage (50V/div), inverter dc-side current, (10A/div) and injected current (10A/div), time: 5ms/div

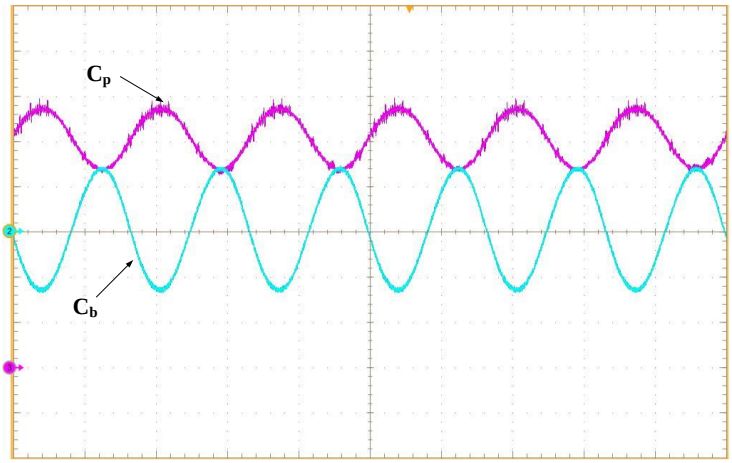


Figure 4.35. The voltage of Cb (50V/div, peak ~65V) and Cp (80V/div, peak ~64V) , time: 5ms/div

The voltage ripple is reduced to ~11V. The percentage is ~5.6%. The experiments has some tolerance compared with simulation, because there is device spike and some high-frequency ripple is still not fully cancelled out. This can be further improved with closed-loop control. Fig.4.35 shows the C_p and C_b voltage.

In conclusion, the experimental results verify that the pulse current exists in the inverter dc-side. It can be eliminated with the proper control method. The voltage ripple can be reduced in small dc-link capacitance condition.

4.8. Discussion

The IPPC concept can be widely applied in dc-dc, dc-ac, ac-dc applications. The aim of this paper is to propose this concept and make a detailed case study on single-phase DC-AC application. For example, Fig.4.36 shows the basic schematic of Buck dc-dc converter with IPPC concept. Here briefly shows the concept level without detailed circuits considered. Although increasing Buck switching frequency can reduce LC filter, the input capacitor is still large volume. An IPPC compensator can be applied in Buck converter to compensate the input pulsating power to minimize the input capacitance.

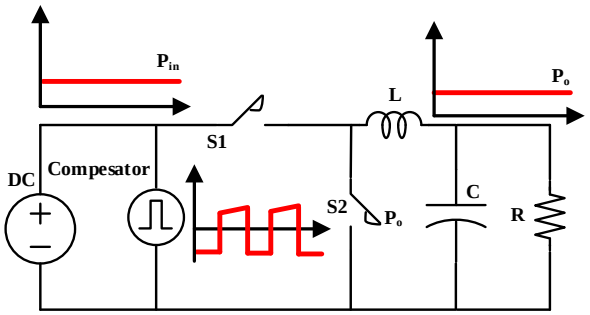


Figure 4.36. Buck converter with IPPC concept

Three-phase inverters are widely used in hybrid electric vehicles (HEVs) and electric vehicles (EVs). However, a known problem of three-phase inverter is large-size and short- lifetime dc-link capacitor because of root mean square (rms) current [64]. Fig.4.37 shows basic schematic of three-phase inverter and detailed inverter-side current waveform of SPWM in one switching period. Unlike single-phase pulse current, three-phase inverters have special waveform of inverter-side current I_{inv}. IPPC concept can be applicable to three-phase inverters to reduce the capacitor rms value by injecting special current waveform similar with inverter-side current shape to prevent large-size capacitor self-heating.

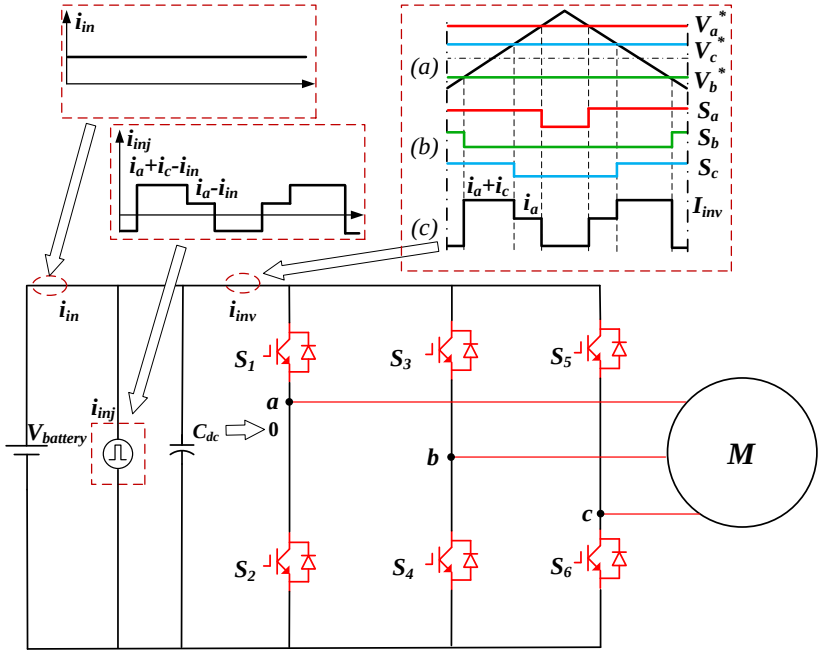


Figure 4.37. IPPC concept for high density three-phase inverter system

For MMC applications, the circulating current in phase legs is an inherent phenomenon. The circulating current affects various aspects of MMC performance, such as power losses, capacitor voltage ripples, and the required current rating of semiconductors. Traditionally, different kinds of control methods are taken to eliminate the circulating current. IPPC concept can also be applicable to this situation to reduce circulating current with low-stress wide bandgap devices. The feasibility of these high density applications with IPPC concept will be studied in the future research work.

5. CONTROLLER DESIGN FOR SINGLE-PHASE GRID-TIED INVERTER

5.1. Introduction

This chapter presents the controller design for single-phase grid-tied inverter. Single phase inverter is focus on low and medium power application, such as feed energy from Photovoltaics (PV) panel to the power grid. Different kinds of researches have been carried out regarding single phase inverter. Besides power decoupling issues analyzed above, inverter control issues are also one of the hottest area. Among the control strategy of single phase inverters, some researchers devote to reducing the dc link capacitor to increase to power density [84], some researchers are focusing on reducing the power loss on inverter operation. Also, controllers that process features such as fast response and low THD [85] and robustness [86] are proposed in the past years since the THD of current that has been feedback to grid must meet the requirement and more reliable controllers are desired if an inverter needs to connect to the power grid. [87]-[93] shows how to design output filters. As mentioned above, a variety of control related issues and corresponding solutions have been proposed during the recent years. This chapter will have a discussion on how to go through all the procedures fast and easily with Matlab controller design tool and PLECS simulation software. Furthermore, one prototype is successfully connected into Grid with Transphorm.Inc GaN based 600V devices TPH3006PS.

5.2. Controller Design with Matlab Tool

The controller design for grid-tied inverter is normally complex and the whole procedure takes lots of time. This chapter shows one method from theoretical analysis to final experimental analysis with Matlab SISO tool. Fig.5.1 shows the LCL filter for the single-phase inverter design. And Fig.5.2 shows the simplified control system block. The open-loop transfer function can be

easily got in (Eq. 5.1). With ESR considered for each passive component, the detailed transfer function for LCL filer can be expressed in (Eq. 5.2).

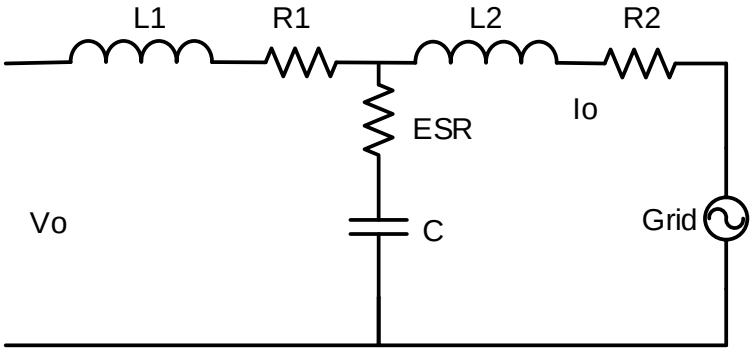


Figure 5.1. Schematic for LCL filter

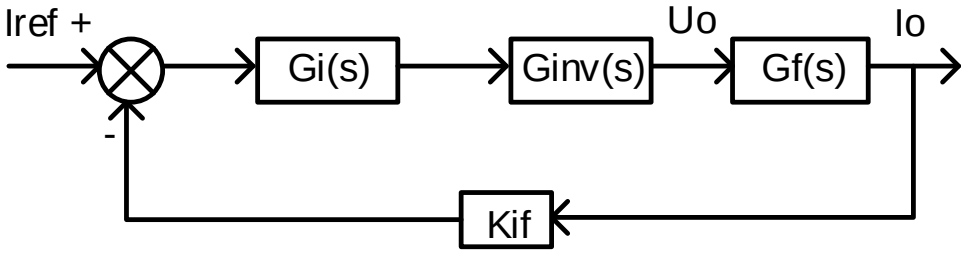


Figure 5.2. Simplified control system block

$$G_{open}(s) = G_{inv}(s) * G_f(s) = \frac{K_{pwm}}{T_s s + 1} * G_f(s) \quad \text{(Eq. 5.1)}$$

$$G_f(s) = \frac{C_c R_c s + 1}{L_1 L_2 C_c s^3 + (C_c R_c L_1 + C_c R_2 L_1 + C_c R_1 L_2 + C_c R_c L_2) s^2 + (L_1 + C_c R_1 R_c + C_c R_1 R_2 + C_c R_2 R_c + L_2) s + R_1 + R_2} \quad \text{(Eq. 5.2)}$$

With detailed parameters in the real prototype, The Bode plot can be presented in Fig.5.3 and Fig.5.4 with magnitude and phase plot, respectively. The inductor value for L1 is 275*2uH, as two inductors are taken here and each inductance is 275uH. The equivalent series resistance (ESR) for L1 is 35m*2. Similarly, the inductor value for L2 is 41.25uH and ESR for L2, which means R2 is equal to 0.2. The capacitor value is 2.2uF with ESR 12.4m. As a result, put all the detailed parameters into transfer function can easily get the final transfer function. The plot can be drawn in Mathcad to briefly show the waveform and do some quick analysis based on Bode plot.

Furthermore, in order to do the closed-loop controller design, the transfer function needs to be written with Matlab code.

Table 5.1. Detailed parameters for LCL filter

L1	275*2uH	R1	35m*2
L2	41.25uH	R2	0.2
Cc	2.2uF	ESR	12.4m

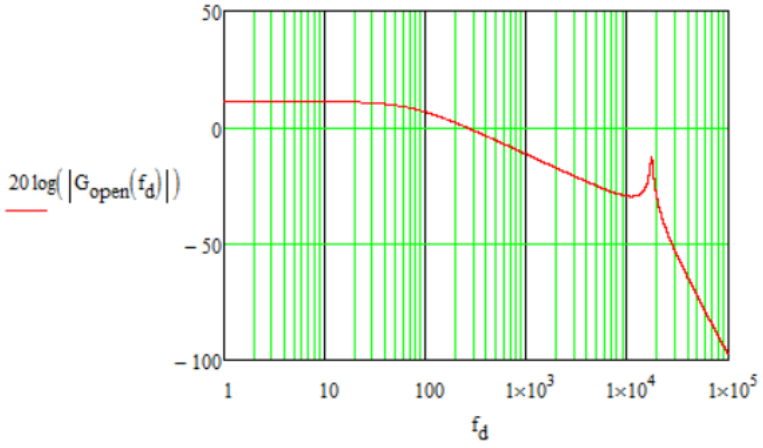


Figure 5.3. Bode plot (Magnitude) with detailed parameters

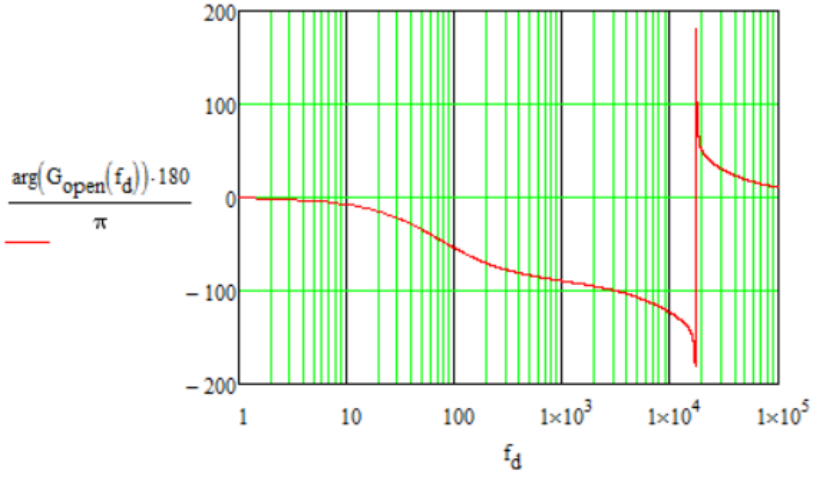


Figure 5.4. Bode plot (Phase) with detailed parameters

Fig.5.5 shows the magnitude Bode plot with Matlab C code and it matches with the plot in Mathcad. Then with Matlab SISO tool, it easily can get the PI parameters and verify the step response to see whether the PI parameters are good or not. Fig.5.6 shows the closed-loop figure with P=0.1 and I=1000 with good dynamic performance and stead-state performance as well.

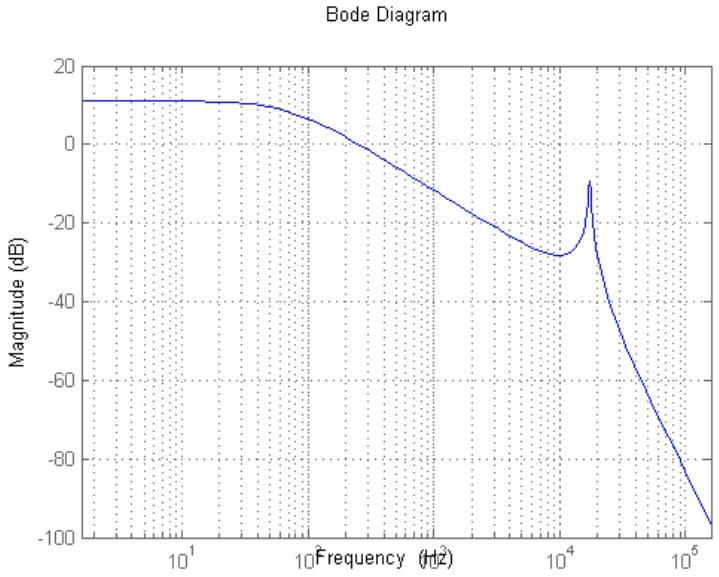


Figure 5.5. Bode plot with Matlab code for PI design

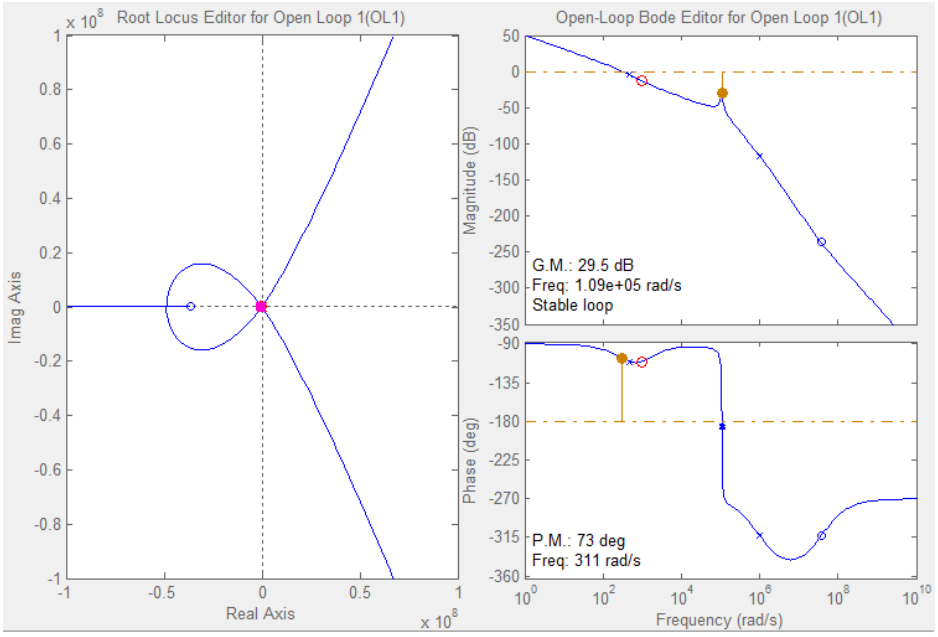


Figure 5.6. Matlab SISO tool PI design with P=0.1 and I=1000

Fig.5.7 shows the step response with P=0.1 and I=1000 with good dynamic performance 0.018s and stead-state performance with no error.

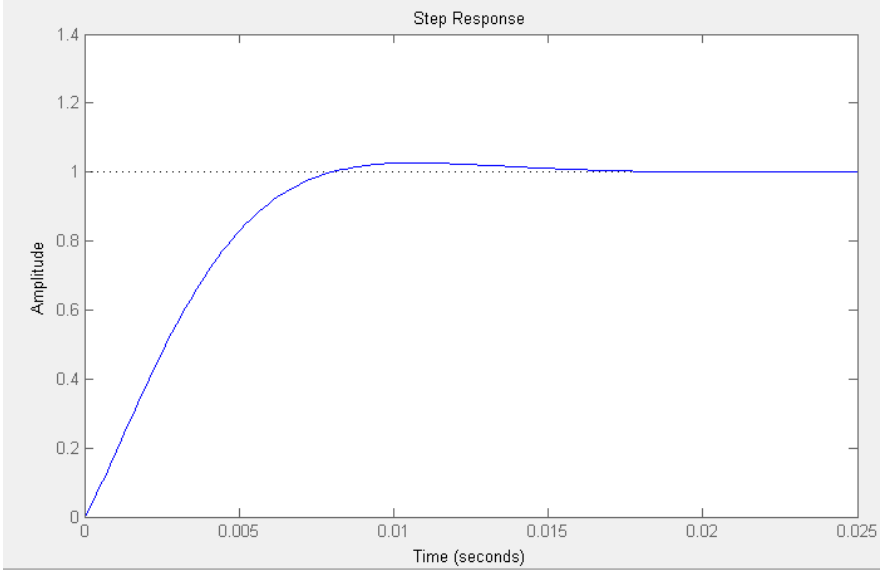


Figure 5.7. Closed-loop step response with P=0.1 and I=1000

5.3. Simulation and Experimental Results

The simulation is conducted with designed PI parameters in PLECS software shown in Fig.5.8. The MOSFET device here is chosen TPH3006PS from Transphorm Inc. The dc voltage is 350V and all the detailed LCL filter parameters follow Table.5.1. With detailed devices, the PI parameters are adjusted to P=0.01 and I=500. The output voltage and output current are shown in Fig.5.9. And the output voltage is 208V rms, 60 Hz. The rms current is ~5A.

Fig.5.10 shows the grid-tied test bench together with 1.5kW prototype. The experimental results are shown in Fig.5.11 and Fig.5.12. Fig.5.11 shows the working power rating is at 125W with P=0.01 and I=1000 and Fig.5.12 shows the power rating is at 290W with P=0.02 and I=1100.

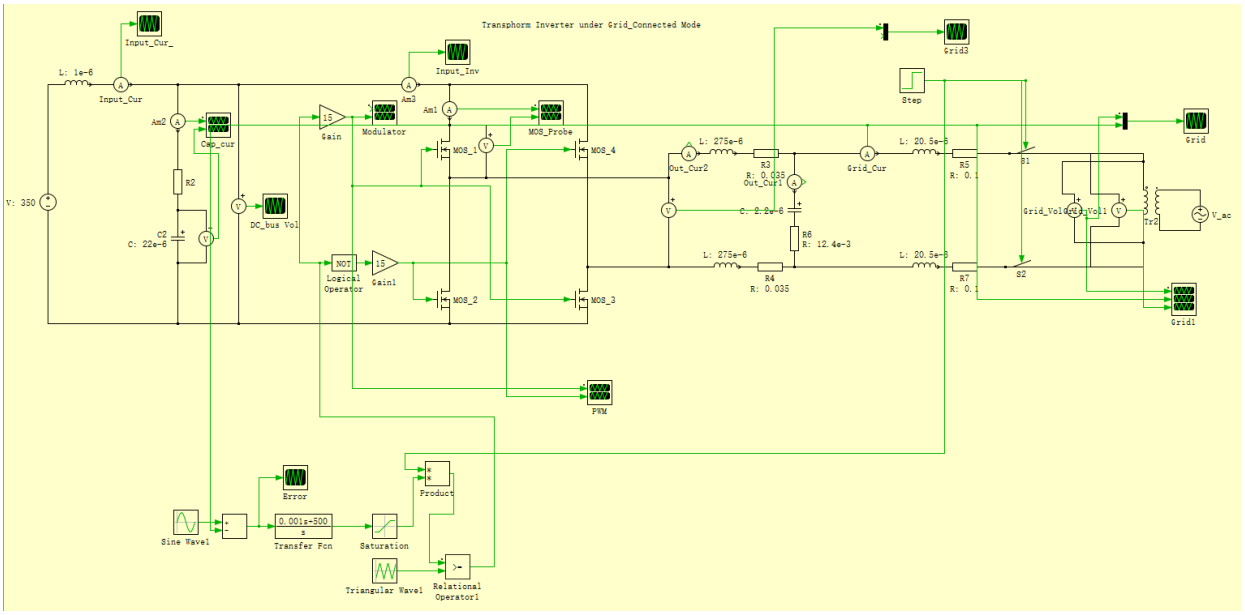


Figure 5.8. Simulation with PLECS software

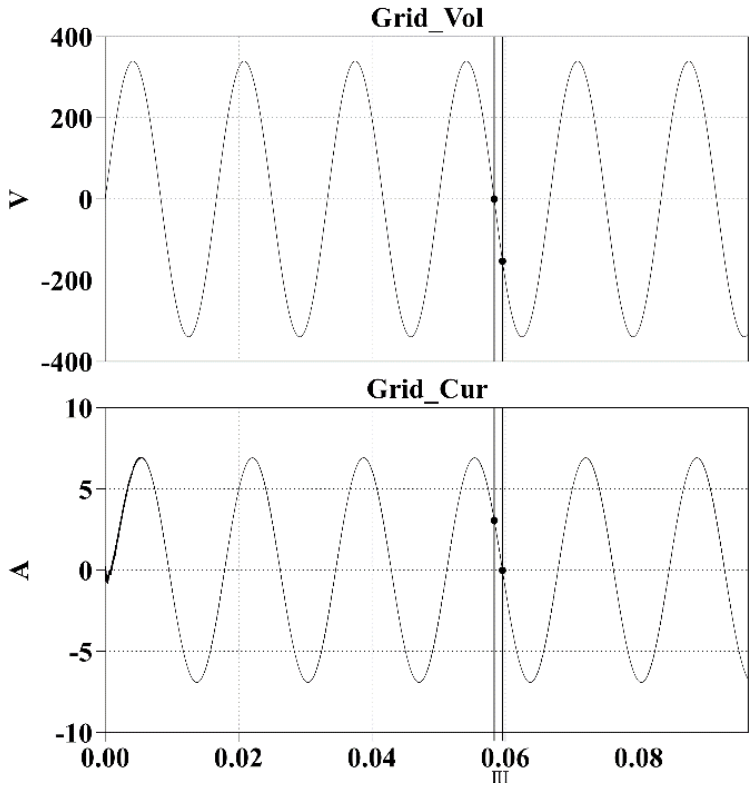


Figure 5.9. Output voltage and current waveforms

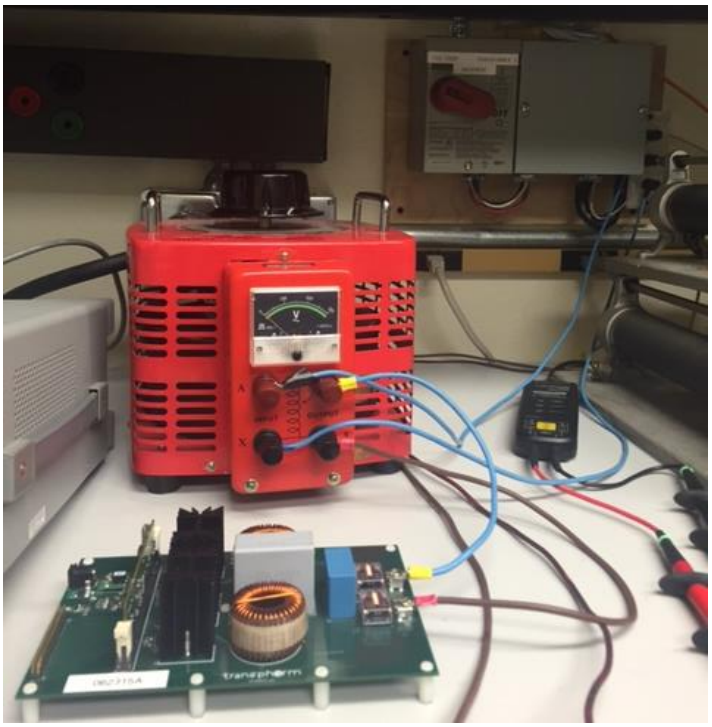


Figure 5.10. Grid-tied test-bench set-up

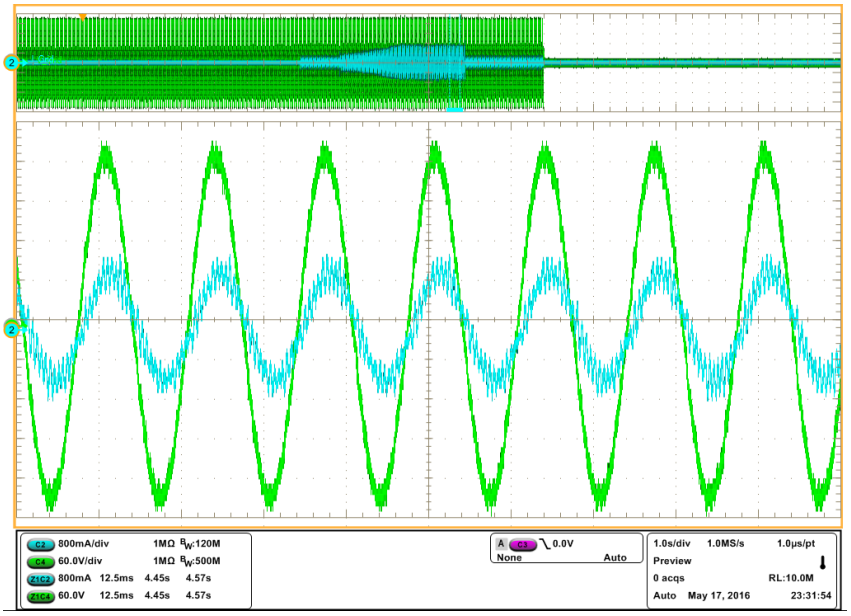


Figure 5.11. Experimental results at 125W

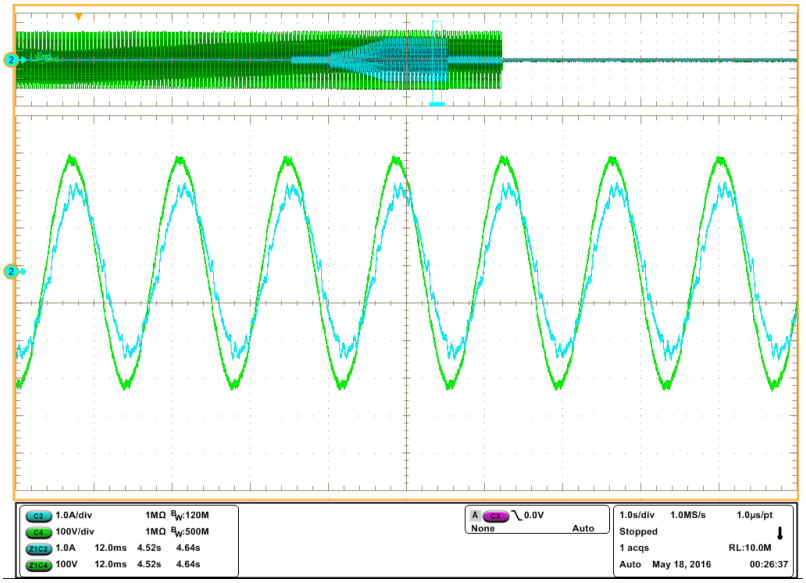


Figure 5.12. Experimental results at 290W

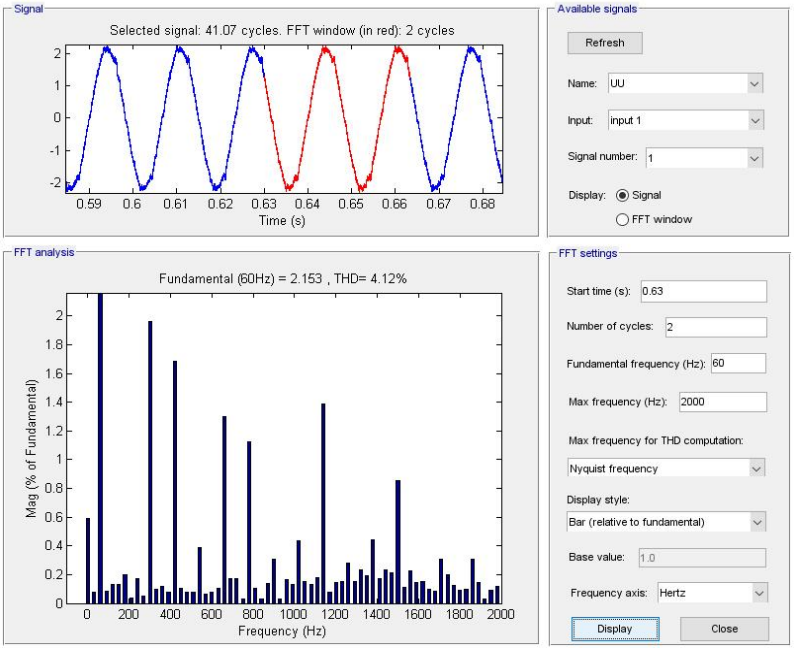


Figure 5.13. Matlab spectrum analysis with real data

Furthermore, after getting the current waveform data, it can be imported into Matlab tool to do spectrum analysis. Fig.5.13 shows the current waveform for the grid-tied test at 290kW. The spectrum can be done quickly and each harmonic component will be presented as well. The THD can be calculated with this tool at 4.12%. Also power factor can also be calculated at 0.96.

5.4. Inrush Current Issue and Its Solution

In practical grid-tied applications, inrush current is a big issue when the prototype is hooked up to the grid. This is because when the prototype is connected, there is large over-shoot current and voltage on the grid-side. This over-shoot current or voltage will damage the switch device immediately. So how to smartly solve inrush current issue is very important in the real case. Fig.5.14 shows the relay G6C-1117P-US-DC5 onboard. The function of this relay is to isolate the prototype or connect the prototype to the grid.

Figure 5.14. G6C-1117P-US-DC5 relay with operate time 10ms max

This relay have 10ms operate time, which will not be ideal one in the practical application. This will cause inrush current issues. Fig.5.15 shows the waveforms when the prototype detect zero voltage points. When the DSP detect zero points, it will turn-on the relay. However, the real relay has a delay. After this delay time, the grid voltage is not zero. So there is inrush current back into the board and damage it when the prototype starts to work. Fig.5.16 shows the zoom-in waveform for this phenomenon.

So how to solve this issue is modelled and conducted with Saber software. Saber has a similar modeling relay, which can be revised with the real product parameters. The circuit modeling is built in Fig.5.17. A delay is made by phase shifted the control signal with different degrees.

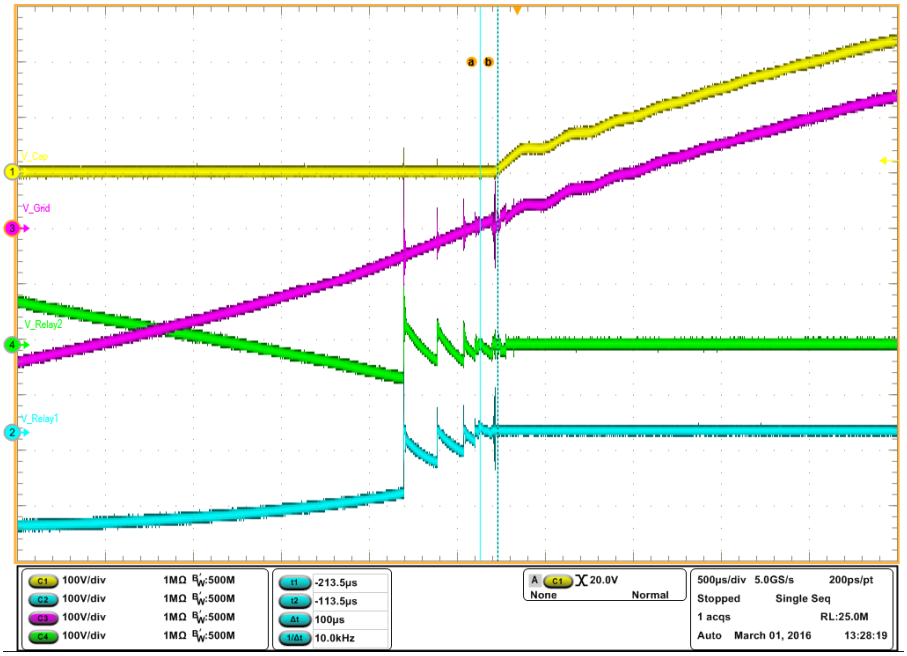


Figure 5.15. Relay operation time delay issues

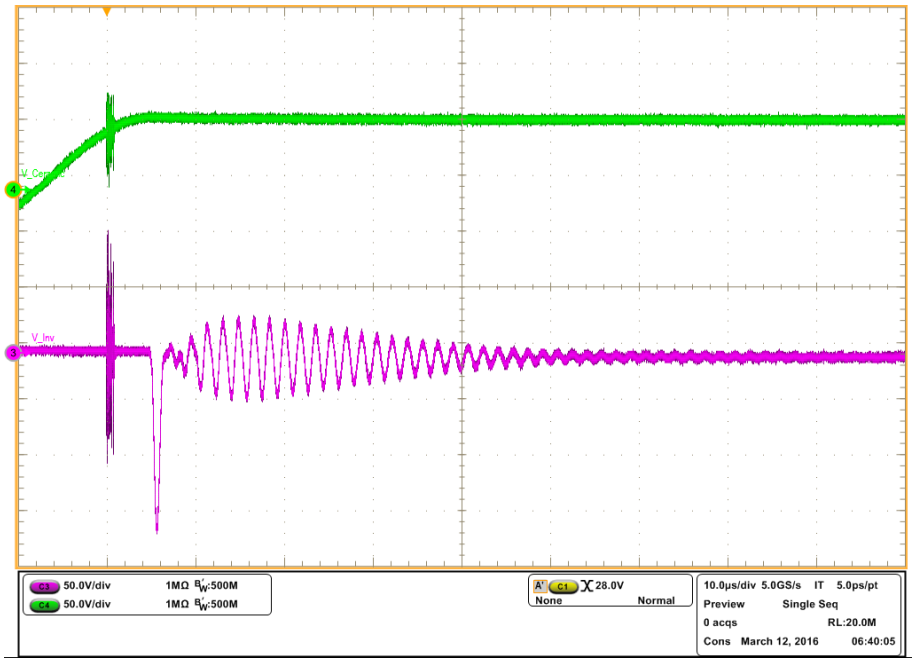


Figure 5.16. Zoom-in for relay operation time delay issues

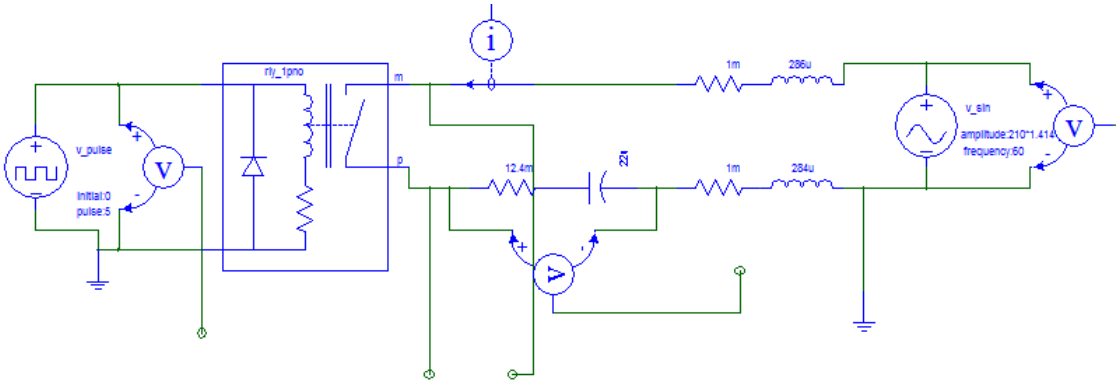


Figure 5.17. Investigate on delay issues with Saber

Fig.5.18 to Fig.5.21 show different delay time compensation with 90 degree, 45 degree, 30 degree and 10 degree, respectively.

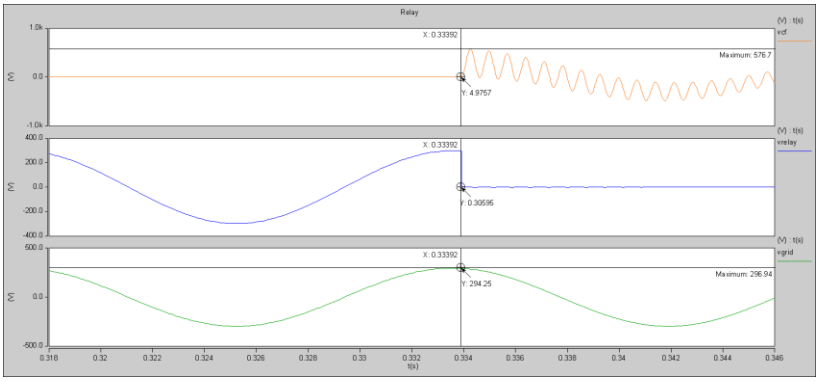


Figure 5.18. 90 degree phase delay with max_voltage 577V

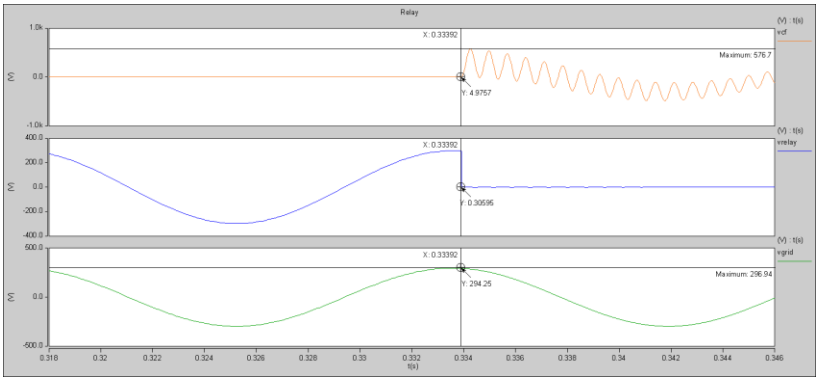


Figure 5.19. 45 degree phase delay with max_voltage 483V

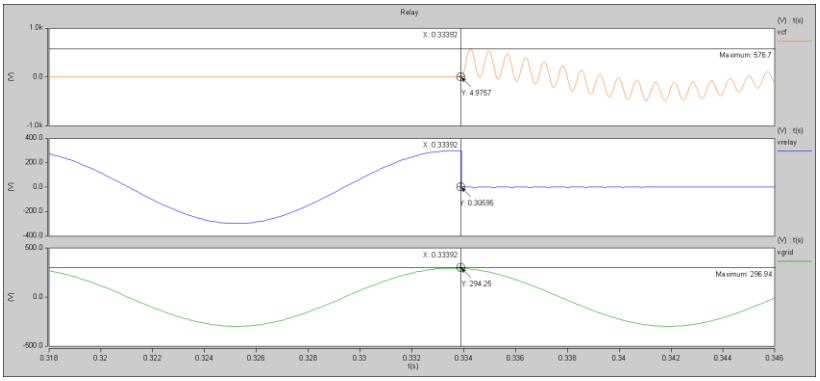


Figure 5.20. 30 degree phase delay with max_voltage 426V

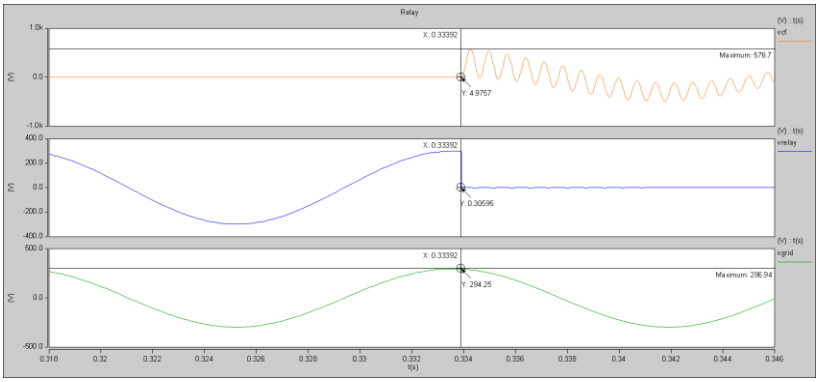


Figure 5.21. 10 degree phase delay with max_voltage 334V

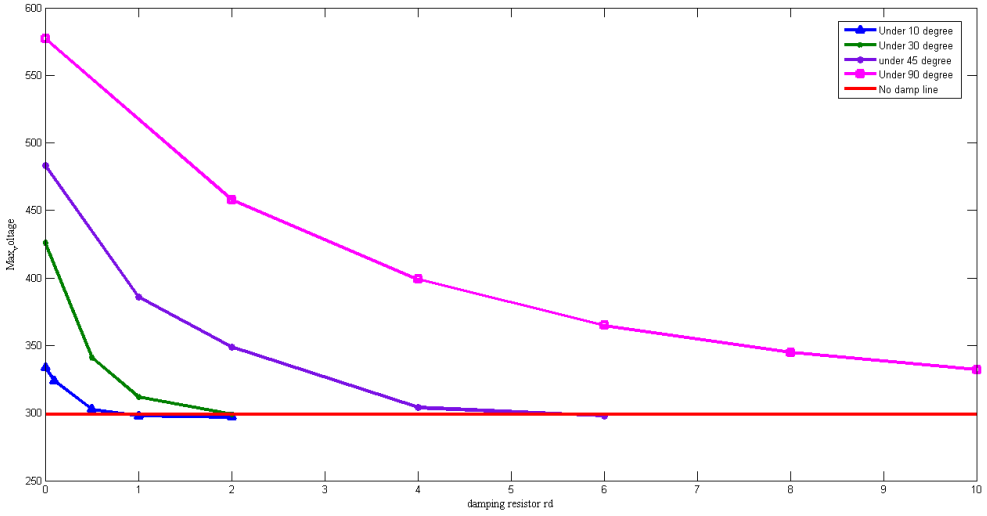


Figure 5.22. Voltage overshoot via damp resistor and delay compensation

Furthermore, different damp resistance on the capacitor are also investigated here. Fig. 5.22 shows under different damp resistors and delay time, the over-shoot voltage values can be got. It

proves that below 10 degree phase shift delay, there is no need for damp resistor at all. It means just with software delay time, this issue can be solved.

Fig.5.23 shows without any software compensation, there is huge inrush current. With proper delay compensation in Fig.5.24, the inrush current can be eliminated very well. Fig.5.25 shows the zoom-in waveform without any inrush current. So this issue can be solved well.

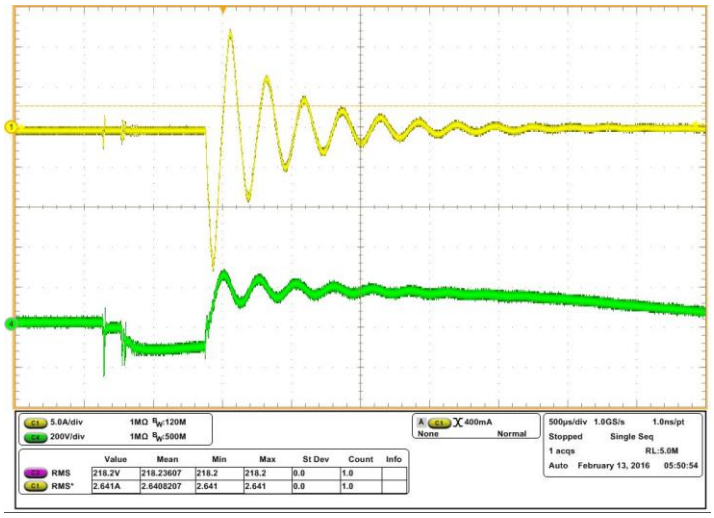


Figure 5.23. Inrush current with no CNT delay

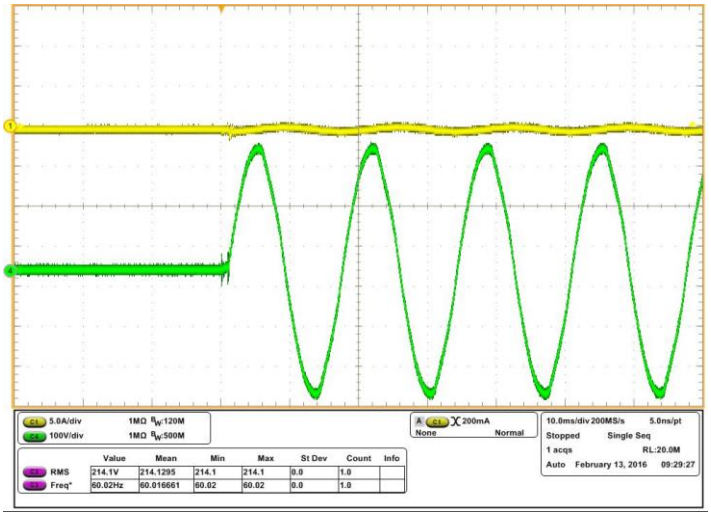


Figure 5.24. No inrush current with CNT=113 delay

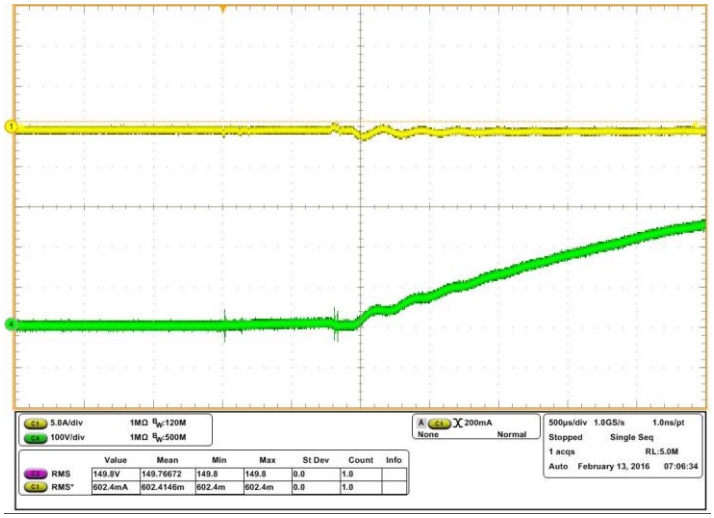


Figure 5.25. Zoom in for no inrush current with CNT=113 delay

5.5. Conclusion

This chapter presents an easy design procedure for grid-tied single-phase inverter controller design. The transfer function can be presented in Mathcad to briefly analyze the dynamic and steady-state performance. Then, with Matlab SISO tool, the open-loop and closed-loop Bode plot can be quickly drawn with detailed PI parameters. After PI parameters designed, PLECS software can verify the system performance. With designed PI parameters, experimental results are got in the real prototype. And grid current waveform can be analyzed from scope to Matlab tool. The spectrum can be shown in the Matlab tool easily. Different harmonic components can be got. Furthermore, THD and power factor (PF) can also be calculated automatically. Step response can be generated fast in this tool to see the system dynamic performance and steady-state performance. Good PI parameters can be generated and tried in this whole operating loop and finally it can get best parameters for grid-tied inverter system with both good dynamic performance and good steady-state performance with no error.

6. N-MODULE PARALLELED INTERLEAVING METHOD FOR HIGH-POWER-DENSITY THREE-PHASE INVERTER

6.1. Introduction

This chapter presents a three-phase inverter dc-link capacitor RMS current reduction method. The proposed method is especially suitable for high current electric drive application while multiple switching devices have to be connected in parallel at the package level, such as Toyota Camry or Tesla Model S. This paper analyzed the proposed method theoretically using double Fourier analysis, and derived the optimal operating point. Furthermore, the effectiveness of the proposed method is also verified by simulation under different PWM strategies, (SPWM, SVPWM, and DPWM1), carrier shapes (triangle and saw-tooth) and power factors. The proposed dc-link capacitor current cancellation method could lead to smaller dc-link capacitor design, the system volume reduction and cost are also estimated with different number of device packages in parallel. The experimental results are also provided using a 6kW SiC based inverter prototype assuming three paralleled devices in each phase leg, which are consistent with theoretical analysis and simulation results.

There is increased demand for the high-power-density inverter. For example, high power density single-phase inverters are used in uninterruptible power supply (UPS), data center, photovoltaics (PV) and vehicle-to-grid technology (V2G). And also high power density 3-phase inverters are applied in on-board ships, oil & gas, electric vehicle (EV) and hybrid electric vehicle (HEV).

In general, dc-link capacitor is the key component for obtaining a stiff dc-link voltage and smooth current. For single-phase inverter system, there is usually a large-size electrolytic capacitor to absorb the pulsating power at twice the fundamental frequency. To minimize the dc-link

capacitor, there are many proposed methods [94]-[95] to solve 2nd harmonic energy storage for single-phase inverter. On the other hand, unlike the single-phase inverter problem, for 3-phase inverter system, they have no 2nd harmonic or even low frequency harmonics issue. However, there is still a large volume capacitor selected, because of bus-bar stray inductance and device spike existing in the real system, what is worse, even several large capacitors are in parallel in order to prevent their self-heating, because of the equivalent series resistance (ESR). As a result, the root-mean-square (RMS) value of the dc-link ripple current is of great importance as reducing this value means high power density and long life time for the whole system.

As described above, the introduction part will be divided into three parts, including 3-phase inverter dc-link current RMS value analysis, the state of the art review for methods to reduce 3-phase inverter dc-link current RMS value and discussion on 3-phase inverter system architecture and its interleaving method application. Finally, the proposed method and its application are given and introduced.

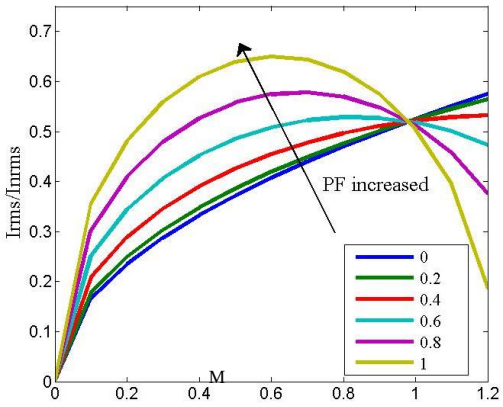


Figure 6.1. Relationship among power factor, modulation index and RMS current value

A. Analysis on 3-phase inverter dc-link current RMS value

Until now there are many papers [96]-[105] to analyze the RMS value of dc-link capacitors. In general, the RMS value of the dc-link ripple current for 3-phase inverters is determined by the

topology, the modulation strategy, modulation index, and peak value and power factor of the output phase current. The principle to analyze the RMS value is either based on time domain [96] or frequency domain [106]. Paper [96] shows the basic analysis based on the space vector modulation used in three phase inverter system. This method is easy to calculate, however, it is limited to space vector control method and it is not so accurate compared with frequency domain analysis. Fig.6.1 shows the relationship among power factor, modulation index and dc-link capacitor RMS current value. Furthermore, [104] shows a general analytical method with double Fourier method. This method is calculated based on half-bridge topology with double Fourier method. So it can be widely used in single-phase inverter, 3-phase inverter system and even multi-level inverter system.

B. A state of the art review for methods to reduce 3-phase inverter dc-link current RMS value

In general, to reduce the dc-link capacitor for 3-phase inverter system, there are kinds of methods shown in Fig.6.2. First of all, from topology level, [107] and [108] show traditional current source inverter and quasi-Z source inverter shown in Fig.6.3 (a) and (b), there is no need a large capacitor on the dc-side, however, the power loss and large inductor in dc-side are still issues to prevent their application.

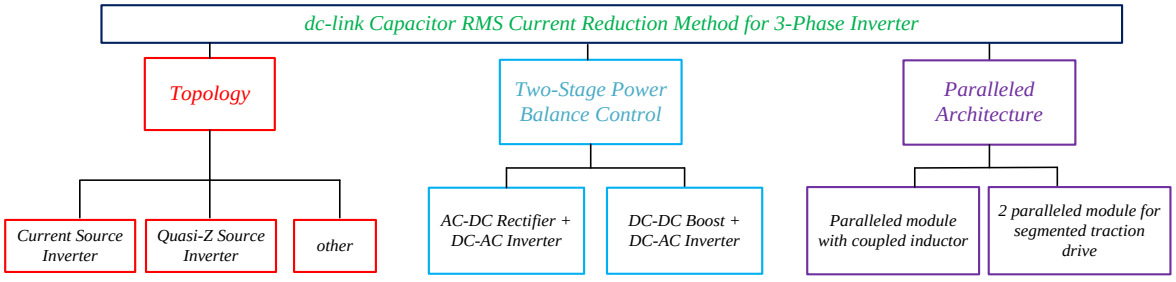


Figure 6.2. An overview diagram for 3-phase dc-link capacitor RMS current reduction technologies

From now on, most papers are focused on system level solution. [109]-[112] show the traditional two-stage converter system, normally, AC-DC plus DC-AC or DC-DC plus DC-AC shown in Fig.6.4 (a) and (b), respectively. For two-stage system, the main solution idea is to reduce the second stage dc-side current ripple by using the first stage converter dc output current ripple. With special and complex control [109]-[112], or fix the switching frequency relationship between two stages [112], the dc-link current ripple can be significantly reduced. However, this kind of method is quite limited to its system structure.

It is widely used to reduce 3-phase inverter dc-link capacitor RMS current by interleaving method for paralleled inverter system. The RMS value of dc-link capacitor is depend on the carrier waveform and its phase-shifted angle. Normally, carrier phase-shifted method is widely used in multilevel application [113]-[116]. [117]-[122] focus on interleaving scheme or phase-shifted carrier PWM technique to reduce the RMS value. [117] investigates both tri-angle and saw-tooth control methods. [120] shows RMS reduction with 2 inverters in-parallel under different load conditions. However, the relationship between RMS current value and N module in-parallel is not given. There is few papers to give a full analysis on how to reduce dc-link capacitor by adding inverter module number and how many modules can achieve the whole system highest power density. This is because introducing the inverter module also increases the whole system volume, although dc-link capacitance is reduced. So this paper pays more attention on these parts compared with the existing papers.

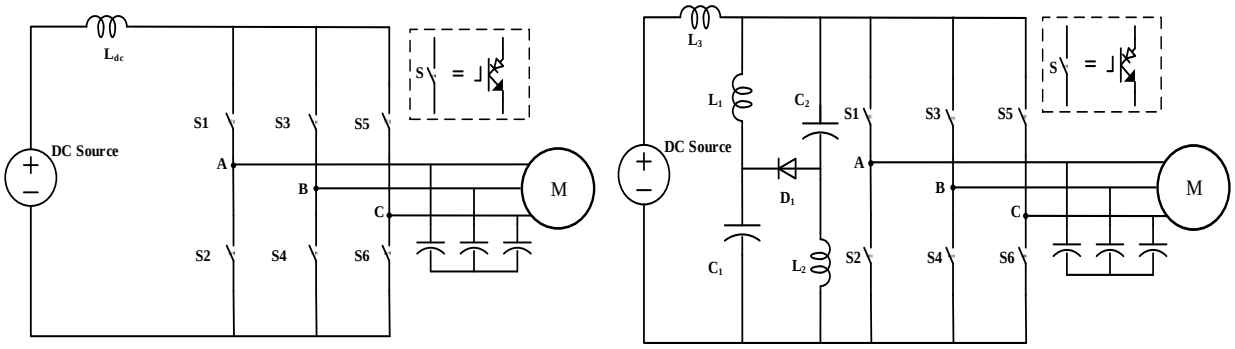
C. Discussion on 3-phase inverter system-level architecture and interleaving methods

For 3-phase dc-link capacitor RMS reduction, some papers look for other methods from the system-level architecture. [117], [125]-[126] reduce RMS value with special interleaving method by using 2-module paralleled inverter to drive one segmented motor shown in Fig.6.5 (a).

The motor needs to be specifically designed with 2 windings. Also, [123]-[125] use 2-module paralleled inverters with coupled inductor connected to the traditional motor shown in Fig.6.5 (b). This method introduced the extra coupled inductor to reduce dc-link capacitance. In a word, both methods need to connect 2-module inverters in-parallel with interleaving. Actually, this architecture with several inverters are trend to be connected in a paralleled manner for power density, power rating and reliability consideration in the industry application.

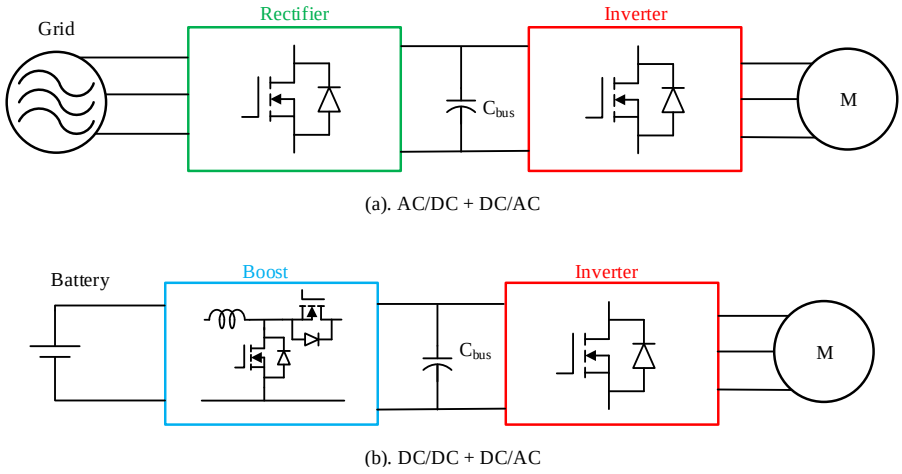
For paralleled inverters used in segmented drive application, [117] just give two modules with interleaving methods. If the paralleled module number continues to be increased, the relationship between module number and power density of the whole system is talked little. So this paper is focused on the relationship between paralleled module number and the dc-link capacitor RMS current value. Furthermore, the method by increasing paralleled module number is fully investigated under SPWM, SVPWM, and DPWM1 with both tri-angle and saw-tooth carrier control schemes, respectively. Also, the power factor effect is briefly investigated when the module number is increased.

The paper is organized as follows. In section II, the proposed method is given and explained. Some basic equations will be derived for N-paralleled inverters application. In section III, analysis and simulation results will be provided under both tri-angle and saw-tooth with SPWM, SVPWM and DPWM1, respectively [97]. Reducing RMS current value through adding inverter module will also be introduced and compared. Besides, the power factor effect on the proposed method is further investigated under SPWM with tri-angle control scheme. In section IV, the system volume and cost are briefly evaluated. Furthermore, experimental results will be presented in section V. Finally, the conclusion of this paper is given in last part, section VI.



(a) Traditional current source inverter (b) Quasi-Z source current source inverter

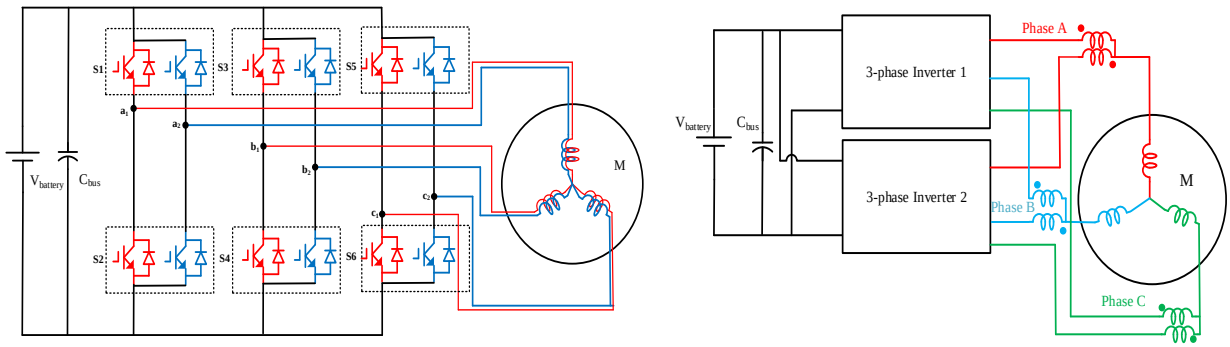
Figure 6.3. Topology solution for 3-phase dc-link current reduction



(a). AC/DC + DC/AC

(b). DC/DC + DC/AC

Figure 6.4. Two-stage structure solution for 3-phase dc-link current reduction



(a) Segmented architecture (b) Coupled inductor architecture

Figure 6.5. Paralleled 3-phase inverter system architecture

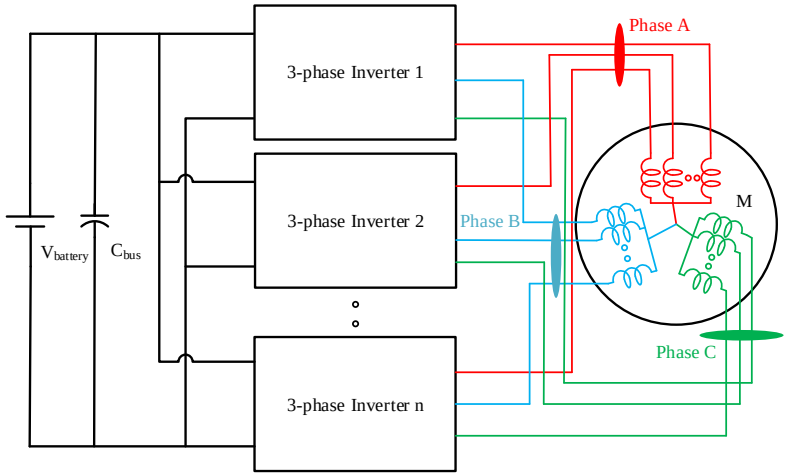


Figure 6.6. The proposed N-module paralleled 3-phase inverter system architecture for segmented traction drive

6.2. Description of Increasing Module Number Method

The proposed method is an extend research based on [117] for segmented traction drive application. Unlike [117]'s interleaving method with 2 modules in-parallel to reduce RMS current, this paper is focused on increasing module number to further reduce RMS current value. The proposed N-module in-parallel architecture is defined shown in Fig.6.6. Ideally, N module inverters are in-parallel to drive one special motor with N windings. In order to investigate how the module number affects the dc-link capacitor RMS value. A series of simulation with different module number from N=1 to N=6 is demonstrated to show how the increased module number affects dc-link capacitor RMS value. Then some explanation is given to prove how the RMS current is reduced by increasing the paralleled module number. Finally, an interleaving control method for different module number is briefly analyzed in theory although it is well known.

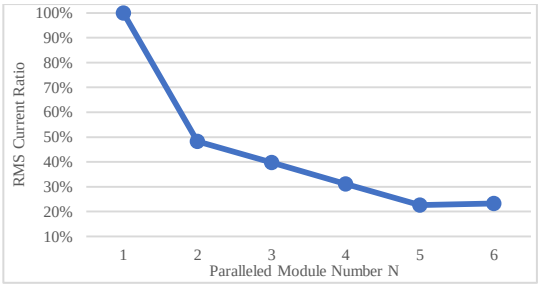


Figure 6.7. Normalized dc-link capacitor RMS current vs N paralleled inverters under different module number

Fig.6.7 shows the normalized dc-link capacitor RMS current value is affected by the paralleled module number under SPWM with tri-angle control scheme. The ordinate value stands for the RMS current ratio, which is defined each of dc-link capacitor current RMS value from N=1 to N=6 over that of N=1. From the results, it is obvious that increasing the paralleled module number with interleaving method can significantly further reduce the capacitor RMS current compared with just 2 modules in-parallel. The key current waveforms from N=1 to N=6 are shown in Fig.6.8 to Fig.6.13 together with their dc-link capacitor current's double Fourier spectrum. The key parameters are shown in Table.6.1. The output phase RMS current are kept the same value at 254.5A. When the paralleled module number is increased, all the modules share the total output phase current. DC-link capacitor RMS current values are 128A with 1 module, 61.7A with 2 modules, 50.9A with 3 modules, 39.9A with 4 modules, 29A with 5 modules and 29.3A with 6 modules. The RMS current reduction will come to a limit when module number is increased to 6. The spectrum for each module's dc-link RMS current show that the dc-link RMS current consists of its multiple integer switching frequency components and their side-band frequency components. Increasing paralleled inverters can significantly reduce these components. The magnitude of the dc-link capacitor current for all the spectrum components are reduced obviously in comparison from Fig.6.8 to Fig.6.13. As the time domain analysis like [96] is hard for paralleled inverter

architecture, double Fourier analysis with complex equations will be adopted to do some analysis on N-module paralleled inverters architecture in theory.

Table 6.1. Key parameters in the proposed circuit

Parameters	Value	Parameters	Value	Parameters	Value
V_{in}	400V	L_s	5uH	C_{bus}	1mF
PF	0.9	I_{phase_total}	200A	ESR	1mΩ
f_s	20kHz	$Module$	1-6	P_o	12kW

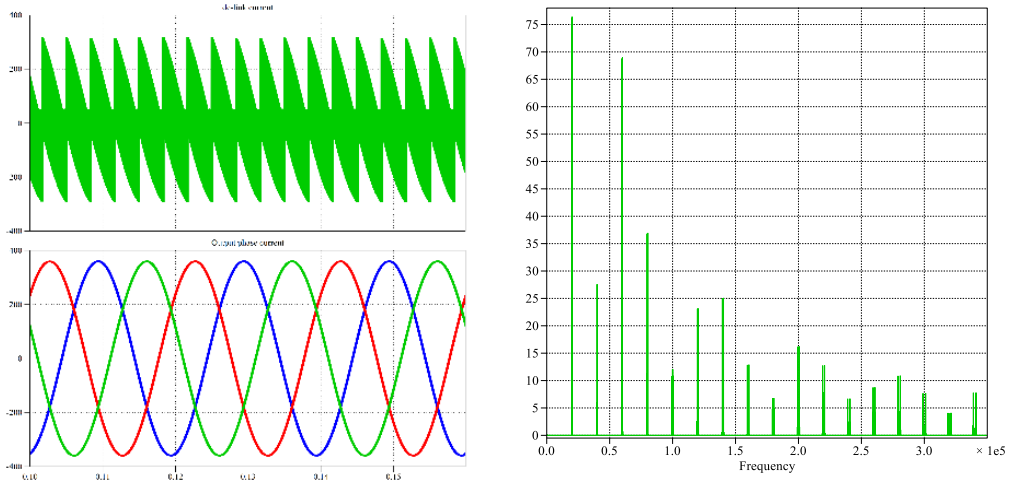


Figure 6.8. DC-link capacitor RMS current and phase current (128A, 254.5A) waveform under 1 inverter SPWM-Tri-angle

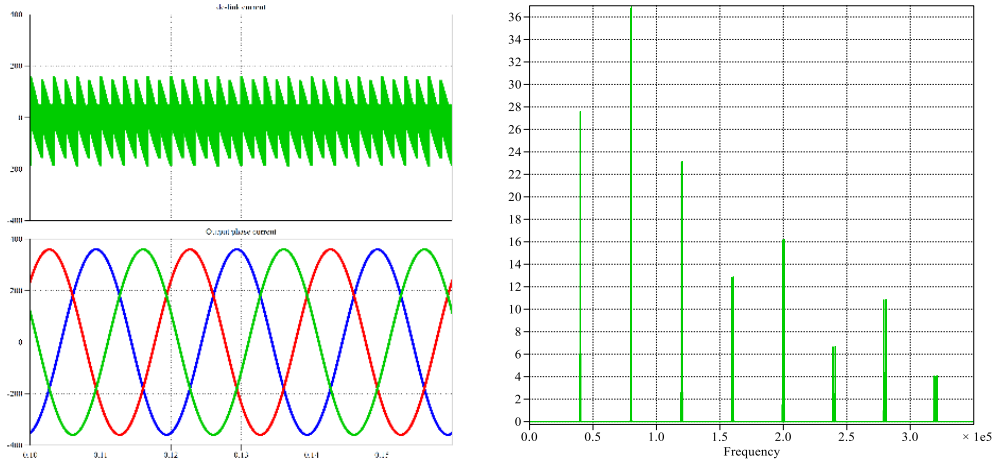


Figure 6.9. DC-link capacitor RMS current and phase current (61.7A, 254.5A) waveform under 2 inverters SPWM-Tri-angle

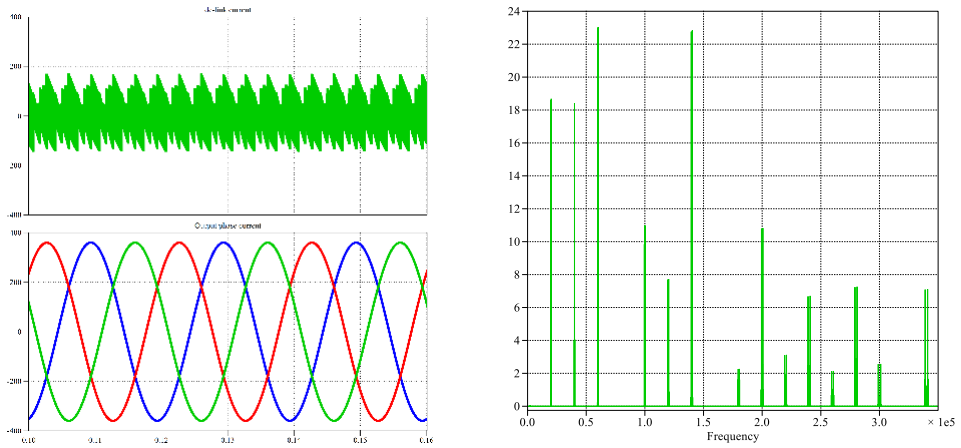


Figure 6.10. DC-link capacitor RMS current and phase current (50.9A, 254.5A) waveform under 3 inverters SPWM-Tri-angle

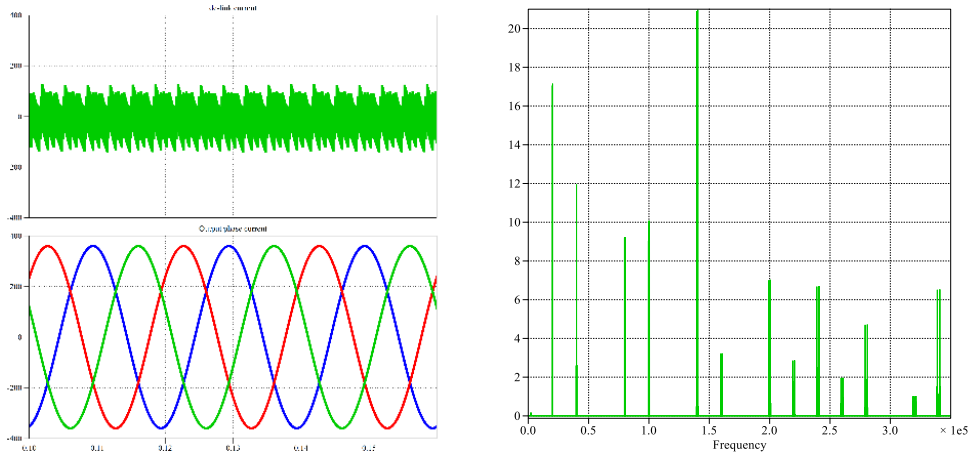


Figure 6.11. DC-link capacitor RMS current and phase current (39.9A, 254.5A) waveform under 4 inverters SPWM-Tri-angle

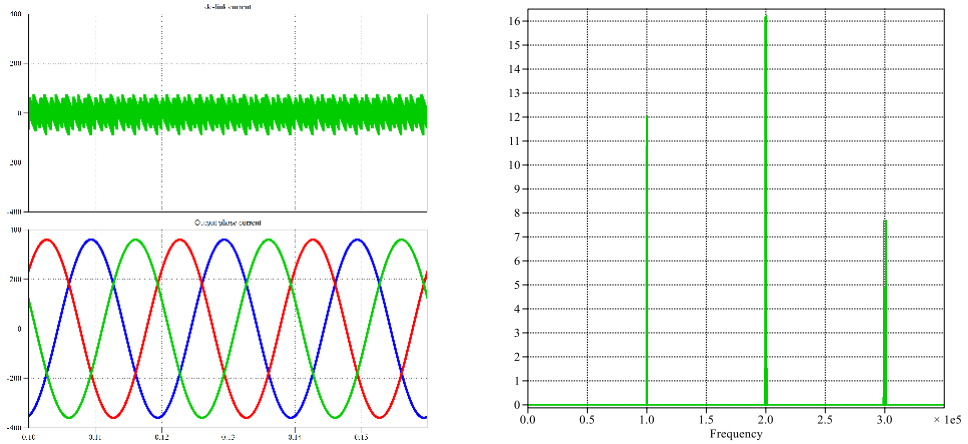


Figure 6.12. DC-link capacitor RMS current and phase current (29A, 254.5A) waveform under 5 inverter SPWM-Tri-angle

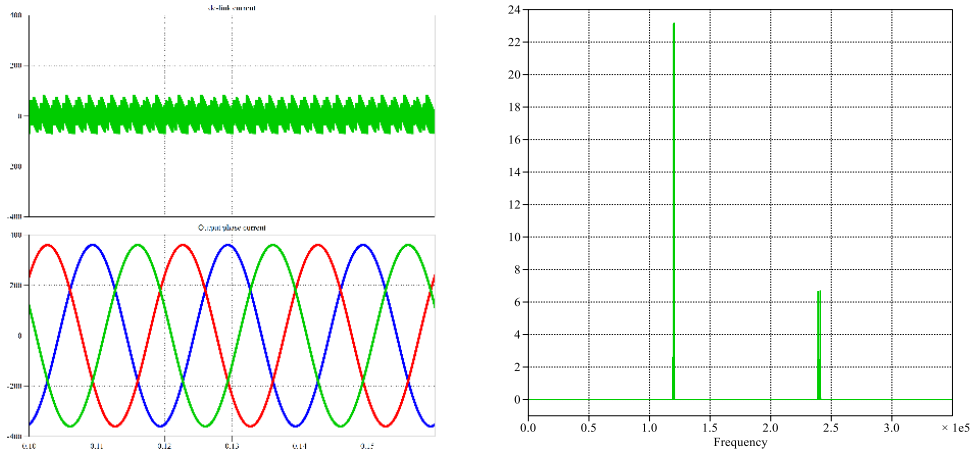


Figure 6.13. DC-link capacitor RMS current and phase current (29.3A, 254.5A) waveform under 6 inverter SPWM-Tri-angle

Based on [98], SPWM control method with triangle carrier waveform in 3-phase inverter system is analyzed as follows, the analysis method is also suitable for other control methods. Easily, the current through the dc-link capacitor can be got as follow for one 3-phase inverter [106].

$$i_c(t) = \frac{3M}{4} I_o cos\emptyset + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [A_{mn} \cos(m\omega_c t + n\omega_o t) + B_{mn} \sin(m\omega_c t + n\omega_o t)]$$

(Eq. 6.1)

where I_o is the phase output current, $\cos\emptyset$ is the power factor, M is the modulation index, ω_c is the angle frequency of carrier waveform and ω_o is the output fundamental angle frequency. A_{mn} and B_{mn} could be defined shown in [72].

Then after some combination and remove the DC component, the ac current ripple current in one 3-phase inverter is shown in (Eq. 6.2).

$$i_{c\_ac}(t) = \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} [I_{m,n} \cos m(\omega_c t + \theta_c) + n\omega_o t + \varphi_{m,n})] \qquad \text{(Eq. 6.2)}$$

where θ_c is the carrier shifted angle and $\varphi_{m,n}$ is phase angle of different harmonics. When N inverters are in parallel. Assuming that all the inverters in parallel are in the same operating conditions and they have the same different orders harmonics as follow,

$$\emptyset(m,n) = m\omega_c t + n\omega_o t + \varphi_{m,n} \quad \text{(Eq. 6.3)}$$

Then when *N* modules 3-phase inverters are all in parallel and one dc-link capacitor is shared, the ac current ripples are all summed up together. The total ac current ripple can be got in (Eq. 6.4).

$$i_{c_{sum_{ac}}}(t) = i_{c1_{ac}}(t) + i_{c2_{ac}}(t) + \cdots + i_{cn_{ac}}(t)$$

$$= \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} I_{m,n}[\cos(\emptyset + m\theta_{c1}) + \cos(\emptyset + m\theta_{c2}) + \cdots + \cos(\emptyset + m\theta_{cn})] \quad \text{(Eq. 6.4)}$$

Assuming that for the *N* (*N*>1) multiple inverter system, *N*+1 and *N* inverter carrier shifted angle is all the same value σ and the first one is assuming that $\theta_{c1} = 0$. Then we can get (Eq. 6.5)

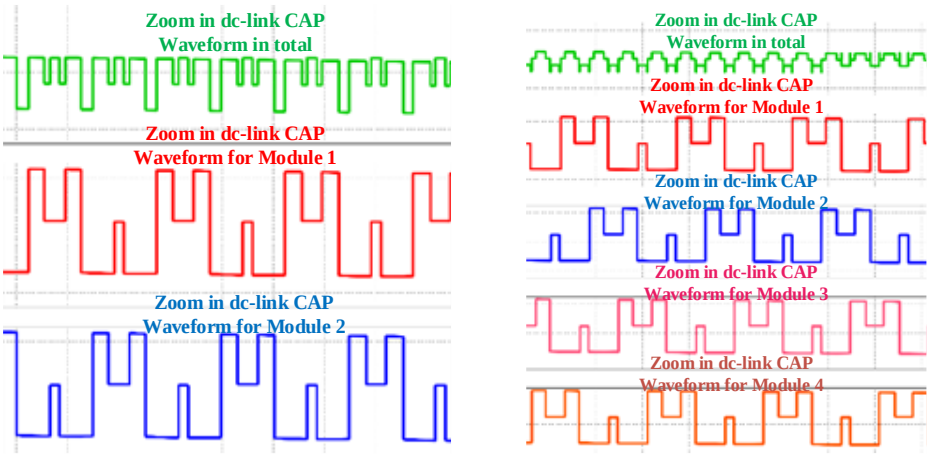
$$i_{c\_sum\_ac}(t) = \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} I_{m,n}[\cos(\emptyset) + \cos(\emptyset + m\sigma) + \cdots + \cos(\emptyset + m(n-1)\sigma)]$$

(Eq. 6.5)

In conclusion, based on the (Eq. 6.5), the optimal interleaving angle can be got shown in (Eq. 6.6) to cancel the DC-link current ripple where n stands for the number of inverters in parallel. *m* determines m^{th} order harmonic of carrier waveform. From (Eq. 6.6), although all the current ripple cannot be avoided, the 1st or 2nd order harmonics occupies a dominant. Thus, the optimal interleaving angle can cancel large part of RMS value, especially when *m*=2 for triangle carrier waveform.

$$\sigma = \frac{2\pi}{mN} \quad \text{(Eq. 6.6)}$$

In general, all the m^{th} orders harmonic components cannot be cancelled out by simply interleaving one particular angle under certain number modules in-parallel. Like 2 modules in-parallel [87], 180° angle shift for 2-modules in-parallel can just reduce some domain frequency components. However, increasing module number, such as 4-modules in-parallel, more domain frequency components can be cancelled out based on equation (Eq. 6.4) and (Eq. 6.5). In a results, the total RMS current will be further reduced.



(a). 180 degree shifted for 2 modules (b). 90 degree shifted for 4 modules

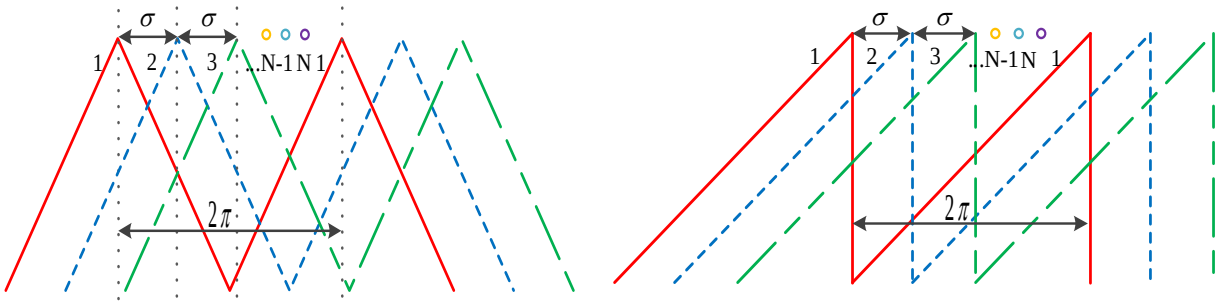
Figure 6.14. DC-link capacitor RMS current waveform under 2 modules and 4 modules with SPWM, tri-angle control scheme

Besides frequency domain analysis above, time domain waveforms based on PLECS simulation are also shown for easy understanding. Fig.6.14 (a) and (b) show the optimal interleaving angle under 2 modules and 4 modules respectively, both with tri-angle and SPWM. The first green waveform stands for the total dc-link current and the others show each module's dc-link current waveform. As is well known, when module number is equal to two, the optimal interleaving angle is 180° and similarly, the module number is equal to four, the optimal interleaving angle is 90°. The relationship between optimal interleaving and the module number is obvious. However, for 4-modules in-parallel, the total current RMS value is much less than that of 2-modules. This is because more pulse current will be eliminated when the modular number is increased.

6.3. Simulation Results

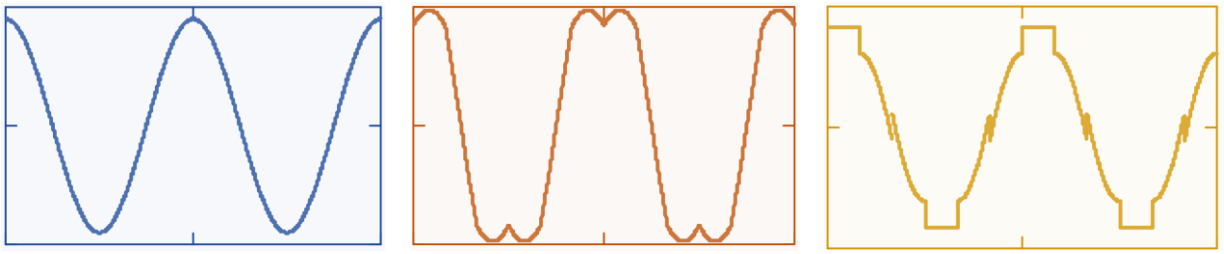
The definition of carrier waveform for interleaving control scheme are shown in Fig.6.15. Also, the definition of carrier waveform for interleaving control scheme are shown in Fig.6.16.

Groups of simulation with PLECS have been designed to verify the relationship between increasing module



(a) Tri-angle (b) Saw-tooth

Figure 6.15. Definition of carrier waveform for interleaving control scheme in N paralleled module inverters



(a) SPWM (b) SVPWM (c) DPWM1

Figure 6.16. Modulation waveform with SPWM, SVPWM, DPWM1, respectively

Number and dc-link RMS current under the optimal interleaving angle. When increasing the paralleled module number, the dc-link capacitor RMS value is significantly reduced.

The carrier waveform is used with triangle, saw-tooth, respectively. When the carrier is used triangle, the dc-link capacitor current is like two pulse waveform. On the contrary, when the carrier is set saw-tooth, the current is shown as one pulse waveform. The modulated is investigated SPWM (sinusoidal pulse width modulation), SVPWM (space vector pulse width modulation) and DPWM1 (discontinuous pulse width modulation), respectively, shown in Fig.6.16. And switching frequency is set at 20k Hz, dc-link voltage is 400V with stray inductance 5uH. The dc-link capacitor is chosen 1mF with ESR (equivalent series resistance) 1mΩ. The detail parameters are

shown in Table.6.1. The control scheme is triangle/saw-tooth with SPWM, SVPWM, and DPWM1's combination. The load is a resistor with an inductor and the power factor is adjusted at 0.9.

Fig.6.17 to Fig.6.26 all show the relationship among dc-link capacitor current RMS value, modulation index, and interleaving angle, paralleled inverter module number. Unlike other traditional papers' concern, this investigation is focused on the relationship between the inverter paralleled module number and dc-link capacitor RMS current value. The ordinate value current RMS ratio shown in from Fig.6.17 to Fig.6.26 is defined the different dc-link capacitor current RMS value over the RMS under the zero point, which means the carrier shifted angle is zero.

From Fig.6.17 to Fig.6.21, it shows the paralleled module number from 2 to 6, with triangle carrier waveform. From Fig.6.22 to Fig.6.26, it shows module number from 2 to 6, with saw-tooth carrier waveform. Each column, from left to right, stands for SPWM, SVPWM and DPWM1, respectively. The optimal interleaving angle is almost matched with the equation derived above. The interesting thing is the RMS current is reduced when the paralleled module number is increased. For one particular paralleled module number, SPWM and SVPWM are better than DPWM1 for reducing the dc-link capacitor RMS current value. Also, for 2 modules, the reduction is ~50% at this working point; 3 modules with ~58% reduction; 4 modules with ~66% reduction; 5 modules with ~70% reduction and 6 modules with ~75% reduction. Compared with the tri-angle control scheme, saw-tooth control scheme in general have a better performance on reducing the dc-link capacitor RMS current value. In details, for 2 modules, the reduction is ~53% at this working point; 3 modules with ~63% reduction; 4 modules with ~70% reduction; 5 modules with ~78% reduction and 6 modules with ~81% reduction.

Finally, based on plenty of simulation and analysis above, the curve between paralleled module number and dc-link capacitor RMS current under different modulation index can be drawn shown. The figures prove that increasing the paralleled modules can be applied in different control schemes. Control schemes and modulation index have a little effect on the RMS current reduction. The trend for reducing the dc-link capacitor RMS current value is the similar.

SPWM SVPWM DPWM1

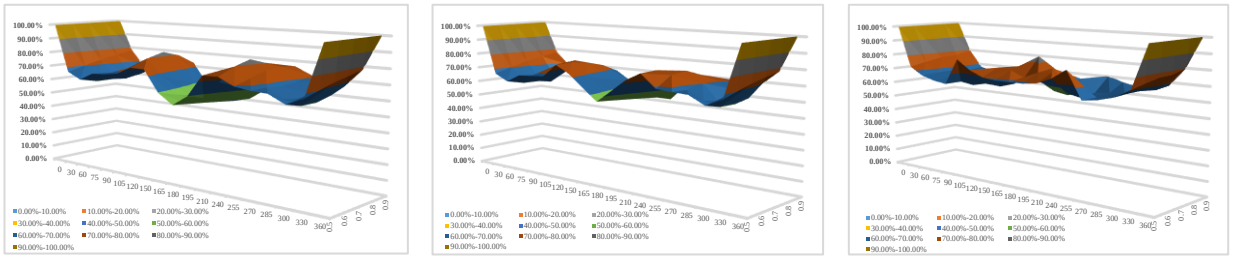


Figure 6.17. RMS current ratio vs carrier shifted angle & Modulation Index with N=2, triangle

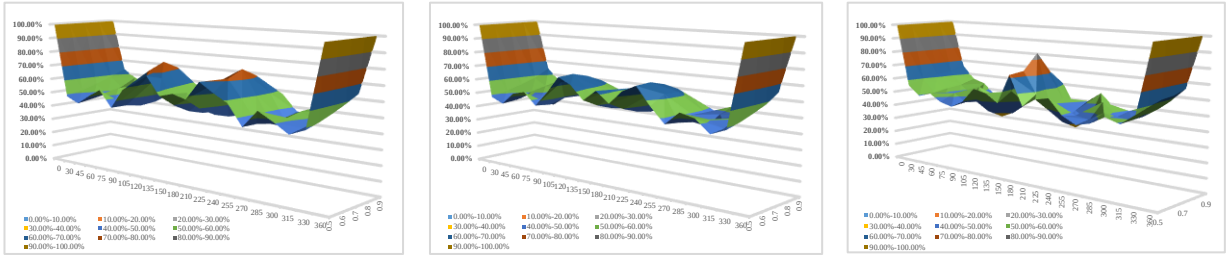


Figure 6.18. RMS current ratio vs carrier shifted angle & Modulation Index with N=3, triangle

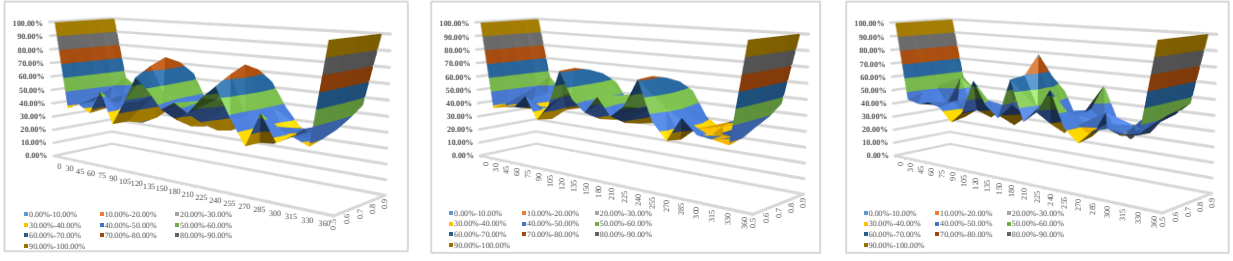


Figure 6.19. RMS current ratio vs carrier shifted angle & Modulation Index with N=4, triangle

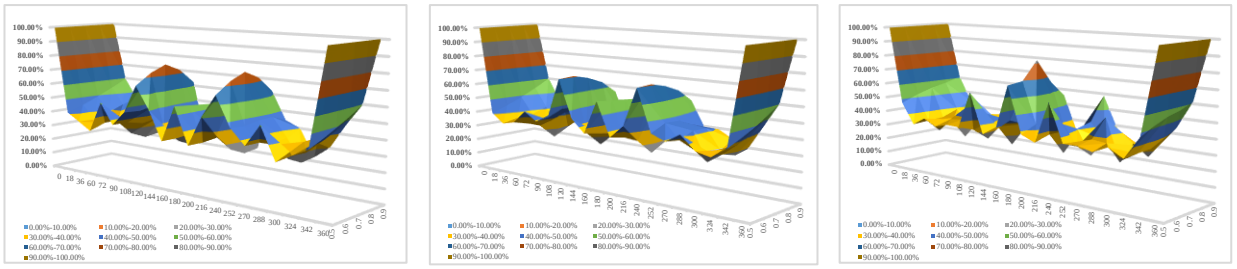


Figure 6.20. RMS current ratio vs carrier shifted angle & Modulation Index with N=5, triangle

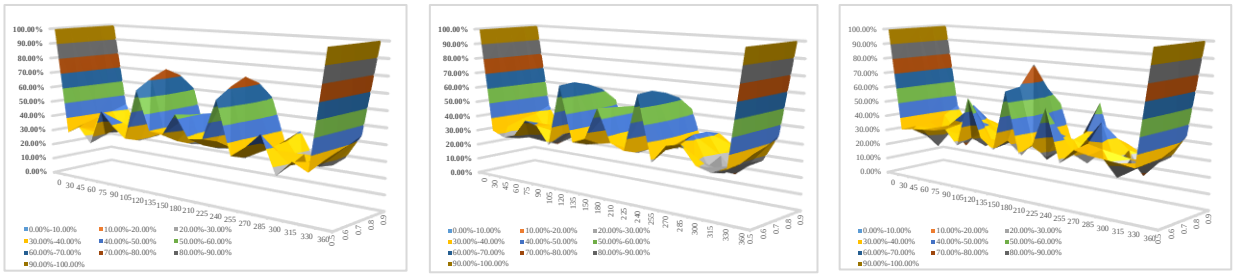


Figure 6.21. RMS current ratio vs carrier shifted angle & Modulation Index with N=6, triangle

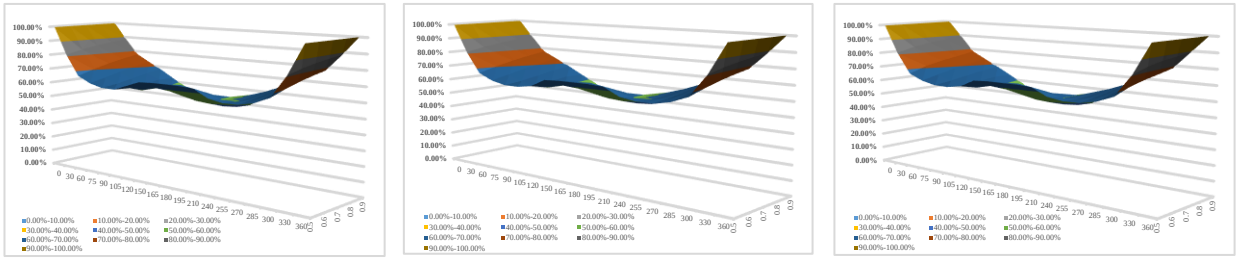


Figure 6.22. RMS current ratio vs carrier shifted angle & Modulation Index with N=2, saw-tooth

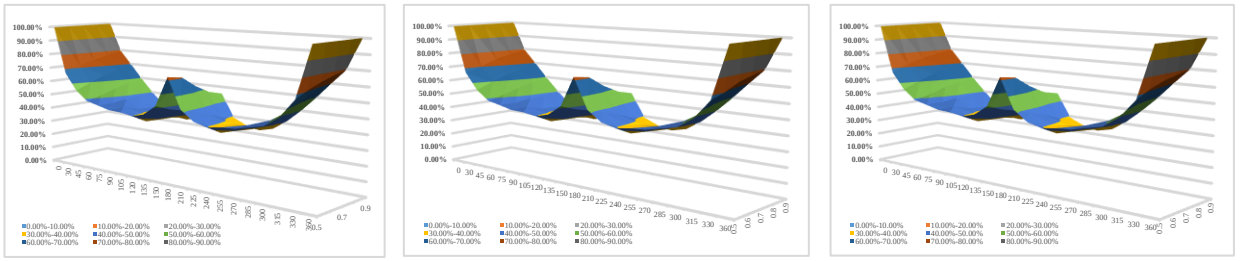


Figure 6.23. RMS current ratio vs carrier shifted angle & Modulation Index with N=3, saw-tooth

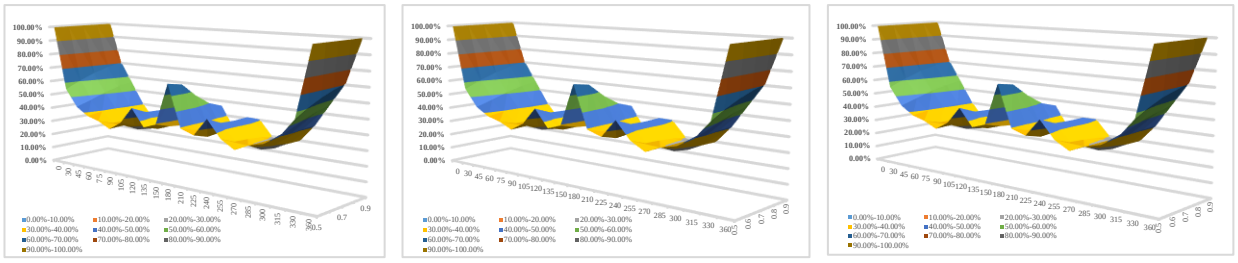


Figure 6.24. RMS current ratio vs carrier shifted angle & Modulation Index with N=4, saw-tooth

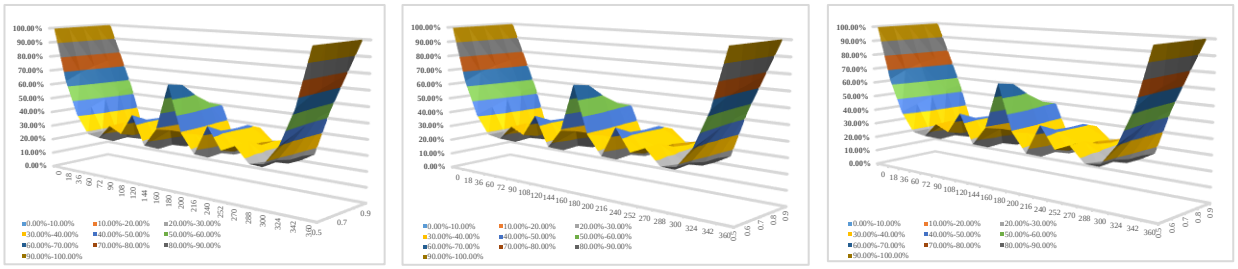


Figure 6.25. RMS current ratio vs carrier shifted angle & Modulation Index with N=5, saw-tooth

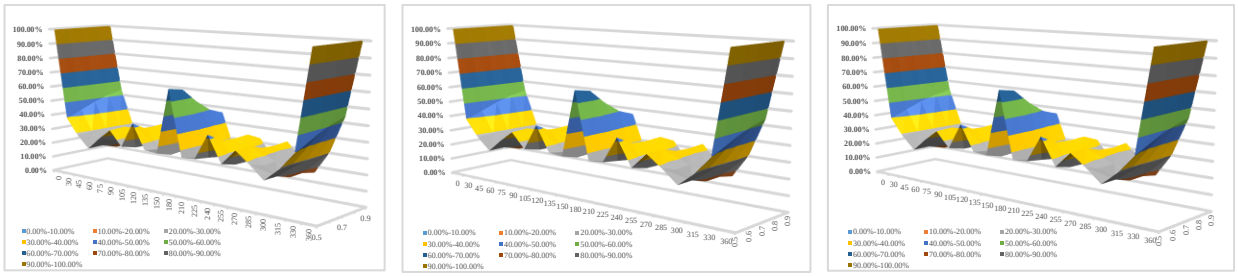
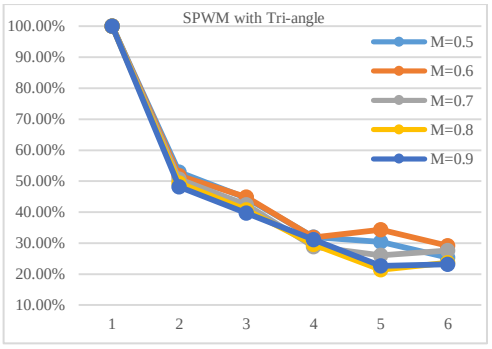


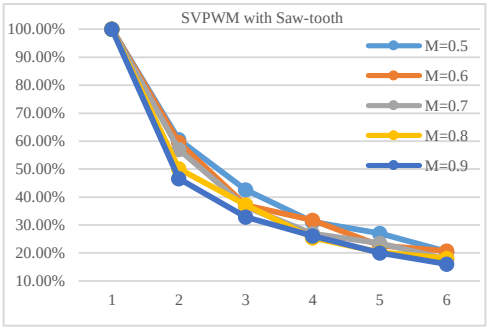
Figure 6.26. RMS current ratio vs carrier shifted angle & Modulation Index with N=6, saw-tooth

In conclusion, increasing the paralleled modules can reduce the dc-link capacitor RMS current value significantly. And this method is applied in SPWM, SVPWM and DPWM1 with both tri-angle and saw-tooth control schemes. Furthermore, in general SPWM and SVPWM has better performance than DPWM1 on reducing the RMS current. The saw-tooth control scheme has a 5% on average improvement on reducing the RMS current, which is better than the tri-angle control scheme.

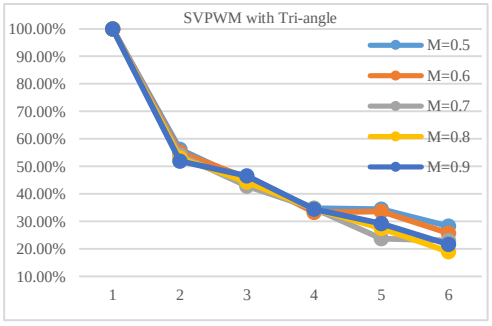


(a). SPWM with Tri-angle

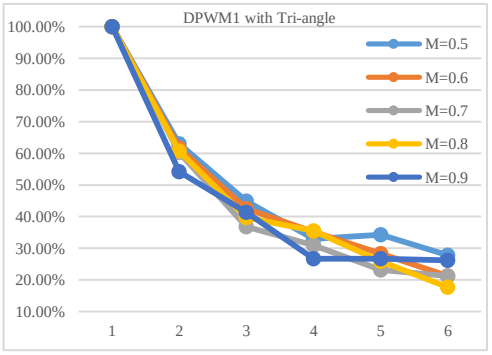
(b). SPWM with Saw-tooth



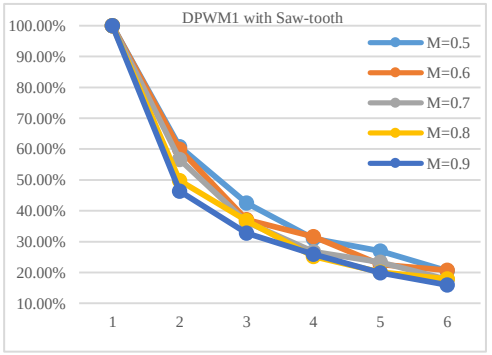
(c). SVPWM with Tri-angle



(d). SVPWM with Saw-tooth



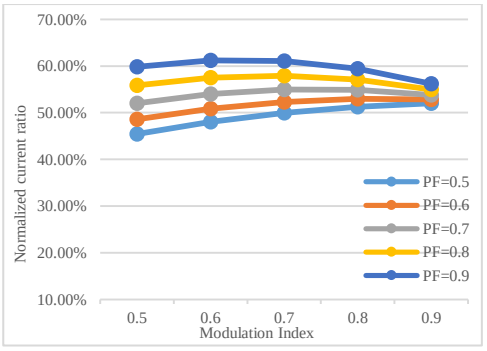
(e). DPWM1 with Tri-angle



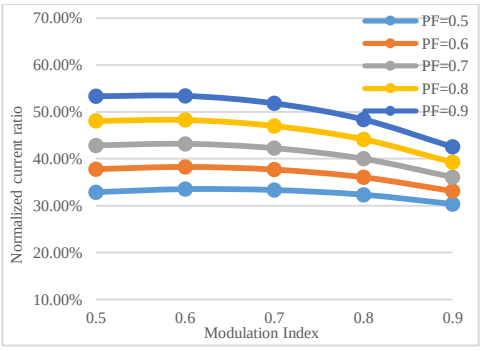
(f). DPWM1 with Saw-tooth

Figure 6.27. Normalized dc-link capacitor RMS current vs N paralleled inverters under different modulation types

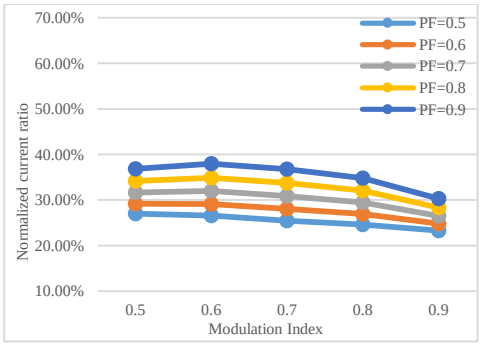
Furthermore, under different power factor, how the dc-link capacitor RMS current value changes is investigated under SPWM with tri-angle control scheme shown in Fig.6.28 (a)-(f). The normalized



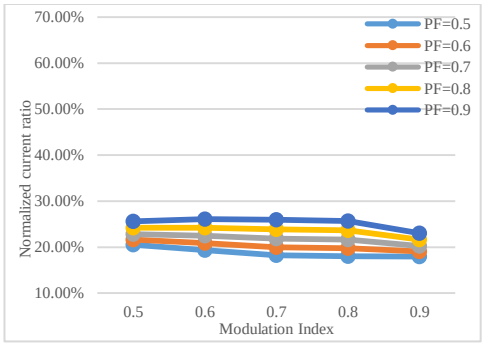
(a). 1 Module



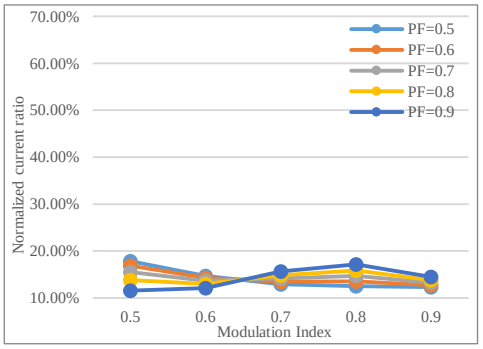
(b). 2 Modules



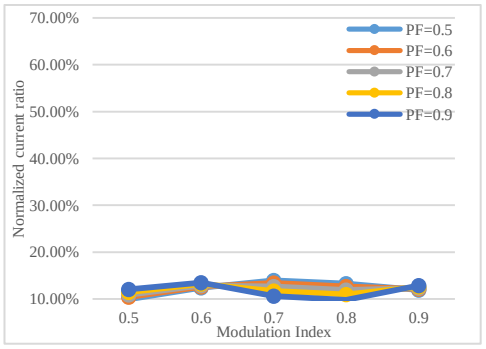
(c). 3 Modules



(d). 4 Modules



(e). 5 Modules



(f). 6 Modules

Figure 6.28. Power factor effect on different paralleled module number

Current ratio is defined as the RMS current going through dc-link capacitor over the RMS value of output phase current. The power factor ranges from 0.5 to 0.9 and modulation index is changed from 0.5 to 0.9. From the figures, we can see that when the paralleled module number is increased, the ratio is decreased, which proves that increasing module number can reduce dc-link capacitor RMS current value. Under certain paralleled module number, for example, 3 paralleled

module inverters, when the power factor increases, the RMS current value increases. When modulation index is equal to certain value, the RMS value is maximum shown in Fig.6.1. However, unlike one module situation [58], for paralleled module inverters, it is not applicable.

In conclusion, the RMS current through dc-link capacitor can be significantly reduced by increasing the paralleled number. When the paralleled inverter module number is increased, the RMS current is reduced. Furthermore, it has a limited reduction when module number is equal to 5 or 6, depending on different control methods. Also, under different number paralleled modules, the relationship among dc-link capacitor RMS value, modulation index, power factor is further investigated. Increasing paralleled inverter module number can really reduce the value of the dc-link capacitor, which makes the whole system high power density. However, increasing paralleled inverter module is also introduced the extra volume, with extra modules, gate driver and power supply. So the total volume of the whole system needs to be investigated to find an optimal module number. It will be shown in the next part.

6.4. Comparison Evaluation of System Volume and Cost

Although the dc-link capacitor current RMS value can be significantly reduced by increasing the paralleled module number. However, this methods also introduced extra volume, such as module itself volume, extra gate driver and power supply. So this section is to give a brief comparison on the whole system volume.

Products, it is not easy to give a standard line. As the module is depend on different manufactory and different power rating. Here just give two examples. The output phase current is assuming 200A and the dc voltage rating is chosen at 600-650V level. The first one is used with Fuji IGBT module size, consider the idea case that the IGBT paralleled power module can be packaged together. The volume is just related with the power rating. So ideally though the

paralleled module number is increased, the module size is the same under the same power rating. Fig.6.30 shows this ideal case. Fig.6.30 (a) shows the detail volume under 1-6 paralleled modules. The blue bar stands for the volume of dc-link capacitor.

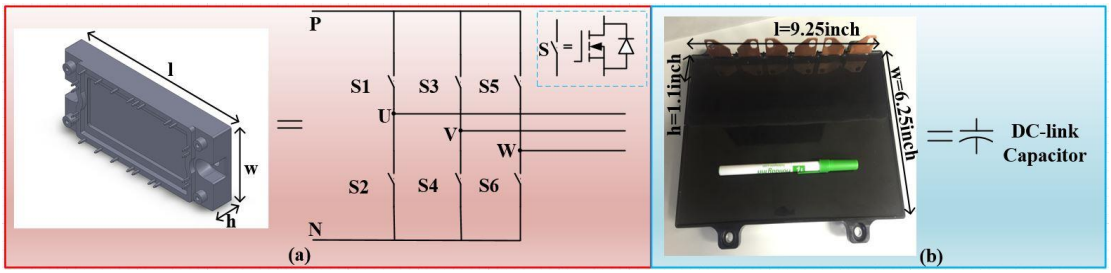


Figure 6.29. An example of commercial 6-pack IGBT module and dc-link capacitor

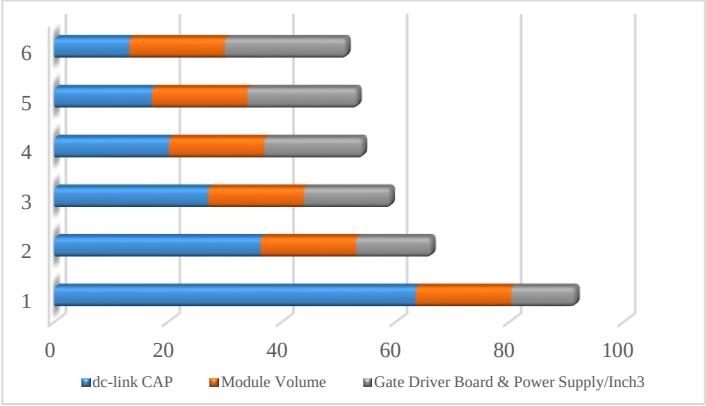


Figure 6.30. Ideal 6-pack volume comparison

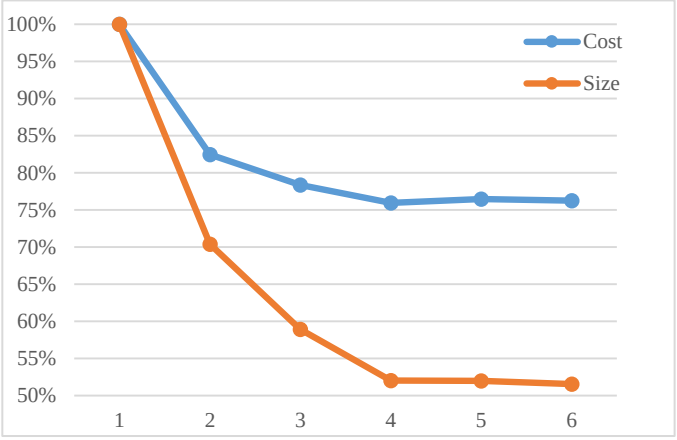


Figure 6.31. Normalized volume with module number

Fig.6.30 shows this ideal case. Fig.6.30 shows the detail volume under 1-6 paralleled modules. The blue bar stands for the volume of dc-link capacitor. It can be seen that when paralleled module number is increased, the size of dc-link capacitor is reduced. For dc-link capacitor, the ideal case is that under certain voltage level, the cost is related with the capacitor value. In the real case, it is known that Tesla used 14 TO247 packaged IGBT in-parallel. The total power module number is 84. The cost and power module size are constant and dc-link capacitor size and cost can be reduced with this method. The final size and cost curves are the similar trend .Also, the voltage ripple will be affected when the small-size capacitor is chosen, and however, based on the (Eq. 6.7), and the dc-link capacitor value is reduced while the AC current component value is also reduced. As a result, the dc-link voltage ripple has little effect with small capacitor.

$$V(\omega) = \sum \frac{I(\omega)}{\omega Cdc} \quad \text{(Eq. 6.7)}$$

The gate driver and its power supply will be increased not too much. This is because the driver board size is normally small and packaged together with IGBT module. For power supply board, the current rating of each inverter is divided, therefore, power supply board can be smaller although the module number is increased. The cost of driver board and power supply is related with size, the normalized cost curve can be drawn and shown in the figure together with the size evaluation shown in Fig.6.31.The detailed calculation equations are based on (Eq. 6.8) and (Eq. 6.9).

$$Volume = V_{module}(I) + V_{cap}(C_{dc-link}) + V_{other} \quad \text{(Eq. 6.8)}$$

$$Cost_{total} = Cost(V_{module}) + Cost(V_{cap}) + Cost(V_{other}) \quad \text{(Eq. 6.9)}$$

6.5. Experimental Results

A 3-phase 2kW inverter prototype is developed in this paper based on the analysis above. Finally, 3 modules of the prototype are made to verify the simulation results. Fig.6.32 shows the overview of test bench. As the number of control signals is as many as 18, the control board is set up with DSP and FPGA. The DSP is responsible for phase shift and carrier waveform shift and FPGA defines the dead time for each phase leg and generates 18 PWM signals for the 3 modules of inverters. Fig.6.33 (a) and (b) show the 3D prototype model for one-cell prototype. The power switching device here are chosen SiC MOSFET, STC2120AF from ROHM. One-module prototype size is 7.25×3.6×1.4 $inch^3$ and the power density of the prototype is about 55W/ $inch^3$.

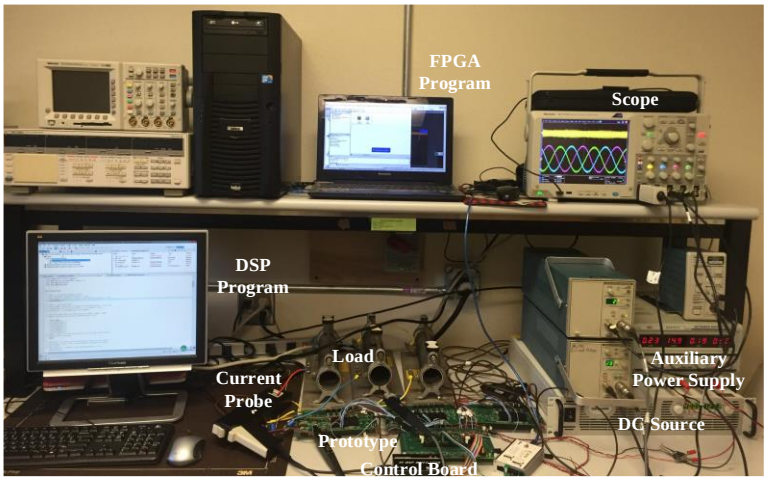


Figure 6.32. Overview of the test bench

Fig.6.34 (a) shows the digital PWM gate signal waveform for one module's 3-phase leg upper device. The control method is chosen SPWM with tri-angle control scheme to verify the proposed idea. The power factor is ~0.9 and modulation index is set at 0.8. Fig.6.35 (a)-(b) show 1 module, 2 modules, 3 modules with output current and dc-link capacitor current, respectively. The output peak current is 1A. The dc-link capacitor RMS current is 456mA, 370mA and 285mA under 1 module, 2 modules and 3 modules, respectively. And Fig.6.36 shows the comparison

between the simulation and experiments. The experimental results are higher than simulation, this is mainly because there are spikes current in the real experiments and also the power factor has a bit difference from the simulation. Although the experiments are verified 3 in-parallel modules, the curve trends to be similar with the simulation.

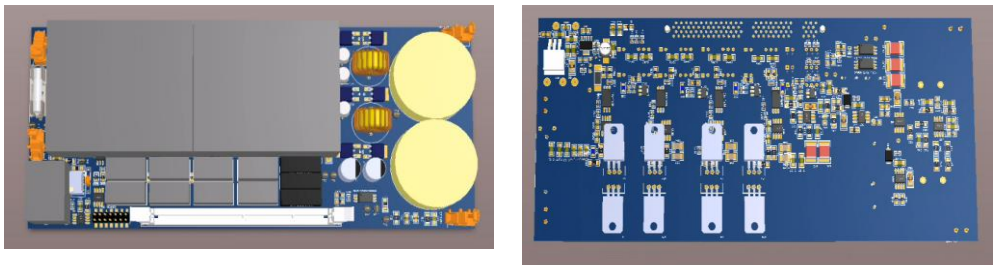


Figure 6.33. (a) Top view of one module 3-D prototype (b) Bottom view of one module 3-D prototype

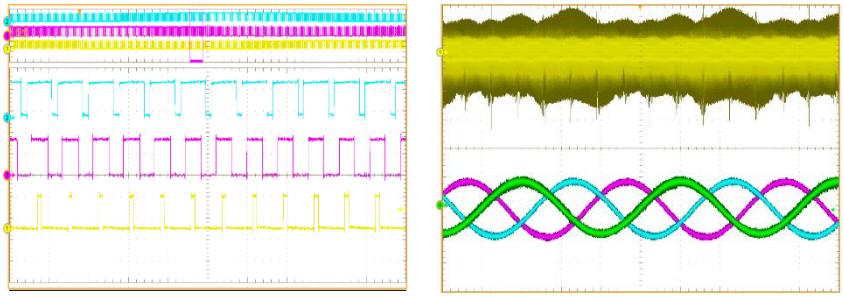


Figure 6.34. (a) Digital gate drive waveform under 20 kHz (2V/div), time scale: 2ms/div (b) 1 module dc-link capacitor current (0.5A/div) and output current (1A/div), time scale: 5ms/div

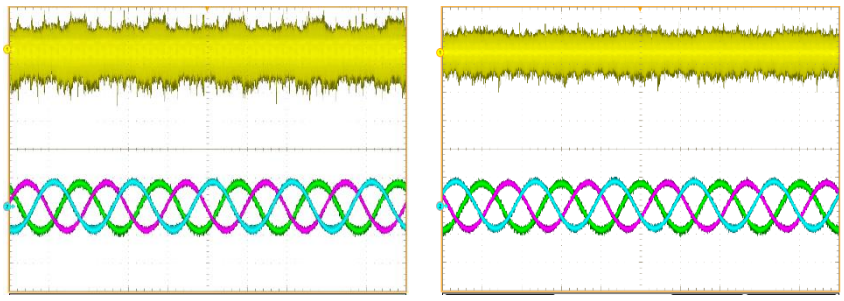


Figure 6.35. (a) 2 paralleled modules dc-link capacitor current (0.5A/div) and output current (1A/div), time scale: 10ms/div (b) 3 paralleled modules dc-link capacitor current (0.5A/div) and output current (1A/div), time scale: 10ms/div

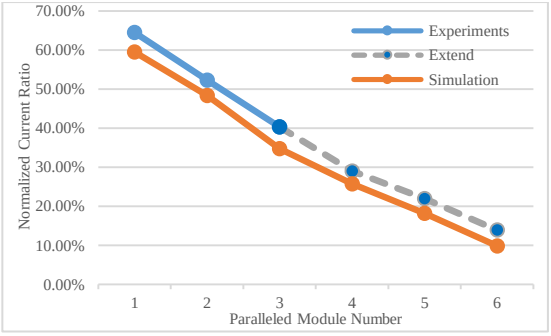


Figure 6.36. RMS current ratio comparison between the simulation and experimental results

So based on these three modules experiments, the extended evaluation is also drawn in the figure. In conclusion, the experimental results are almost consistent with the simulation results.

6.6. Conclusion

This paper presents a 3-phase dc-link capacitor RMS current reduction method by increasing paralleled inverter module number for segmented traction drive. A state of the art for how to reduce 3-phase dc-link capacitor RMS current is summarized in the introduction part. Compared with the existing 2-module paralleled system, this paper further investigates increasing paralleled module number can further reduce the value of dc-link capacitor RMS current. As different paralleled module number, the interleaving angle is total different. With basic double Fourier equation derivation, this interleaving angle for different paralleled module number is briefly analyzed in theory. Furthermore, it is fully investigated under SPWM, SVPWM, and DPWM1 with both tri-angle and saw-tooth carrier control schemes, respectively. A series of PLECS simulation model are built to verify the proposed idea. The simulation results show that although different control schemes have some effects on the dc-link capacitor RMS current, the current value can be significantly reduced by increasing the module number in-parallel. The proposed method can be applied in SPWM, SVPWM and DPWM1 with both tri-angle and saw-tooth control schemes. Furthermore, in general SPWM and SVPWM have better performance than

DPWM1 on reducing the RMS current. The saw-tooth control scheme has a 5% on average improvement on reducing the RMS current, which is better than the tri-angle control scheme.

Also, the power factor effect is investigated when the module number is increased. Finally, the results show that 2 paralleled modules can reduce ~45% and 3 paralleled modules with ~55% reduction, 4 modules with ~70% reduction, 5 modules with ~75% reduction, 6 modules ~80% reduction, respectively, with the proper interleaving control schemes.

Besides, as paralleled inverter modules are introduced extra volume for the whole system, examples of volume evaluation are given based on the commercial IGBT 6-pack module. The results show that when the paralleled module number is selected at 3 or 4, the whole system can achieve the highest power density. This is mainly because increasing the module number comes to a limit reduction for the dc-link capacitor when the paralleled module number is larger than four modules. Finally, 3 modules of 2kW-prototype. The experiments are conducted at 1 module, 2 paralleled modules and 3 modules to verify the simulation. Finally, the experimental results are almost consistent with the simulation results and the trend to 4, 5 and 6 modules are also matched with the simulation results.

7. SWITCHED-TANK CONVERTER FOR 48V DATA CENTER APPLICATION

7.1. Introduction

Nowadays, as cloud computing and big data are more and more popular, energy consumed in data center application continues to increase significantly these years. According to the data center energy usage report [128], the electricity use for U.S. data center will achieve 73 billion kWh in 2020, which will be over 1.8% of total U.S. electricity consumption. Moreover, power supply and other site infrastructure take more and more space. The percent of servers housed in hyperscale data centers will grow linearly from 0% in 2005 to 40% in 2020.

As introduced above, traditional data center power architecture with 12V-bus design is not efficient and bulky. In order to reduce the heavy bus-bar loss and achieve high-efficiency, industry leaders, such as Google [129], proposed higher voltage distribution bus architecture named 48V-bus power architecture shown in Fig.7.1. 48V-bus power architecture can not only reduce bus-bar loss significant but also eliminate the online UPS and related cables. Instead, a local DC UPS with 48V backplane can be added in the novel 48V-bus power architecture. Besides lower loss on the bus, the transient response of the load has less effect on the bus voltage, as well as less effect on the other loads.

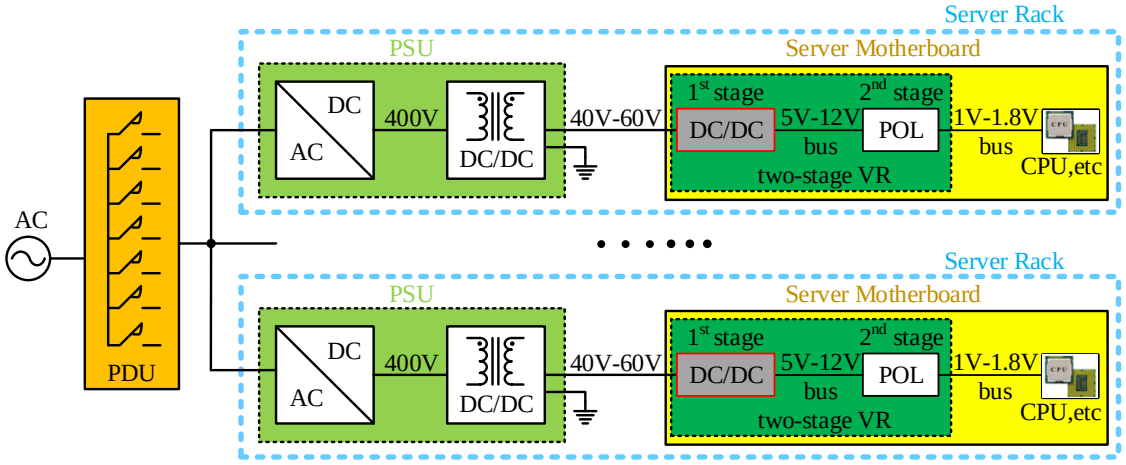


Figure 7.1. Two-stage voltage regulator (VR) architecture for data center application

As all the processor and memory devices are powered from 48V-bus, the 48V voltage regulator (VR) on the server motherboard needs to be significantly designed with high-power-density and high-efficiency. Thus, 48V-bus power architecture can achieve its full benefits when compared with 12V-bus power architecture. Actually, lots of works have been done for the 48V VR.

In general, the structure of 48V bus to point of load (PoL) can be basically summarized into single-stage structure and two-stage structure. One-stage interleaved Quasi-Square-Wave (QSW) VR is proposed in [130]. The power density is low and its efficiency is not high. In other work [131], the push-pull forward converter with integrated magnetics presents good performance. However, when the switching frequency is pushed too high, the efficiency drops a lot. 1MHz self-driven ZVS full-bridge converter is proposed in [132]. The proposed method achieve an efficiency improvement of 4.7% when compared with conventional full-bridge converter. A Resonant LLC VR is proposed in [133] and the drawback of this converter is low efficiency at light load condition. A single-stage multi-phase cascaded buck VR is presented in [134]. Compared with previous VICOR two-stage solution, the efficiency is improved in the whole range, especially at the light load condition. One-stage sigma converter with matrix transformer structure is proposed in [135] and the power density can achieve ~420W/inch^3 with maximum efficiency 93.4%.

When compared with single-stage structure, two-stage structure has the advantages of good deployment flexibility, good transient performance and safe voltage. Normally, the 9~12V bus is typically regulated or unregulated from the low voltage bus 48V~60V, which is achieved by 1st stage converter shown in Fig.7.1. One of the combination for two-stage structure is active-clamped forward for 1st stage and multi-phase interleaving buck for 2nd stage proposed in [136]. However, active-clamped forward converter has low-efficiency performance at the light load conditions,

which is somehow bottleneck for two-stage implement. For industry applications, VICOR's two-stage architecture in [137] is one of the popular and low-cost solutions. When compared with single-stage in [135], the power density with ~450W/inch^3 is competitive, however, the efficiency is still not outstanding.

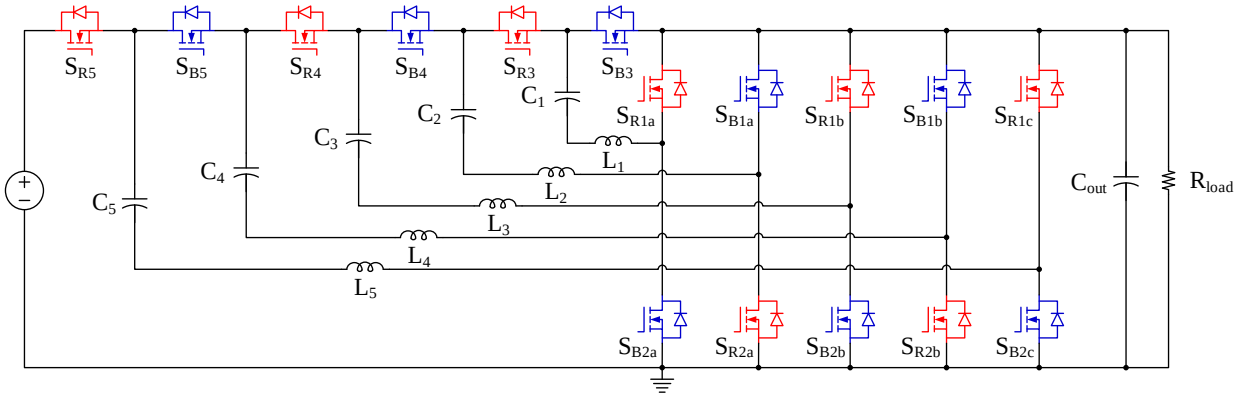
Various topologies can be applied for this 1st stage function [138]-[139], such as LLC, phase-shift ZVS full-bridge, non-isolated buck and multi-phase buck [140], integrated magnetic full-bridge converter [141] for 2nd stage function. For two-stage structure [142], as the efficiency and power density of 1st stage is strictly required, switched-tank resonant dc-dc converters with less-magnetics are more and more popular for this application. So it is emerging to make high-power-density and high-efficiency switched-tank resonant dc-dc converter with high switching frequency, less-magnetics and low voltage spike. Therefore, modeling of switched-tank resonant converter and investigation on circuit parameters are quite important. This paper is focused on how to optimize switched-tank resonant converter to achieve high-power-density and high-efficiency converter for VR 1st stage application.

In this section, an optimal designed unregulated switched-tank ZCS resonant DC-DC converter is presented. It is applied in the first stage for two-stage VR data center application. System configuration and some basic ZCS operation principle are presented. Planar inductor design is shown and simulated with Maxwell software. The converter efficiency evaluation, prototype size and some comparison are also presented.

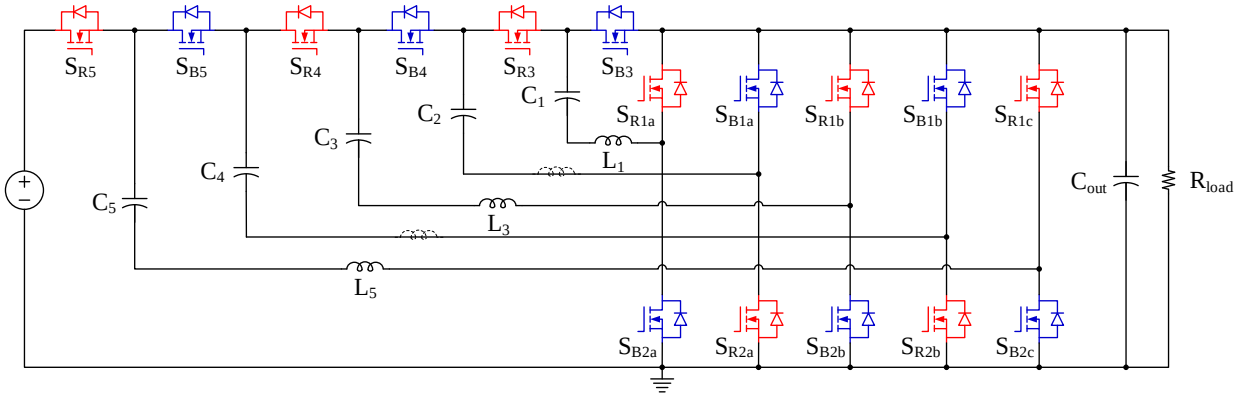
7.2. Switched-Tank Converter and System Structure

Fig.7.2 (a)-(c) show how the switched-tank converter (STC) is derived. The ratio here presents 6 to 1. The wing-side devices include S_{R5}, S_{B5}, S_{R4}, S_{B4}, S_{R3}, S_{B3} and other devices belongs to the bridge-side. The control scheme is the complementary PWM control signals on red and blue

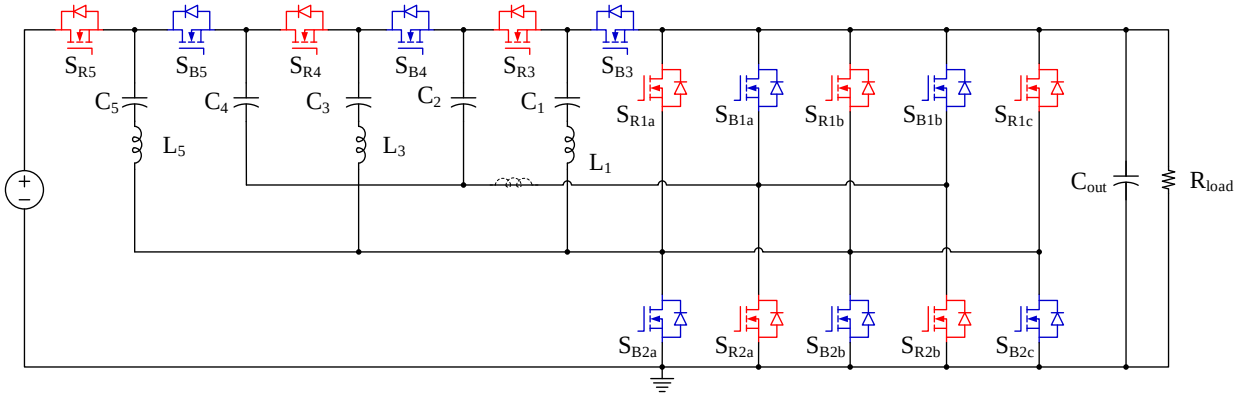
devices. Fig.7.2 (a) presents resonant switched-capacitor converter. Based on this topology, the resonant inductors in the even resonant loops can be removed shown in Fig.7.2 (b). This topology is named switched-tank converter (STC), which can clamp the device voltage spike well.



(a) Structure of the resonant switched-capacitor converter



(b) Derived circuit: switched-tank converter with three inductors



(c) Derived circuit with better voltage clamping for wing side devices

Figure 7.2. Structure of switched-tank converter

Furthermore, the odd loops and eve loops can be connected together before the bridge side shown in Fig.7.2 (c).

7.3. Operation Principle

Fig.7.3 shows the schematic for the proposed resonant switched-tank converter (STC). The ratio here presents 6 to 1. The wing-side devices include S_{R5}, S_{B5}, S_{R4}, S_{B4}, S_{R3}, S_{B3} and other devices belongs to the bridge-side. The control scheme is the complementary PWM control signals on red and blue devices. The zero current switching (ZCS) condition is required as follows;

$$f_s = f_r = \frac{1}{2\pi\sqrt{LC}} \qquad \text{(Eq. 7.1)}$$

where f_s stands for the switching frequency and f_r represents the inductor L and capacitor C resonant frequency. The passive resonant components here refer to L_1, L_3 and L_5 together with C_1, C_3 and C_5.C_2 and C_4 are non-resonant tank capacitors to transfer the energy and clamp the device voltage spike. Fig.7.4 (a) and (b) show two-state equivalent working conditions.

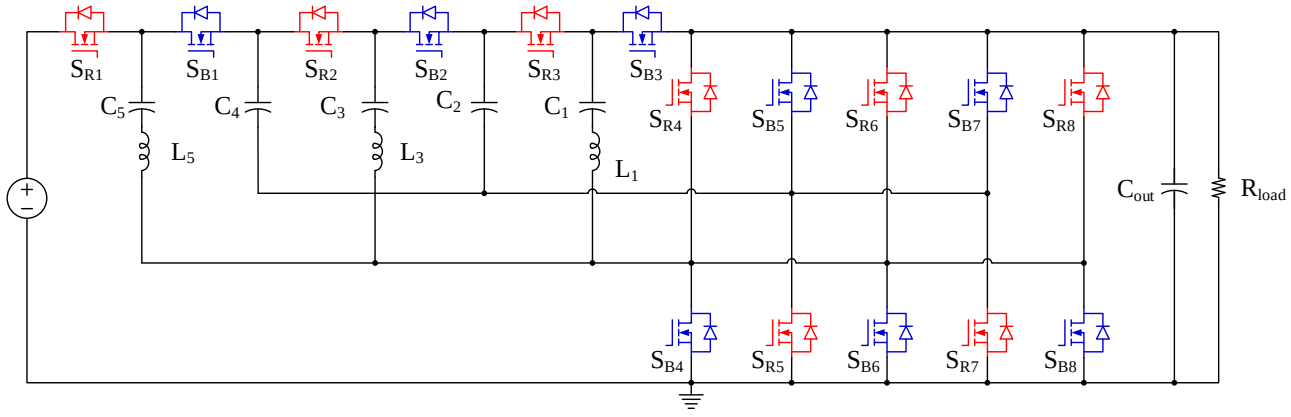
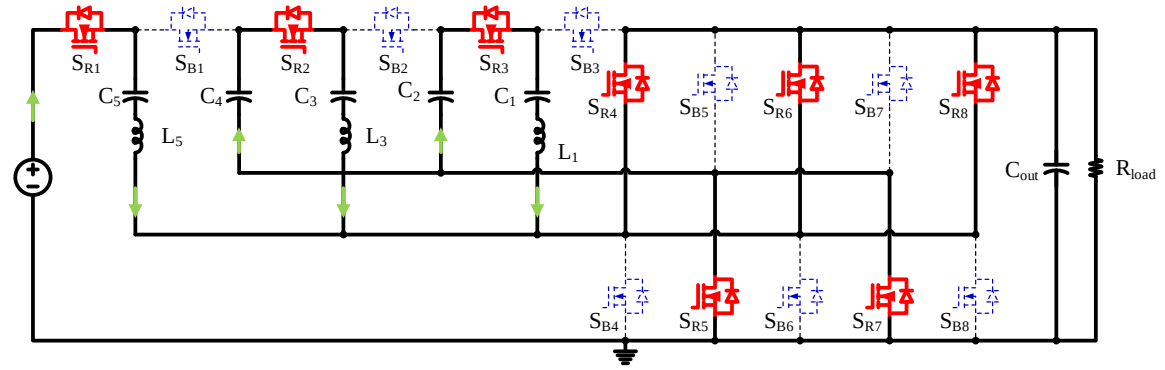
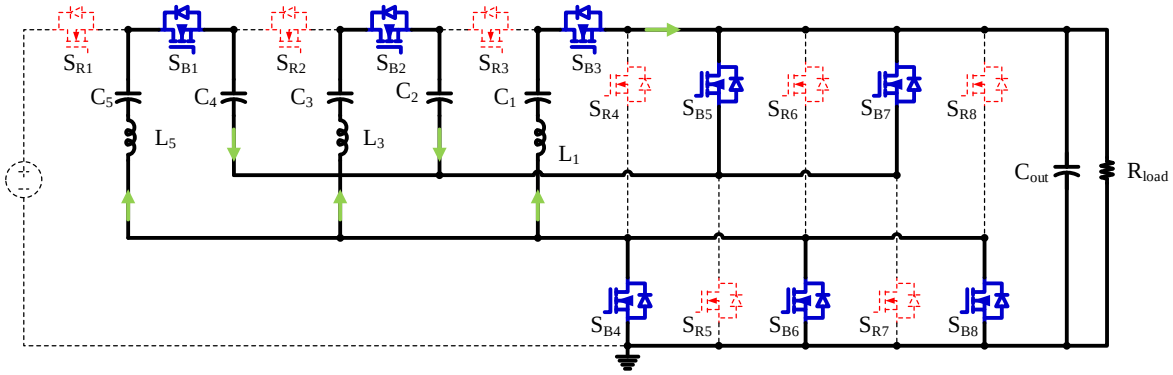


Figure 7.3. Schematic of the proposed resonant switched-tank converter



(a) Equivalent circuit during state 1

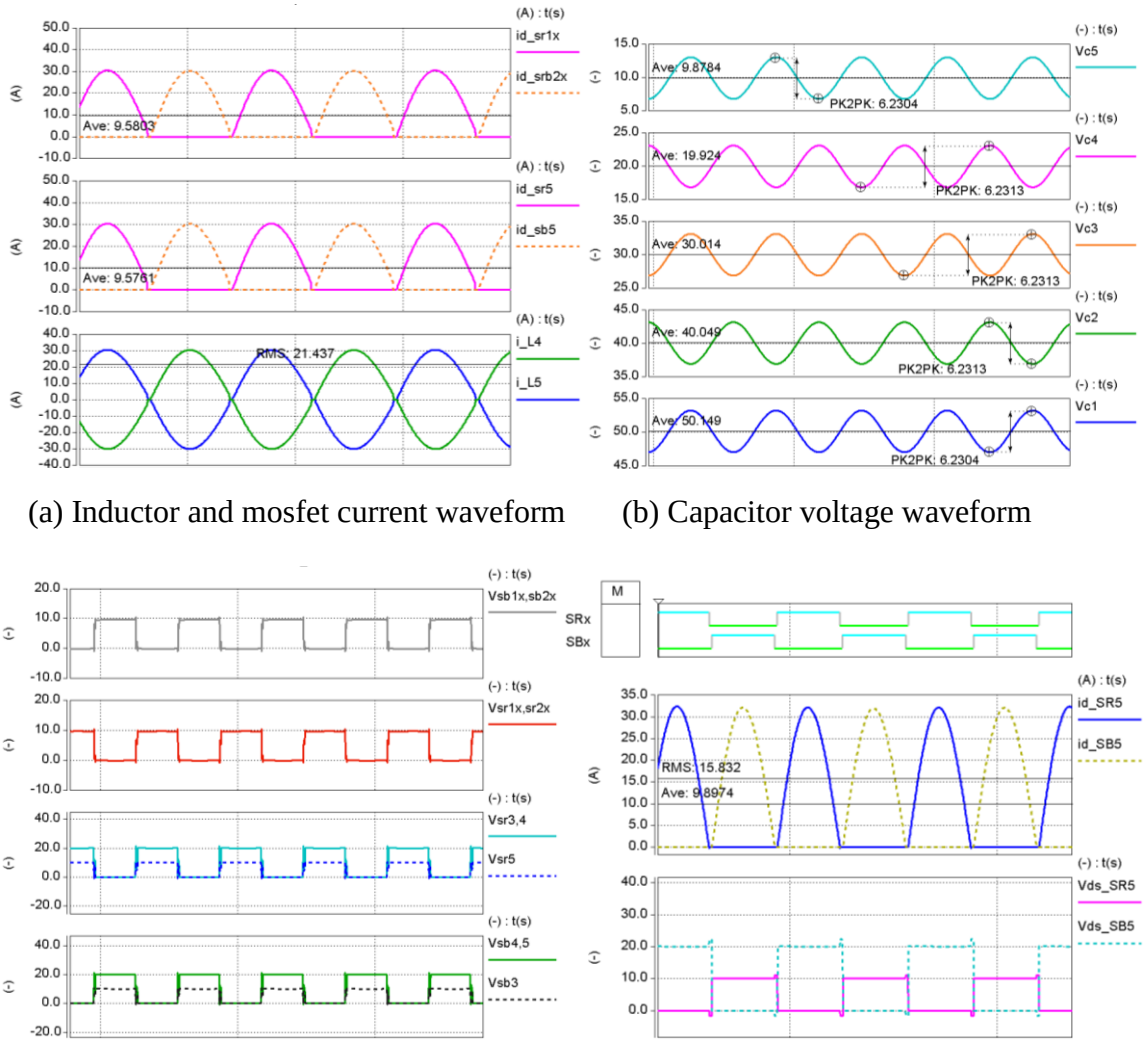


(b) Equivalent circuit during state 2

Figure 7.4. Two-state equivalent circuit

7.4. Simulation Results

Simulation has been performed to verify the theory of the proposed converter with five inductors. The parameters used in the simulation can be found in Table 7.1. Fig.7.5 (a) shows the MOSFET and inductor current waveforms. Fig.7.5 (b) shows the voltage waveforms on each resonant capacitor. When the input has maximum voltage 60V, the average voltage values on C_5 to C_1 are 50V, 40V, 30V, 20V and 10V respectively. Voltage waveforms across all MOSFETs are also captured, as shown in Fig.7.5 (c) and Fig.7.5 (d). The maximum voltage stress on S_{B5}, S_{R4}, S_{B4}, S_{R3} is 20V as expected, while the stress on other devices is 10V.



(a) Inductor and mosfet current waveform (b) Capacitor voltage waveform

(c) Device voltage waveform (d) Wing side device current and voltage waveform

Figure 7.5. Simulation results of the proposed converter with 60V input 10V output operating at 600W

Table.7.1. Parameters used in the experiment @ 387kHz

Description	Items	Values
Input voltage (nominal/max)	Vi_n	54 V / 60V
Output voltage (nominal/max)	V_{out}	9 V / 10V
Output Power (nominal/max)	P_{out}	450 W / 600 W
Resonant capacitor	C_r	2.58 μF
Non-Resonant capacitor	C_{nr}	120 μF
Resonant inductor	L_r	70 nH
Resistor Load	R_{load}	0.167 Ω
Resonant frequency	f_r	375.4 kHz
Switching frequency	f_s	387 kHz
Deadtime	t_d	40 ns

7.5. Planar Inductor Design

In order to increase the system power density, planar inductors are taken in the final prototype. This part shows how to calculate the planar inductance and how to verify the inductance value with ANSYS Maxwell software. Furthermore, to achieve ultra-high efficiency, both core loss and conduct copper loss are analyzed and simulated to optimize the planar inductor.

$$L=\frac{N^2}{2\Re_g+\Re_c} \quad \text{(Eq. 7.2)}$$

$$\Re_g=\frac{l_g}{u_0 A_c} \quad \text{(Eq. 7.3)}$$

$$\Re_c=\frac{l_c}{uA_c} \quad \text{(Eq. 7.4)}$$

$$L=\frac{N^2}{\frac{2l_g}{u_0 A_c}+\frac{l_c}{uA_c}} \quad \text{(Eq. 7.5)}$$

where L stands for the inductance of the planar inductor, based on the circuit parameters design, the inductance value L=70nH . R_g and R_c are the Magnetoresistance for the air and magnetics, respectively. N represents the turns for the planar inductor, here just one turn goes through the UI core. Based on (Eq. 7.2) to (Eq. 7.5), the air gap can be calculated l_g =103um

$$\Delta B = \frac{70\times10^{-9}\times15\times1.414}{1\times12\times10^{-6}} = 0.124 < B_{sat} = 0.47 \qquad \text{(Eq. 7.6)}$$

After calculating the airgap value, the saturation should be verified shown in (Eq. 7.6). Δ B is 0.124, which is smaller than saturation magnetic flux density B. It means it works well at this current point rms 15A.

ANSYS Maxwell simulation tool is easy to verify the calculation and also it can verify the loss distribution and give some optimal design guideline. Fig. 7.6 presents the 3D model for the planar inductor. The core is taken Magnetics Inc. P Material. Inside Maxwell software, four boxes can be added together to make the whole part work. The size for each box are 10.85mm*6.3mm*1.95mm, 10.85mm*6.3mm*1.83mm and two 1.83mm*6.3mm*2.24mm. The core size is finally matched with the real inductor in the prototype.

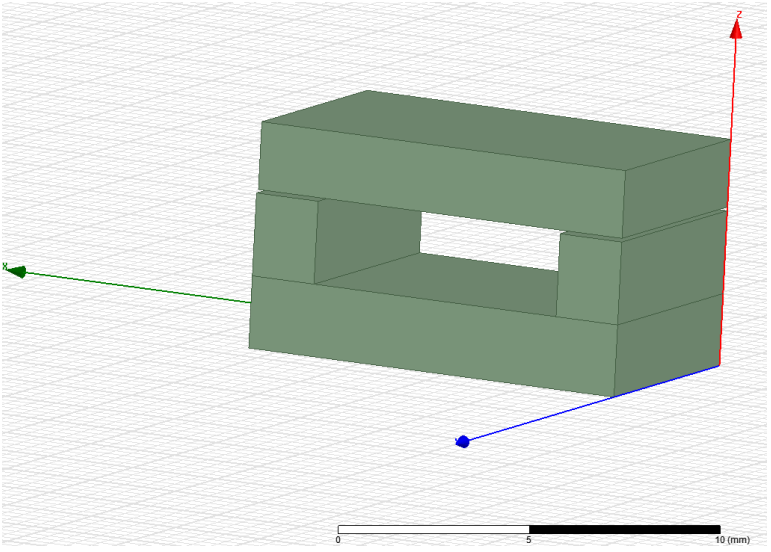


Figure 7.6. Planar inductor modeling with Maxwell

Fig.7.6 presents the 3D model with one turn for the planar inductor. The inductance can be simulated under this condition with the air gap 103um and the simulation result is quite matched with the calculation. The simulation result is 70.4nH shown in Fig.7.8.

Finally, the real planar inductor is made with UI core. The airgap is made with captain tape and the airgap value is ~102um. The final real planar inductor is tested and its value is ~62.4nH, which is good enough for the real experimental testing.

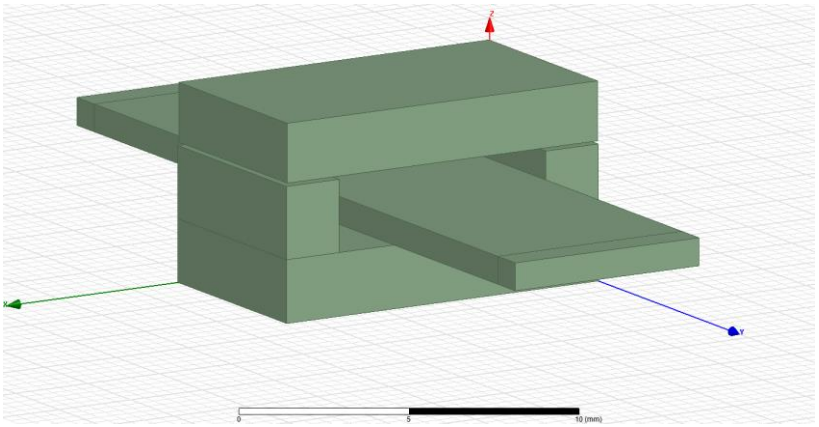


Figure 7.7. Planar inductor modeling with one turn with Maxwell

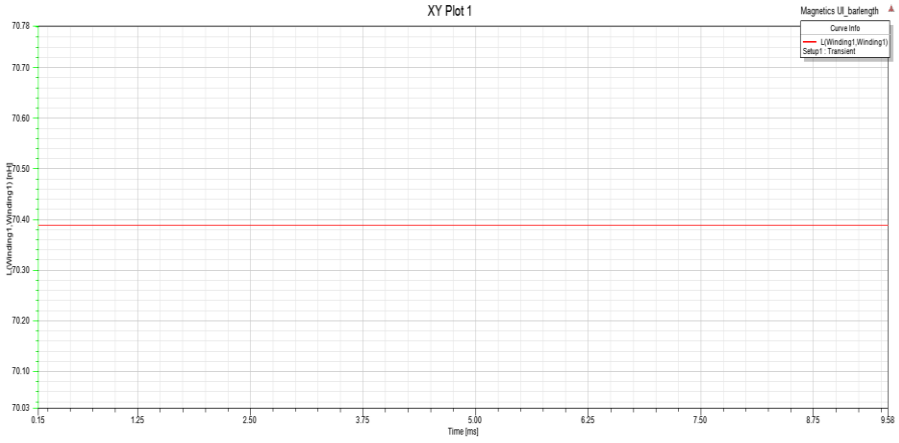


Figure 7.8. Inductance simulation results 70.4nH

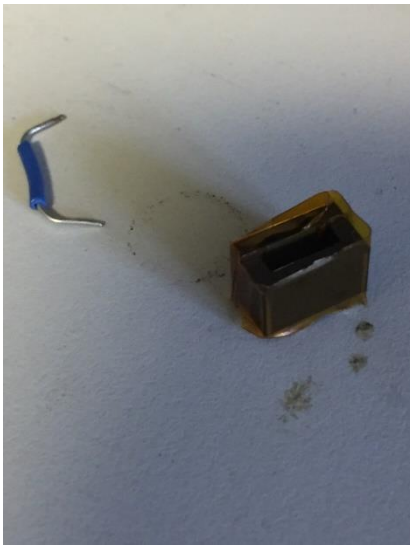


Figure 7.9. Real planar inductor

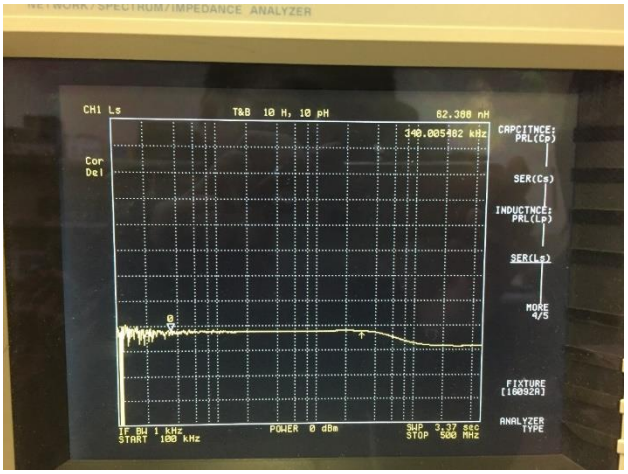


Figure 7.10. Inductance testing 62.4nH

Besides the planar inductance design, the loss analysis is necessary to have an optimal design on high efficiency planar inductor. The core loss can be expressed in (Eq. 7.7). The core loss is related with the switching frequency and magnetic flux density B and different core material.

$$P_{core}=0.0434(f\times10^{-3})^{1.63}(B\times10)^{2.62} \qquad \text{(Eq. 7.7)}$$

Here, $\Delta B=0.124$, $f=340\text{kHz}$, the volume $V=283\text{mm}^3$, the total core loss can be evaluated at 289mW for UI P material core. (Eq. 7.7) represents the P material from Magnetics company. Other material such as F material and J material, also 3C94 and 3F3 from Ferroxcube are also

compared in order to minimize the core loss. Fig.7.11 shows the core loss comparison for different materials. So finally P material is selected here.

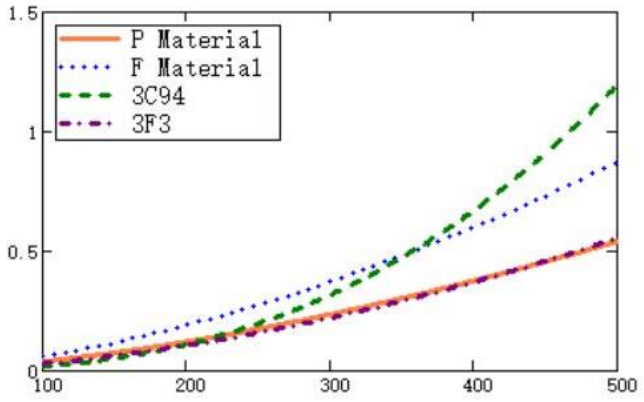


Figure 7.11. Core loss (W) under different switching frequency (kHz)

Besides the core loss, copper loss is also important for ultra-high efficiency converter design. So how to minimize the copper loss with one turn for the planar inductor is very important. As a result, ANSYS Maxwell tool is pretty good to achieve this target. Fig.7.12 shows the copper information from Altium Software. Here, the final prototype takes 10 layers board and each layer copper information can be got from this figure. And these information will be applied in Maxwell.

Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/...	Surface Mate...	0.4	Solder Resist	3.5		
AC Vo+GND	Signal	Copper	1.4				Top
Dielectric 1	Dielectric	Core	10	FR-4	4.2		
AC 0.5GND La...	Signal	Copper	1.417				Not Allowed
Dielectric 4	Dielectric	Prepreg	5		4.2		
DC Vo Layer 1	Signal	Copper	1.417				Not Allowed
Dielectric 6	Dielectric	Core	10		4.2		
DC Vo	Signal	Copper	1.417				Not Allowed
Dielectric 7	Dielectric	Prepreg	5		4.2		
AC GND	Signal	Copper	1.417				Not Allowed
Dielectric 3	Dielectric	Core	10		4.2		
DC Vo Layer 3	Signal	Copper	1.417				Not Allowed
Dielectric 5	Dielectric	Prepreg	5		4.2		
AC GND Layer 4	Signal	Copper	1.417				Not Allowed
Dielectric 2	Dielectric	Core	10		4.2		
AC 0.5Vo+GND	Signal	Copper	1.4				Bottom
Bottom Solder	Solder Mask/...	Surface Mate...	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 7.12. Copper information from Altium software

Fig.7.13 shows the 3D model with 10 copper layers. The thickness for each layer is 2oz copper (0.07112mm). The width of each layer is 6.57mm and width margin is 0.31mm. The conduction material is set to copper and isolated material is set to FR4.

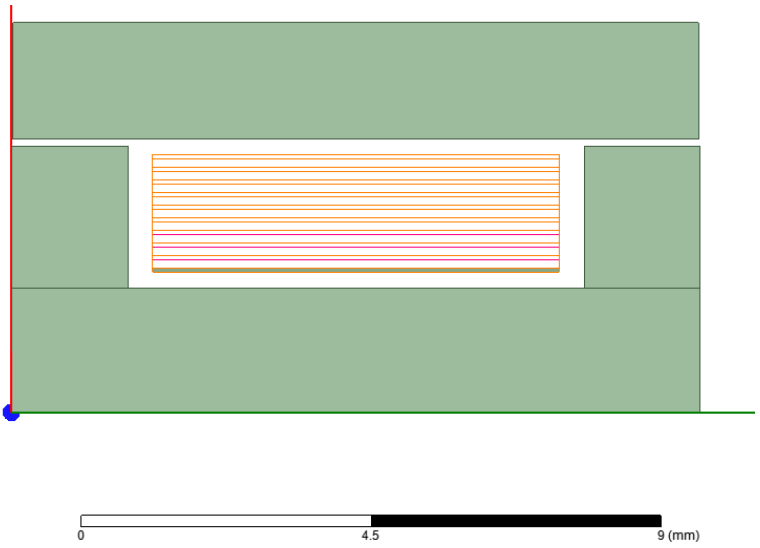


Figure 7.13. Modeling with 10 layers copper

After successful modeling set-up, the copper loss can be simulated with Maxwell tool.

Fig.7.14 and Fig.7.15 are compared when the distance from PCB bottom-side to U core 10mil and 1mil, respectively with ac conduction loss 175mW and 151mW. Fig.7.14 and Fig.7.15 proves that the PCB board had better be far away from the air gap side and this indicated the board should be as closed as U core to minimize the ac conduction loss. Segmented copper structure is also investigated shown in Fig.7.16 to reduce the skin effect, however, it proves that it won't help at all. Fig.7.16 shows 6-segmented copper bars for each layer and the ac conduction loss is increased to 219mW.

Actually, the fringing effect caused by air-gap is the domain part in this application, so orthogonal structure is taken and shown in Fig.7.17. The ac conduction loss can be significantly reduced by cutting some PCB copper trace near the air-gap. To set the air-gap position as the central point, different shapes are further investigated to get the minimized ac conduction loss.

Fig.7.17 to Fig.7.20 show the ac conduction loss under different radius values. Fig.7.21 summarized all the simulations with one fitting curve and shows that under r=1.65mm, the minimum conduction loss can be reduced to 78.6mW, which means 64% improvement on the planar inductor ac conduction loss. This will help for the proposed ultra-high high efficiency converter, because the total power loss is only 2.8W for 98.55% under ~150W. 0.14*3 W loss saving also matters a lot.

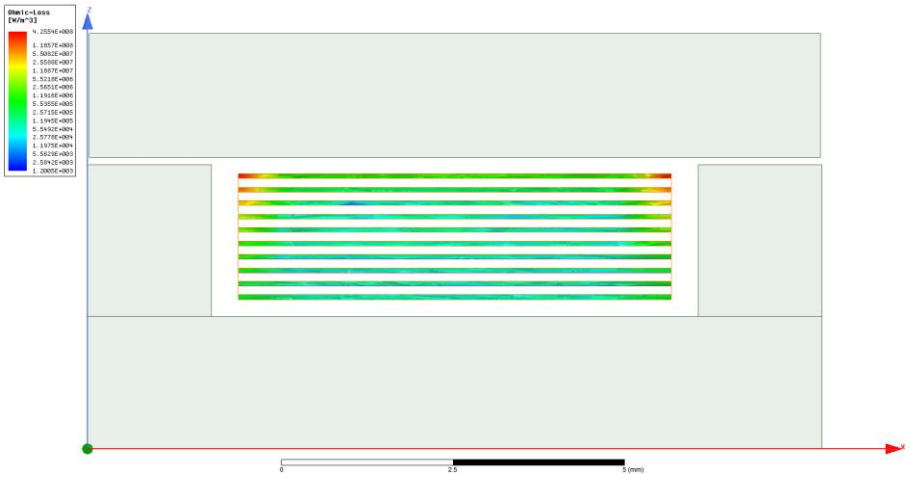


Figure 7.14. AC conduction loss under distance 10mil, P=175mW

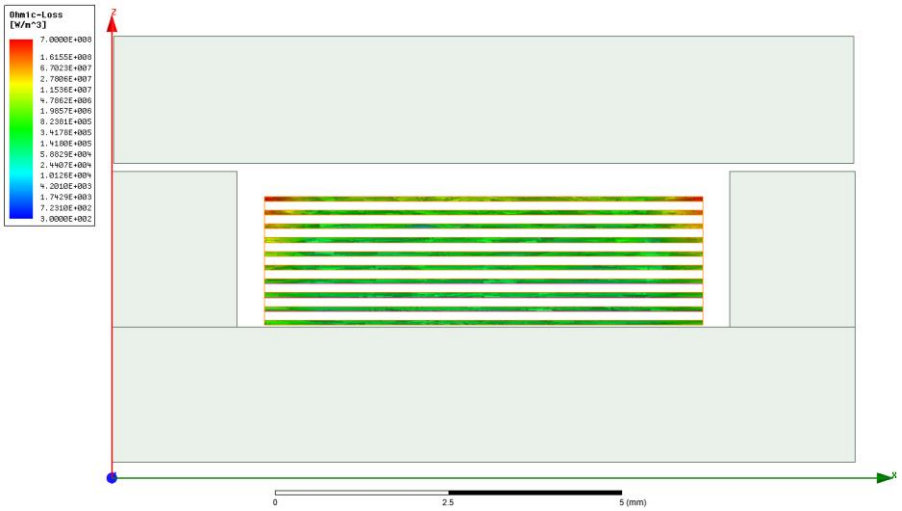


Figure 7.15. AC conduction loss under distance 1mil, P=151mW

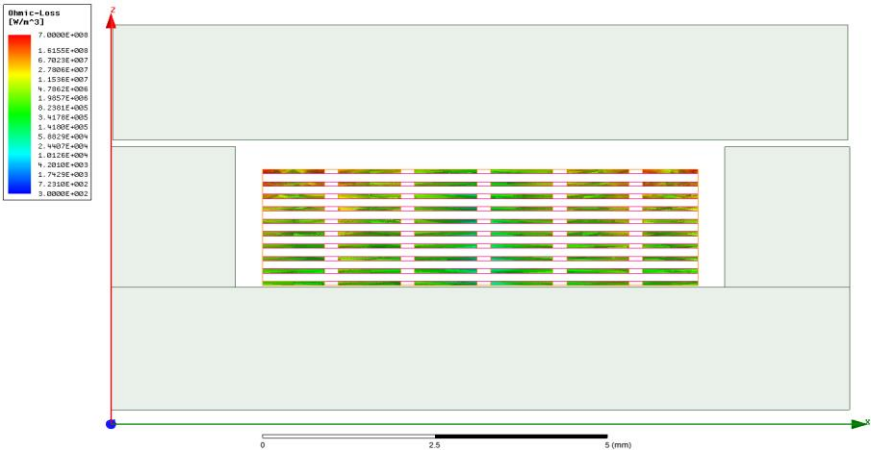


Figure 7.16. 6-segmented copper bars each layer, P=219mW

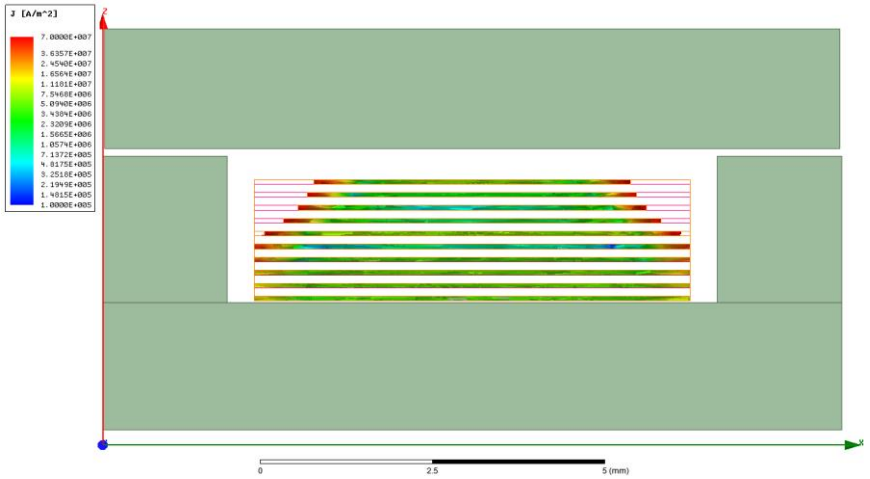


Figure 7.17. Current density with orthogonal structure with r=1.263mm,P=86.9mW

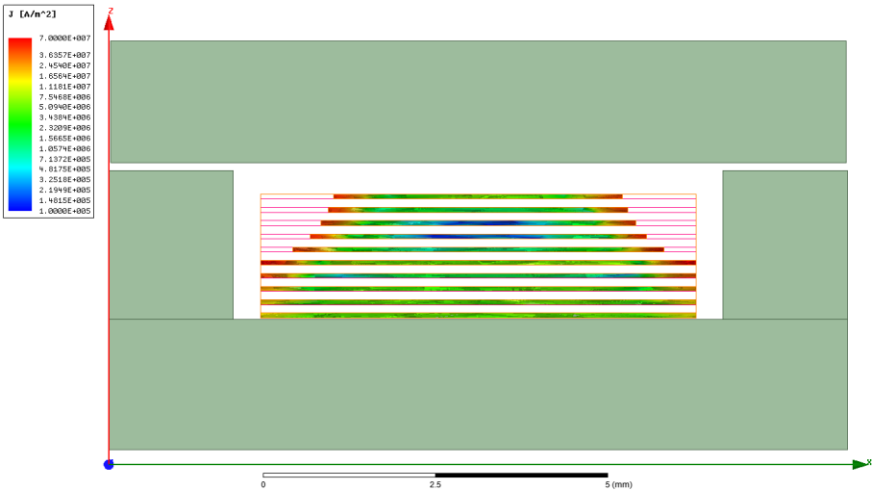


Figure 7.18. Orthogonal structure with r=1.456mm P=80.6mW

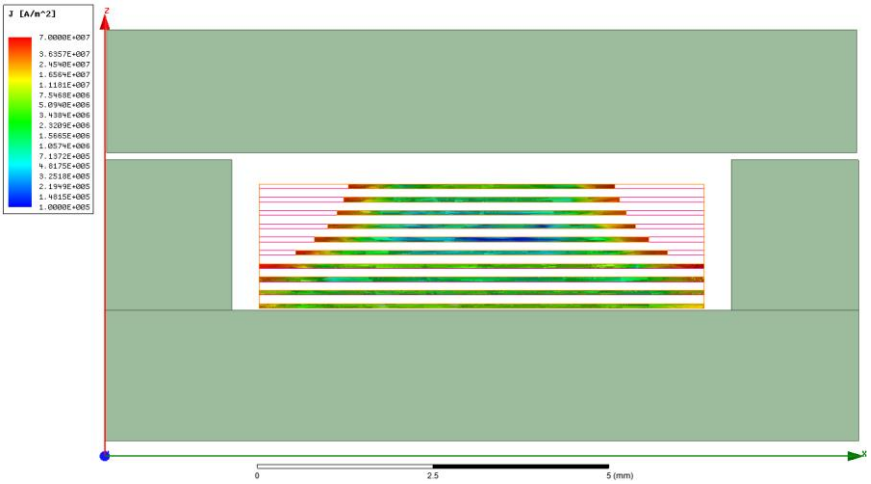


Figure 7.19. Orthogonal structure with r=1.65mm P=78.6mW

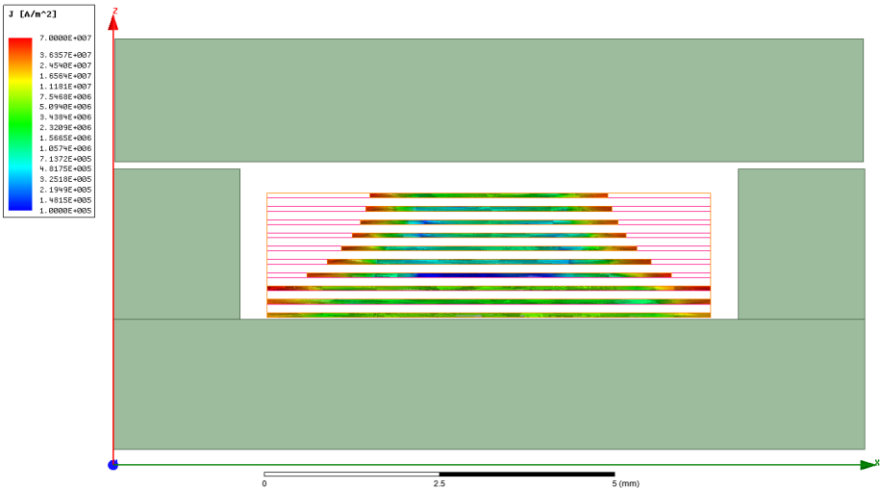


Figure 7.20. Orthogonal structure with r=1.845mm P=79.5mW

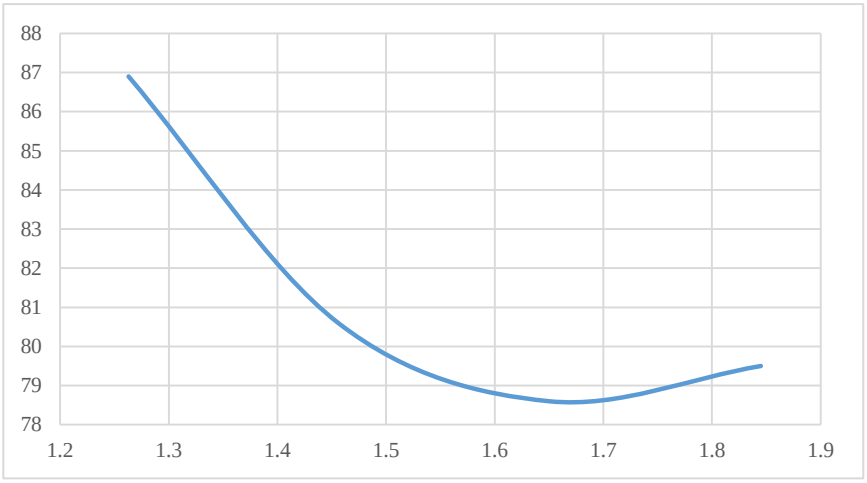


Figure 7.21. AC conduction loss fitting curve under different r

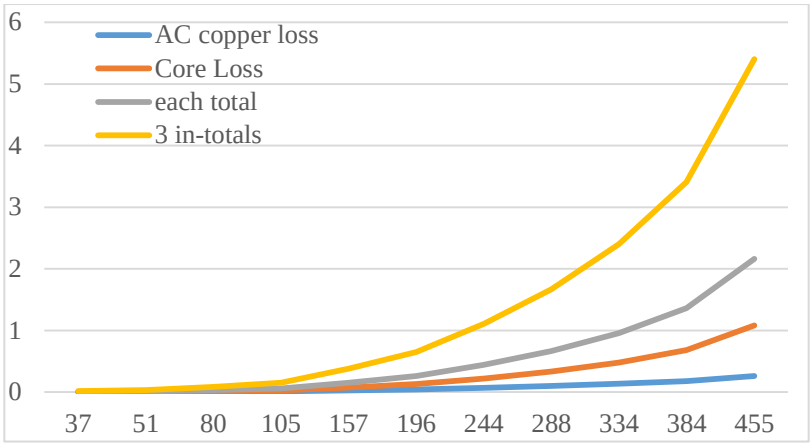


Figure 7.22. Planar inductor loss under different power rating

Table.7.2. Maxwell simulation at different power rating conditions

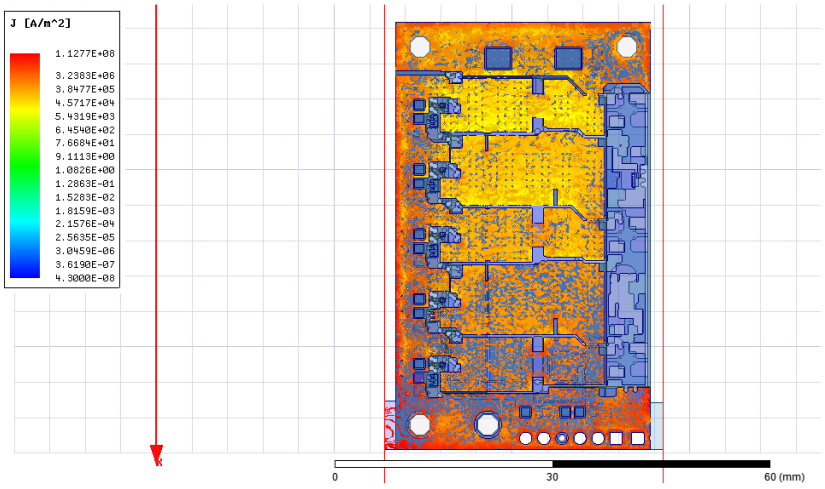
P_o(W)	Peak current (A)	Copper loss (W)	Core loss (W)
37	2.55	0.002	0.0014
51	3.42	0.0036	0.0029
80	5.13	0.008	0.0085
157	9.88	0.0297	0.047
288	18.2	0.1005	0.233
384	24.39	0.1796	0.502
455	29.4	0.26	0.82

Finally, based on the best structure, conduction loss for various power rating conditions are shown in Fig.7.22 including the core loss. As the prototype has 3 resonant planar inductors, each inductor total loss and 3 inductors in total loss are all shown here. Besides, Table.7.2 shows the different values at different power rating for both ac copper loss and magnetic core loss.

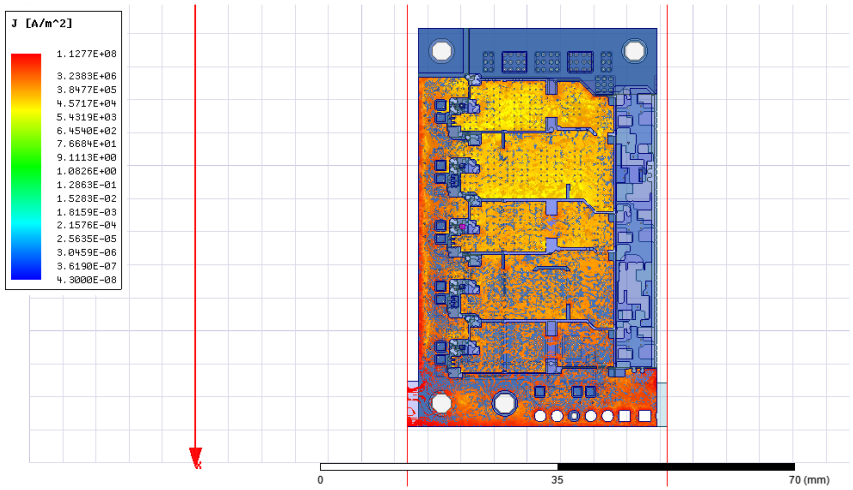
7.6. Prototype and Experimental Results

Besides the traditional loss breakdown analysis, such as device loss, passive component loss; it is also important to analyze PCB copper loss. This is because the output current is quite high and power density is also extremely high. To achieve ultra-high efficiency, PCB board copper loss is sensitive to the final system efficiency. The final prototype design can be exported from

Altium into Maxwell to simulate the exactly same case as the final experiments. The simulation is conducted at 360 kHz switching frequency at 200W. The current distribution is shown in Fig.7.23 (a) and (b), respectively for both 2 state conditions. The average power loss for the prototype is ~694mW at 200W power rating. As the operating state has 3 separated loops and they share the same output bus bar, the final output terminal will hold 3 times in-parallel current. So the optimal design should let all the loop current go directly to the output terminals to minimize the copper bus loss.



(a) state 1, P=690mW



(b) state 2, P=698mW

Figure 7.23. PCB copper loss simulation for two states

Furthermore, PCB copper loss is verified at different switching frequency to investigate the PCB ac loss. Fig.7.24 shows the PCB copper loss under different operating frequency from 100 kHz, 525mW to 1 MHz, 830mW.

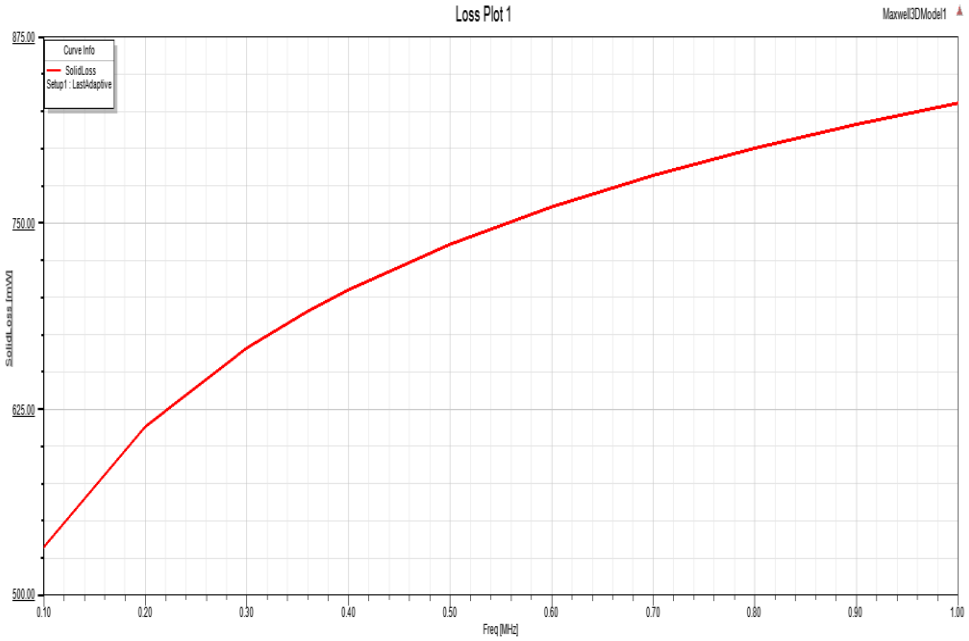


Figure 7.24. Copper loss from 100k to 1MHz

Table.7.3. Specification of prototype

Description	Part#	Manufacture
Digital controller	TMS320F28335	TI
Resonant capacitor	C2220C334J1GAC	Kemet
Resonant inductor	SLC7649S-700	Coilcraft
Switching device	EPC2023	EPC
Level shifter	ADUM6200CRWZ	ADI
Gate Driver	LM5113	TI
Digital Isolator	Si8620BB	Silicon Labs

A GaN (EPC2023) based prototype is built and tested to verify the theoretical analysis. The specification of the prototype is shown in Table.7.3. Fig.7.25 shows the 3D model and Fig.7.26 shows the real testing prototype. The proposed converter can achieve the peak efficiency at 98.55% and power density can achieve ~750W/inch^3. Fig.7.27 and Fig.7.28 show resonant inductor current and zoom-in ZCS operation. Fig.7.29 shows the input 54V and output 8.7V voltage waveforms. Fig.7.30 presents the difference between measured efficiency and estimated efficiency. The simulated PCB copper loss is matched for the gap. Fig.7.31 shows prototype thermal picture under 450W with fan. The highest temperature is 64℃ and the resonant planar inductor temperature is 51.7℃. Efficiency curves under different switching frequency are shown in Fig.7.32. It can achieve 98.55% under 253kHz by adding resonant caps. The total height is controlled the maximum height of the board.

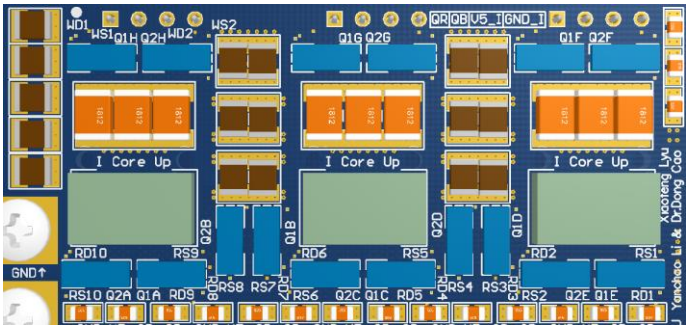


Figure 7.25. 3D model with Altium software

Figure 7.26. Real testing prototype

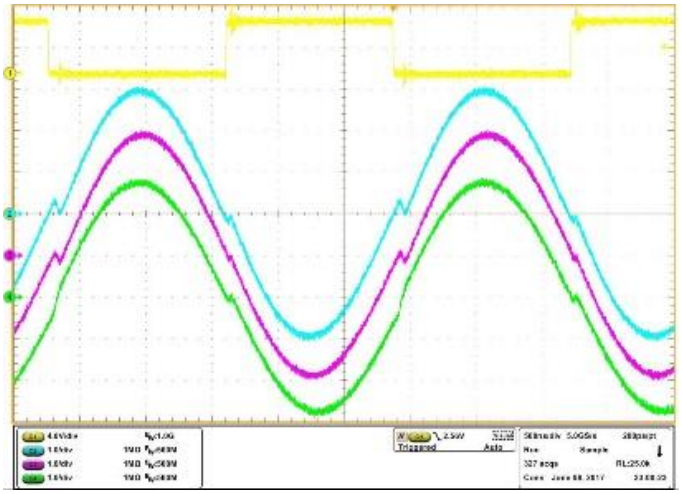


Figure 7.27. 3 resonant inductor current, Gate (4V/div) and inductor current (10A/div, 500ns/div)

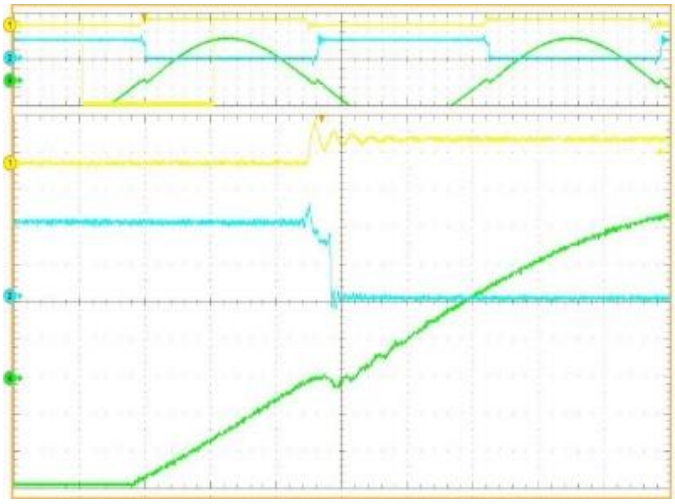


Figure 7.28. Zoom-in one device ZCS waveform

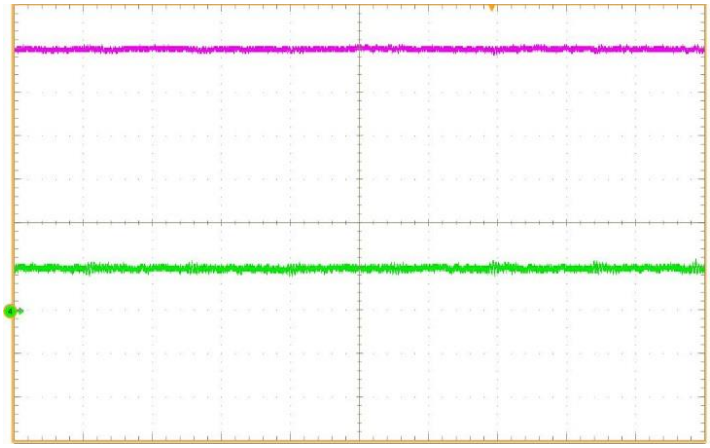


Figure 7.29. Input 54V and output 8.7V voltage waveforms

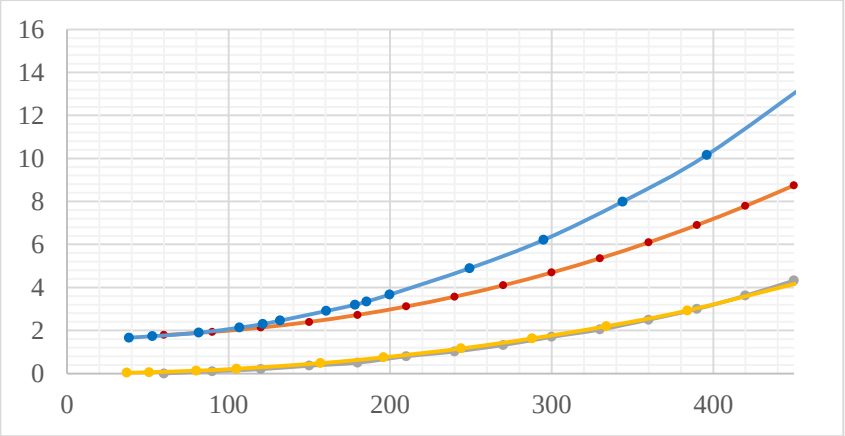


Figure 7.30. PCB loss match between measured loss difference and simulation loss

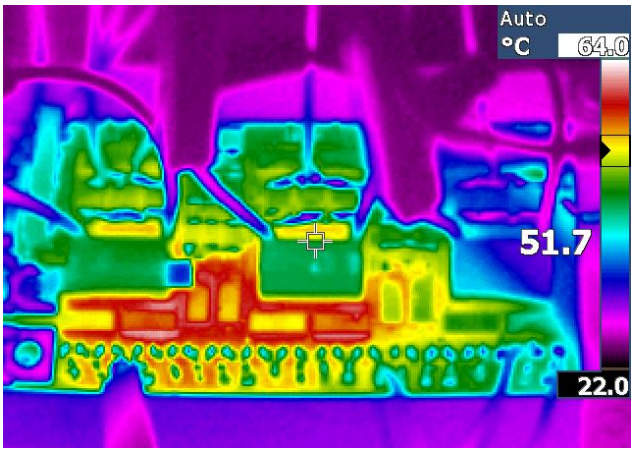


Figure 7.31. Thermal picture under 54V input, 450W

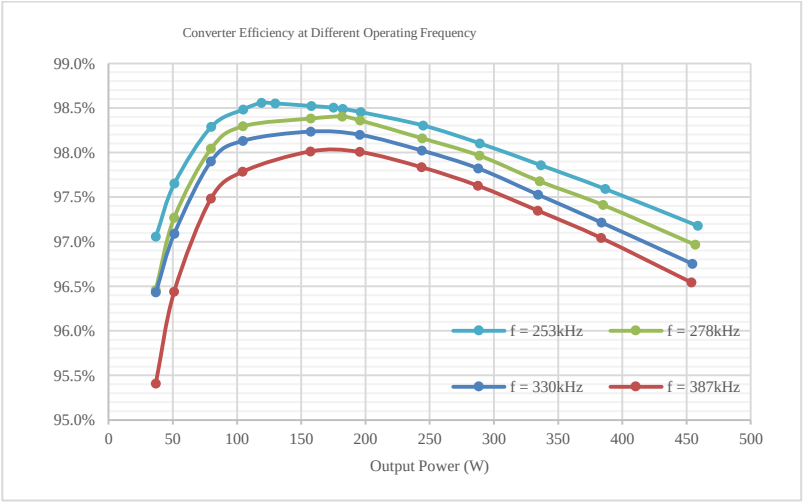


Figure 7.32. System efficiency curve under different f_s

Table.7.4. Comparison with existing products

Part#	Power Density	Peak Efficiency	Manufacture
IB048E120T40Px	635.32W/inch^3	97.8%	Vicor
NEB-300DMA0AN	366.3W/inch^3	95.2%	Murata
E48SC12025	337.08W/inch^3	95.0%	Delta
iEH48025A120V	289.86W/inch^3	95.5%	TDK
FPER48T01225	321.89W/inch^3	96.3%	FDK
0PKB4413D	424.53W/inch^3	96.0%	Ericsson
---	750W/inch^3	98.55%	NDSU

Furthermore, detailed comparison with some existing products is presented in Table.7.4. The company Vicor is well-known in this dc-dc area. The proposed prototype power density 750W/inch^3 and efficiency can be 98.55%, which is better than Vicor's product.

7.7. Comparison with Cascaded Voltage Divider Topology

This section shows the comparison on efficiency and power density between switched-tank converter (STC) and cascaded voltage divider (CVD). Fig.7.33 shows the basic schematic of 8X-STC. 8X here means the ratio is 8:1. The ratio is chosen at 8 to make a fair comparison, because CVD can only generate 2^N ratio. N stands for cascaded stages. When compared with multi-level resonant switched-capacitor converter (MRSCC), the even number resonant inductors are removed. The even number capacitors, which are named tank capacitors, are to clamp the voltage spike for the wing side devices. The wing side devices are consisted of S_{R6}, S_{B6}, S_{R5}, S_{B5}, S_{R4}, S_{B4}, S_{R3}, and S_{B3} shown in Fig.7.33. The bridge-side has 7 half-bridges. The red switches and blue ones have the complementary control signals. C_1, C_3, C_5 and C_7 with L_1, L_3, L_5 and L_7 are the resonant passive components. Each resonant inductor here is chosen at 50nH (SLC7649S-500) and each resonant

capacitor is stacked with 330nF (C2220C334J1GAC) *14 small ceramic capacitors.

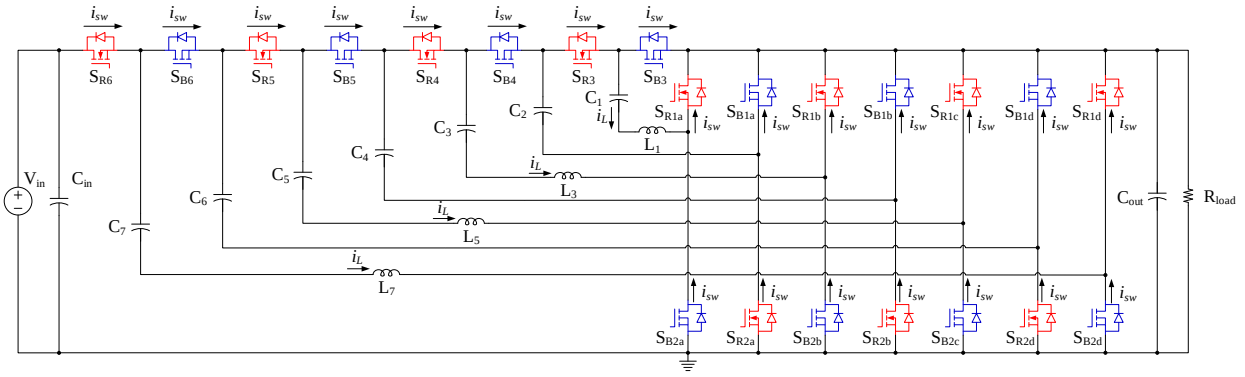


Figure 7.33. 8X switched-tank converter (8X-STC)

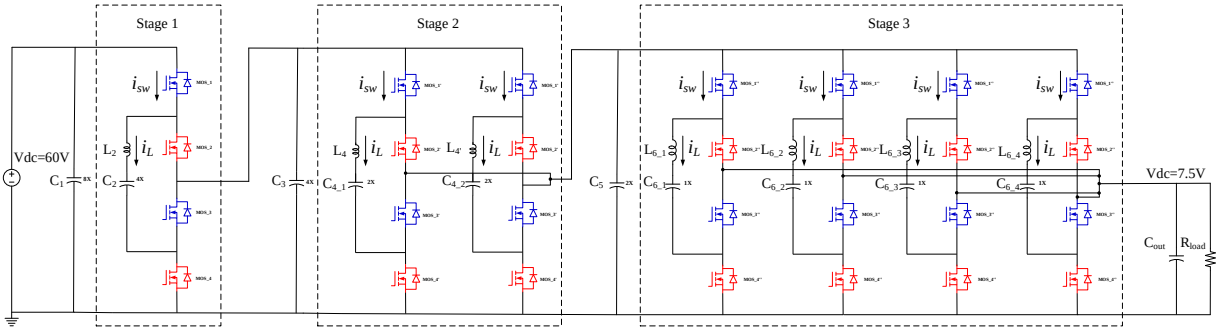


Figure 7.34. 3-cascaded voltage divider DC-DC Converter with the same current stress

Besides, C_2, C_4 and C_6 are non-resonant capacitors or tank capacitors are stacked with 1uF (C1210C105K1RAC) *27. All the switching devices are chosen EPC2023 with the switching frequency at ~320 kHz. The input voltage is 60V and the unregulated output is about 7.5V with the ratio 8:1. The power rating is 600W.

Fig.7.34 shows the basic schematic of cascaded voltage divider circuit with the ratio 2^3:1 (3X-CVD). The final ratio is also 8:1. 3X here means 2^3. The input, output voltage and power rating are the same with STC. The input voltage is 60V and output voltage is ~7.5V. The 1st stage device are chosen EPC2024. All the other switching devices are chosen EPC2023 (block voltage 30V) with switching frequency at ~320 kHz. The power rating is also 600W. The control signals of two kinds of device are complementary and are similar that the blue device and the red device

have 50% duty cycle. L_2, C_2; L_4, C_4 and L_6, C_6 are resonant passive components. C_1, C_3 and C_5 are the dc-link non-resonant capacitors.

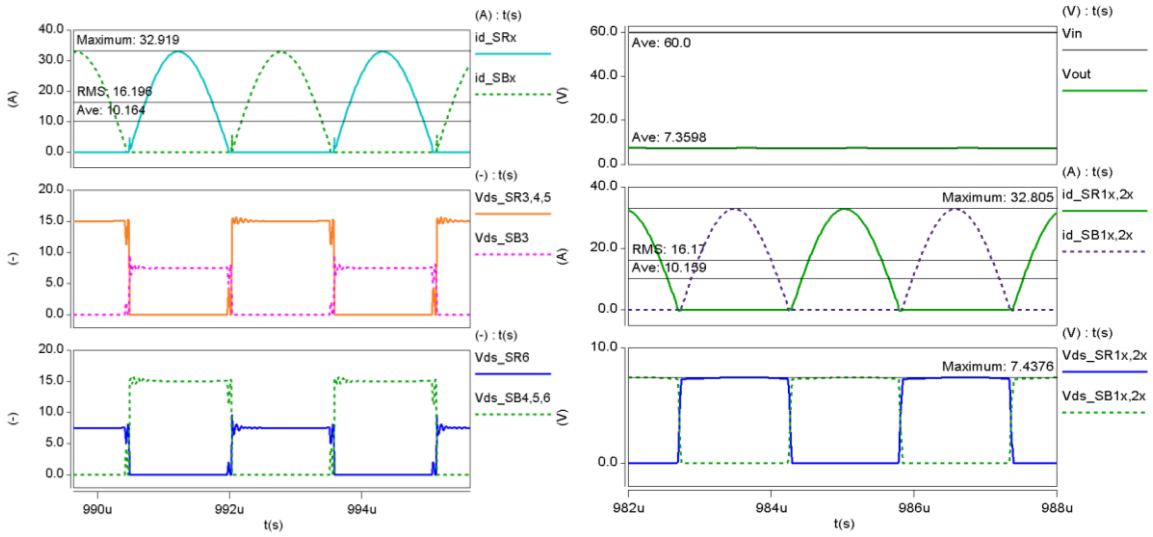
As this cascaded structure makes the device current stress high, 2 branches are paralleled in the 2nd stage and 4 branches are paralleled in the 3rd stage to guarantee to make the apple to apple comparison under the same current stress when compared with STC. Each branch contains four devices, one resonant inductor and one resonant capacitor. The total number of switching devices for this proposal is 28. The device number for 8X-STC is 22. The deliver power from input to output for STC is parallel output. However, for CVD the power is cascade from input to output. The operating switching frequency is all the same at 320 kHz. The resonant inductor number for STC is 4 and 3X-CVD resonant inductor is 7. Similarly, the resonant capacitor number for STC is 4 stacks and each stack is 14 C2220C334J1GAC. For CVD, it needs 7 stacks and each stack is 14 C2220C334J1GAC. The non-resonant capacitor for 8X-STC is 3 stacks with 47 C1210C105K1RAC each. However, for 3X-CVD topology, it needs 2 link capacitors with 100 C1210C105K5RAC each. This is because for each stage output, there needs the non-resonant capacitor to hold the dc-link voltage in order to support the steady voltage for the next stage input. The input and output capacitors are the same for both candidates and are not compared here. And the detailed comparison of these two candidates is summarized in Table.7.5.

Table.7.5. Comparison between STC and CVD

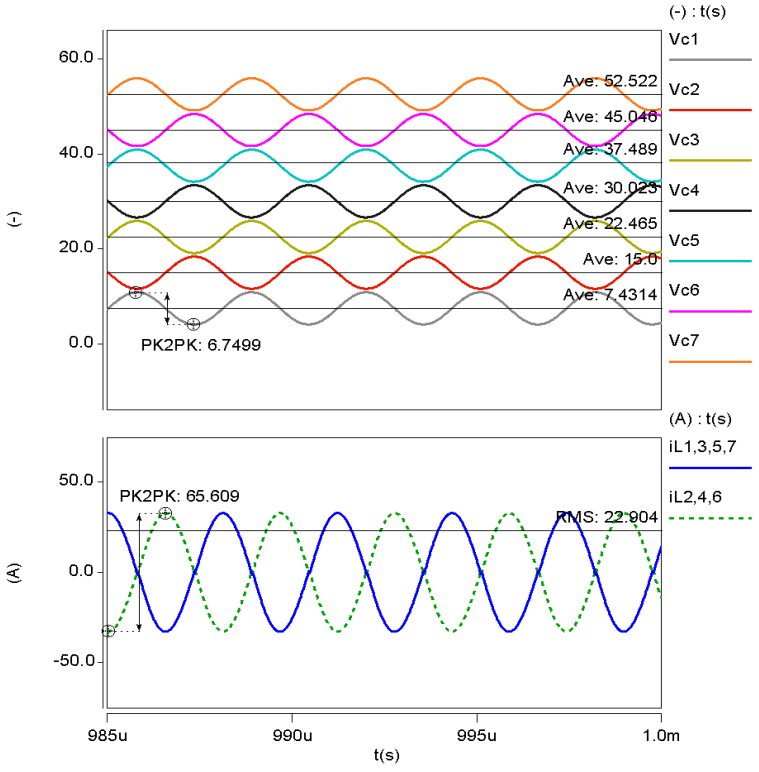
Part#	Device	V_{ds} & I_d	Resonant Inductor	Resonant Cap	Non-Resonant Cap
STC	22 EPC2023	30V/60A	4 SLC7649S-500	4*14 C2220C334J1GAC	3 * 47 C1210C105K1RAC
CVD	4EPC2024 24EPC2023	40V/90A 30V/60A	7 SLC7649S-500	(1+2+4)*14 C2220C334J1GAC	2 * 100 C1210C105K5RAC

As analyzed above, simulations with Saber are conducted respectively with 8X-STC and 3X-CVD. Fig.7.35 (a)-(c) shows the key waveforms for 8X-STC. Each resonant capacitor voltage and inductor current are shown here. Furthermore, each device voltage and current stress are presented for further comparison. For the wing side devices in STC, the device S_{B3}, S_{R6}, which are the first device and the last device for the wing side, have 1X voltage stress shown in Fig.7.35 (a). X here stands for the output voltage value. The other devices for the wing side have 2X voltage stress. The RMS current for each device is ~16.2A. The input voltage is 60V and output voltage is ~7.36V because of some voltage drop on the devices. The voltage stress for the bridge side is 1X (7.4V) and current stress is also ~16.2A. The voltage on the resonant capacitors and current on the resonant inductors are also shown in Fig.7.35 (c).

Similarly, Fig.7.36 (a)-(d) show the key waveforms of 3X-CVD converter. The resonant capacitor voltage C_2, C_4 and C_6 are shown in Fig. 7.36 (a). C_2 has a dc bias voltage ~30V; C_4 and C_6 have dc bias voltage ~15V and ~7.5V, respectively. Furthermore, each device voltage and current stress are shown in Fig.7.36 (b) and (c). Resonant inductor current are shown in Fig.7.36 (d). The simulation is verified for each single device. That is why the peak to peak inductor currents are 63A, 124A and 241A, respectively. So there is two branches in 2nd stage and four branches in the 3rd stage to guarantee the current stress is similar to STC.



(a) Device voltage and current waveforms (b) Input and output voltage waveforms

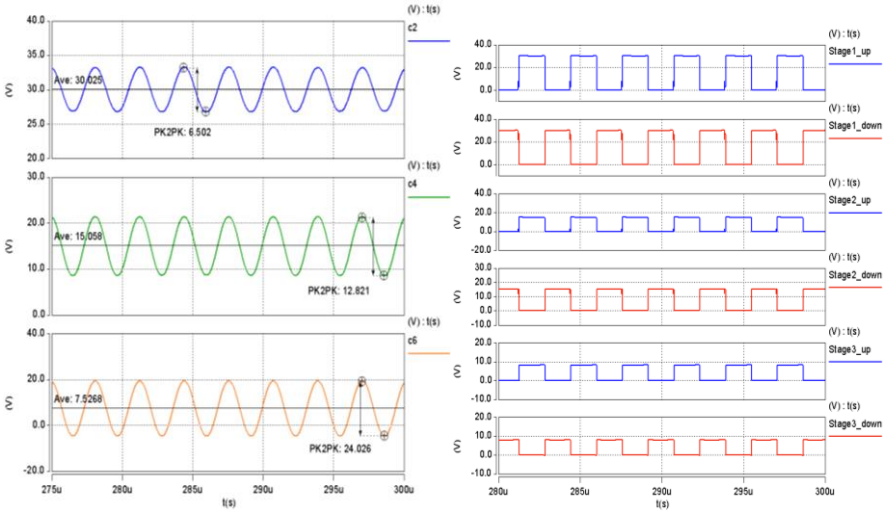


(c) Capacitor voltage and inductor current waveforms

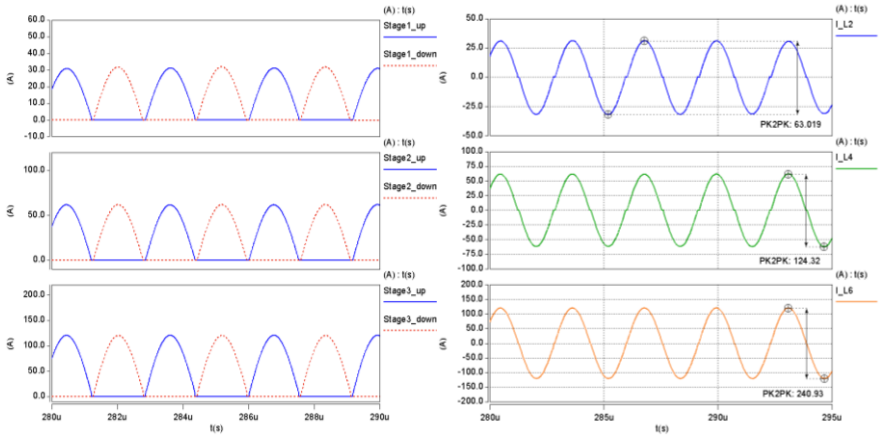
Figure 7.35. Key Simulation Waveforms for STC

When compared Fig.7.35 and Fig.7.36, it can be seen that the current stress for 3X CVD is different and there is more current stress on the 2nd and 3rd stage device. This is because the

cascaded structure, at the same power rating, the voltage is low and the current stress will be much higher. On the contrary, the device current stress of 8X-STC is smaller than those of 3X-CVD. This is because the topology structure make is work in- parallel to share the total current. The conduct loss of 8X-STC will be smaller when compared with 3X-CVD.



(a) Capacitor voltage waveforms (b) Device voltage waveforms



(c) Device current waveforms (d) Inductor current waveforms

Figure 7.36. Key simulation waveforms for CVD

As presented above, the whole system efficiency of two converters are analyzed and calculated. Fig.7.37 shows the system efficiency curves. Fig.7.38 shows the power loss curves and Fig.7.39 presents power loss breakdown analysis.

It is shown that under the same condition, 8X-STC efficiency is higher than 3X-CVD in the whole range. At full power load, STC is 1% higher than CVD. Furthermore, at 10% light load, STC is 3% higher than CVD. The power loss shown in Fig.7.39 is calculated with non-resonant (NR) capacitor, such as input/output capacitor, resonant ceramic capacitor and inductor, switching device loss, respectively. The STC efficiency is high, mainly because it delivers the power at the parallel mode. For cascaded structure, it is connected in-series and current is high. Fig.7.40 shows the details of size comparison of 8X-STC and 3X-CVD. As cascaded structure makes high current, in order to have the same current stress on the devices, 3X-CVD has more branches circuit compared with 8X-STC. The device number of 3X-CVD is 28. 8X-STC just has 22. Also the inductor number of 8X-STC is 4 less than 3X-CVD. The resonant capacitor of 8X-STC is also much smaller than that of 3X-CVD. The total size of 8X-STC is 63% that of 3X-CVD, which can improve 37% power density under the same condition.

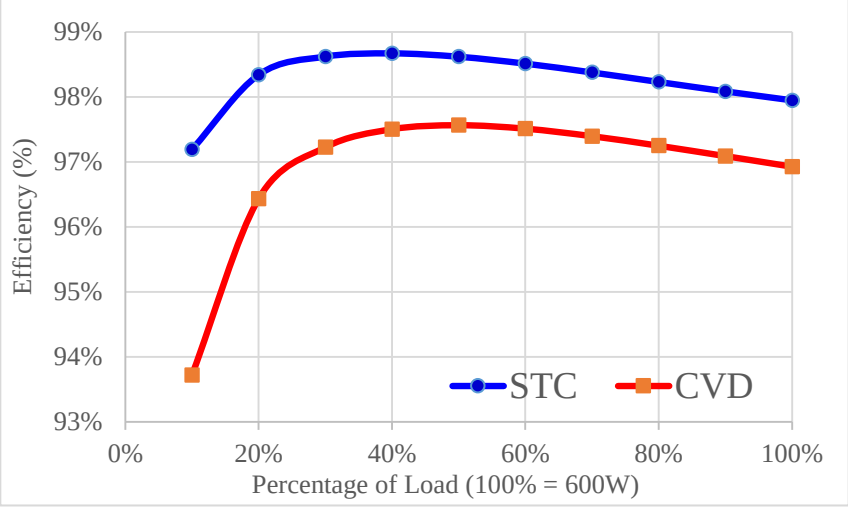


Figure 7.37. Comparison on system efficiency

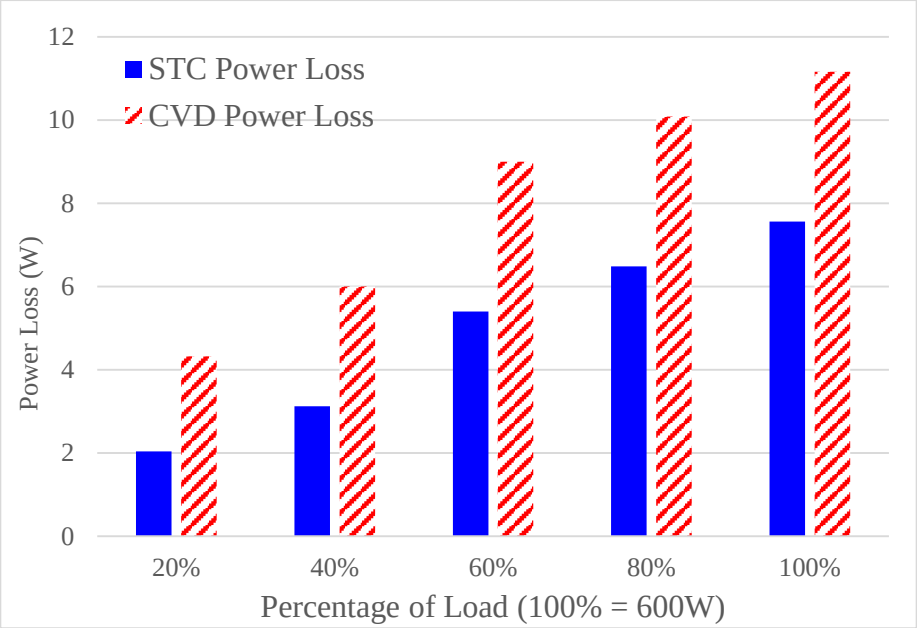


Figure 7.38. Comparison on power loss

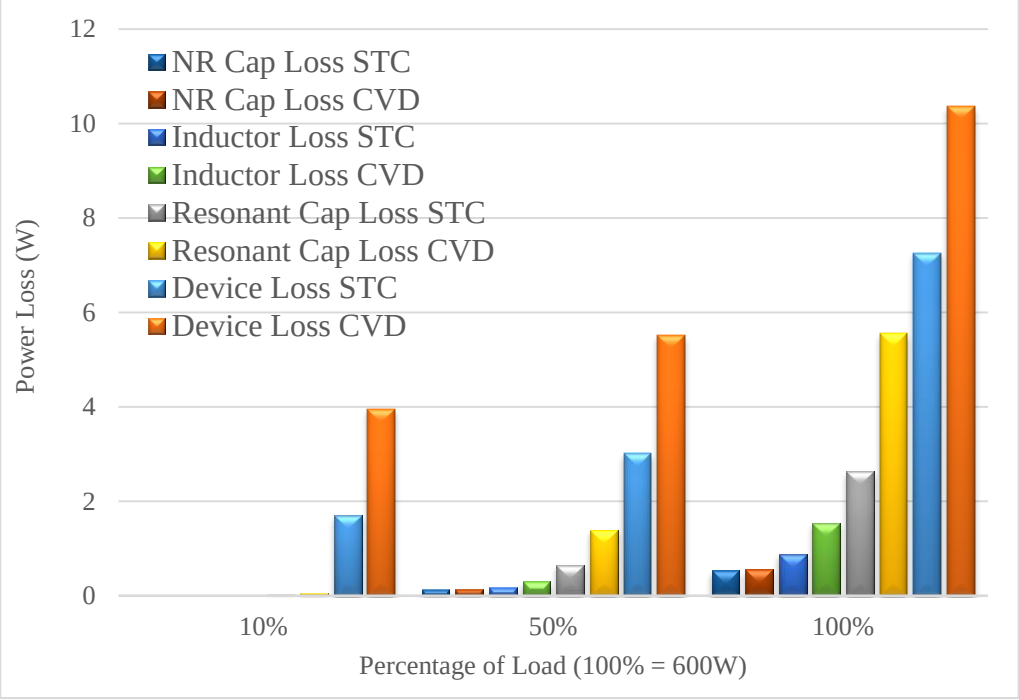


Figure 7.39. Comparison on power loss breakdown

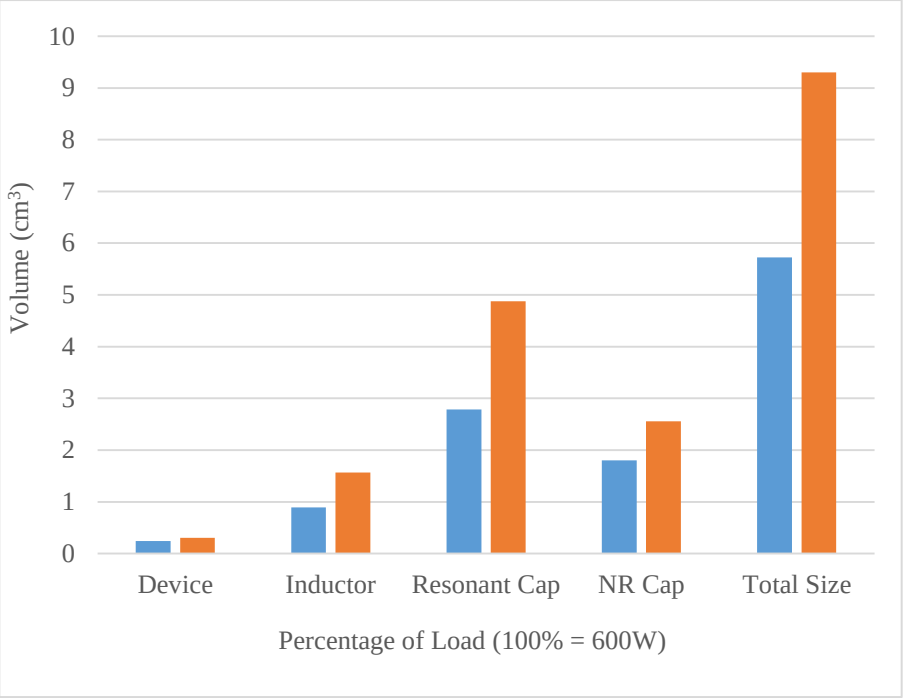


Figure 7.40. Comparison on size

This section presents comparison of switched-tank converter (STC) and traditional cascaded voltage divider (CVD) for data center applications. The detailed operation principle and equivalent circuits are shown. Simulations for each resonant components and device stress are compared. The whole system efficiency are fully compared and made breakdown analysis. It is shown that under the same condition, STC can achieve 1% higher efficiency at full load and over 2% higher efficiency at light load when compared with CVD. Under the same current stress, STC can achieve ~37% power-density improvement when compared with CVD. The ratio between input and output for CVD has to be 2^N, however, for STC it is flexible with ratio N.

7.8. Composite Modular Power Delivery Architecture and Future Work

Actually, switched-tank converter is a very good power delivery architecture. This is because all the devices are in-series to share the voltage stress and all modules are in-parallel to generate output current. Based on the detailed study above, this section will have a brief discussion

on this architecture, which can be named Composite Modular Power Delivery Architecture (COMPDA)

Fig.7.41 shows the generalized N-ratio COMPDA. N-ratio converter needs N-1 modular and each modular contains two cells and one LC impedance network. Each cell includes one half-bridge and one small clamping capacitor. Each device in the cell has the same output voltage stress and current stress. Assuming that the conversion ratio of Buck converter shown in Fig.7.42 is N, device stress can be defined as $V_{in}*I_o$. And assuming that $P=V_{in}*I_{in}$, then total device stress can be expressed as N*P. It can be easily got that the Flying-capacitor topology shown in Fig.7.42 is also the same N*P. Meanwhile, the proposed COMPDA ratio is also N. Then the total device stress can be expressed as 2*(N-1)*P/N. If the input power is normalized, the total device stress via different ratio can be compared and shown in Fig.7.43. It shows that the proposed converter has good feature of high-ratio conversion with much lower stress for total device when compared with Buck and Flying-capacitor topology.

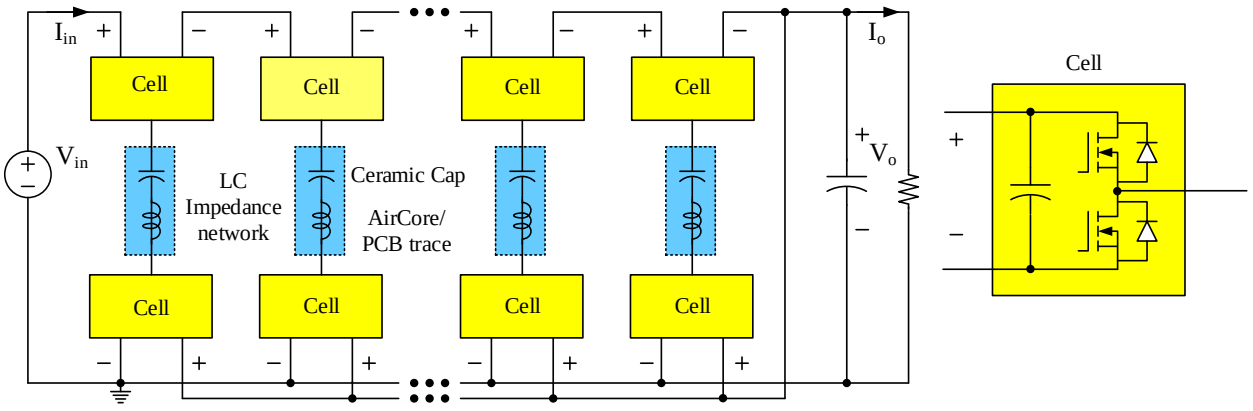


Figure 7.41. Composite modular power delivery architecture

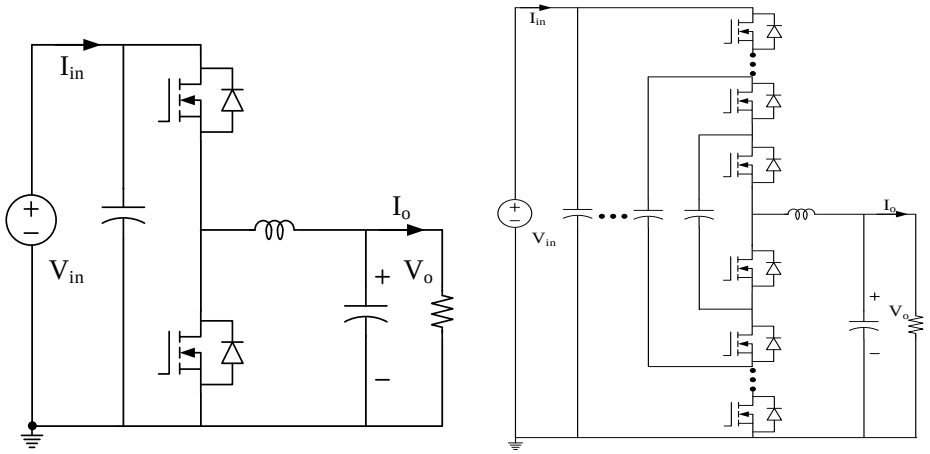


Figure 7.42. Buck converter and flying-capacitor converter

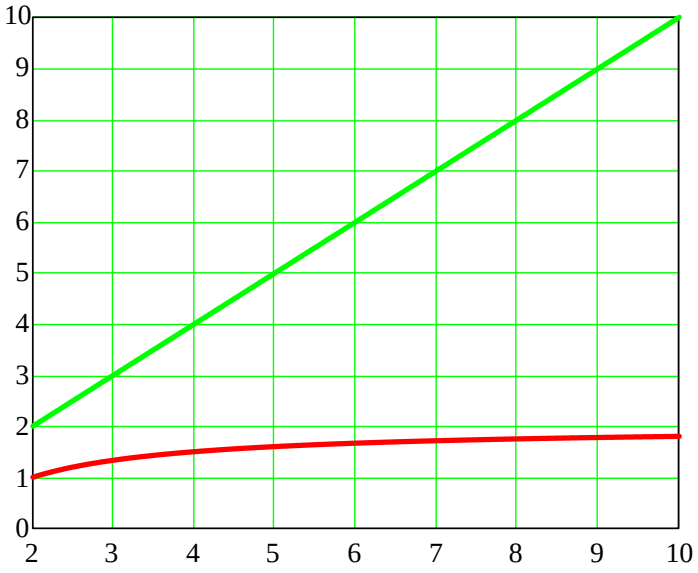


Figure 7.43. Normalized total device stress via different ratio

For the regulated applications, one regulator converter, such as Buck can be connected in-series on the input line or output line shown in Fig.7.44. The output V_o is the feedback parameter and this regulator just deals with low input current and can be low power guilty for the whole system. Fig.7.45 presents one example for COMPDA 4X DC-DC converter. And Fig.7.46 presents one partial power processing with Buck to have regulation function.

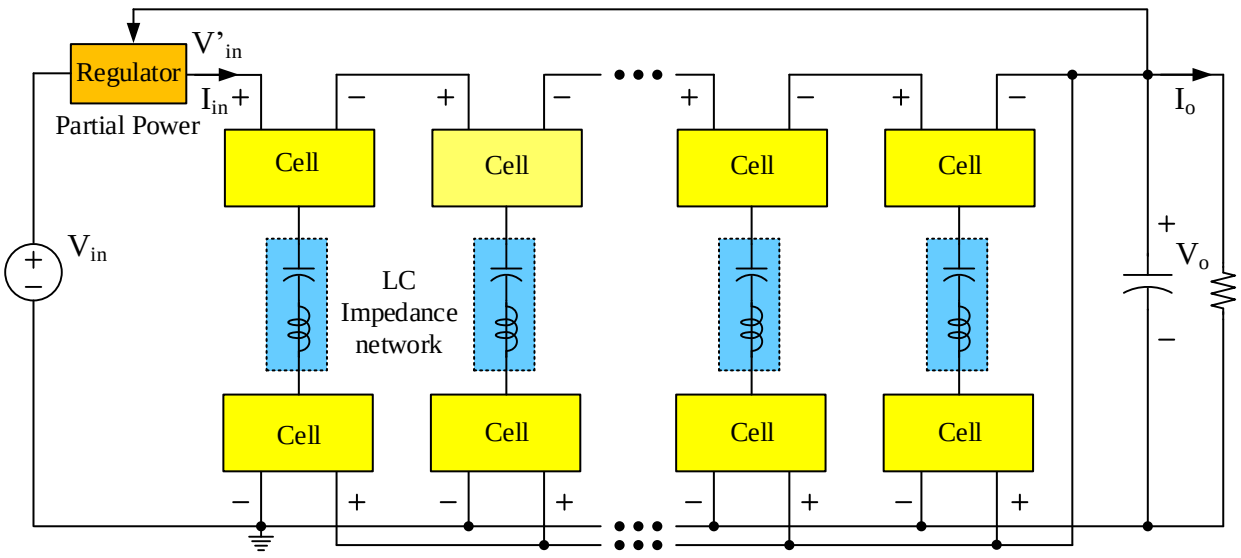


Figure 7.44. Regulated COMPDA based converter

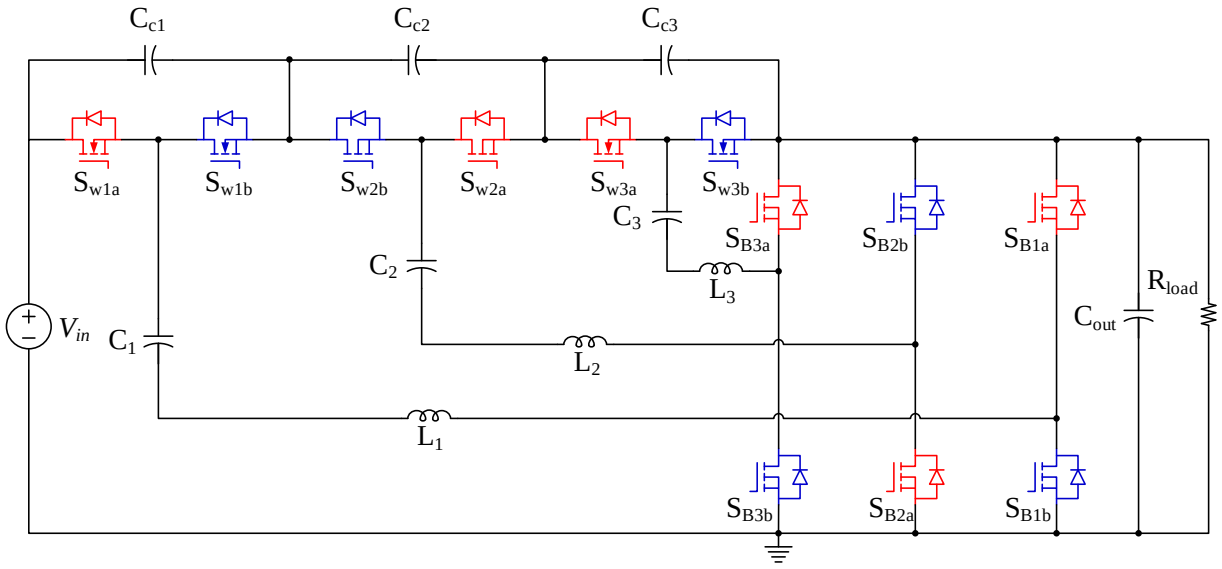


Figure 7.45. 4X COMPDA DC-DC converter

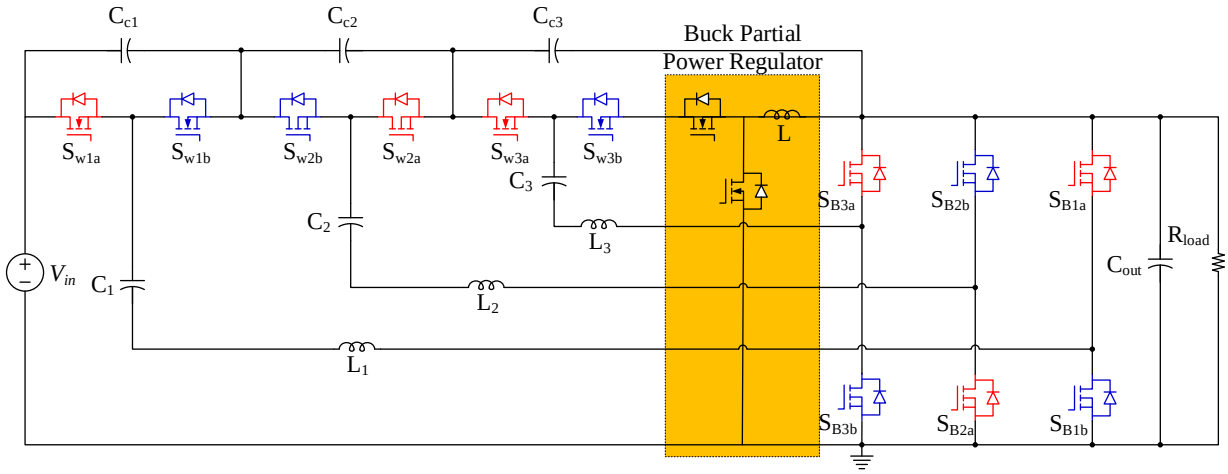


Figure 7.46. 4X COMPDA DC-DC converter with Buck partial power regulator

In conclusion, Composite Modular Power Delivery Architecture (COMPDA) has good features, such as same switch voltage stress and current stress, modular, low total device stress, suitable for all ratios, especially high ratio applications, partial power regulation. Actually, besides DC-DC STC applications, this smart architecture can generate various topologies applied in AC-DC buck rectifier applications, DC-AC boost inverter applications and AC-AC frequency changers.

7.9. Conclusion

In conclusion, in order to achieve ultra-high efficiency and high power density for the proposed converter, this paper presents the detailed optimal design for the resonant planar inductor and PCB design. Besides typical device loss analysis, the planar inductor and PCB copper loss are also important. It is shown that the proposed converter can be higher efficiency and higher power density when compared with some existing products. Furthermore, STC is compared with CVD and STC efficiency is higher than CVD. Good features of COMPDA is discussed in this section and will be further studied in the future.

8. CONCLUSION AND RECOMMENDATION

8.1. Contributions

This dissertation presents the high-power-density and high-efficiency converters for renewable energy applications. The contributions of this dissertation are as follows;

First of all, for the LED lighting applications, this dissertation proposed an advanced concave current control method applied in linear LED driver indoor application. The control method is patented and applied in the commercial products.

For PV applications, this dissertation proposed high-power-density inverter with in-series and in-parallel combinational power decoupling method. It can significantly reduce the dc-link passive capacitor and make the system high-power-density. Furthermore, beyond traditional 2^{nd} order decoupling method, this dissertation presented a novel instantaneous pulse power compensator (IPPC) method. When compared with traditional 2^{nd} order decoupling method, it can further increase system power density with little efficiency guilty. Furthermore, how to quickly design the controller for the grid-tied single-phase inverter is summarized in this section.

For EV/HEV application, interleaved three-phase inverters for segmented motor applications are studied under different control methods, such as SPWM, SVPWM and DPWM with tri-angle and saw-tooth, respectively. The best control method is investigated with interleaved control method. And optimal interleaved point is studied and compared with the industrial product.

At last, high-power-density and ultra-high efficiency switched-tank converter (STC) is proposed in this dissertation. It can replace the existing products in industry for 48V data center applications. The prototype is tested and verified. The project is cooperated with Google and the prototype will be applied for their data center application in the near future.

8.2. Recommendation for Future Works

Here are some recommendation for future works. For IPPC methods in Chapter 4, actually it can be applied for not only single phase inverter system, but also three phase inverter system. As three phase inverter system has higher power rating and lower switching frequency when compared with single-phase inverter, it can be better applied in three phase inverter with IPPC method. However, unlike single-phase inverter pulse current, three phase inverter has more complex current shape. So how to deal with this complex pulse current with simple injection decoupling circuit is a difficulty.

Besides the inverter applications, dc-dc resonant converter for data center application is still has some issues to solve, for example, how to adjust the dc-dc switched-capacitor ratio with the existing topology still needs to be investigated. Also, besides in-series LC resonant impedance network, other resonant networks are also interested in the future works. Composite Modular Power Delivery Architecture are applied into DC-AC, AC-DC and AC-AC applications, which is a very interesting topic. For example, single-phase DC-AC inverter and three-phase DC-AC inverters can be applied with COMPDA. Also AC-DC rectifiers are also suitable. More research work will be going for the high-power-density and high-efficiency converter for different renewable energy applications in the future.

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