ELECTRICAL PERFORMANCE ANALYSIS OF A NOVEL EMBEDDED CHIP TECHNOLOGY

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Ferdous Sarwar

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By

Ferdous Sarwar

The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

DOCTOR OF PHILOSOPHY

SUPERVISORY COMMITTEE:

Dr. Val Marinov

Chair

Dr. Orven Swenson

Dr. Om Prakash Yadav

Dr. Chao You

Approved:

June 12, 2012 — Date

Dr. John R Cook — Department Chair

ABSTRACT

Recently ultra-thin embedded die technology gained much attention for their reduced footprint, light weight, conformality and three-dimensional assembly capabilities. The traditional flexible circuit fabrication process showed its limitations to meet the demand for increasing packaging density. The embedded die technology can be successfully utilized to develop flexible printed circuits that will satisfy the demand for reliable and high density packaging. With a tremendous application potential in wearable and disposable electronics, the reliability of the flexible embedded die package is of paramount importance. Presented is the author's contribution to the novel fabrication process for flexible packages with ultrathin (below 50 µm) dice embedded into organic polymer substrate and the results from the investigation of the electrical performance of embedded bare dice bumped using three different techniques. In this research, embedded flexible microelectronic packaging technology was developed and reliability of different packages was evaluated through JEDEC test standards based on their electrical performance. The reliability test of the developed packages suggested the better and stable performance of stud bump bonded packages. This research also covered the thinning and handling ultra-thin chips, die metallization, stud bump formation, laser ablation of polymers, and assembly of ultra-thin die. The stud bumped flexible packages that were designed and developed in this research have promising application potential in wearable RFID tags, smart textile and three dimensional-stacked packaging, among the many other application areas.

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DEDICATION

This dissertation is dedicated to my family and friends who have meant so much to me in my life and during my journey to obtain my Ph.D. To my wife, Rukhsana Najnin for always encouraging me with kind words during my bad time. I could not have gotten through this without her. To my grandmother, Late Professor Jannatul Ferdous, who was my inspiration for starting this journey and would be very much proud to hear about my finishing the degree. To my mother, who has always been proud of me. To my father, whose wisdom and knowledge I hope I have inherited, and who has never stopped urging me to learn more. To all my aunts, uncles and cousins, who always make me feel the warmth of a big family. Without the support of my friends and family, I could not have made it this far.

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CHAPTER 1. INTRODUCTION

In the microelectronics industry, the importance of assembly and packaging is increasing and is often considered the limiting factor for cost and performance of microelectronic devices. The drive towards low cost, miniaturization, functional and integration density has created advanced concepts for microelectronic packaging. The concept of wearable, conformal and flexible electronics will create a significant trend in next generation electronics when flexible silicon dice are embedded into flexible substrates. If the die thickness is reduced below 50 µm, the die becomes flexible. If the dice are mounted using flip chip technology, without any underfill, the fabrication process will be very cost effective with enhanced productivity compared to traditional flip chip technology.

In pursuit of the miniaturization of the package, unpackaged bare dice were introduced to reduce the package footprint significantly. The next step towards miniaturization was the functional integration of sub-systems, i.e. System-in-Package [1-3]. The latest trend for function integration gained a high momentum with the advent of embedded chip technology [4-6]. Embedding of active and passive circuitry in the substrates became a reality with the incorporation of ultra-thin chips. One of the first introductions of the embedded chip technology (known as “Chip in Polymer”) was accomplished by Fraunhofer IZM and TU Berlin [7, 8]. The variation of this technology is being practiced to fabricate multi-stacked chip package [9]. The first stage of this novel technology was accomplished by embedding a die in the PCB build up layer (Figure 1). The embedding of thin chips into flexible substrates offers various advantages such as good electrical performance, miniaturization and possible low cost [10]. In this method, interconnects having shorter length provide lower power dissipation and better electromagnetic shielding [11]. Due to coefficient of thermal expansion (CTE) mismatch of the materials in the

embedded package, die cracking and metal bump failure may create serious issue in terms of process yield and service life.

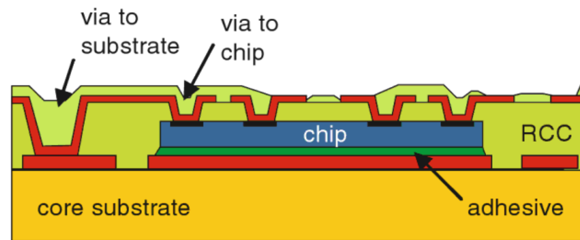

Figure 1 Schematic view of an embedded die in a PCB build up layer [12]

Flexible electronic devices based on ultra-thin chips find new and exciting applications in microelectronics, wearable and low-cost disposable electronics, space applications, MEMS, solar cells, document security, biomedical and other fields [13, 14]. An application area with a huge marketing potential for ultra-thin chips are the low-cost, disposable single-chip electronic products such as RFID tags and bank cards. The most widely used technology for fabricating these products is based on an embedded flip chip bonded to an etched (or printed/stamped) spiral antenna. Flexibility is an essential requirement for an RFID tag/smart label that needs to bend repeatedly or conform to random-shape surfaces. Bank cards are laminated under pressure at high temperature. Under these conditions, it may be expected that the rigid and fragile thick dice would crack. The use of ultra-thin, flexible silicon dice should reduce the probability for mechanical failure in these applications.

In this research, electroplating (or wire bonding), laser micromachining and polymer thin film technology was integrated to achieve the robustness of the package. Integration of a 50μm thick bare test die into a liquid crystal polymer (LCP) substrate was accomplished in order to demonstrate the embedded die structure. The ultra-thin dice were singulated using deep reactive

ion etching (DRIE) technology. An LCP substrate was micro-machined by Nd: YVO_4 laser ablation method. The bare die was metalized using wire bond, micro-lithography and electroplating techniques. The proposed method involve transferring a bumped die inside a receptor pocket and filling the ablated trenches with conductive ink containing silver micron-sized particles using a squeegee, referred to as polymer thick film inlaid (PTFI) method. Laser micro-machined vias were used to connect the pocket and the trenches. In this work, the point of interest was to determine the process yield. In embedded technology, defective dice cannot be reworked, so only known-good dice (KGD) are considered for the experiments. On the other hand, the Cu interconnects can result in thermal and mechanical fatigue failure. The thermal management of the embedded dice is another important issue. This method applied the concept of flip chip technology due to some advantages over traditional wire bonding such as increased functionality, superior signal integrity and reduced package footprint [11]. This method increases the electrical performance of flip chip by reducing the interconnection length, and consequently reducing the package thickness. This is desirable for those industries having a drive for the low z-direction profiles such as mobile phone applications. The additional advantages are the reduced form factor and increased functionality.

The RFID market is already estimated in trillions of tags per year [15]. The bank cards used in the U.S. usually store data on a magnetic stripe. Most of the developed countries are already replacing the magstripe cards with the so-called “smart cards” in which the encrypted data is stored in an embedded chip. Replacing all payment cards only in the U.S. could cost as much as $2.85 billion [16] creating yet another big market segment for the embedded ultra-thin chip technology.

Another exciting new application is the RFID banknote. There are indications that the European Central Bank [17] and the Bank of Japan [18] are considering embedding chips into the banknotes to foil counterfeiters. This would create an additional huge market for the embedded ultra-thin chips. Banknote paper is typically 80 to 100-µm thick which necessitates the use of ultra-thin dice. To address this application, Hitachi Ltd. has developed its µ-Chip, a 0.15-mm square, 7.5-µm thick chip [19]. It is unclear what technology the company uses to embed this chip into the banknotes.

The current drive of the microelectronic industry towards miniaturization of electronic products leads to development of low profile electronic packages that offers smaller space requirements, lighter weight, portability and higher functionality. These characteristics are very significant in the development of miniaturized electronics and handheld products such as e-reader, tablets, smart phones, notebooks, RFID tags, digital cameras, human-body adapted medical devices and portable game consoles. The concept of flip chip technology paved the way for the versatile use of flexible electronics in consumer electronic products.

1.1. Flip Chip Technology

Flip Chip is an advanced form of surface mount technology (SMT), in which semiconductor chips are flipped upside down and bonded directly into or onto rigid or flexible substrate (Figure 2). This technology uses an area array formation that gives the highest I/O interconnection density compared to other bonding techniques and thus proved its potential in complex system architectures and high-density packaging [20]. Flip chip can be attached to the package (level 1 of the IC packaging hierarchy), to the multi-chip module (level 1.5) or directly to the substrate (level 2). Typically, electrical connection is maintained through conductive bumps fabricated on the functional chips.

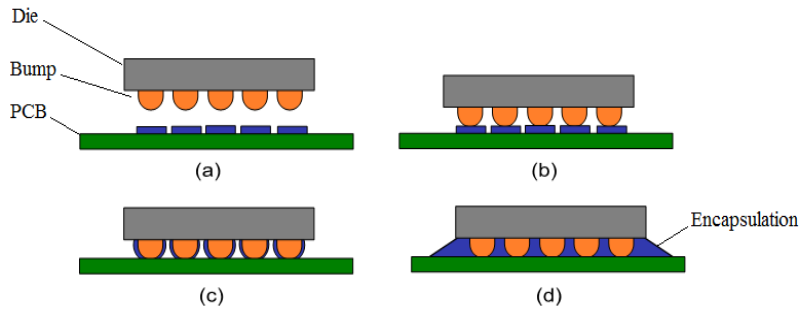

Figure 2 Illustration of flip-chip technology. Flip-chip package with (a) solder-plated metal balls and pads on PCB; (b) flux application and placement; (c) reflow soldering; (d) underfill

There are different types of flip chip methods such as flip chip on glass (FCOG), flip chip on flex (FCOF) and flip chip on rigid substrate. FCOG is defined as the process to mount the IC directly on to the glass [21]. This technology is commonly used for flat panel display production (Figure 3) [22].

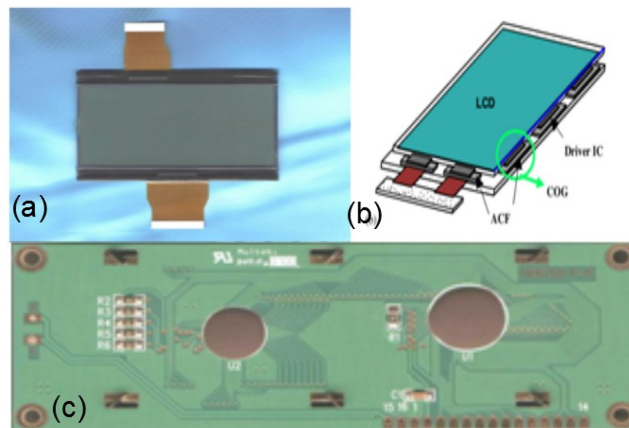

Figure 3 (a) The cross-section of COG (b) A sample of COG-COG bonding using ACF in LCD modules (c) Flip chip on rigid substrate [22, 23]

Flip chip components can be mounted on rigid substrates such as FR-4 [24] or ceramic [25] (see Figure 4c). Witty et al [26] reported that flip chip reliability is governed by combined materials interactions after evaluating many materials and assembly process combinations.

The method in which a chip is attached directly into or onto the flexible substrate is termed as flip-chip-on-flex (FCOF) [27, 28]. It is rapidly becoming an attractive process for the construction of microelectronic devices. It requires minimum footprint, has the lowest form factor and the direct interconnection between die and substrate improves electrical performance [29]. Flip chip on flex achieved a reduction in the interconnect inductance also. The die bond-pad pitch is generally in the range of about 0.175–0.25 mm [30]. The use of flexible circuits enables lower product weight and size, and eliminates multiple substrates and the associated cost and reliability risk of interconnections. These circuits are lead-free and flux less. The other advantages are the low process temperature and higher interconnection density. Different application of this technology is shown in Figure 4.

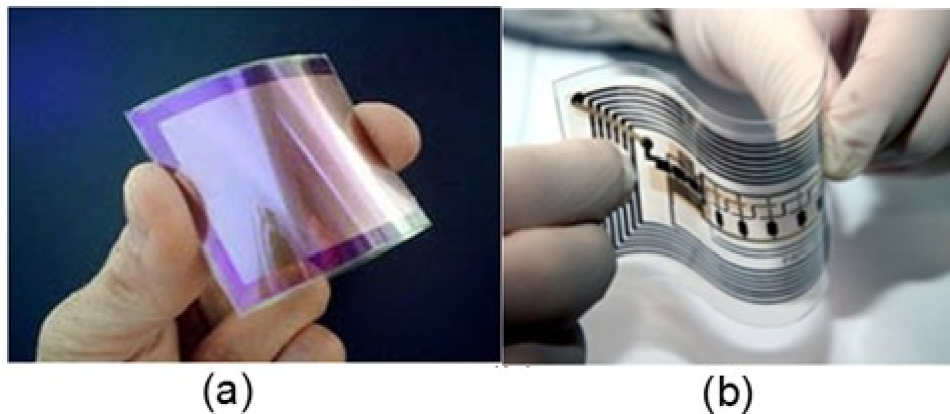

Figure 4 Application of flexible chip assembly (a) Flexible battery developed in University of Waseda, Japan (b) Printed RFID from Sunchon National University, Korea

1.2. Embedded Die Technology

The conventional IC package is nothing but a small piece of silicon, or a bare die, attached to and encapsulated in a plastic encasement with bonding wires or balls and a metal lead system for connecting the die circuit to the external world. These additional elements of the IC package serve to protect the die and facilitate the assembly process, they are not essential to the

functions of the chip. Miniaturization requires the size of the electronic components to be as small as possible. To reduce its footprint, the IC package has to shed all these nonessential elements, ultimately leading to what is known in the industry as a wafer-level package. The transition from a plastic to wafer-level IC package reduces the footprint but this may not be enough for a flexible electronic device. The flexibility of the package can be achieved only if the thickness of the silicon die is reduced to 50 µm or less [31, 32]. Embedding bare dice in the substrate allows the entire device to bend and flex uniformly like one homogeneous material. Since the die can be placed at or near the neutral plane, the bending stresses in the silicon will be minimized thus reducing the probability for fracture failure. Die embedding provides a solution for realizing a 3D packaging integration with the highest level of miniaturization [14, 33-35] as well as designing hybrid systems in which the thin silicon IC technology compliments the printable electronics to create highly efficient and inexpensive devices [14]. The use of embedded thinned Si devices also provides the advantage of reducing the parasitic influences of Si which is especially advantageous for high frequency (GHz) devices [36]. It is well known that the shorter interconnects provide a better electrical performance [35].

Cost is of a paramount importance especially for the disposable electronics. Cost of silicon is often times the largest contributor to the total cost of a disposable electronic device such as an RFID tag [37]. It is well known in the trade that the cost of the semiconductor die scales with area raised to the 1.5 – 2 power [34]. Therefore, reducing the die size by half would reduce the cost of silicon by a factor of 8 to 16. Cost depends also on the die thickness. Thinner wafers mean more slices from the ingot, ergo, less cost per wafer.

The embedded technology is classified into two main categories: embedding of passive components and embedding of active devices. The embedded capacitors are classified based on

the properties of dielectrics (paraelectric or ferroelectric) that control the sheet capacitance values. Embedded resistors are created by stencil or screen-printing of resistive pastes [38]. The resistance per square can be controlled by dispensing intrinsically conductive polymers (IPC) using drop-on-demand ink-jet device [39]. Embedded inductors are patterned on a metal layer on organic substrates using traditional metallization technology [40].

Embedding of active devices was accomplished through different approaches such as integrated module board technology, chip in polymer and chip embedding in flex technology. The embedding process is completed by placing a functional die inside a PCB or flex substrate to facilitate miniaturization and functional diversification. This concept proved very helpful to realize wearable electronics [41]. The functional die is connected to the conductive traces through plated or conductive paste filled microvias. The die may be bumped or sputtered, depending on the purpose and reliability level of the package. The traditional fabrication process of the flip chip technology can be successfully used with necessary modification. The embedded die technology opened the door to the research of ultra-thin die integration in the embedded system. The bumps may be solder balls [42], printed polymer bumps [43], electroplated/ electroless plated bumps [44] or stud bumps [45]. Au, Cu and most solders such as 95Pb5Sn, 63Sn37Pb (eutectic), 50Pb50In and 37Pb63Sn are used for bumping [46]. Christiaens et al [47] reported a fabrication process for embedding 15 µm thin dice in between polyimide layers in a sandwich-like configuration with a thickness of 50-60 µm. In their approach, PI was spun on a rigid career and BCB was dispensed on PI. Then the ultra-thin die was placed face-up, following spinning of another PI layer on the top of the die. Later, through-hole vias were laser micro-machined and metalized to ensure electrical connections. The process flow of the UTCP method is shown in the Figure 5. There are a number of packaging technologies developed for attaching

the ultra-thin bare die to the flexible substrate. Some of them are briefly discussed in the next sections.

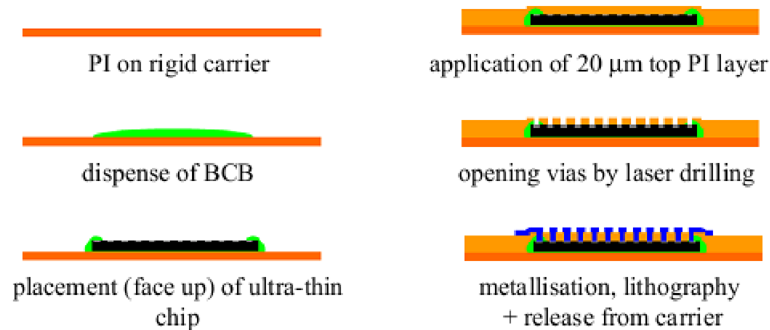

Figure 5 Overview of UTCP process flow [47]

1.2.1. Flip chip bonding of dice onto the substrate surface

In the conventional flip-chip technology, also called chip-last approach [48], the dice are flip-chip bonded face down. The flip chips are then assembled either using reflow soldering [49-51] or thermode bonding [51-53]. The major advantage of the flip-chip technology is its maturity. The drawbacks are the larger overall thickness of the assembly, the need for underfill, and placing the fragile die away from the bending neutral plane, thus increasing the probability for brittle fracture under bending. In an attempt to reduce the overall thickness, R. Wayne Johnson's group at Auburn University [51, 54-56] suggested soldering the flip chips to pads on the opposite site of the substrate by placing solder or stud bumps into through-vias.

There are indications that in the case of ultra-thin dice the flip-chip soldering may be a problem [57, 58]. Using anisotropic conductive adhesives has shown promising results especially for heat sensitive substrate materials but it may lead to die fracturing due to high bonding force applied to realize conductive paths between the die and substrate pads [59]. It is also difficult to

control the dispensing of a suitable amount of adhesive [60]. More details about the thermode and adhesive bonding of ultra-thin flip chips are available in [53].

1.2.2. "Sandwiching" the die between the substrate and a cover film(s)

In this chip-first approach the die is first bonded to the substrate face up and then covered with a dielectric layer. The coverlayer is then exposed and developed to access the die pads for electrical interconnection and additional routing. In another implementation, called isoplanar interconnection [57, 58, 61], the conductor lines are led across the die edge and then connected to the circuitry on the top of the coverlayer. The chip-first approach has been and is still being actively developed mostly in Europe, especially by the Fraunhofer group in Germany [13, 35, 57, 58, 61-63] where it is called "Chip-in-Polymer," abbreviated CHiP or CiP. A similar technique was developed in Belgium as reported by Iker et al. [48] and Christiaens, Vanfleteren and co-workers [33, 64]. In the method developed by Samsung [65] the chip attachment and electrical connections are performed simultaneously before laminating the substrate. Alternative chip-first methods are discussed in [66].

1.2.3. Integrating (embedding) the die into the substrate (Chip-in-Flex)

The difference between this and the previous method is that through or blind holes are machined in the substrate to accommodate the bare die. This approach has been demonstrated by Texas Instruments [67]. In the process developed at the Helsinki University of Technology [68] the bare die is placed face down into through holes drilled in the substrate and then encapsulated using elastic molding compound. The electrical interconnections are realized on the back side of the substrate following the routine photolithography/electroless copper deposition sequence. In another modification of this approach [69], the cavity is not fabricated in the substrate but in a thick layer of photo-definable polyimide spin-coated onto the base polyimide layer. Another

polyimide layer is spin-coated to cover the die and provide a surface for metallization and interconnection. The most important fabrication methods of the embedded die technology are described in the following sections.

1.3. Wafer Thinning

In today's microelectronics industry, the advancement in wafer thinning technology is pushing towards thinner and smaller package to facilitate portable and hand-held products. The microchip's thermal resistance can be lowered by improving heat dissipation through use of thinner wafer [70]. The standard thickness of the Si wafer is in the range of 500-700 μm whereas the thickness of the active layer ranges from 3 to 10 μm [71]. The flexible substrate requires not only a small but a flexible bare die. This can be achieved only if the thickness of the silicon is reduced to 50 μm or less [31, 32]. Fragile yet flexible enough, the ultra-thin bare dice provide the flexibility required for the flexible electronics applications. For example, the allowable bend radius for a 25 μm thick silicon wafer is only 1 cm [72]. The reasons for the acquired flexibility are quite simple – the maximum tensile and compression stresses in a plate subjected to bending develop on the outer and inner surface of the plate and are proportional to the plate thickness. If this thickness is small enough, as in the ultra-thin dice, the bending stresses are below the fracture limit, turning an intrinsically brittle and rigid material such as silicon into a flexible material. Obviously, the thinner the die the more flexible it becomes. The die will not be subject to fracture provided that the die must be placed on or around the neutral plane of the flexible substrate. Different processes are available in the industry to thin wafer such as mechanical surface grinding, plasma etching, wet etching and chemical mechanical polishing (CMP).

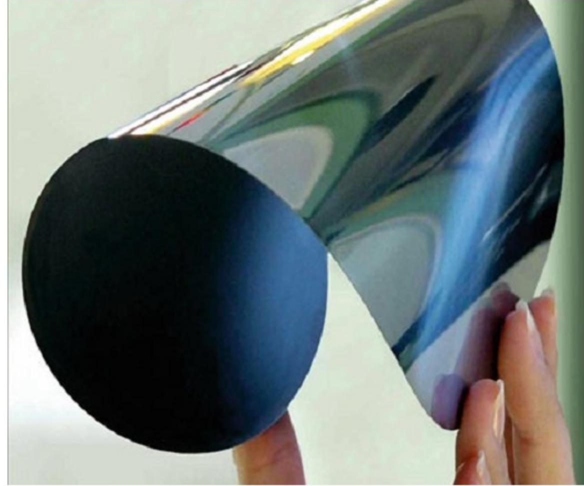

Figure 6 Flexible 50 µm thin wafer [14]

In microelectronic industry, wafer back-grinding technology is used to reduce wafer thickness for chip fabrication. This is one of the most important technologies necessary to pave the way for ultra-thin die fabrication. Embedded packages and multi-stacked packages cannot be realized without advancement of wafer back-grinding technology. A significant amount of R&D efforts have been invested in the wafer thinning technologies to facilitate the ultra-thin die fabrication. With course of time, wafer backgrinding method such as mechanical grinding, chemical etching, chemical mechanical polishing (CMP), deep reactive ion etching (DRIE), and atmospheric downstream plasma (ADP) have been evolved. In semiconductor industry, the grinding is performed in two stages; coarse grinding (350-500 grits) and fine grinding (2000-3000 grits). A thick wafer can be thinned to required thickness. In order to fabricate ultra-thin embedded die package, wafers of 50 µm thickness is necessary as they become flexible (as shown in Figure 6).

Handling and processing is a major issue regarding ultra-thin wafers. Chipping, cracking and rough edge formation were observed while dicing thin wafer. Die strength deteriorates due to crystal defects, scratches and stress formation while thinning [73]. It was reported that

subsurface damage may occur due to back-grinding. Blech and Dang [74] reported the effect of mechanical grinding on the deformation mechanism of wafer. The die fracture strength was studied based on surface roughness and removal thickness. It was also reported that plasma etching of silicon improves the fracture strength and flexibility in the wafer [75]. Grinding direction also has a considerable effect on the die strength [76]. Dicing before grinding (DBG) method was reported as a suitable method for ultra-thin dice enhancing the chip strength around 10-15% [77]. The stress relief method such as chemical mechanical polishing (CMP), dry polishing, wet chemical etching, dry or plasma etching can be used to control the initial die strength of the silicon.

1.3.1. Mechanical surface grinding

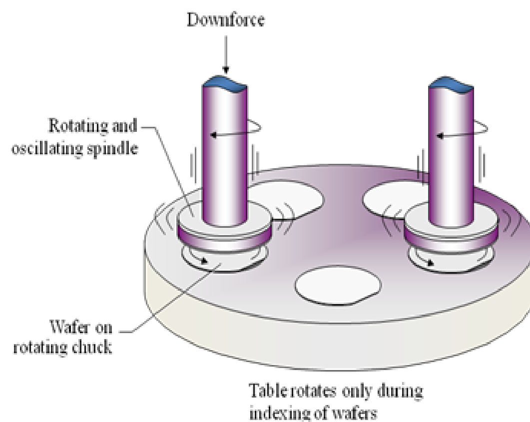

Figure 7 Schematic of the wafer backgrinding process [78]

This is a widely used technique in industry where a thick wafer is thinned by lapping method using diamond abrasive grinding wheel. The grinding is accomplished in two steps, coarse grinding and fine grinding [79-81]. The coarse abrasive grinding wheel (typically 350–500 grit diamond) creates defects on the wafer’s backside surface while thinning it rapid (as shown in Figure 7) [81]. In order to remove the damage and reduce the surface roughness, coarse

grinding is followed by fine grinding using finer abrasive (typically 2000-3000 grit) [82]. The main drawback of mechanical grinding is the significant stress and damage induced in the wafer. Chen and Wolf [81] reported the evidence of warpage in the wafer due to stress and showed that the stress can be mitigated using dry etching. Jiun et al [75] studied the difference of the surface polish for coarse and fine grinding using atomic force microscopy. The evidence of subsurface damage was also investigated by various research groups [83-86]. It was also reported that the fracture strength of dice depends on the grinding orientation [76, 87]. The fast rate of material removal made the mechanical grinding method affordable for industrial use.

1.3.2. Chemical mechanical polishing (CMP)

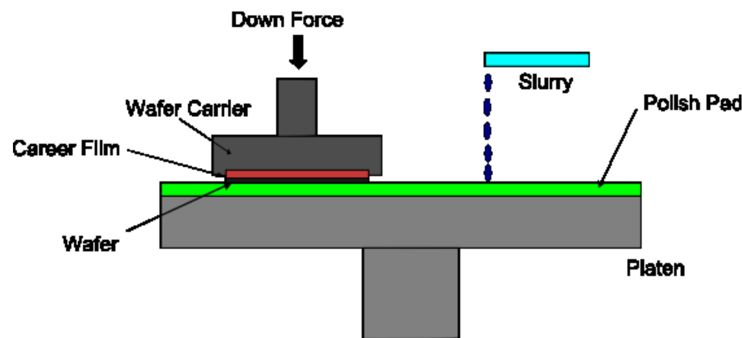

Figure 8 Chemical mechanical polishing

In this process, the rotating wafer surface is thinned by pressing against a polishing pad (polyurethane) which rotates in the same or the opposite direction of the wafer rotation (Figure 8). CMP can be used in silicon wafer fabrication along with IC manufacturing [88]. In silicon wafer fabrication it plays the role of final material removal step. Slurry containing silica [89] or ceria particles [90] is used to remove silicon from the wafer surface. The material removal in CMP process is a combined result of chemical reaction of the slurry with the wafer surface and the mechanical interaction between the pad and the wafer [91].

1.3.3. Wet chemical etching

Wet chemical etching is widely used in the wafer manufacturing industry. The thinning can be accomplished by spin etching technique. In this process, the etchant (usually a mixture of HF: HNO3) is applied on the rotating wafer in the form of thin jet of stream. The mechanism of wet chemical etching is shown in Figure 9. The etchant rate can be controlled by changing the mixing ratio of hydrofluoric acid (HF) and nitric acid (HNO3). The KOH etch provides a uniform etching rate, but results in a rougher surface than the acid etch due to crystallographic orientation dependency of KOH etch mechanism [92].The 10 μm/minute etch rate obtained in this method is generally used to achieve industrial grade etching standard. The surface flatness is a function of the etching time and the flow of etchant across the wafer surface. The total thickness variation (TTV) value of wet chemical etching is comparable to that of CMP process. The roughness value of spin-etched silicon is below 1 nm [93]. The unique ability of this process is reducing stress in wafers and planarizing the device surface.

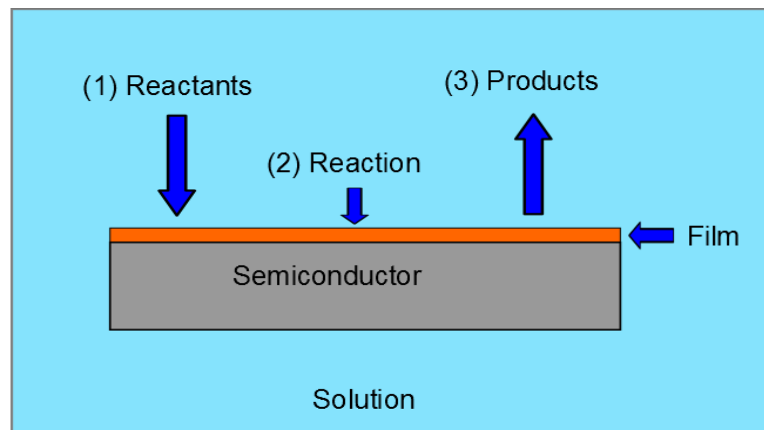

Figure 9 Mechanism of wet chemical etching: 1) Reactants transported by diffusion to surface 2) Reactions occur at surface 3) Products from surface removed by diffusion

1.3.4. Plasma etching

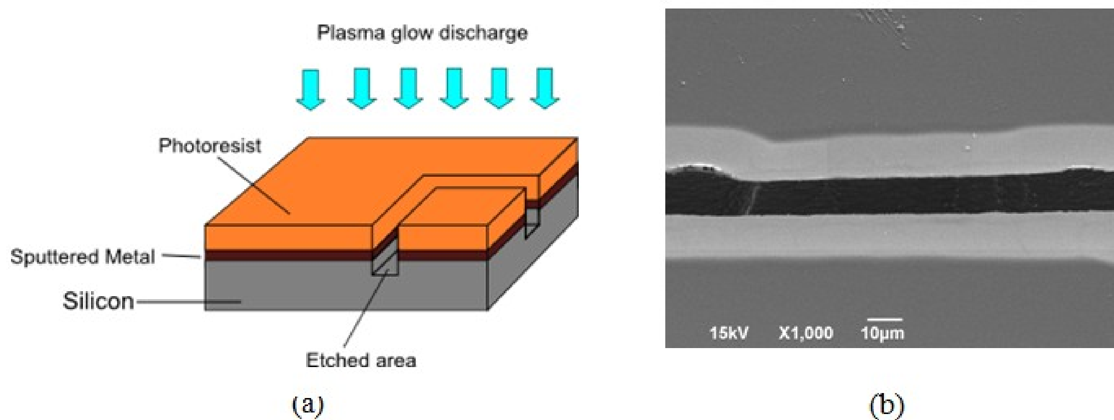

Figure 10 (a) The schematic view of plasma etching of silicon (b) 20 μm wide trench created by deep reactive ion etching of silicon

The use of plasma etching in silicon thinning is popular in electronic device microfabrication, especially in microelectromechanical systems (MEMS) [94-96]. The plasma is generated by ionizing gaseous etchants within an electrical field into electrons, radicals and neutral particles. Etching process is comprised of the three sequential steps of adsorption, reaction and desorption. The silicon surface is bombarded by the reactive radicals that combine with silicon atoms to form a volatile substance that escapes from the bulk silicon with the assistance of heat or lower pressure. The schematic view of plasma etching and 20 μm wide trench created in this method is shown in Figure 11a and 11b. Atmospheric Downstream Plasma (ADP) process is the most successful plasma etching process developed by TruSi Technologies [97]. ADP has some unique advantages such as absence of devise protection, resist application and defect removal by wet etch [98]. The successful use of ADP in the dicing by thinning technology was reported [99].

1.4. Flexible Substrate Materials

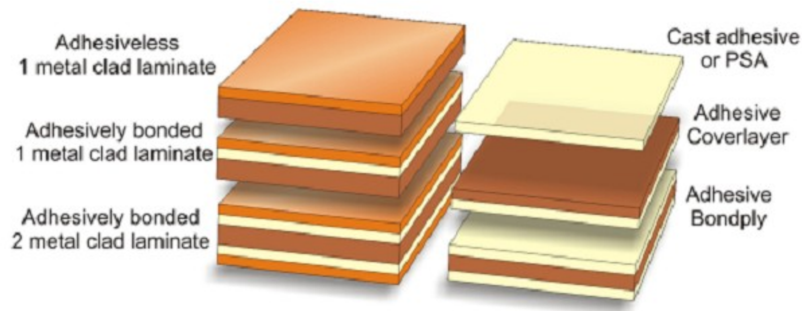

Figure 11 Basic material used in flex circuits [105]

The major function of the substrate is to mount the ICs and components or provide for the integration with external circuit elements. An ideal substrate for microelectronic application should have some unique properties [100] such as good insulating characteristics, low dielectric constants, high strength and toughness, high dimensional stability and low coefficients of thermal expansion. Flexible circuit materials, being thin and compliant, can be used as substrate to handle high-density chips with very good results. The overall cost is also determined by the substrate material. Polyimide is routinely used today due to its excellent electrical and mechanical properties, including high-temperature processing capabilities unattainable by the other common materials. Unfortunately, polyimide is an expensive material. Cheaper materials such as PEN or PET can reduce the substrate costs by a factor of 5–10 [101]. The use of these materials mandates a change in the substrate technology from etched copper to printed conductors [102]. The polyimide class of substrate, such as Kapton ® (Dupont), Apical ® (Kaneka Texas Corporation), Norton TH ® (Saint-Gobain Performance Plastics) and Kaptrex ® (Professional Plastics Inc.) is noted for extra-ordinary high-temperature performance [103]. The tensile strength is typically in the range of 75-90 MPa. Polyimide films do not usually need to be mixed with flame retardants due to inherent resistance to combustion [104]. Thin polymer films

are used as the base dielectric in flexible circuits. Various type of commercial polymer can be utilized for the purpose as a support structure for the electrical interconnection pattern. The material composition of flexible substrate is shown in Figure 11.

1.4.1. Polyimide

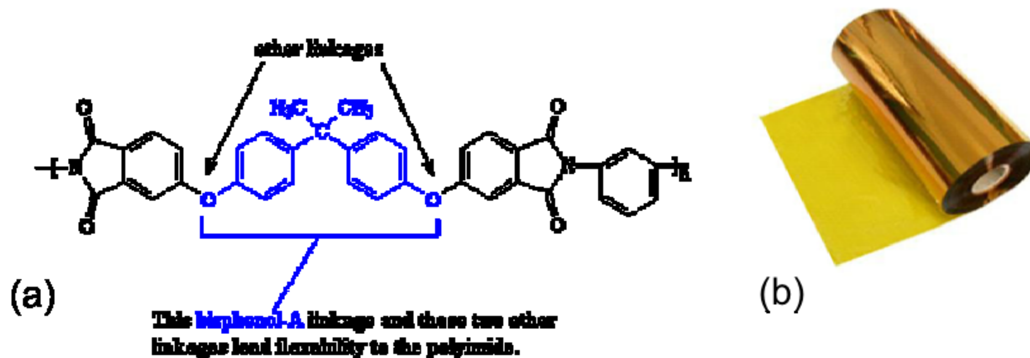

Figure 12 (a) The chemical configuration of polyimide (b) A roll of off-the-shelf polyimide

Polyimide belongs to the family of high temperature thermosetting polymers that are widely used in high-density flexible circuit application (Figure 12)[106, 107]. It was first developed by DuPont™. It has some outstanding properties such as excellent electrical insulation, high mechanical strength, high temperature endurance and excellent chemical resistance [108]. The nitrogen and carbonyl groups in its polymer structure have provided these characteristics that support their application in fine feature electronics and roll-to-roll fabrication. The copper cladding can be applied on the polyimide base film with or without adhesive. Adhesive polyimide laminate has some drawbacks such as high thickness and weight, less adhesive strength at higher temperature and copper thickness limitation. The adhesive-less laminates are thin and light which are used in the interconnection of hard drive and chip scale packages. Polyimide absorbs moisture at a high rate [109] which is considered as a major

drawback. As water has a polar molecule, the high moisture absorption degrades signal performance of the embedded chip at high frequencies [110].

1.4.2. Liquid crystal polymer (LCP)

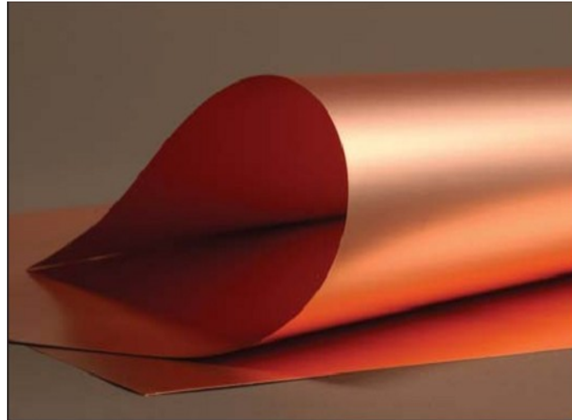

Figure 13 Copper-cladded ULTRALAM® 3000 series liquid crystalline polymer

Liquid Crystal Polymers belong to thermoplastic aromatic polyesters. The segments of the polymer can be aligned in a near crystalline structure in the molten or liquid state which creates its name. Printed circuit manufacturers initiated the use of LCPs for application in multilayer circuits [111]. LCPs are lower in cost than Teflon® (Dupont) and ceramic based materials. It has some excellent properties such as low loss factor of 0.004 and low dielectric constant [112]. LCPs are expected to be widely used in high moisture environment as their moisture absorption is less than 0.1% [113]. The other important advantages are low coefficient of thermal expansion (CTE), high temperature capability, excellent dimensional stability and extraordinary barrier properties for hermetic packaging [114]. It has a rigid-rod nature which creates the difficulty in processing. While extruding the LCP, polymer segments get aligned in the extrusion direction resulting highly oriented micro-structure in the flow direction. As a result, tensile strength of LCP in the machine direction (MD) will be higher than that in transverse

direction (TD) [115]. A double-clad LCP substrate, procured from Rogers Corp., is shown in Figure 13.

1.4.3. Polyester

Among different polyesters, Polyethylene terephthalate (PET) is widely used as flexible substrate circuit material for its tensile strength and fatigue resistance [116]. It has widespread application in membrane switches [16], point-of-sale (POS) terminals and medical equipment [17]. Polyethylene naphthalate (PEN) is also used in flex circuit application [117]. The advantages are higher glass transition temperature, and better chemical resistance properties.

1.5. Conductive Traces Fabrication

1.5.1. Copper etch

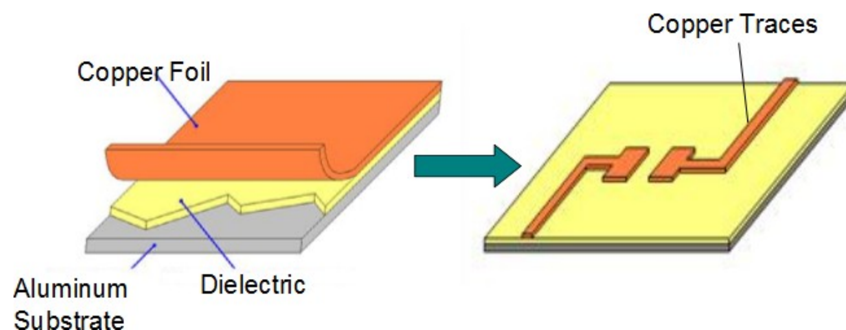

Figure 14 Etched copper circuit trace on thermal dielectric [118]

This is a subtractive process in which the PCB is chemically coated with photosensitive material, exposed to UV and subsequently developed. The etching removes all of the copper that is not coated with etch-resistant photoresist leaving the desired circuit traces (Figure 14). The current technology limit is 18 μ lines and 28 μ spaces [119].

1.5.2. Screen printing

Conductive traces can be printed on the outer surface of the flexible substrate through screen printing. Thick film paste can be applied to the substrate through a stainless steel mesh screen, coated with a photosensitive material or emulsion. The generated artwork is used to expose the substrate to generate the pattern. The unprotected area of the emulsion is hardened by the ultra-violet (UV) light. The screen is placed in the screen printer, the substrate is placed directly under the screen and the paste is applied to the top of the screen. Then the automated squeegee travels across the surface of the screen, forcing the paste through the openings onto the substrate (Figure 15). For screen, mesh count (the number of wires/unit length) is the most important parameter which may vary from 80 wires/in.-400 wires/in [120].

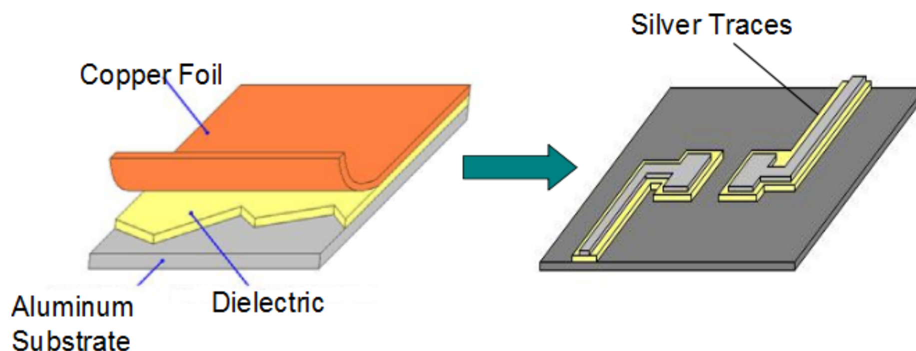

Figure 15 Screen printed silver trace on thermal dielectric [118]

1.5.3. Polymer thick film inlaid (PTFI)

A modified mill-and-fill interconnect technology, referred to as polymer thick film-inlaid (PTF-I) was developed in CNSE [121, 122], in which trenches with the desired width, depth and configuration are formed and then filled with a conductive paste to produce after curing a high-resolution conductive trace pattern. Polymer Thick-Film Inlaid (PTFI) is a low-cost method for

forming a high-density pattern of conductive traces on a flexible substrate that can be easily integrated in a roll-to-roll (R2R) production line [123].

In this method, shown in Figure 16, the substrate surface is first treated to incorporate high hydrophobic behavior. In the next step, trench patterns with desired profile are formed either by hot embossing or laser micromachining. Finally, the trenches are plugged with PTF conductive material using a squeegee followed by curing of the material. The process can be further enhanced by using a multiple-blade squeegee and introducing a small-amplitude, high-frequency vibrations.

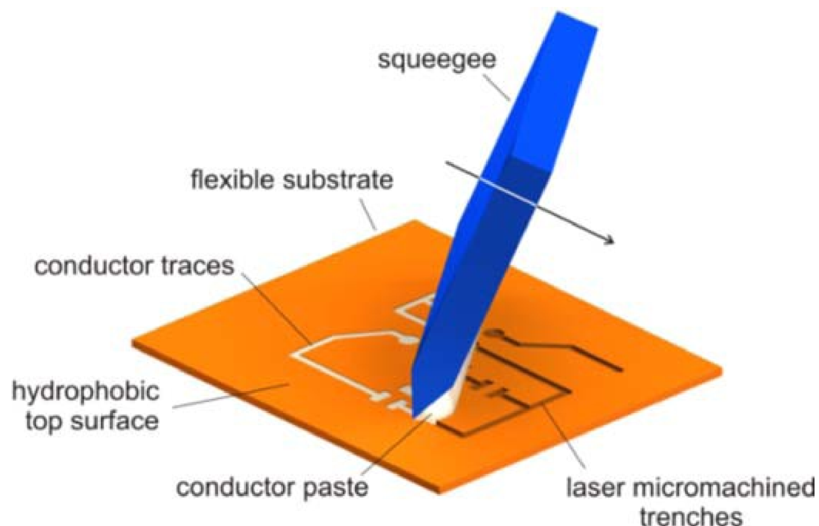

Figure 16 A schematic illustrating the PTFI method [123]

1.6. Die Preparation

1.6.1. Solder balls

The first flip chip bumping process used mechanically deposited Ni-Au plated Cu balls. In this process, small diameter balls (100–125µm) can be directly placed on the chip [46]. Micro-spheres of solders are also directly placed on the under bump metallization (UBM) in solder ball placement bumping [120]. Eutectic Sn/Pb is used as the standard solder balls (as shown in Figure

17), but is vulnerable to fatigue and will fracture eventually if subjected to continuous stress [124]. Another approach is *solder jetting* in which solder balls are placed on Ni-Au UBM by controlling a stream of molten solder droplets. Solder jet printing is accomplished in two processing modes: the demand mode and the continuous mode.

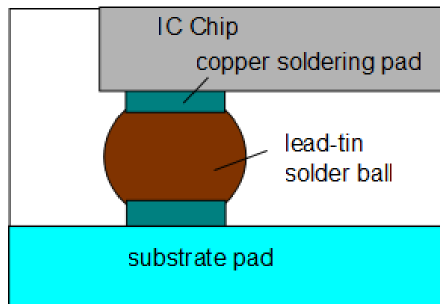

Figure 17 Schematic view of flip chip solder balls

Demand mode jetting systems use piezoelectric or resistive heating to create droplets. The droplet placement is directed by mechanical positioning. A continuous stream of solder droplets are used in continuous mode jetting systems in which placement is controlled with electrostatic deflection of the charged droplets [125]. Molten droplets as small as 25 μm in diameter can be deposited at a rate of 2000/s [46]. Stud bump bonding is another unique method to create solder-balls on the die without under bump metallization (UBM). A solder ball is directly bonded onto the bond pad using a solder wire in a modified wire bonder. The solder wire is broken off to leave the bump on the pad. Later the bump is reflowed to make solder balls. In printed bump technique, solder paste is printed onto the under bump metallization (UBM) by stencil and reflowed to form solder bump (Figure 18). IBM developed a process (refereed as IBM C-4) in which UBM is deposited and patterned, followed by solder deposition. After reflow, the solder takes the shape of a ball [126].

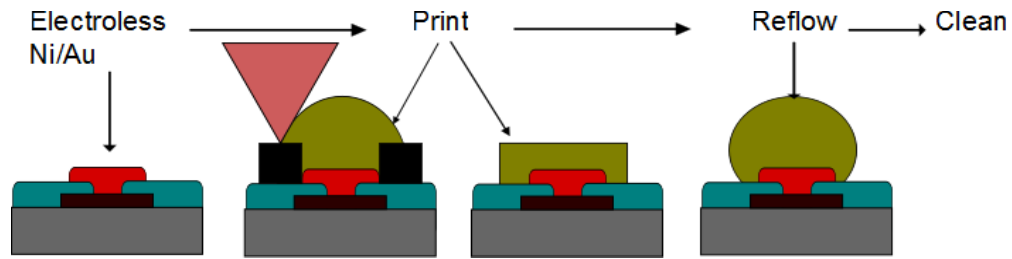

Figure 18 Process flow of stencil printed bump

1.6.2. Electroplated or electroless-plated bumps

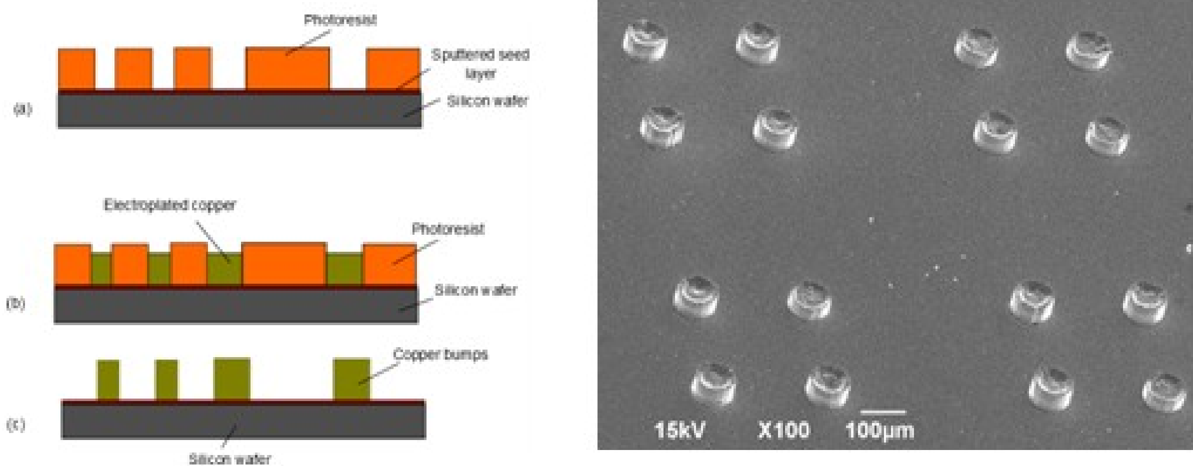

Figure 19 (a) Electroplating method (b) SEM of electroplated bumps

Conventional electroplating of Au, Cu or Au-Sn solder is very popular to fabricate the metallic interconnects. The development of high aspect ratio photopolymers paved the way to concentrate on HAR bump fabrication. The photoresist is spin-coated on the wafer, followed by exposure to UV or X-ray and immersion development to open the vias. Later the wafer was transferred to electroplating bath to fill up the vias with desired metal using electroplating process. Depositions are controlled by process variables such as current flow, time, temperature, and agitation. Electroplated copper bumps, fabricated using traditional photolithography and electroplating process, is shown in Figure 19. The electroless Ni-Immersion Au processes is low

cost and mask less. It also serves as a method for bumping bare dice. The 0.05-0.5 µm thick Au layer prevents passivation of the nickel. In this method, bump heights in the 15-20 µm range is achievable [126].

1.6.3. Printed adhesive bumps

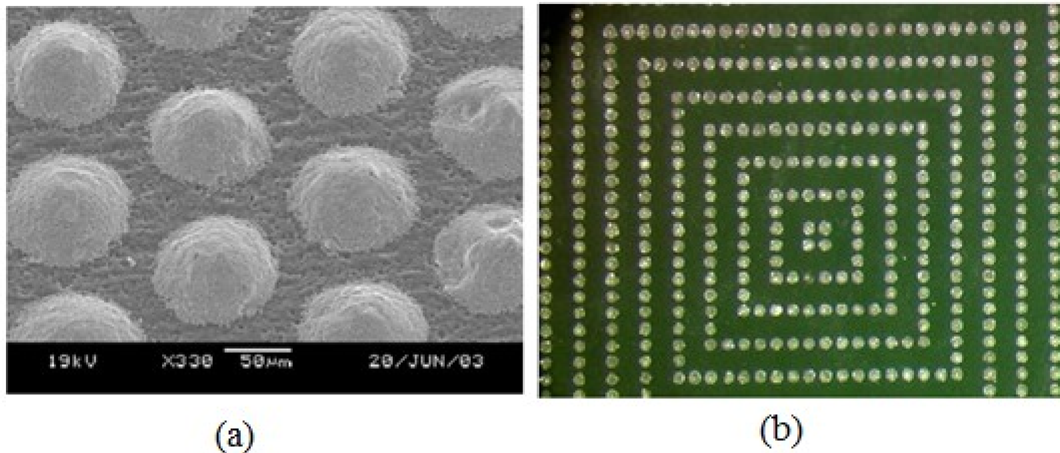

Figure 20 a) SEM Image of 90 µm pitch adhesive print deposits b) Optical image of 100 µm pitch adhesive print deposits [127]

In this method, the conductive adhesive is stencil printed on the die that provides a robust contact between the bump and the bonding pad (as shown in Figure 20). An alternative approach uses a template made of organic film such as polyimide, photosensitive film, or a pre-defined Kapton® film). The application is limited to bump pitch of 200 µm and greater due to stencil manufacturing [46].

1.6.4. Stud bump

Stud bump bonding (SBB) technology was first developed by Matsushita that is based on conventional wire bonding method [45]. In SBB technology, the bump is created by shearing the fine wire above the free air ball height. This method is known as dry bumping, as no lithography is required. Au stud bumps are most common, though processing of copper and solder bumps

were reported. First, two stepped Au bumps are bonded on the metallic pad by wire bonding method. The advantage of two stepped Au bumps is the easier transferability of conductive adhesive due to increased surface area. Later, the “coining” operation is used to level the bump height by transforming the pointed peak into a flat surface. The coining is realized by press with a load of 50 g/bump to a uniform height of 45 ± 1 μm [129]. The chip is mounted to the flexible substrate with a mounted load of 2 gm/bump [45]. SEM of an Au stud bump is shown in Figure 22b. It also has an excellent reliability regarding thermal stress. Holland et al [128] reported the formation of Au stud bumped die followed by assembly onto LCP substrate using thermocompression bonding method (as shown in Figure 21a).

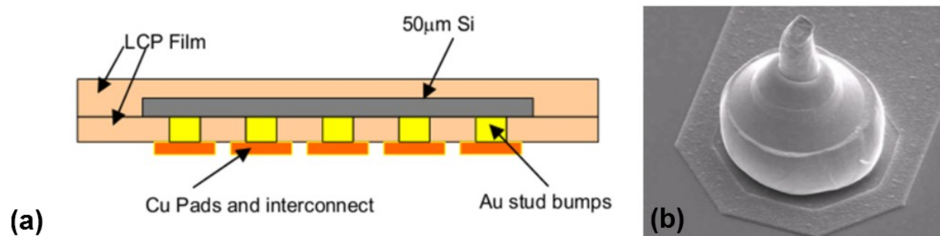

Figure 21 (a) Illustration of Au stud bump assembly approach in liquid crystal polymer (LCP) substrate (b) A single stud bump formed on a gold pad [128]

1.7. Dicing of Thinned Wafer

The singulation of bare or bumped dice is the next step in embedded package fabrication. In the traditional process sequence the front-end-processed wafer is thinned, handled, and then diced. The methods for wafer handling and component assembly used for thick wafers can be modified and adapted for assembly of ultra-thin dice on flexible substrates but this is not a trivial task [57, 68]. The ultra-thin wafer needs to be singulated to fabricate dice for further processing. The process can be accomplished in different ways such as blade dicing, ablation laser dicing, stealth dicing, dicing by thinning (DbyT) or DRIE dicing. According to Iker et al. [48], the

plasma etching before thinning provides the best results. A process called "dicing by thinning" was suggested [50, 58, 61, 130] in which trenches with a depth of the final chip thickness are sawn or etched on the wafer's front side before thinning. After bonding to a handle wafer, the sawn wafer is thinned until trenches are opened and dice separated. The singulated bare dice are placed on a tape carrier for use in the component placement equipment. When applied to ultra-thin dice, this process requires handling of ultra-thin wafers, which is one major challenge because the ultra-thin wafers are fragile and tend to warp making the use of automated robot handling difficult if possible at all [68]. For example, it was shown that 200-mm diameter wafers thinner than 200 µm cannot be handled by the standard equipment [57]. Burghartz [14] developed the *Chipfilm*™ technology which creates narrow cavity underneath the die areas. The dice are singulated by breaking the anchors underneath the chips, and then supported and transferred to the substrate using the *Pick, Crack & Place*™ process. J. A. Rogers's group at the University of Illinois at Urbana-Champaign [131] reported a similar method based on the silicon-on-insulator material technology.

1.7.1. Blade dicing

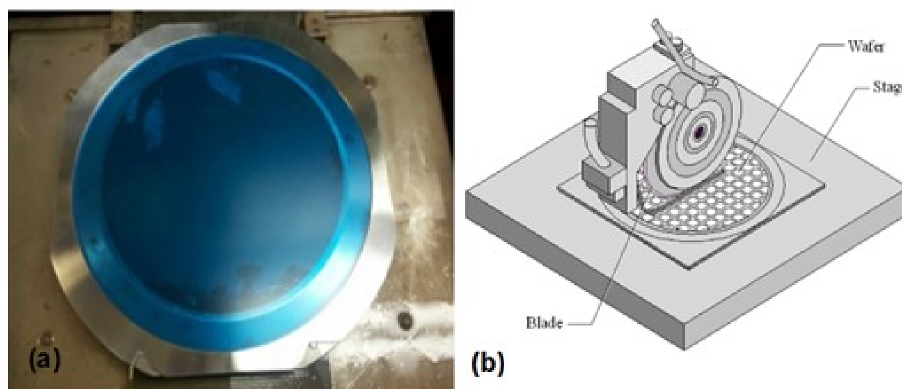

Figure 22 (a) A wafer mounted to dicing tape, ready for blade dicing (b) Wafer saw and sliced wafer

Semiconductor wafers are traditionally diced by a diamond coated nickel-bond dicing blade (typically 0.8-1 mil in width) which is mounted in an automated precision mechanical saw (as shown in Figure 22). The diamond grit size is typically 4-6 μm. It was reported to be not so suitable for dicing ultra-thin dice due to die cracking and chipping [132]. This is a through-the-wafer cutting method in which the wafer is attached to backing tape, aligned using mechanical control system and diced. Flat applicator removes air bubbles from the backside of the wafer. At 30000-50000 rpm of the blade, the feed rate is typically 25-75 mm/sec. The heat affected zone is cooled using cooling fluid. The cooling fluid may create some adverse effect on the ultra-thin dice such as die movement and cracks. The quality of the wafer dicing process depends on material hardness, brittleness, and thickness. Semiconductor industry is facing new and greater challenges in improving dicing productivity with the introduction of new wafer materials like gallium arsenide or lithium tantalite. The blade dicing was proved not very useful in this research due to warping of ultra-thin wafer and use of high-pressure cooling fluid. After dicing, loss of bare tiles and fracture in the wafer was observed in visual inspection.

1.7.2. Laser dicing

1.7.2.1. Ablation laser dicing. Laser dicing of silicon wafers is a relatively new technology – and it is a growing phenomenon. As the wafers become thinner and lasers become cheaper and more powerful, their performance advantages increase dramatically. In this process irradiation of laser pulses is used to remove wafer material. A range of laser systems with different wavelengths, pulse widths and power levels are used. The wavelength and pulse width varies from short UV [133] to long CO_2 [134] and femtosecond [135, 136] to nanosecond [137] respectively. The laser-material interaction consists of heating, melting, vaporization, ejection of atoms, ions and molecules, shock waves, plasma initiation and plasma expansion [138]. The laser beam

parameters such as pulse duration, fluence and wavelength control the laser-induced plasma, distribution of the Heat Affected Zone (HAZ) and debris. The laser pulse locally creates melt and vapor. The vapor pressure drives the molten material out of the wafer. The void generated in this process is refereed as kerf. This technology is predominantly used for through wafer dicing method. The choice of laser type depends on wafer material, thickness, throughput, and die size. The cutting speed can be increased by increasing distribution of energy into the silicon using longer pulse widths and longer wavelengths [133]. Laser dicing process shows evidence of thermal damages such as die strength degradation and subsequent die cracking, amorphization, and residual stress buildup [133, 139, 140]. These thermal affects may result in increased damage to sensitive electronics on the die while singulation. Femtosecond lasers are gaining popularity for minimal damage and high-precision ablation due to significantly small thermal diffusion depth [138]. The interaction between laser beam and laser-induced plasma was absent during dicing due to very short pulse duration of femtosecond laser. It was also reported that infrared femtosecond laser induced plasma has a shorter lifetime than longer laser pulses [141, 142]. Moreover, highly efficient material ablation can be achieved due to full deposition of absorbed laser energy [143]. A damage-free laser dicing process using water-jet was also developed [144].

With the trend towards smaller circuits and thinner wafers, the limitations of blade dicing interferes with the quality and productivity. Especially, chipping and cracking occurs under forces of cutting blade if blade dicing is used to singulated ultra-thin wafers. Moreover, low-k dielectrics, used for higher performance logic circuit, are more porous than usual; hence prone to chipping while mechanical cutting operation takes place. Laser dicing gets the edge to mitigate the issue being a thermal material removal process rather than mechanical such as blade dicing.

The forces acting on the silicon wafer is significantly reduced if compared to blade dicing process. The laser dicing process produces narrower streets and results in drastically improved productivity. The scanning electron micrograph of a 20 µm wide laser diced trench is shown in Figure 23.

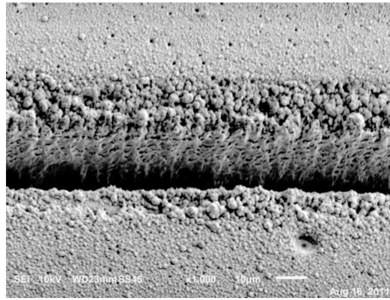

Figure 23 20 µm wide trench ablated by Nd:YVO_4 laser in CNSE at NDSU

1.7.2.2. Stealth dicing. This process was developed to avoid debris contaminants and thermal damages on wafers [145, 146]. In this process, focused laser pulse inside the wafer substrate generates a polycrystalline structure that originates singulation process [147]. The substrate material becomes locally weak and dice are singulated using a breaking device (as shown in Figure 24). To make the process work, there cannot be any top passivation and test structures on the streets. If there is any DAF formed on the backside, additional steps are necessary to singulate them. The major advantages [148] of SD process are 1) chipping-free and high-speed dicing; 2) lack of debris; 3) completely dry process. This method is successfully used in MEMS, ultra-thin wafer singulation, and imaging devices such as CMOS/CCD [148, 149].

1.7.2.3. Multiple beam technology. The use of high powered industrial laser may damage the die, deteriorating the quality of the microelectronic assembly. Dice can be singulated without chipping or cracking with minimum HAZ if low powered laser is used. The obvious issue that

lies with low power is low material removal rates and low dicing speed. This issue can be solved using multiple laser beam technology developed by Philips and ALSI [151]. The laser beam is split into multiple low powered laser beams. The group of beams keeps the material removal rate and the dicing speed high. The high power laser beam passes through a beam splitting device, referred as a diffractive optical element (DOE).

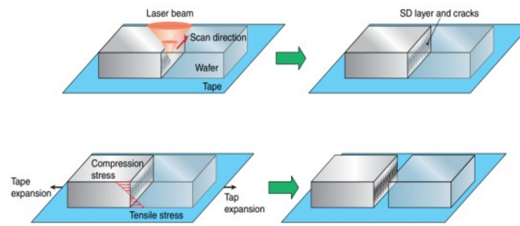

Figure 24 (a) Laser process (b) Separation process [150]

1.7.2.4. Dicing by thinning. In this method, trenches are cut into the silicon using wafer saw or dry etch technique on the top side. The singulation of dice are accomplished by thinning the backside of the wafer and opening the grooves. The process flow of dicing by thinning is shown in Figure 25. After thinning, etchant is used to round the street sidewall corner and remove residual micro-cracks. The minimum street size that can be obtained by dry etching is 10 μm leads to a very high yield of chips per wafer.

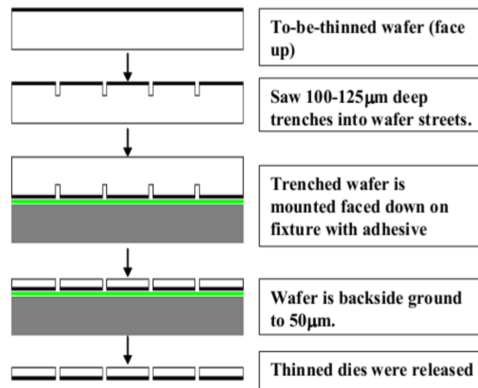

Figure 25 Flowchart of dicing by thinning process [51]

1.8. Handling of Thinned Wafer

The safe handling and transfer of ultra-thin chips is another challenging task. The traditional pick-and-place equipment does not offer satisfactory result. There are several reports about special means to handle ultra-thin chips such as thermal release tape, solvable thermoplastic glue layer and mobile electrostatic carriers.

1.8.1. Thermal release tapes

Thermal release tapes are very popular for attach wafers while thinning process. They are generally double-sided adhesive tapes with one thermal releasable side. Using the thermal release tape, the wafer can be thinned down to 10 µm. After back-grinding operation, the career is removed by a heat treatment of 90ºC to 150ºC. This method also can be used for functional wafers by covering the device topography. Feil et al [61] reported the successful use of this method in wafer thinning, die singulation and transferring 25 µm thin flexible RFID chips.

1.8.2. Solvable thermoplastic glue layer

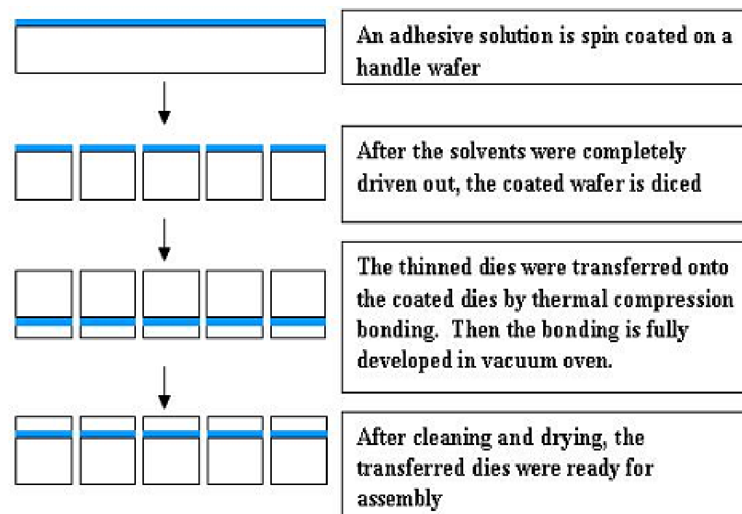

Figure 26 Thinned die transfer process [51]

In this method, thermoplastic adhesive material is spin-coated on a handle substrate to form very thin and uniform adhesive layer. This is a very useful method to handle very thin wafers (around 10 µm). The adhesive layer also helps to embed the surface topography. If "Dicing-by- Thinning" technology is combined with chemical mechanical polishing, the thermoplastic adhesive layer can protect the front side chip trenches and thereby prevent chip cracking. After the dice are thinned and separated, the adhesive film is dissolved by immersion of the career wafer into a solvent bath. After removal of adhesive, the released dice are collected. Robert et al [152] used this method to fabricate 10 – 15 µm thin sensor chips silicon from CMOS image sensor wafers (diameter 200 mm). Wayne Johnson's research group at Auburn University demonstrated an effective transfer process of thinned die [51], as shown in Figure 26.

1.8.3. Mobile electrostatic carriers

Ultra-thin wafers can be attached to the handle wafers using electrostatic forces that quickly create bonding and de-bonding of the wafer. Bock et al [153] reported that permanent polarization state remains active even above 400 °C. For this research, first the silicon was diced using laser ablation. Later, DRIE thinning was adopted to avoid debris formation.

1.9. Die Assembly

1.9.1. Traditional (pick and place)

This process starts with the fabrication of an array of devices comprising individual circuits on the wafer. Later the wafer is mounted on a tape and singulated into discrete dice. Individual dice are detached from the tape using an ejector assembly on the chip mount equipment and placed on a receiving pad of a lead frame formed on an insulating substrate. A typical chip mount apparatus includes an x/y movable table, an ejector assembly, an ejector

motor and one or more ejector pins. An arm having a vacuum tip to remove the ejected chip is also provided [155]. The process sequence is shown in Figure 27. The placement rate of high speed ‘chip shooter” is 13000 components per hour. Fully automated sequential placement is faster, with a capacity of up to 60000 components per hour [156]. The important parameters are flexibility and placement rate.

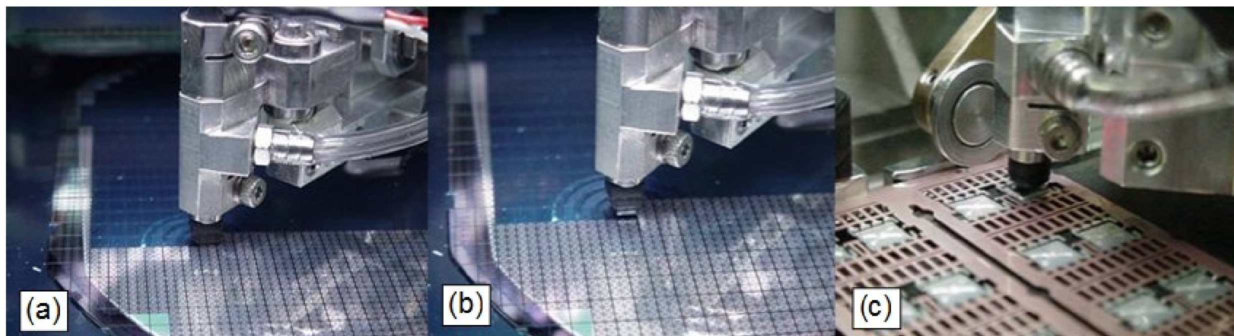

Figure 27 (a) Bonding arm lower to pick level and position (b) Ejector rises up and bonding arm lift up the die by vacuum (c) Bonding arm swings to bond level and position for bonding [154]

The traditional pick-and-place equipment that is widely used for direct chip attach process faces many issues while handling ultrathin die [61, 157]. Adapted die bonders [35, 60, 62, 68] can be used to handle ultra-thin dice but they are costly and the results are not very satisfactory. To use pick and place equipment, ultra-thin dice are attached to the carrier tape. If the components have a characteristic length of less than 300 μm, stiction of the die may become a problem for the pick-and-place equipments to produce optimal yields [158]. If the dice are attached with adhesive, stiction may be avoided but it becomes more difficult to detach the die from the adhesive film unharmed. After picking the die from the tape, placement nozzle is used to put them onto or into the substrate to enable good connections between the bumps and the contact pads. The down-force of the placement nozzle often cracks the die while placing them on the substrate [61]. Johnson et al [51, 54-56] suggested using a thick “releasable handle” to

support the thinned die so that traditional pick-and-place equipment can be used to handle them. But this approach needs an additional process step to remove the handles using acetone. Though a single-nozzle placement machine may have the precision to place extremely fine pitch components [159], this equipment cannot handle ultrathin dice and similar components at a rate sufficient for high throughput assembly (>10 cps) [61]. Therefore, the die placement is increasingly becoming the limiting factor for the widespread use of ultrathin dice. The die bonders can process thick dice at a rate of 3000 cph [160]. This rate should be much lower for precision assembly of ultrathin dice because placement accuracy and rate are inversely correlated.

1.9.2. Fluidic self-assembly, surface tension

Fluidic self-assembly (FSA) is used for the mass assembly of very small dice. This technology was invented by Mark Hadley at University of California, Berkley [161]. In this process floating semiconductor devices in a fluid medium are flowed over a surface to settle them into correspondingly shaped receptors in a self-assembly [162-166]. This is illustrated in Figure 28a and 28b.

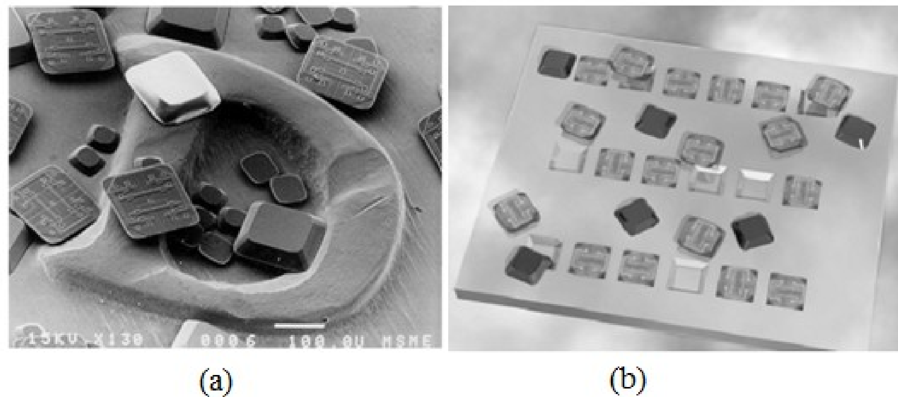

Figure 28 (a) Microphotograph of individual nanoblocks on the surface of a dime (b) Nanoblocks falling into substrate holes [167]

Specifically shaped blocks and holes are formed by silicon micromachining through photolithography and ion-milling technique. The dice attached to a sacrificial layer are released using acid etching to a transport fluid. Later they are dispersed over silicon substrate with etched receptor holes. The process is fast, for example, a substrate with 191 holes can be totally filled within 2.5 minutes. The fill ratio can be increased by roughening the substrate. FSA has been successfully used in the high-volume manufacture of RFID tags. The assembly rate of NanoBlock ® ICs into RFID tags in FSA method is 2,000,000 components per hour whereas assembly of 10,000 components per hour is possible with conventional pick-and-place method [168].

1.9.3. Laser induced forward transfer (LIFT) [169]

The basic concept of the technique known as "Laser Induced Forward Transfer" (LIFT) includes using a polymeric sacrificial layer to attach the components to be transferred to a laser-transparent carrier [169]. The sacrificial material used to attach the component on the substrate is ablated by a laser pulse to generate fast moving gases that pushes the component down to a receiving substrate. The use of a laser for the transfer and placement of discrete components onto a receiving substrate was first reported by Holmes and Saidam [170, 171]. Recently, LIFT has been applied to the transfer of semiconductor bare dice. Karlitskaya and coworkers have developed a simple model that predicts the fluence threshold for the release of 200 × 200 μm by 150 μm thick Si squares adhesively attached to a sacrificial PVC tape [172]. In a subsequent study [173], the authors described similar experiments for laser transfer of 300 × 300 μm by 130 μm thick Si squares in two distinct modes – ablative and thermal releasing, using a relatively long pulse infrared and green lasers. Recently, Sheats [174] has described a process in which, in order to re-lease the die, the release layer is heated up to a temperature of 100 – 150^0 C by

optically irradiating it with a dose similar to that used in optical lithography. Although this process does not use a laser, it is very similar in nature to the thermal releasing process described by Karlitskaya et al [173]. Karlitskaya et al. [175] have proposed and studied two mechanisms of die release–ablative and thermal. They defined ablative releasing as a die release process with a high-fluence single laser pulse, which evaporates the release material thus creating high pressure and releasing the die at high speed. The thermal releasing is a less intensive process in which the release material is heated gradually until the material starts to decompose, as a result reducing to zero the adhesion of the die to the release substrate and literally dropping the die onto the receiving substrate. A novel technology using the thermo-mechanical blister formation was developed in Center for Nanoscale Science & Engineering of NDSU. The details of the research were reported elsewhere [176].

1.10. Flexible Package Assembly Process

The fabrication of interconnects from the functional chip to the flexible substrate is the most important part of the thin flexible assembly. Thinned silicon dice tend to warp; hence the reliability of the package is critical. They also have mechanical vulnerability due to very low thickness if compared with conventional dice. A common approach is to employ handle wafer to support thinned wafers.

The reliability concern takes place due to the deformation of flexible substrates if exposed to harsh environments, for example to temperatures higher than the glass transition temperature. Especially in case of flip-chip-on-flex, solder joints may exhibit a hyperboloid contour due to warpage of the flexible substrate during reflow cycle of the solder joints. This problem can be mitigated using a vacuum chuck to secure the flexible substrate on a flat surface [177, 178].

1.10.1. Reflow soldering

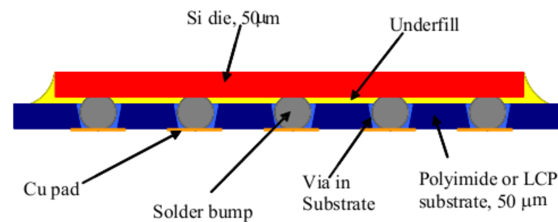

Figure 29 Illustration of polyimide or LCP substrate and solder assembly approach [128]

This method can be described as modified Controlled Collapse Chip Connection (C4) technology tailored for thinned die assembly. Wayne Johnson's group [51, 128] at Auburn University assembled thin flip chips on polyimide and LCP flex substrates using conventional flip chip equipment using thin dice on handles (Figure 29). The solder bumped die were assembled into the flex substrate, followed by reflow soldering. The thinned dice were attached to the handle while reflow. Later, underfill material was dispensed and cured.

1.10.2. Thermode bonding

Thermode bonding was introduced by Fraunhofer IZM to assemble solder bump die onto a flex substrate [179]. The solder bumps were deposited using immersion soldering. The underfill material was applied using stencil printer on the bump side of the die in a special method, known as no-flow underfilling technology. Bonding nozzles were used to produce pulsed heat at a high rate to the die. The bonding temperature, higher than melting point of the solder, is applied only for a short duration of time to reflow the solder joint.

1.10.3. Adhesive bonding

In flip-chip technology, electrically conductive adhesive (ECA) is used as connector. They can be categorized into anisotropically conductive adhesives (ACA) and isotropically conductive adhesives (ICA) based on conductive filler loading level (as shown in Figure 30).

The anisotropic conductive adhesive (ACA) is a thermoset or thermoplastic material consisting of a stable matrix of metalized glass or polymer beads (typically 3–5 µm in diameter). The nickel and gold plated beads are coated with a final insulating layer [46]. The adhesive is deposited by dispensing or stencil printing to create a film (ACF). The current limit of ACA is 800 μm^2 pads with 10 µm spaces between them. A typical bonding parameter is 150-210 ° C and 40-300 grams/bump for 5-20 seconds [180].

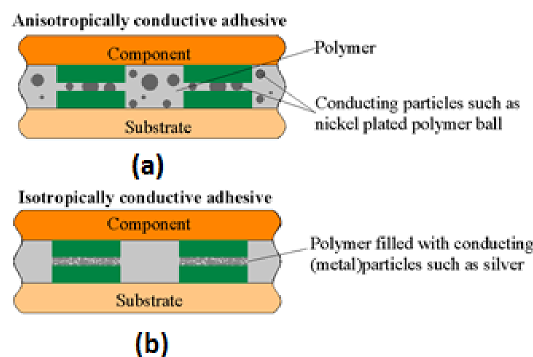

Figure 30 Schematic view of (a) anisotropic conductive adhesive (b) isotropic conductive adhesive [183]

Isotropic conductive adhesive (ICA) consists of polymer resin composites and conductive fillers. The electrical and mechanical bonds are established among interconnects trough an adhesive matrix made of thermosetting and thermoplastic materials. When using in the flip chip application, ICA paste can be deposited by screen or stencil printing. At high temperature, degradation of adhesion occurs which is considered as a major drawback. Moreover, the solvent present in polyimide-based ICAs evaporates during heating creating void [181]. The reliability is better if gold-plated polymer particles are used as conductive fillers instead of nickel particles [182]. The target placement accuracy is 10 to 20% of the die bump diameter. The tighter tolerance (10 to 12µm) of placement can be achieved by using machine assisted alignment, for example, using a flip chip-aligner bonder [126].

1.11. Statement of Work

The objective of this work was to study the electrical performance of embedded ultrathin silicon bare dice bumped using three different methods as explained in the next chapter and subjected to accelerated thermal and mechanical bending cyclic stresses. The criteria used to evaluate the package reliability were the change in the dc resistance as measured through the package between two plugged vias as well as the evidence of a total failure event defined as an electrical discontinuity in the package. A novel chip embedding process was developed in the Center for Nanoscale Science and Engineering (CNSE) at NDSU in order to permit the high volume assembly of ultrathin, ultrafine pitch components with sufficient accuracy and precision (Figure 31) [176, 184, 185].

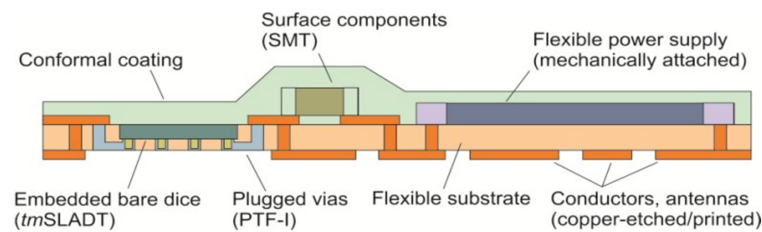

Figure 31 A functional die embedded in the organic flexible substrate [18]

Part of this work required investigating the most reliable bumping method and assembly process. This work determined the advantage of the bumped (wire bonded/electroplated) interconnects on the embedded dice in terms of conductivity. The work reported in this dissertation is divided into five major phases: die preparation, die metallization, substrate preparation, assembly and accelerated test. The accelerated test and failure analysis is performed by CNSE Electronic Design and Testing Laboratory, NDSU. The manually assembled package was subject to bend test and thermal cycling test (according to JEDEC A-1040C Standard) to test the electrical performance of the package.

CHAPTER 2. EXPERIMENTAL METHODS

2.1. Introduction

The embedded die packages were fabricated, assembled and subjected to performance tests to assess the electrical performance. Various microfabrication methods were optimized and integrated to develop a process flow to fabricate the samples. Thick wafers were thinned down to 50 μm to achieve the desired flexibility. A novel die singulation method was developed for sputtered silicon wafer. Dice were metalized applying the photolithography and electroplating process. The laser ablation parameters to create the receptor pockets and trenches were optimized. A conductive micron-sized ink was formulated and used to fill the trenches manually. Last of all, the dice were transferred into the substrate and assembled manually. After the samples are prepared, they were subjected to accelerated thermal cyclic loading and mechanical bend test.

2.2. Specimen Preparation

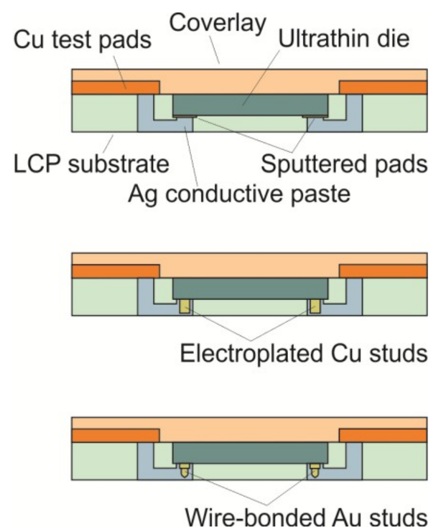

Figure 32 Schematic view of different embedded packages

In this work, three different types of dice i.e. sputtered die, electroplated die and stud bumped die were used to prepare embedded die packages, as shown in Figure 32. The assembly of the ultra-thin chips was the final step in package fabrication following the die preparation, metallization and substrate preparation. At least five samples were prepared for each die size and package type. In total, 90 packages were assembled for the thermal and bend test, as shown in Table 1. The assembly process was accomplished in the class 10000 cleanroom manually with the help of a Leica inverted microscope. The silicon dice were carefully placed upside down with plastic tweezers and sealed to the ablated receptor pockets with Kapton ® tape. It was made sure that the assembly was free from any air bubbles.

Table 1. Assembled samples for reliability test

Sample Set	Sample number	Die Size (µm x µm)	Bump Type	Test Method
1	5	350x350	Sputtered	Thermal Test (JEDEC JESD22-A140C)
2	5	670x670	Plated bump	
3	5	1000x1000	SBB	
4	5	350x350	Sputtered	
5	5	670x670	Plated bump	
6	5	1000x1000	SBB	
7	5	350x350	Sputtered	
8	5	670x670	Plated bump	
9	5	1000x1000	SBB	
10	5	350x350	Sputtered	Bend Test
11	5	670x670	Plated bump	
12	5	1000x1000	SBB	
13	5	350x350	Sputtered	
14	5	670x670	Plated bump	
15	5	1000x1000	SBB	
16	5	350x350	Sputtered	
17	5	670x670	Plated bump	
18	5	1000x1000	SBB	

After the assembly, the packages were plasma treated using TRION RIE Plasma Etcher to clean the residue and oxide formed in the exposed trenches and bumps. The next step was to plug the trenches with conductive silver paste in PTFI method and cure the packages in the convection oven for 8 hours at 150 ° C. The process flow of the assembly is shown in Figure 33. The assemblies were inspected using a Leica inverted microscope to check for any shorted connection. The SEM of an assembled die is shown in Figure 34.

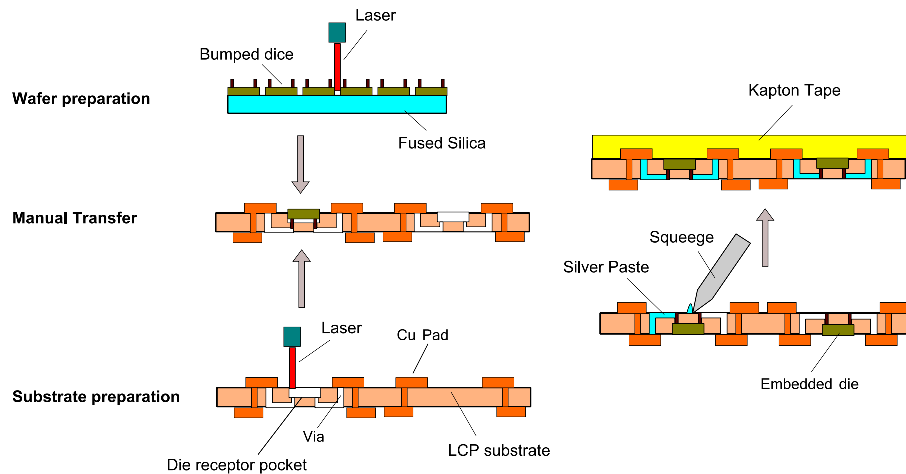

Figure 33 The process flow of embedded die package fabrication

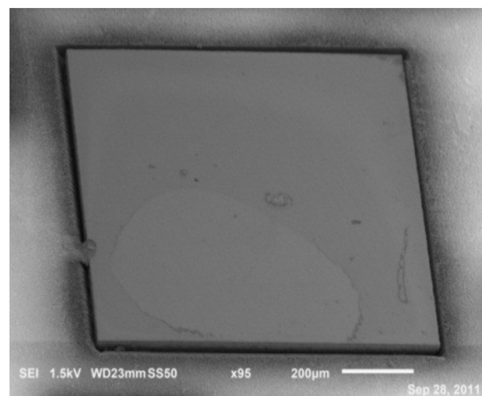

Figure 34 A bare die after assembly

2.3. Preparation of Ultra-Thin Die

The fabrication and handling of ultra-thin dice for embedded assembly in the flexible substrate is a challenging task using conventional methods. Typically, microfabrication processes are used to fabricate integrated circuitry on the die. The circuit layer is a nonsymmetrical structure built on the silicon base material. The ultra-thin (<50 µm) functional chips have a tendency to warp due to significantly reduced die thickness. In traditional pick-and-place technology, the image clarity of the die is very important to ensure the placement accuracy of the die onto the substrate. As the ultra-thin die shows high tendency for warp, they generates deformed image that may not be recognized by the vision-based program of the pick-and-place equipment [186]. The planarity of the interconnection bumps on the warped die is also affected by the die curvature. As a result, the degrading contact between the bumps and the pads on the substrate prevents the uniform continuity between the die and the substrate. To avoid the problems associated with singulation of ultra-thin die, laser dicing and deep-reactive ion etching method was adopted in this research.

2.3.1. Laser dicing of ultra-thin wafer

In this work, mechanical grade wafers were procured from Silicon Valley Microelectronics, Inc. The standard thickness of 200 mm p-type silicon wafer was 750 µm ± 5 µm. The wafer was thinned down to 50 µm (by GDSI) using traditional cassettes-to-cassette method by attaching onto an UV curable acrylic adhesive tape. Rectangular cut-outs from the wafers were prepared using laser-machining. Later, the adhesive tape was removed using high-suction vacuum chucks.

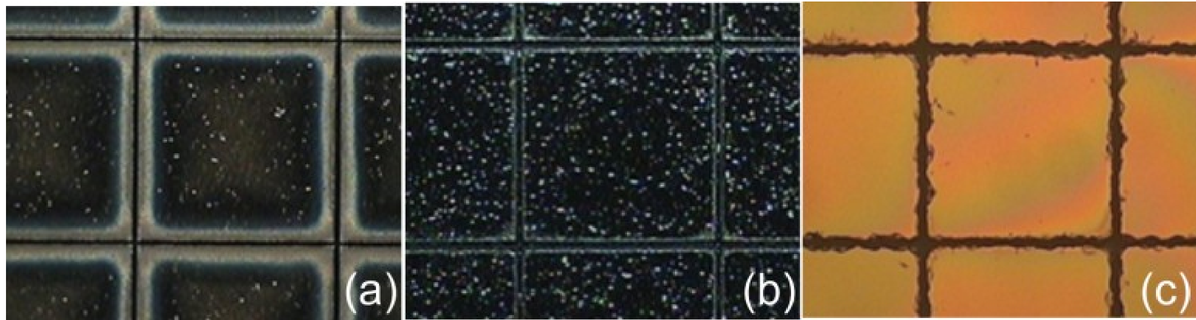

Figure 35 Optical microscope pictures of (a) the wafer immediately after dicing showing the debris haze around the cuts; (b) the wafer after stripping the photoresist (the dots on the sample are intrinsic to the silicon and were observed before dicing.); (c) the bottom of the wafer after dicing [184]

In the preliminary laser dicing experiments, a 50 µm thin piece of wafer was attached to a 76.2 mm diameter fused silica disc. The wafer was scanned 70 times with a high speed (400 mm/s) and high repetition rate (80 kHz), using a flat-top 355 nm HIPPO laser. An average power of 3.0 W was used and the pulse energy was calculated as 37.5 µJ. in the early stage of experiment, a 1 µm thin layer of PFI-38A positive-tone i-line photoresist (Sumitomo Chemical) was coated on the wafer, prior to dicing, to prevent debris on the die bumps. Later, the photoresist was stripped using acetone to remove the debris accumulated on the adjacent area of the streets (as shown in Figure 35).

The laser dicing of silicon was performed in two different schemes. For the bare die package, the silicon piece was sputtered with 500 Å titanium layer in a DC Magnetron Sputterer, followed by 3000 Å deposition of copper seed layer. The titanium film promotes the adhesion of the copper film to the wafer substrate. The laser diced silicon tiles are shown in Figure 36. After the laser dicing, debris was found in the adjacent area of the streets, as seen in the Figure 37 (a). Plasma treatment can be used to remove the debris, as shown in Figure 37 (b). In order to avoid the debris formation, DRIE thinning was adopted to singulate the bare dice.

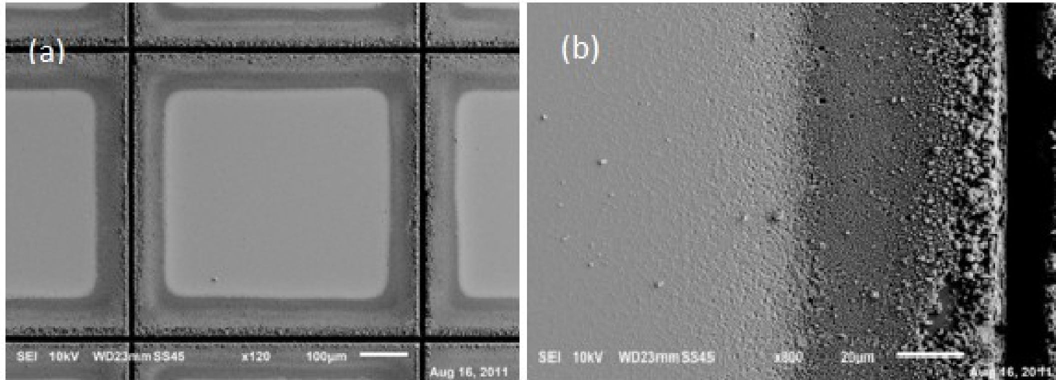

Figure 36 (a) Laser diced silicon tiles (b) Scanning electron micrograph of the ablated trench shows the debris formed during ablation

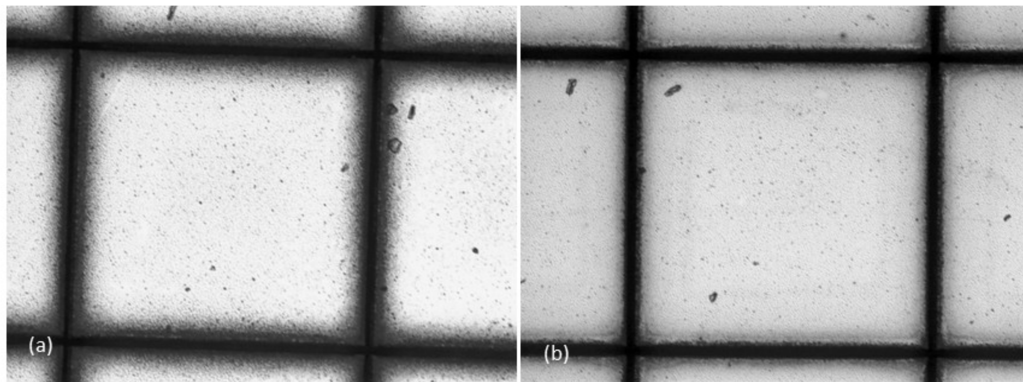

Figure 37 The optical micrograph of the diced silicon surface (top) (a) before and (b) after plasma treatment

For the bumped dice, dicing cannot be accomplished prior to the electroforming process, because the photolithography process needs a continuous electrically conductive seed layer throughout the wafer surface. The wafer was bumped using electroplating or stud bumping method. The laser dicing was accomplished after the bump formation. In this approach, debris cannot reach the bump pad area due to bumped structure. The schematic view of the two different approaches is presented in Figure 38.

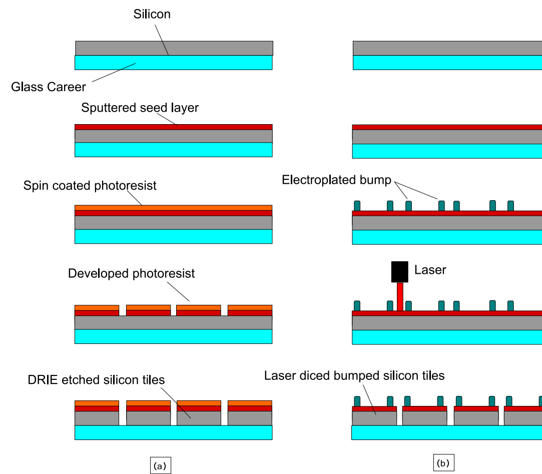

Figure 38 The process flow of (a) bare die singulation (b) bumped die singulation

2.3.2. Deep reactive ion etching (DRIE) for die separation

Die singulation using a fluorine plasma gas is a new concept utilized to manufacture ultra-thin silicon chips [187]. First, a standard wafer is back-grinded down to desired thickness (<50 μm). Photolithography and dry-etch techniques were used together to separate the silicon tiles protected by resist layer. Street patterns are defined on the silicon surface by developing a thin layer of structured photoresist film that is used as an etching mask [188]. In the dry etch approach, combination of different chip size and shapes can be easily realized. This is a very fast and secure technique that produces intact chips without any cracks. The sidewall profile of the chips shows no mechanical damage. The fracture strength of the dice remain high that enables the assembly of mechanically flexible electronic packages. Chip yield can also be drastically increased due to very narrow street formation, if compared to wafer sawing technology. This process is highly productive because the etching of all the dice on the silicon wafer is accomplished in one step. Sometimes, the laser ablation and the DRIE technique is combined together, especially when the metal patterns are present in the street layout.

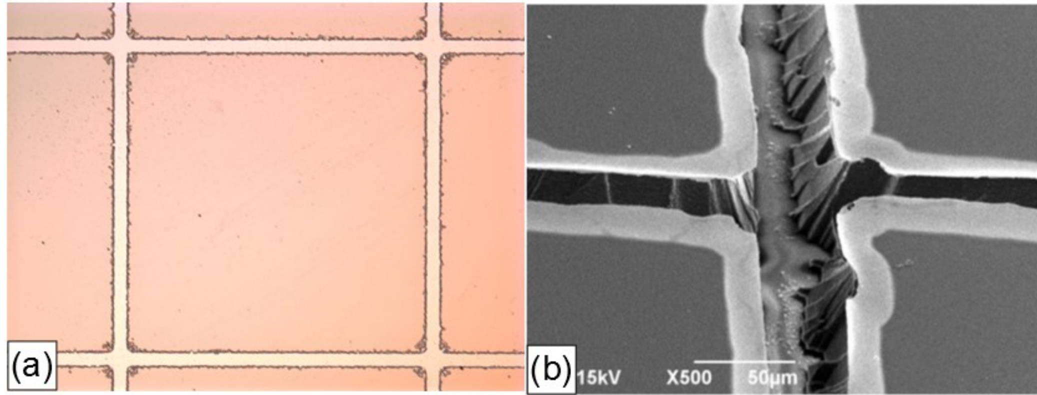

Figure 39 (a) Developed photoresist film on silicon wafer (b) The opened streets is etched using plasma, leaving the islands as silicon tiles

In this approach, a standard wafer of 750 ± 5 μm thickness was grinded down to 50 μm by Grinding and Dicing Services Inc. Then the wafer was cut into 1x2 squared inch pieces. A fused silica was spin coated with adhesive material and the silicon pieces were attached to the adhesive surface. Then the wafer was sputtered with 3000 Å Cu layer and spincoated with i-line (a positive tone photoresist) using Karl Suss RC-8 Spin Coater to form a 1.5 μm thick protective layer (Figure 39a). The SEM of DRIE etched streets is shown in the Figure 39b. The spin-coating recipe to form 1 μm thick protective coating is given in Table 2.

Table 2. Spin coating recipe to form protective photoresist coating

Cycle	Speed(rpm)	Acceleration(rpm)	Time (s)
1	1100	1000	3
2	3000	1000	23

The photoresist layer was patterned using a Mylar mask to create square blocks of size 350x350 μ m, 670x670 μ m and 1000x1000 μ m tiles with 40 μm wide streets. The photoresist was developed for 20 s using OPD262 (Fujifilm) developer solution to open the streets in WAFAB solvent sink. After development, the wafer was inspected using Nikon Microscope in

the class 100 cleanroom in an UV-protected environment. Later the copper seed layer that is exposed in the developed street of the wafer was chemically etched using APS-100 (Ammonium persulfate+H_2O) mixture. The silicon tiles were still covered with copper seed layer and photoresist. The sample was put in the Phantom TRION Reactive Ion Etcher to dry etch the silicon. The etch rate for the following recipe (in Table 3) is 0.45 µm/min. The SEM of the sidewall profile of the DRIE diced ultra-thin wafer (Figure 43a) shows that it has rougher surface than laser diced wafer (Figure 43b). For the reliability issue, the sidewall profile does not play any significant role. The SEMs of singulated bare dice are shown in the Figure 40c, 40d and 40e.

Table 3. Recipe for etching silicon

Cycle	Pressure	Power	Time	CF_4	O_2	SF_6	CHF_3
1	50	100	400	100	0	0	30
2	150	100	15	0	50	0	0
3	100	100	6700	0	9	26	11
4	150	100	15	0	50	0	0

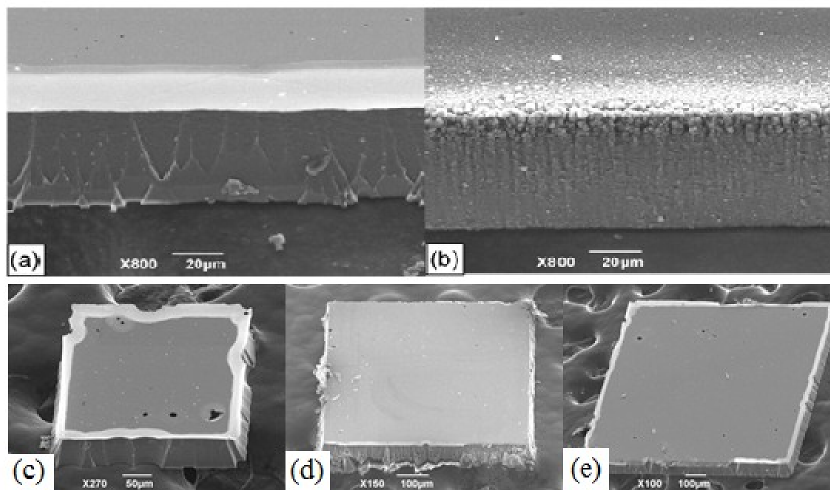

Figure 40 The sidewall profile of (a) deep reactive ion etched silicon die (b) laser ablated silicon die; scanning electron micrograph of (c) 350x350 µm (d) 670x670 µm (e)1000x1000 µm bare die, singulated by DRIE method

2.3.3. Transfer of ultra-thin die

The amount of literature published in the past decade indicates a strong interest in the ultra-thin embedded die technology. The critical points in this technology are the wafer thinning, dicing, handling, and, especially, ultra-thin die placement and assembly. Various methods have been developed to successfully solve most of these problems except the latter. The traditional thick-wafer methods can be modified for assembling small and ultra-thin dice on a flexible substrate but the results are far from optimal. Placement accuracy and rate for the pick-and-place machines are inversely correlated. According to Gilleo [159], the most advanced single nozzle placement machines are capable of 4σ placement accuracies of ±15 μm at a rate of 2000 components per hour (cph). Multiple nozzle placement machines are capable of up to 100,000 cph but with the 4σ placement accuracy degraded to ±100 μm. Though a single nozzle placement machine may have the precision to place extremely fine pitch components, its inability to place ultra-thin dice [61] and similar components at a rate sufficient for high throughput assembly (>10 components/sec) has led to the pursuit of other techniques.

Thin chips are typically used in mass produced devices. In order to decrease the production cost of flexible electronic products, roll-to-roll (R2R) manufacturing have been accepted as industry standard [189]. Each step in the manufacturing process, from the wafer to the final packaging must be scalable to high volume, low cost manufacturing. Die bonders are currently used to assemble ultra-thin bare dice on flexible substrates. Typical die bonder systems process thick dice at a rate of 3000 cph [160], even slower for precision assembly of ultra-thin dice, which may not be sufficient for an R2R type of manufacturing. Therefore, the die placement is increasingly becoming the limiting factor for the widespread use of the ultra-thin embedded dice.

2.3.4. Thermo mechanical selective laser assisted die transfer (tmSLADT)

The key concept of the "Laser Induced Forward Transfer" (LIFT) technology is to transfer functional chips attached to a polymeric sacrificial film to the substrate by laser ablation of the career film. Typically, a career object that is optically transparent to laser is spin-coated with the polymeric film to mount the functional die. A laser pulse is used to ablate the spin-coated sacrificial material and generate quickly expanding gas to push the chip towards a receiving substrate. LIFT techniques may be used instead of the traditional pick-and-place method to transfer small-size, ultra-thin semiconductor bare dice at a high yield rate. It was reported that components with footprints of 2.6x2.6 mm to 100x100 µm and thicknesses as small as 10 µm can be successfully transferred with this technology [190]. The die transfer rate was also reported to be very high – 100 components/sec compared to 1-2 components/sec for the conventional pick-and-place machines [171, 190].

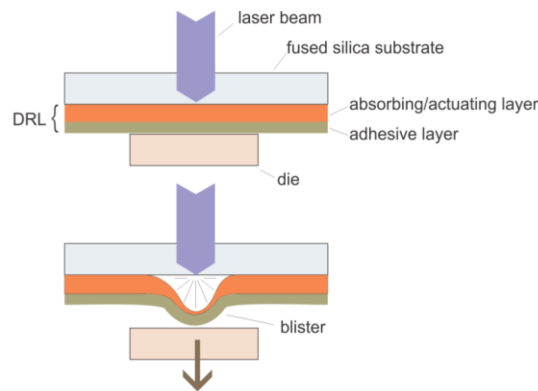

Figure 41 A schematic illustrating the principles of tmSLADT. The DRL absorbs the laser pulse with energy below the blister rupture threshold of absorbing layer. This contains the gasses generated during absorption and provides an actuator mechanism to transfer the discrete component [176]

The major challenge of LIFT techniques is the accuracy and precision of placement of the transferred die. The die transfer method using generated gas results in non-predictable placement

patterns due to release dynamics and flight instability of the laser ablative method. Moreover, the thermal release method does not produce expected results due to the inability of gravitational force to overcome the surface attraction acting on the ultra-thin dice.

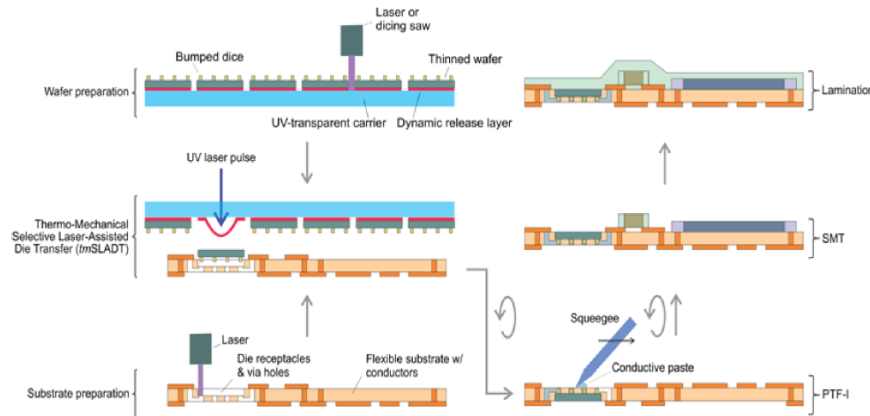

Figure 42 The process flow of the SLADT process [184]

A novel method was proposed by the LEAP research group at CNSE to alleviate these problems. In this method, an UV-transparent career is spin-coated with Dynamic Releasing Layer (DRL) that is used to mount the ultra-thin die, followed by laser dicing process. After dicing, the sample is mounted in a specially designed fixture and the DRL is irradiated with UV laser pulses to create the actuator blisters that transfer the dice from the releasing to receiving substrate. The laser ablation of the DRL material creates rapidly expanding gas that forms a blister (Figure 41). That blister pushes the die towards the receiving substrate, thereby serving as a mechanical actuator. The transfer mechanism involves partial ablation of the DRL layer. At first stage, the absorbed laser energy vaporizes a shallow region of the DRL corresponding to the absorption depth and creates the rapidly expanding gas. Later, the confined gas exerts an outward force on the non-vaporized region of the DRL layer and forms a blister. The process flow of the SLADT process is shown in the Figure 42.

2.4. Die Metallization

Die metallization is a critical step in the embedded package fabrication because stress concentration and mechanical failures come into effect in the interconnect area [191-193]. The main purpose of metallic bumps is to ensure the electrical signal conduction from the functional die to the metallic traces through the bond pads. Advances in microelectronics technology are pushing the IC industry towards the challenge of achieving finer pitch, higher performance, and better reliability. The demand for the higher I/O interconnect count requires finer interconnect pitches. In recent days, fabrication processes of copper column interconnects and solder bumps using thick photoresist electroforming molds and electrodeposition process gained much attention [194-198]. Considering higher stand-off as an important factor in package reliability [199], the thick photoresist mold with high aspect ratio shows promising results in fabrication of more reliable interconnects. High aspect ratio ultra-thick photoresist molds are also important in micro electro-mechanical components such as micro-channels [200], coils [194], cantilevers [195], sensors [197] and valves [201]. Metallic bumping in flip chip assembly has some advantages such as greater mechanical strength, improved reliability, increased manufacturability, extended temperature range, higher connection density, and improved electrical and heat-dissipating performance [202].

2.4.1. Function of bumps in the flip chip technology

The mechanical stress caused by difference in the coefficient of thermal expansion (CTE) between the chip and the substrate materials is an important reliability issue in the flip chip assembly process [203, 204]. When the package is subjected to temperature change, differential thermal expansion creates shearing force on the bumps that increases with the distance from the neutral plane of the chip [205]. It was reported that bump-pad interface area is most prone to

failure [206, 207]. Typically repeated thermal cycling leads to fatigue cracking of the bumps, especially with solder bump flip chip assembly. Solder bumps are most common. Gold [45] or polymer bumps [43] can be used instead of solder bumps.

The failure caused by differential thermal expansion can be reduced by increasing the vertical distance between the chip and the flexible substrate, though the die needs to be embedded into the substrate in order to reduce the package footprint. The embedded approach also made possible the fabrication of 3-D packages. In the embedded structure, the metallic bumps absorb the shear force. To address the CTE related problem, non-melting high aspect ratio bumps are used to increase the chip to substrate distance. A lower-temperature eutectic solder on the substrate pad can be reflowed to complete the connection. To increase the I/O density, the bump must have higher aspect ratio. It has a negative side-effect as the longer conductive path increases both the electrical and the thermal resistance. The electroplated copper bumps maintain greater chip-to-substrate height and provides stress relief to the die. The construction of the package without any underfill is another possibility. If the assembly process includes the application of underfill, the increased chip-to-substrate height facilitates faster flow and more uniform distribution. The copper bumps offer greater mechanical shear strength and increase the overall robustness of the assembly. A lead-free solder or silver cap may be used to protect the bump from ambient oxidation. Recently, the fabrication of copper column array area studs using thick photoresist molds and electrodeposition process has gained much attention. Fabrication of extra-long stud bumps on the metallic pads of the RFID chips is possible solution to the problems associated with underfill technology. The higher stand-off is an important factor in the package reliability [48] and the thick photoresist shows promising results in fabricating more reliable interconnects with high aspect ratios. As the copper interconnects are high aspect ratio

structures themselves, ultra-thick photoresist electroforming molds are used to fabricate them. SU-8, a popular thick film photoresist, already proved its usefulness in fabricating ultra-thick molds but the complete stripping after electroplating is a serious issue [195, 208, 209]. SU-8 is a permanent resist and its stripping is very difficult due to cross-linked formation in the mold. The cross-linked SU-8 can be removed by water jet, bead blast, high-temperature ashing and laser ablation. Aggressive removal process of SU-8 leads to deterioration of the integrity of microstructures. In an effort to find easily strippable thick film photoresist for microforming, PMMA [162], THB151N [159], DiaPlate 133 [163], and KMPR [164] was reported to be used for the preparation of HAR molds.

2.4.2. Microfabrication process with THB151N

THB151N (JSR Corp., Japan) is a negative photoresist that is extensively used for fabricating HAR microstructures. Such features require a thick layer of resists and THB151N provides these capabilities. For example, the possibility to spin-coat a 130µm thick film with this photoresist was demonstrated [210]. Thick photoresist such as THB151N are widely used in the fine-pitch flip-chip applications because they provide a suitable mold for electrodeposition of HAR metallic interconnects that allow the flip chips to be assembled to the substrate without underfill. There are other applications of this material such as the fabrication of microchannels [200], coils [194], cantilevers [195], sensors [197] and valves [201]. THB151N is easily strippable compared to another HAR material, the commonly used epoxy-based negative SU-8 photoresist. The same photoresist was successfully used in this work for fabrication of copper interconnects, even with a higher length.

2.4.3. Laser ablation of THB151N

As the development of the unexposed portion of the negative photoresist becomes difficult with the increase in the aspect ratio, a laser dry etching technique [49] was used to open up the microvias before the electroplating. There are some reported problems associated with dry etching, such as low absorption coefficient [50], material carbonization [51] and debris contamination [52]. In order to mitigate these problems, a novel photopolymer based on the stock THB151N resist was developed and optimized for laser ablation at 248 nm wavelength. The procedure shown in Figure 43a was followed to synthesize the novel carrier gas sensitizer, herein designated as 9-Ph-OX.

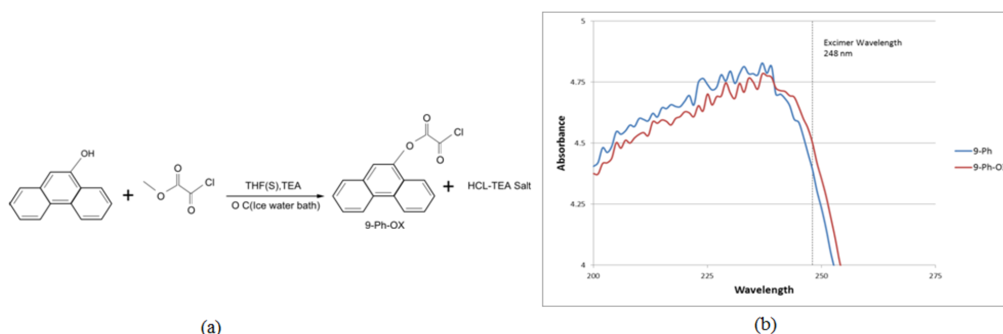

Figure 43 (a) Synthesis of the 9-Ph-OX carrier gas sensitizer (b) Ultraviolet-visible (UV-Vis) spectra of 9-Ph-OX and 9-Ph [132]

The UV-vis spectra of 9-Ph-OX and 9-Ph are shown in Figure 43b, which indicates strong absorption in the 248 nm range. The detail of the synthesis process of 9-Ph-OX was reported elsewhere [132]. In this work, a uniform layer of THB151N photoresist with a thickness of 160 µm in a double spin coating process on a 200 mm diameter wafer was formed. The microvias were ablated on the resist layer using an Optec MicroMaster Excimer Laser Station. The laser station in these experiments was equipped with a 248nm ATLEX 300 SI short pulse excimer UV laser source and a three-element confocal UV micromachining module. The repetition rate could be varied from a single shot to 500 Hz. The ablated vias were characterized

by scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDX). The SEM images were taken using a JEOL JSM-6490LV Scanning Electron Microscope. The EDX analysis was performed to analyze the debris found on the bottom of the microvias. X-ray information of the debris was obtained via a Thermo Nanotrace Energy Dispersive X-ray detector with NSS-300e acquisition engine. Examples of laser ablated microvias in the stock and modified resists are compared in Figure 44. The laser ablated microvias in the stock resist were conically shaped, the ablated surface very rough (Figure 44a), and the ablation rate low. After the material modification, the ablation rate showed significant improvements and microvias with nearly straight walls were easily achieved (Figure 44b).

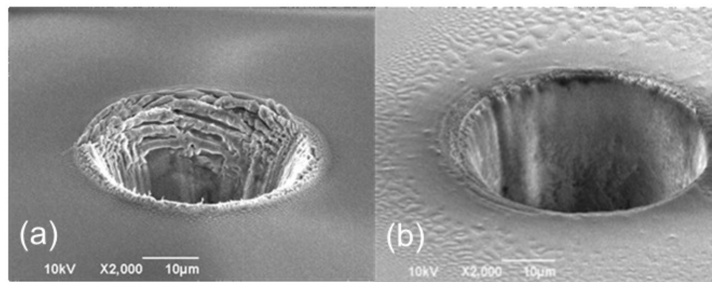

Figure 44 (a) Laser ablated microvia in unmodified THB151N film (b) Laser ablated microvia in modified THB151N film [132]

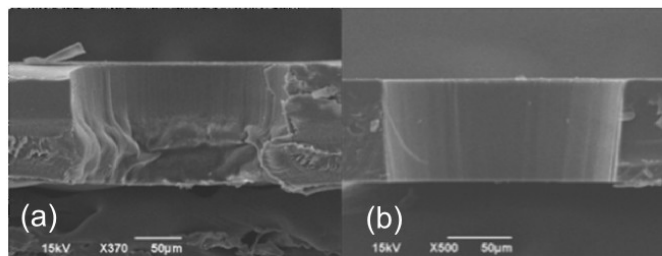

Figure 45 (a) Cross section of the ablated microvia in unmodified THB151N film (b) Cross section of the ablated microvia in modified THB151N film [132]

The cross-section of the microvia formed in the unmodified THB151N shows the deformation inside the microvia hole (Figure 45a). The contrast with the cross-section of the

microvia in the modified THB151N is striking. As seen in Figure 45b, the laser ablation of the modified resist produced nearly straight microvias with a smooth surface finish.

The most important criteria for successful laser ablation of polymers are the high absorptivity, existence of exothermic decomposition of the material, and generation of gaseous ablation products[194]. The faster and cleaner ablation of the “drop in” sensitizer modified THB151N was attributed to the enhanced absorption at the incident laser wavelength at 248 nm due to the addition of 9-Ph-OX. In addition, the new sensitizer is comprised of anthracene and oxalyl group that act as a UV laser energy absorber and carrier gas generator, respectively. Previous research suggested that the oxalyl group combined in the photoresist photochemically decompose into gaseous small molecule gases such as CO, CO_2 and CH_4, which eject out from the ablation spot with supersonic velocity carrying ablation debris away [211]. Traces of carbon-based debris were observed on the surface but corona treatment can remove them successfully. The laser-ablated microvias were successfully utilized as a mold in the process of copper electroplating used to stud bump silicon wafer for flip-chip applications.

2.4.4. Electroplating with THB151N

In another approach, 50 μm tall bumps were electroplated on the bare dice using THB-151N in the traditional UV-photolithography method. At first, Cu-sputtered silicon wafers (200 mm dia.) were used to fabricate copper interconnects. The wafers were cleaned thoroughly in piranha bath to get rid of any organic residue and then sputtered with 3000 Å copper films by DC magnetron sputtering. This thin film was used as the seed layer for the copper electroplating. The photoresist was spun on the wafer in a SUSS RC-8 Spin coater system. Figure 46 shows the spin curve for the THB151N.

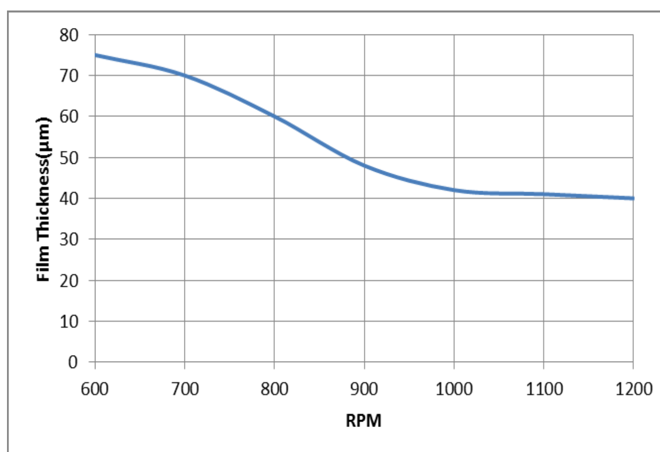

Figure 46 Single coating spin curve for THB-151N

At low spin speed, the uniformity of the resist layer is very poor. To achieve the target thickness of 160 µm, spin coating was performed twice and the spin speed and soft baking time was optimized. The optimized parameters for the double-step spin-coating operation are presented in table 4.

Table 4. Spin coating recipe for THB151N photoresist

Layer	Dispense Speed (rpm)	Dispense Time (s)	Spin Speed (rpm)	Spin Time (s)	Soft bake temperature (°C)	Soft bake duration (min)	Average layer thickness (µm)
First	300	10	1000	20	120	5	90
Second	300	10	1000	20	120	5	160

Due to the high viscosity, the photoresist tend to form edge beads which make some difficulties in the exposure process. To get rid of the edge bead effect, acetone was used for the last 15 s while spinning. A soft baking for 5 minutes at 120° C was carried out right after spin coating to evaporate the solvent out of the layer. The photoresist mold was exposed in a Carl-Suss mask aligner for 150 s at 10 mJ/cm^2 followed by development for 20 min in PD523AD

developer. 100 µm diameter vias were opened quickly in the 160 µm thick mold. The resist thickness and the vias are reproducible using the given parameter. After development, it was hard baked for 60 s at 90° C followed by plasma etching treatment in a Phantom TRION plasma etcher (250 mTorr, 200W, 240 s and O_2 at 45 sccm) for 6 min to clean the residue in the bottom of the microvias. The developed microvias were electroplated with copper in a copper plating bath with the current density 20 mA/cm^2. Both the DC plating and pulse plating were used to compare the plating quality. The DC plating produced the more uniform electroplating rate and denser deposition layer. The deposition rate 0.33-0.50 µm/hour could be achieved depending on the position of the microvias in the photoresist mold. The electroplating was stopped when the Cu bumps reach the desired height. Then it was electroplated with Ag to place 5 µm thick protective silver caps on top of the bumps to prevent ambient oxidization. The electroplating parameters to fabricate the tall pillars were optimized. Long immersion in the stripper showed delamination problem of the Cu seed layer. The plasma etching also makes the stripping difficult. In total, 232000 interconnects can be fabricated altogether on a 200 mm Alien Higgs-3 RFID Wafer in a single process. The scanning electron micrographs of electroplated copper bumps are shown in Figure 47. The cross-section of copper stud bumps is presented in Figure 48.

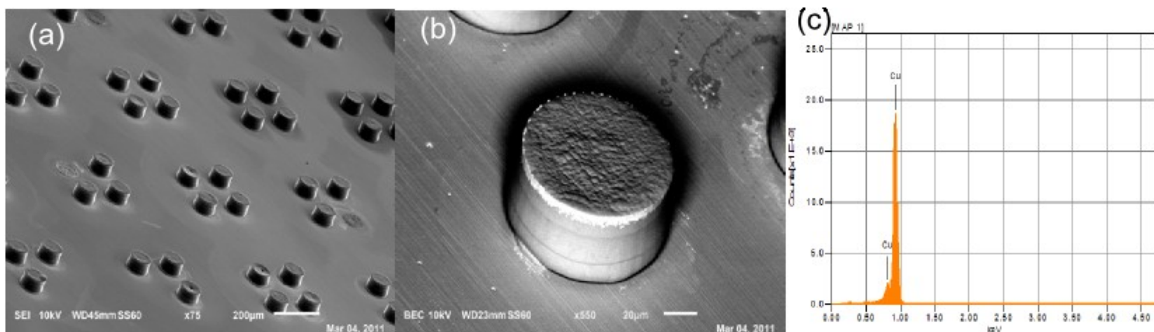

Figure 47 Scanning electron micrograph of (a) electroplated bump array (b) a single bump (c) EDS of the bump shows the purity of copper plating

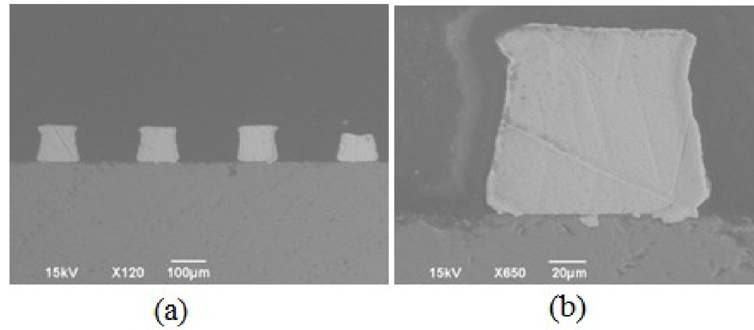

Figure 48 Scanning electron micrographs of (a) array of copper bumps (b) a single bump

2.4.5. Microfabrication with KMPR negative-tone photoresist

In another approach, the electroplated bumps were fabricated using KMPR 1050 negative-tone photoresist which is high contrast and epoxy based. The stripping of KMPR 1050 is fast if developed using alkaline developer. It offers excellent adhesion, chemical and plasma resistance. It offers some unique advantages such as good mechanical properties and low optical absorption in the near-UV range [208, 212]. 1000 µm thick photo resist film with a 40:1 aspect ratio can be formed in a single spin cycle [198]. KMPR shows much stronger moisture resistance properties than SU-8 [213]. Electroplating of 4 µm wide lines with an aspect ratio of 4:1 using KMPR molds were reported in the literature [214]. Electroplating a 50 µm thick nickel support (having 50µm lines) for a thin palladium membrane was also reported by Zhang et al [215].

2.4.6. Experimental details

In this work, a 50 µm thin wafer was attached to a handle wafer (200 mm diameter) with the help of copper adhesive tape. The conductive tape ensures continuous conductivity while electroplating. The handle wafer with the attached thin wafer was sputtered with 500 Å Titanium and 3000 Å thick Cu film. The titanium was used as an adhesive to prevent Cu seed layer from being delaminated. The sample was spin coated with KMPR-1000 following the spin curve shown in Figure 49.

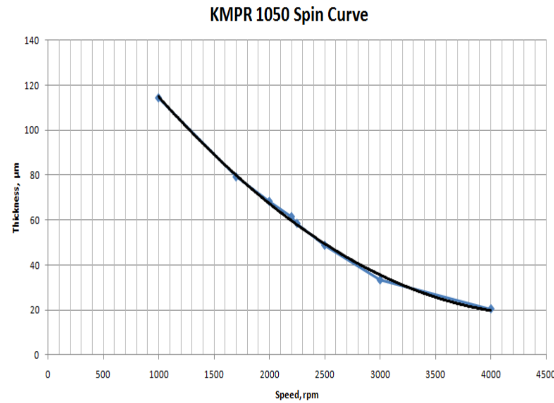

Figure 49 Spin curve for KMPR 1050

The photoresist was kept in syringe in a cold environment to facilitate future deposition. Before using, it must be thawed for 24 hours at 20ºC. Developer should be removed from fridge and allowed to approach ambient temperature. Hot plates were turned on and allowed to settle at the desired temperature. The wafer was cleaned using plasma etching and primed to increase adhesion. 3 ml of KMPR was dispensed on the 6 inch wafer to make a puddle and kept for 10 min to get rid of any possible air bubble. The photoresist was spin-coated on the wafer using a Carl-Suss RC-8 spin coater. The spinning cycle had two stages. Initially the photoresist was spun at 500 rpm for 10 s, and then it was spun at 2250 rpm for 30 s to fabricate a 62 µm thick electroforming mold. After the spin coating cycle, the coated wafer was heated on two separate hotplates, initially for 10 min at 65° C and then for 20 min at 95° C to evaporate the solvent in the photoresist. After the soft bake, the wafer was UV-exposed in a Carl-Suss UV mask aligner using hard contact method for 47.5 s at the power intensity 10 mJ/cm^2. The Mylar mask was used to expose microvias of 70 µm diameter. After exposure, the wafer was hard baked for 5 min at 65° C, following a 4 m heating at 95° C. It was developed in a KOH bench using PD523AD developer. It took 20 min to fully develop a 62 µm thick mold. It was rinsed with DI water and dried with N2 blow gun. The mold was inspected using a Nikon Microscope to make sure that

the opened vias are clear of residue. Later, the sample was plasma treated in TRION Phantom Plasma Etcher using 100W power at 100mTorr and 10sccm-O_2 for 120 s.

2.4.7. Copper electroplating

The copper bumps were electroplated at 200 mA for 60 min using WA-4 electroplating bath. The sample was attached to an electroplating housing and immersed in the plating bath at 25°C. The temperature was maintained constant to ensure the uniform plating rate. The additive was used to maintain the concentration of the plating bath constant, thereby achieving dense surface structure. The height of the bumps was determined using Tencor profiler in a regular interval to measure the plating rate. The SEMs of the electroplated bumps are shown in Figure 50.

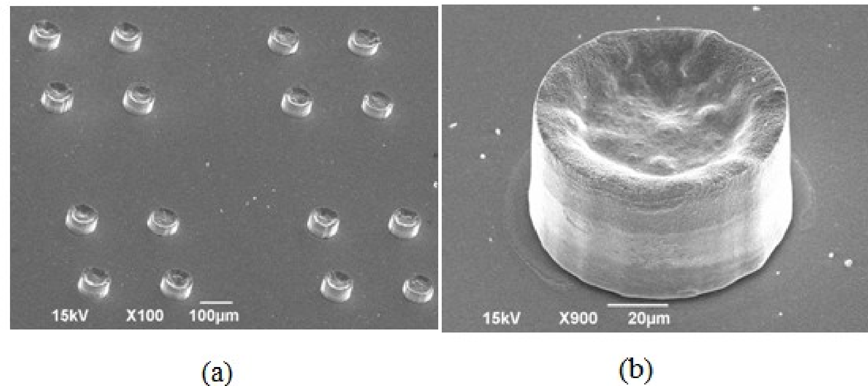

Figure 50 (a) An array of electroplated bumps (b) A single electroplated bump

The plating rate and the bump planarity is a function of the current density, the concentration of electrolyte solution and the area to be plated [210]. The uniformity of the Cu bumps was within the range of 5 µm throughout the wafer. After electroplating the stud bumps, the photoresist was stripped using the ALEG Baker-625 stripper at 80° C. Later, the bumped silicon was laser-diced to singulated the bumped dice. The SEMs of the bumped silicon dice are shown in Figure 51.

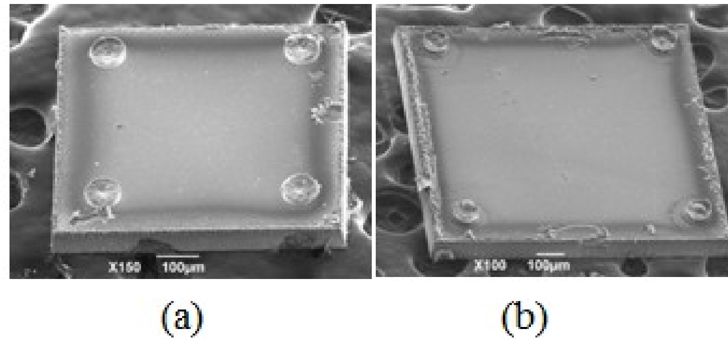

Figure 51 Scanning electron micrograph of (a) 670x670 µm (b)1000x1000 µm electroplated bumped die

2.4.8. Wire bonding

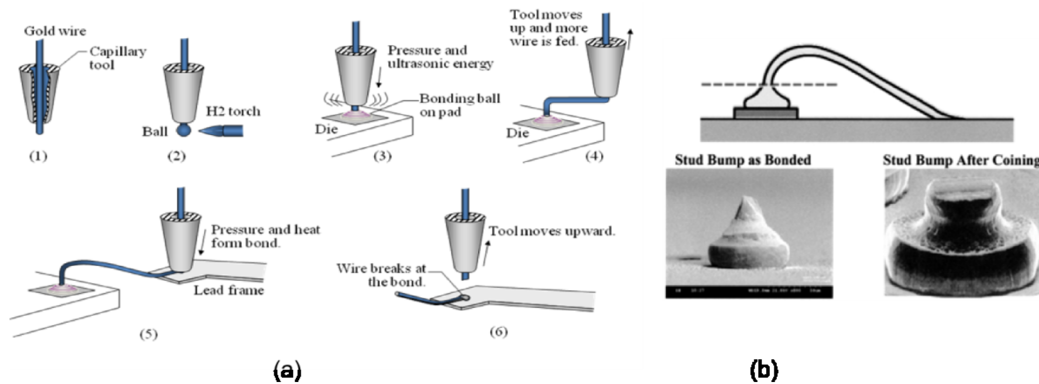

Figure 52 (a) Process sequence of thermosonic ball and wedge bonding (b) Shearing of wire to form stud bumps

In conventional flip chip method, lead-based solder paste is stencil printed or electroplated onto the under bumping metallization (UBM) surface of the die. The printed solder bumps are reflowed to fabricate semispherical solder bumps [216]. A newer approach that offer fast bump formation in flip chip technology is thermosonic stud bump bonding (SBB) [45, 216-220]. Stud-bump bonding (SBB) technology, first developed by Matsushita [221], proved useful and reliable to overcome the thermal stress problem in the microelectronics assembly process.

From a design point of view, gold bumps can carry higher currents than solder bumps and can be used for power applications. Stud-bumped dice can be assembled using anisotropic conductive adhesives at ambient or moderately high work temperature that helps reduce thermal damage to the chips.

The use of conductive adhesives eliminates solder defects such as flux residues that may cause problems with underfill adhesion and corrosion [217] and still represents the lowest-cost assembly for lower-density products [222]. Kumano et al. [45] reported chip-on-flex (COF) using SBB flip-chip technology. The interconnections between electrodes and the substrate were fabricated as a two-stepped Au bumps using the conventional wire-bonding method. For low to medium I/O devices, stud bumping has significant cost advantages over electroplated or solder deposited bumps [223]. Wire bonding is a wide spread method for the interconnect fabrication between the functional chip and the PCB. There are different variation of wire bonding technology such as ultrasonic wedge bonding, thermocompression bonding, thermosonic ball and wedge bonding etc [224]. It can also be used to fabricate stud bumps on the bonding pads. The process sequence of thermosonic ball and wedge bonding (as shown in Figure 52) is modified to fabricate stud bumps. In this method, the bump is created on the bond pad, followed by the shearing of wire to form pillar-like studs on top of the ball [225]. The stud bumping method has several important attributes[226] such as (1) no requirement for UBM (2) entirely mechanical (3) lead-free (4) lack of any environmental issues. The major drawback is that the studs are not uniform in tail heights and subsequent coining process might be necessary[227]. It is also not suitable for high aspect ratio studs. Copper, gold or aluminum wires can be used for wire bonding. Gold wires are better in making taller bumps [224]. Off-the-shelf gold wires are designed for manual wire bonder (breaking load, 6-8 g) and high-speed autobonder (breaking

load, 8-12 g). This extra strength is necessary in the heat-affected neck region for better loop formation and thermal cycle performance. Sometimes, different dopants such as beryllium or calcium are used to stabilize these wires. Gold wires are typically supplied in annealed state. The portion immediately above the ball would become annealed during wire melting and ball formation, allowing easy break-off at the neck. The HAZ (heat affected zone) shows hardness 20% lower than the rest of the wire. The bondability between metals is presented in Figure 53.

	Al	Be	Cu	Ge	Au	Fe	Mg	Mo	Ni	Cb	Pd	Pt	Re	Si	Ag	Ta	Sn	Ti	W	U	Zr	Pb
Aluminum	●	●	●	●	●	●	●	●	●		●	●		●	●	●	●	●		●	●	
Beryllium		●	●			●												●				
Copper			●		●	●	●	●	●			●	●		●	●		●			●	
Germanium					●							●										
Gold					●	●			●			●		●	●			●	●		●	
Iron						●		●	●			●	●		●	●		●	●	●	●	
Magnesium							●								●			●				
Molybdenum								●	●							●		●	●		●	
Nickel									●	●		●	●		●	●		●	●			
Columbium										●						●						
Palladium											●				●							
Platinum												●		●								
Rhenium													●			●		●				
Silicon																●						
Silver															●	●					●	
Tantalum																●		●	●			
Tin																	●					
Titanium																		●	●			
Tungsten																			●			
Uranium																				●	●	
Zirconium																					●	

Figure 53 Metals which have been successfully joined together by ultrasonic welding or in which welding feasibility has been demonstrated [228]

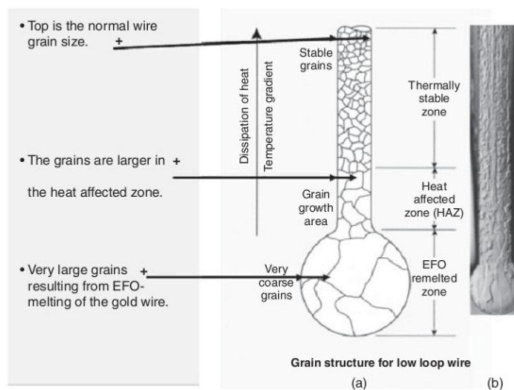

Figure 54 (a) Sketch of the grain structure for a gold wire before and after ball formation, showing the heat-affected zone (b) An etched gold wire and ball revealing the actual grain structure [229]

This table is not customized for micro-electronic activities but may be used as a guideline to explore new bonding possibilities. The grain structures of a formed stud bump have three

distinguishable regions. The free air ball region has the largest grain size. The heat affected zone also has larger grain size than normal. The regions are depicted in Figure 54.

In this work, AW-9 gold wires (Kulicke and Soffa) were used to form stud bumps. The gold purity of the AW-9 is >99.99% and the non-gold ppm is <100. The thermal conductivity is 3.17 W/cm-K, electrical resistivity is 2.3 μΩ-cm and the CTE is 14.2 ppm [230]. Au studs were fabricated using a K&S 8028 semi-automatic wire bonding machine. The AW-9 wire was chosen because of its wider bonding window, lower force and power requirements, and better bondability than the traditional wires. Horsting [231] reported that the bond will remain strong even after long times at high temperatures if the bond is well made and there are no impurities present in the bond interface. If impurities are in the interface or the bond is poorly welded, then the bond-strength may degrade rapidly during thermal cyclic stress. The aluminum seed layer was plasma treated before wire bonding operation in order to clean all impurities. The formation of intermetallic compounds in the interface was reported when Au is thermosonically bonded to Al seed layer [229]. The intermetallic compounds appear during the actual bonding process[232]. Gold-aluminum intermetallic compound formation and associated Kirkendall voids is an important reliability issue for stud bump bonded dice. Philofsky [233-235] reported the relation between intermetallic formation and high process temperature while microelectronic bonding. Murali et al [236, 237] reported that in case of 1-mil wire size, Kirkendall void growth is less significant, based on the analysis of interface morphology and metallurgical behavior of the bond during thermal ageing. As a proof-of-concept experiment, 25-μm (1-mil) diameter AW-9 wires were used to make the studs on the 80×80 μm bond pads of test die. After the initial screening experiments, five parameters (separation height, bump height, smoothing speed, fab diameter,and bond force) were selected for a further optimization study with an objective

maximizing the length of the studs. The candidate parameters for the design of experiments are given in Table 5:

Table 5. Parameters for design of experiment (DOE) study

	Low	High
Separation height	0.5	1.0
Bump Height	0.5	2.0
Smoothing Speed	75	100
FAB Diameter	2.3	2.6
Bond Force	20	40

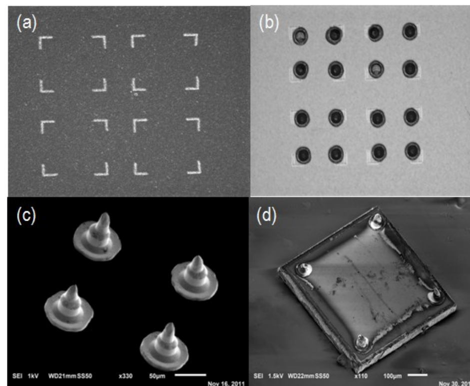

Figure 55 (a) Laser marking on seed layer (b) Stud bumps on Al seed layer (c) Scanning electron micrograph of stud bumps on silicon substrate (d) A single stud-bumped die

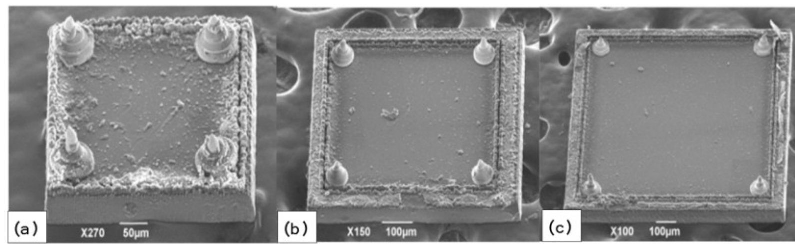

Figure 56 Scanning electron micrograph of (a) 350x350 µm (b) 670x670 µm (c)1000x1000 µm stud bumped die

The parameters were selected from empirical data and the concept of the design of experiments (DOE) have been applied for optimize the process. A 25 full factorial design with a total of 32 experiments was carried out with these parameters. Their optimum values were identified and then used to fabricate 50-µm tall stud bumps at a bonding temperature of 200° C. as the one shown in Figure 55. The silicon substrate was sputtered with 2 µm thick Al as a bonding surface. The Al layer also provides continuity to the singulated dice. The intended positions were marked with laser (Figure 55a) so that stud bumps can be easily placed on wafer (Figure 55b). Later, the bumped silicon substrate was laser-diced to singulated bumped dice. The SEMs of stud bumped dice are shown in Figure 56.

2.5. Preparation of Flexible Substrate

The key idea of the embedded package, used in this research, was to accommodate the versatile uses through the unique flexibility of the package. Based on the electrical, physical and chemical properties of different flexible substrates, liquid crystal polymer (LCP) was selected as the substrate material. A face-up approach was followed while designing the embedded package. Conventional clean room fabrication techniques and laser micromachining were employed to prepare LCP substrates for the test structure of embedded dice. The details of the fabrication process will be described in this chapter, along with an explanation of the process flow.

2.5.1. Flexible substrate material

LCP is a thermoplastic polymer material that is very suitable for microelectronic packaging. LCP offers excellent structural and physical properties which is better than other engineering polymers. It contains interlinked rigid and flexible monomers. Rigid sections of the molecules coordinate themselves side-by-side in the shear flow direction while in the liquid

crystal state. After the formation of final orientation, their direction and structure remain stable below the melting temperature [238, 239]. Traditional microfabrication techniques such as plasma etching, laser micromachining and metallization can be accomplished with LCP [240]. The application of LCP for high-density printed circuit board (PCB) fabrication [113, 241] and semiconductor packaging [238] was reported. LCP has excellent chemical resistance, very low moisture absorption (~0.02%), low moisture permeability and high barrier performance for most of the gases [238]. Most acids, bases and solvents cannot alter the properties of LCP for a substantially long duration of time [113]. LCP is widely used for flexible antenna array [242], RF MEMS [243], Conformal Double Exponentially Tapered Slot Antenna [244] and 3D integrated package [245].

2.5.2. Laser ablation of polymers

The history of laser ablation started almost 20 years ago, when it was first reported by Kawamura et al [246] and Srinivasan [247]. Laser ablation can be referred as a one-step dry etch process in which energy-concentrated, highly directional laser beam is used to pattern a material. The advantages are fewer manufacturing steps, higher production throughput, lower costs and the elimination of wet chemicals used in the development stage as compared to the photo etching process [248]. Today, this is one of the most popular techniques in the area of microelectronic fabrication, micromachining, film deposition and MEMS. Laser beam is considered as an important processing tool for high-precision micromachining of polymeric materials. Laser have been used for a long time for processing materials in the form of material removal, laser annealing, laser microdrilling or laser machining. The material removal mechanism in laser ablation is accomplished by breaking the chemical bonds using the fluence of incident laser beam that exceeds the ablation threshold value. When the material is ablated, it turns into

energetic fragments such as atoms, groups of atoms, ions and electrons. These fragments are ejected from the processing zone at a supersonic speed. Solid debris and energetic gas is created in the ablation process. The substrate of the processing zone is exposed to little thermal damage as most of the absorbed energy is carried off with the ejected material. The physical mechanism of laser ablation is shown in Figure 57.

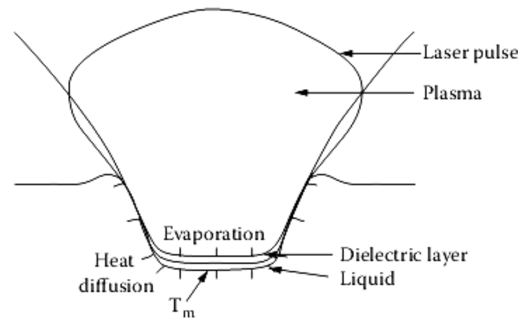

Figure 57 Relationship between plasma generated during laser pulse and interaction with the polymer and its surroundings [249]

The laser radiation parameters and the material properties controls optical absorption, heat conduction, phase transitions, evaporation kinetics and plasma dynamics[250]. It was also reported that the ablation by pulsed UV laser creates less thermal damage than that by lasers with longer wavelengths. Short UV optical penetration depth and the small spatial extent of heat diffusion is the main reason behind the absence of significant thermal damage [251]. Excimer and Nd: YAG lasers were successfully used to direct imaging of the flexible circuits[252, 253]. Ablation rate of an UV pulsed laser in LCP is linearly dependent on fluence [254]. According to their work, the laser ablation of LCP is a photothermal process. It was reported that frequency harmonized Nd: YAG lasers have several advantages such as a relatively low operational cost and high repetition rate, is compared to Excimer lasers [254].Laser ablation of commercially available polymers such as polyimide (PI), poly (methyl methacrylate) (PMMA), poly (ethylenterephthalate) (PET), and Teflon (PTFE) have been studied extensively. The results

concluded that photochemical decomposition mechanism dominates under shorter UV wavelength laser ablation and the photothermal decomposition mechanism is more significant under higher fluence and longer UV wavelength laser ablation. The higher resolution in terms of laser ablated micro-patterns in polymer materials is provided by the laser-induced photochemical decomposition.

2.5.3. Cu test pad fabrication

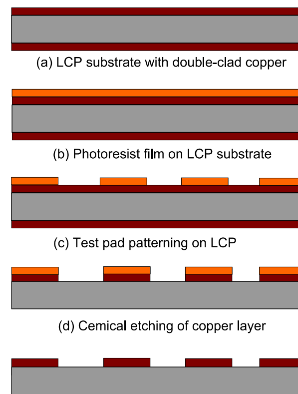

Figure 58 The process flow of copper test pad fabrication

The laser ablation characteristics of LCP were very suitable for the embedded package structure that was designed for this research. A double copper clad laminate LCP (Rogers Corporation) with a melting temperature of 315° C was used in package preparation. Its properties are specified in Table 6. The LCP was spin-coated with i-line photoresist to form a 1 μm thick film. The pattern of the test pad was created on the photoresist layer using the UV aligner. It was developed in OPD262 positive photoresist developer to realize the patterns. The sample was chemically etched to remove the unwanted copper clad regions following acetone stripping to remove the protective i-line resist films. The process flow of copper pad fabrication on LCP substrate is shown in Figure 58.

Table 6. LCP sheet material properties

	Typical Value	Unit
Mechanical Properties		
Dielectric Thickness	2.0	mil
Metal Cladding	Rolled Annealed Cu	
Metal Thickness	18(0.5)	µm(oz./ft^2)
Initiation Tear Strength, min	1.4	Kg
Tensile Strength	200	MPa
Tensile Modulus	2255	MPa
Density	1.4	gm/cm3, Typical
Thermal Properties		
Coefficient of Thermal Expansion, CTE (30°C to 150°C)	17	ppm/°C
	17	
	150	
Melting Temperature	315	°C (Typical)
Relative Thermal Index - RTI	190	°C (Typical)
	240	
Thermal Conductivity	0.2	W/m/°K
Thermal Coefficient of εr,-50°C to 150°C	24	ppm/°C
Electrical Properties		
Dielectric Constant, 10 GHz,23°C	2.9	
Dissipation Factor, 10 GHz,23°C	0.0025	
Surface Resistivity	$1x10^{10}$	MOhm
Volume Resistivity	$1x10^{12}$	MOhm cm
Dielectric Breakdown Strength	1378	KV/cm
Environmental Properties		
Chemical Resistance	98.7	%
Water Absorption (23°C, 24hrs)	0.04	%
Coefficient of Hygroscopic Expansion, CHE (60°C)	4	ppm/%RH
Flammability	Vtm-0	

2.5.4. Laser ablation of LCP

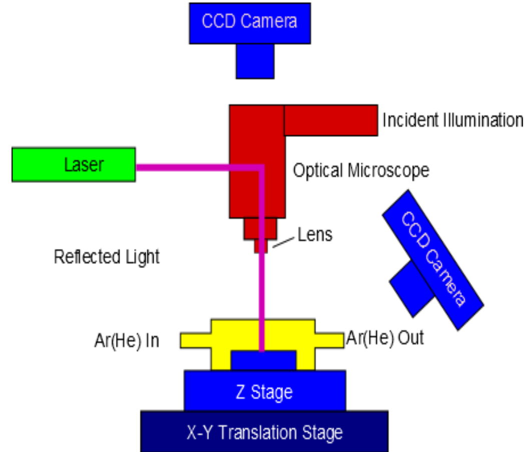

Figure 59 Schematic view of laser ablation system

In the next step the LCP substrate was transferred to an Optek short-pulse 248 nm excimer laser system for receptor pocket, via and trench micromachining. The schematic view of the laser system is shown in Figure 59. It was a critical process step to ensure precise micromachining, thereby providing good connection, accommodation of electroplated bumps and unobstructed flow of conductive silver paste. In case of blind via drilling, thermal damage to the chip is an important concern [47]. A shaped, top-hat beam profile was used to accomplish this step. In our approach, via holes were drilled before the die placement, making the process much simpler and straight-forward. The blind via holes that ensure the connection to the test pads required more careful operation. The bottoms of these vias were cleaned using laser ablation. The copper pads were thick enough (18 µm) to tolerate the laser ablation of LCP substrate. Typical ablation parameters were 10 bursts at a rate of 50 Hz with pulse energy of around 140 µJ measured at the sample stage. Stage speed was set at 100 µm/sec giving ablation rates of about 16 µm per pass in both the substrate and laminate material. The targeted dimension on the bottom of the receptor hole was 380x380 µm (die size is 350 µm square), 700×700 µm

(die size is 680 µm square) and 1030x1030 µm (die size is 1000 µm square). The ablated receptor pockets are shown in Figure 60.

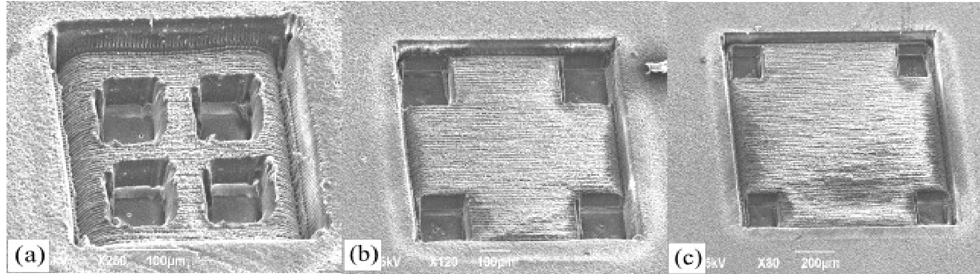

Figure 60 Scanning electron micrograph of (a) 380x380 µm (b) 700×700 µm (c) 1030x1030 µm receptor pockets

Dual-step, 150-µm wide trenches were ablated to interconnect the die to the Cu traces on the opposite side of the substrate. The trenches were 25 µm deep while connecting the die but gradually sloping down towards the copper traces to expose the copper material as seen in Figure 64a. Vias were drilled in the last micromachining step to connect the receptor hole on one side with the trench on the other. After ablation, the micro-machine debris noticed on via bottoms was cleaned using ultra-sonic cleaning for 10 min. The laser ablated trenches were 50 µm deep and 100 µm wide with straight walls. The bottom surface of the trenches was rough due to ablation of polymer and beneficial for making good contacts with PTFI-ed conductive silver paste. The contact profile of a single trench is shown in Figure 61b.

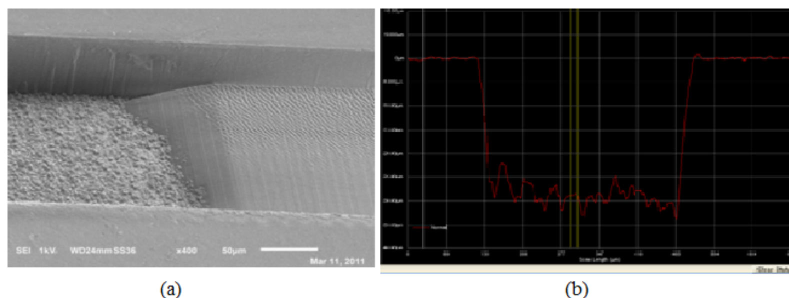

Figure 61 (a) Scanning electron micrograph of the ablated trench structure (b) Contact profile of ablated trench

2.6. Polymer Thick Film Inlaid

The thick-film methods, used to fabricate conductive traces on flexible substrates, are not very effective for resolutions below 50 μm [255]. In order to fabricate high resolution patterns, the alternative to think-film method can be thin-film technology which is comparatively expensive to produce low cost electronic packages. To address this need, a modified mill-and-fill interconnect technology, referred to as Polymer Thick Film Inlaid (PTF-I) was developed in Center for Nanoscale Science and Engineering [121, 122], in which laser-ablated trenches are filled with a conductive paste to produce a high-resolution conductive trace pattern. A similar method was investigated in the Holst Centre in the Netherlands [102, 189].

2.6.1. Experimental results

Previous research indicated that the use of nano-sized conductive particles in the PTF-I paste is extremely important [121]. A conductive paste having low electrical resistivity and suitable for applications by the PTF-I method was developed in CNSE using a mixture of acrylate oligomers as binder, tert-butyl acetate as solvent and μm-sized silver flakes as conductive filler. The chemical composition of the material is shown in Table 7 [256]. The solvent tert-butyl acetate is a VOC-exempt solvent and therefore the formulation is environmentally friendly. Additional advantages of this formulation were lower shrinkage and less cracking during bending test.

Typically, the metallic nano-size pastes consist of polymeric binder, solvent and metallic particles. Curing of a metallic nano-sized paste is referred to as a thermally activated cross-linking process of polymer in which the metallic particles are dispensed. The printed or deposited nano-particle paste can be cured by heating the entire substrate in the oven. The volatiles present in the paste are removed during the curing process. When the polymer cross-

links, or cures, it shrinks and bring the particles together thus improving conductivity, there is no material transfer between the particles in curing method. In the formulated paste, the acrylate molecules are used as a reactive solvent. The monomers lose their viscosity prior to polymerization and then form a solid film. The benzoyl peroxide, present in the binder system, is thermal free-radical initiator. While thermal curing, it decomposes to give free radicals that initiate polymerization of the monomers (as shown in Figure 62) [257].

Table 7. Conductive silver paste formulation

Component	Description
Binder	Combination of acrylated epoxidized soybean oil, and trifunctional acrylate (19.8 wt.%) and small concentration of benzoyl peroxide as thermal initiator.
Solvent	Tert-butyl acetate (approx. 2 wt.%)
Conductive particles	Silver flakes, 2-4 µm. (78.2 wt.%)

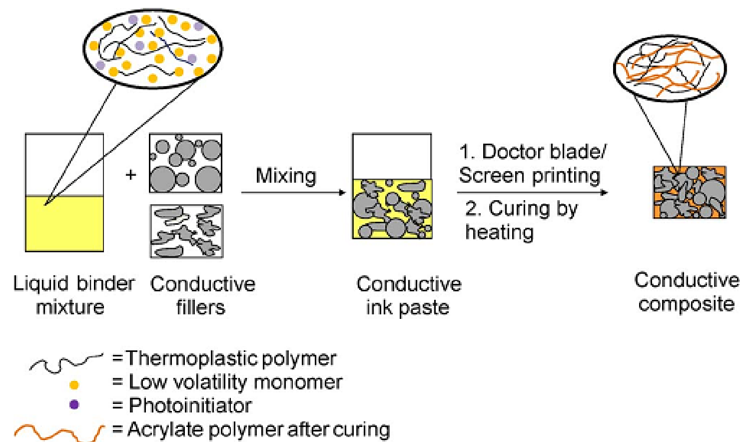

Figure 62 Illustration of the conductive paste system [256]

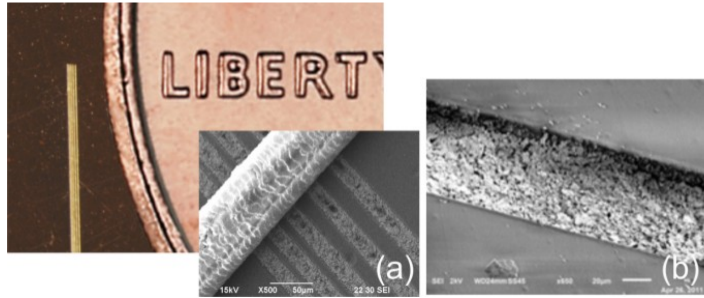

Figure 63 (a) Close-up of PTFI-ed high-density silver lines next to a penny; (Inset) a high-magnification SEM photograph of the same conductor lines compared to a human hair; (b) A cured PTFI line showing no cracking in the material or delamination from the wall [258]

In the proof-of-concept experiment, 20 µm wide conductive traces with an excellent profile were fabricated. The gap between the lines was as low as 6 µm. The minimum linewidth is limited by laser micromachining parameters and metallic nanoparticle diameter in the conductive paste. PTFI process is capable to produce high quality, high density, and high precision trenches at low cost and high throughput [121, 184]. The SEMs of ablated trenches are shown in Figure 63.

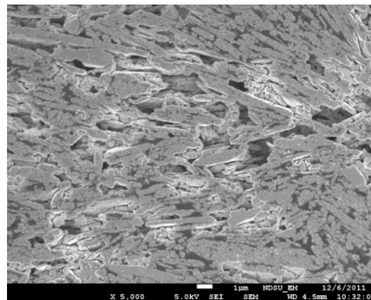

Figure 64 The cured silver nano-particles after 8 hours of curing at 150ºC

The SEM of cured nano-sized paste is shown in Figure 64. The trenches were laser ablated in round corner and square corner design. The trenches were manually filled with conductive silver nano-particle paste. They were subjected to thermal and bend test. Crack

propagation was noticed along the trenches. The SEMs of two different regions are shown in Figure 65.

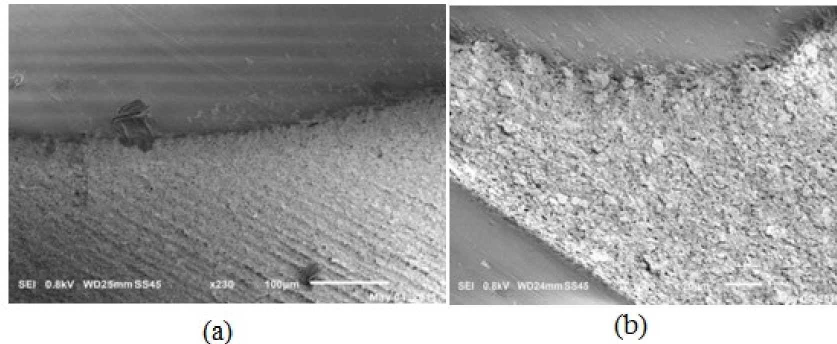

Figure 65 (a) The region between trench and larger pad (b) The region between trench and smaller pad

2.6.2. Thermal cyclic test

In this experiment, 20 square and round cornered trenches were ablated and PTFI-ed with silver nanosized paste and affixed to glass substrate. The samples were put in the ESPEC TSD-100 temperature shock chamber for 100 hours according to JEDEC JESD22-A140C (-55°C to 125°C) test standard. Cycling took place between +125°C to -55°C with a dwell of 10 minutes and a transition time of less than 1 minute. The test was accelerated so that the package could be exposed to two full cycles an hour. The sheet resistance was measured before and after the test. The average sheet resistance for the square trenches measured was 0.018 Ω/sq with a standard deviation of 0.001. The average sheet resistance for the round trenches measured was 0.037 Ω/sq with a standard deviation of 0.014. After the thermal test, the square cornered trenches experienced crack propagation (as shown in Figure 66) and the resistance measurements suggested 16% increase. On the other hand, the round cornered trenches did not show any significant change.

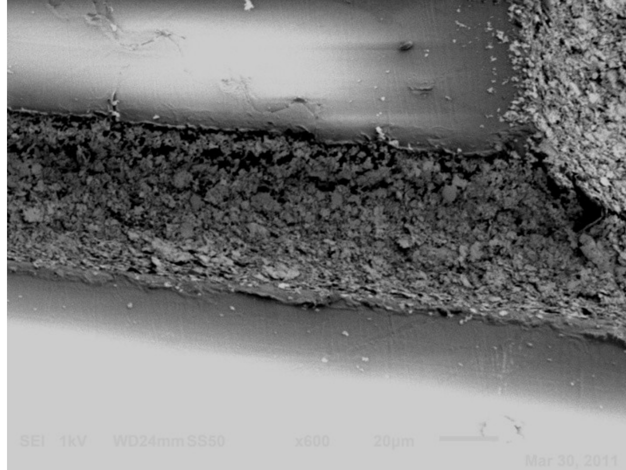

Figure 66 SEM of the crack propagation around the sharp corners in the PTFI-ed trench

2.6.3. Bend test

In order to test the mechanical properties of the material, 25-mm long, 100-µm wide trenches were laser micromachined into a polyimide substrate and PTF-I filled with the paste. 36 samples for each pattern (round and square) were prepared and cured at 150°C overnight after which resistance measurements were taken. For the round pattern, the mean line resistance measured was 2.54 Ω with a standard deviation of 0.23 Ω. For the square pattern, the mean line resistance measured was 2.68 Ω with a standard deviation of 0.27 Ω. The substrates were then subjected to bend tests (100 repetitions each) onto a 50-mm diameter mandrel and the resistance was measured after each test. In the first test the Ag filled trenches were facing the mandrel, essentially subjecting the Ag conductor lines to compression and in the s test the trenches were facing away from the mandrel surface thus stretching the Ag material. The measurements from the round patterns after the first and second bend tests showed mean resistances of 2.73 Ω and 2.87 Ω with standard deviations of 0.19 Ω and 0.43 Ω, respectively. The measurements from the square patterns after the first and second bend tests showed mean resistances of 2.58 Ω and 2.69 Ω with standard deviations of 0.23 Ω and 0.28 Ω, respectively. For the round cornered trenches,

line filling was complete and no cracking or delamination was observed in the lines under optical microscope and SEM imaging. These experiments concluded that the in-house prepared conductive paste possesses the required flexibility, conductivity, and morphology required for creating reliable and small linewidth printed conductors on a flexible substrate such as polyimide or LCP.

2.7. Accelerated Test

Extensive reliability tests are necessary to ensure the electrical performance of the microelectronic packages. The standard tests are selected in such a way so that they reflect the actual working condition of the package. Accelerated tests are carried out in special thermal chambers that simulate the working temperature range. The resistance data collected during the test helps to determine the qualification and performance of the package. The accelerated test creates higher stress in the packages than the normal stress in their operational life time which triggers the failure mechanisms much faster. The actual life time can be predicted using the acceleration factor which can be determined based on the accelerated thermal loading test data. Nowadays, the electronic packages are being used in harsh environment conditions such as space stations experiencing extreme temperatures or aerial combat drones flying at high altitudes. Especially the military grade use of electronic components has imposed rigorous standards for reliability performance.

2.7.1. Accelerated thermal cyclic test

In this work, JEDEC JESD22-A140C test standard was followed to investigate the thermal loading effect on the package. According to this standard, the test must be conducted for 10 cycles to determine the resistance of the package to extremes of high and low temperatures

and ability to withstand cyclical stresses. For evaluating assembly reliability, the thermal cycling test was conducted in an ESPEC TSD-100 temperature shock chamber (Figure 67) according to JEDEC JESD22-A140C test standard. 45 samples were mounted to a glass substrate and put in the thermal shock chamber. The packages were affixed to the substrate with Kapton® tape. Cycling took place between +125°C to -55°C with a dwell of 10 minutes and a transition time of less than 1 minute (as shown in Figure 68). The test was accelerated so that the package could be exposed to two full cycles an hour. This particular temperature range was chosen because they are considered as a good benchmark for harsh conditions.

Figure 67 ESPEC 100 thermal shock chamber

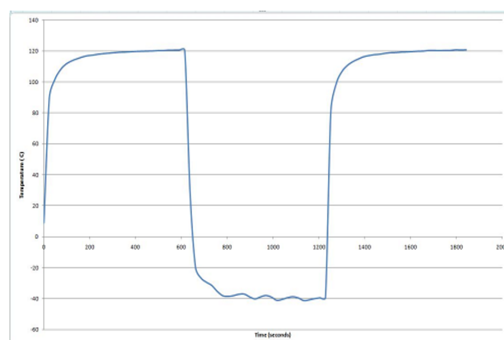

Figure 68 Thermal shock profile captured from thermocouple in thermal chamber

2.7.2. Mechanical bend test

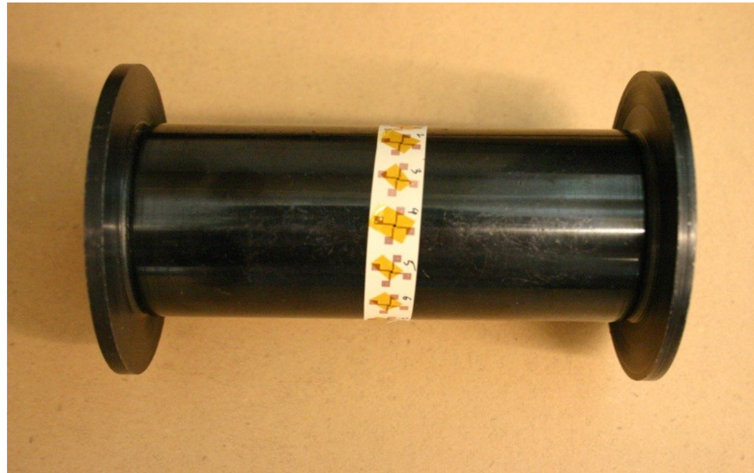

Figure 69 Samples taped to the test fixture in the bending test

The mechanical flexibility property of the package was evaluated through bend test. The test was carried out on 45 samples. The samples were taped on a cylinder of 50 mm diameter (as shown in Figure 69). The flexible substrate was bent backwards 100 times so that the trenches were subject to compression. Then the substrate was bent forwards 100 times so that the trenches were subject to tension. The conductivity data was taken after the backward and forward bending.

2.8. Characterization

In this research, specially designed daisy chain test structures were used. The test patterns used for contact integrity testing were realized onto the LCP substrate with four fan-out copper pad design (18 µm thick), as shown in Figure 70(a). After micromachining the receptor pockets and trenches, the dice were manually transferred into the substrate and sealed with Kapton® tape, as shown in Figure 70(b). At the last step, the trenches were manually filled with silver conductive paste and cured in the oven. A major issue in the design will be the electrical

performance of the package as a function of deformation. The contact resistance between pad-to-pad and the vias connecting the dice with conductive trench was measured. The performance measurement was done using Fluke 179 true RMS multimeter in the class 10000 cleanroom with the help of a Leica inverted microscope. After 100 cycles, the samples were taken out of the chamber and their resistance was measured again. The package was dry etched to clean the oxides prior to the continuity measurement. The average resistance of different packages was analyzed using one-way ANOVA and Tukey test to establish the significant difference between results. In the one-way ANOVA test, the null hypothesis was all resistance means are equal, and the alternative hypothesis was that at least one mean resistance is different. If the null hypothesis is rejected, it will be revealed that the differences among the average resistances of the package types are significant. The collected data points were assumed normally distributed for this test which was supported by normality test. A follow-up Tukey post hoc range test was applied to compare every group mean with every other group mean.

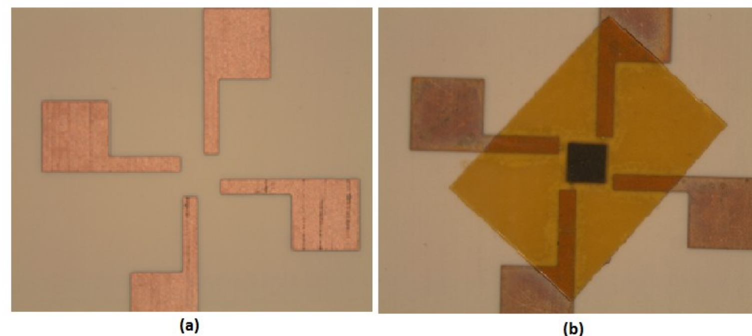

Figure 70 (a)The daisy chain structure of test pads (b) The embedded die in the receptor pocket, laminated with Kapton® tape

In order to investigate the failure mode, the sample was mounted to a molybdenum block using Crystalbond™ (Ted Pella, Redding CA) or carbon tape. Surfaces were exposed using a JEOL IB-09010CP Cross Sectional Polisher (JEOL USA, Peabody MA). Argon milling

conditions were 5kV accelerating voltage for 2 hours or less. The edge of the sample was placed perpendicular to the center of the beam and pivoted +/- 5° during polishing cycle. After polishing, the cross-sections were characterized by scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDX). The SEM images were taken using a JEOL JSM-6490LV Scanning Electron Microscope. The EDX analysis was performed to detect the atomic diffusion of adjacent metallic layers. X-ray information was obtained via a Thermo Nanotrace Energy Dispersive X-ray detector with NSS-300e acquisition engine.

CHAPTER 3. RESULT AND DISCUSSION

3.1. Introduction

After the preparation of embedded die packages was accomplished using the methods described in the previous chapter, thermal cyclic loading test and mechanical bend test were used to assess the electrical performance of the package. The via-to-via resistance measurements were taken before subjecting the packages to thermal loading test and mechanical bend test. Some vias were not perfectly plugged in with silver paste due to manual PTFI operation. These vias were tagged as “bad” and excluded from the performance analysis. The cross-section of a good via is shown in Figure 71(a). The SEM indicates that the silver paste established good contacts with the conductive seed layer on the die. No major delamination was observed. In some packages, delamination along the trench wall was observed (Figure 71b). The high pad-to-pad resistance measurement is the result of the paste delamination at the copper pad interface. As a result, the pad-to-pad measurements were excluded from the performance evaluation.

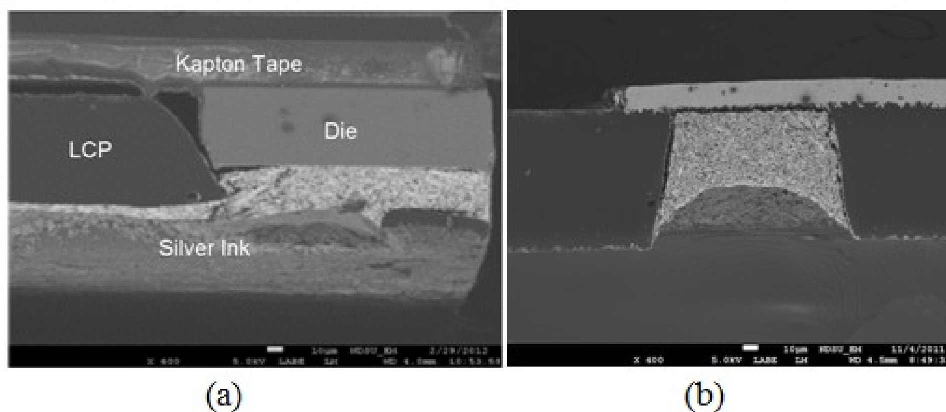

Figure 71 Cross-section of an embedded bare die (a) along the trench (b) across the trench

Two separate via maps were prepared based on the resistance measurement of the vias, as shown in Figure 72. The vias showing high resistance (above 5 Ohms) were marked as defective. The resistance measurements between the defective vias were excluded from the performance evaluation. The resistance measurements were taken again after the tests were finished.

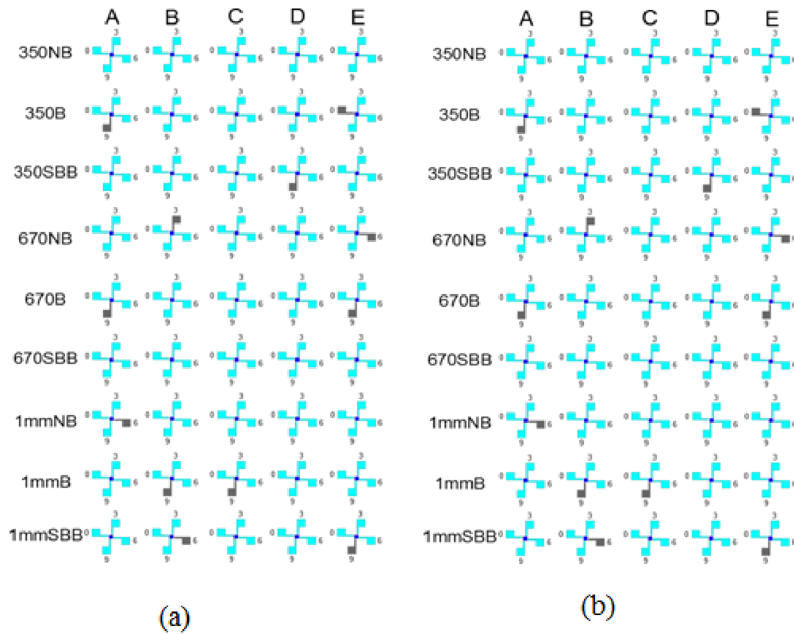

Figure 72 Map of the substrate with the samples showing the "good" and the "bad" vias. The latter are shown in black

3.2. Performance Analysis after Thermal Test

The accelerated thermal test simulates behavior of an electronic package in response to harsh environments, revealing stress related failures as a result of different thermo-mechanical properties as shown in Table 8. The low CTE of silicon die and high CTE of flex substrate may create package warpage, pull and shear stress concentration at the chip/bump interface, as indicated in previous research [259]. If the application temperature exceeds T_g, the organic flex substrates' material properties change drastically leading to early device failure. Care must be

taken to keep the application temperature below T_g. Interconnect failures occur due to thermo-mechanical load through two different mechanisms-thermal effects and thermo-mechanical effects. Thermal effects create metallic embrittlement occurred by the formation of intermetallics in the interface and polymeric degradation in the flex substrate. Many events of thermal failures were reported for flip chip technology [260, 261]. The first degradation effects occurred between 200 º C and 300 º C [262]. Thermo-mechanical failures may occur due to cyclic thermal loading. The bumps are exposed to full stress due to conductive paste delamination. Humidity is an important critical load which influences reliability of the flip chip and embedded chip technology. Failure mechanism is triggered due to die cracking, delamination, interconnect failure, and bond lifting.

Table 8. Typical thermo-mechanical properties of the materials used for flip chip assemblies

	CTE	Poisson Ratio	Young’s modulus
Substrate, LCP	17	0.40	10.6
Chip, Silicon	3.2	0.28	112.4
Bump, Copper	16.7	0.34	110
Bump, Gold	14	0.42	79
Silver conductive paste	17	0.37	76

The bare die package offers larger contact area for the conductive paste to flow and connect the sputtered die to the PTFI-ed trench. Moreover, there is no possibility of stress concentration or joint failure due to bumpless construction. The only possible failure may occur due to delamination of the paste at the paste-copper pad interface as seen in the scanning electron micrograph of the cross-section of the package. The high resistance measurement from the bare die package is the result of the paste delamination at the copper pad interface. In the

electroplated bumped package, the bump diameter is a point of concern because they may crate obstacles to the free flow of the conductive paste. Moreover, the mechanical failure of the plated bumps was reported by several research groups [263, 264].

After the thermal test, the continuity of via-to-via and pad-to-pad locations was tested and no failure was observed. The box-plots of the mean resistance measurements (via-to-via) of the embedded die packages are shown in the Figure 73. For the 350x350 µm embedded die package, the average via-to-via resistance measurement of bare die, bumped die and SBB die package is 0.89, 2.96 and 1.8Ω. The data suggests that the bare package shows the minimum average resistance. Though, the SEM of the cross-section indicates the possibility of short due to paste overflow. For the 670x670 µm embedded die package, the average resistance measurement of bare die, bumped die and SBB die package is 3.18, 3.32 and 1.97 Ω respectively. The data suggests that the SBB package shows the minimum average resistance. For the1000x1000 µm embedded die package, the average resistance measurement of bare die, bumped die and SBB die package is 3.18, 3.32 and 1.97 Ω respectively. For these samples, the SBB packages showed best electrical performance.

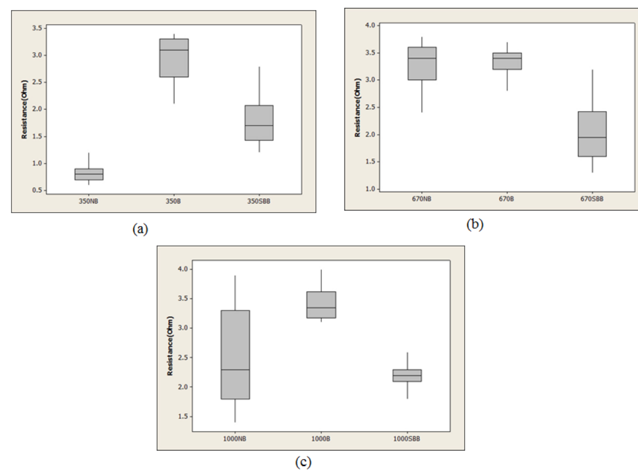

Figure 73 Box-plot of via-to-via resistance measurement of (a) 350x350 µm (b) 670x670 µm (c) 1000x1000 µm die package

The one-way ANOVA test revealed that the mean resistance values for the different die sizes are significantly different. The average resistance values of the three different package types are also significantly different as the F-value is very high and p-value is zero according to the ANOVA result. The Tukey test pair-wise comparison revealed that all the package types showed significantly different performances with a 95% confidence interval. On the basis of the average resistance of the embedded packages, the SBB die packages shows the lowest resistance and percentage change after the thermal test, as shown in the Figure 74.

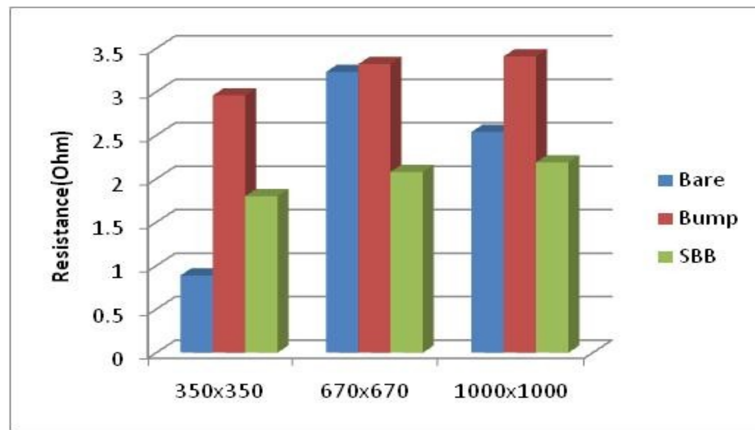

Figure 74 The performance comparison of the three embedded package types after thermal test

The average continuity reading for three different package type suggested that the SBB packages have the lowest and most stable electrical performance. The highest average resistance was observed with electroplated bump packages. The SEM of the cross-section showed that the bumps obstruct the free flow of conductive paste to the die surface as there is a little margin between via walls and the bump profiles. For the SBB package, the diameter of the Au bumps are very convenient (1 mil) to allow the conductive paste to reach the bottom. The Au bumps do not get oxidized easily and makes excellent connections to the bare die. From the result, it is clear that stud bumping is beneficial for good electrical performance of the embedded package.

The bare die package showed the good continuity due to absence of any bumps that may obstruct the free flow of conductive paste. Occasional delamination in the copper pad-silver paste interface spiked the resistance measurement. The thermal loading test did not create any failure in any package. In one set of sample (350x350µm), short due to paste overflow was noticed; hence very low resistance measurement was observed. The pad-to-pad measurements were usually high. The SEM of copper pad-silver paste interface shows occasional delamination effect, hence establishing highly resistive connection (Figure 75a). The satisfactory contact at the silver paste-copper pad interface contributed towards the low resistance measurements (Figure 75b). The lowest resistance measurements were observed in via-to-via measurements.

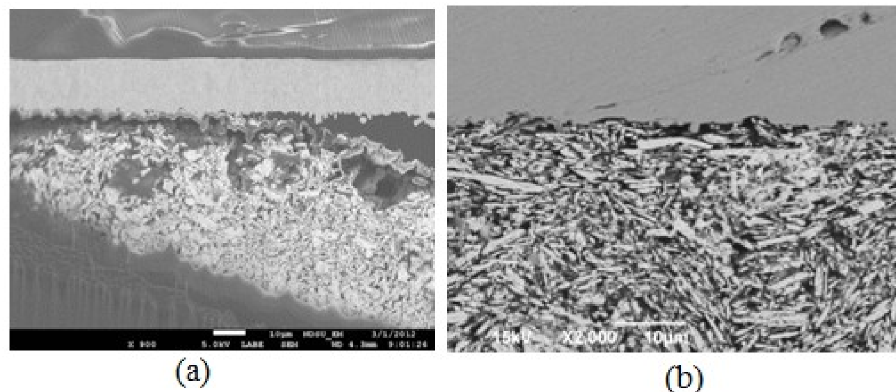

Figure 75 (a) The delamination of silver paste-copper pad interface (b) The good connection at silver paste-copper pad interface

The bumped package showed significant problems regarding the resistance measurements. The electroplated bumps were 70 µm in diameter. When the bumped dice were assembled upside down, the bumps experience a smaller margin while pushing towards 100x100 µm square vias. The continuity measurement showed high resistance measurements most of the cases. The cross-section of a good and bad connection is shown in Figure 76a and 76b respectively.

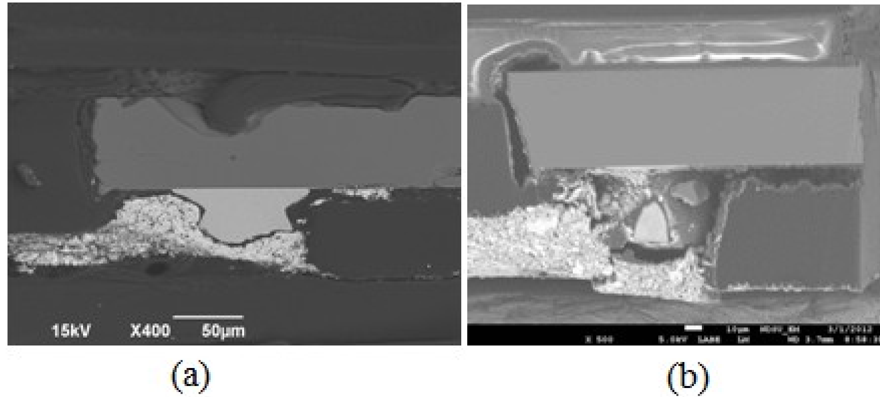

Figure 76 Cross-section of (a) good and (b) bad bumped die package

In the proposed embedded chip fabrication process, reflow step is not required in the thermosonic stud bump bonding that eliminates the possibility of thermal stress at the gold bump-pad interface. Aluminum was chosen as the seed layer to create the bonding of stud bumps to the substrate. If copper seed layer was used, perfect bondability between stud bumps and die surface would be difficult to achieve due to oxidation in the copper seed layer in the ambient temperature. A semi-quantitative analysis method, Energy-dispersive X-ray spectroscopy (EDS), was used to map the atomic diffusion of Aluminum to the gold bump after 50 hours of exposure in thermal loading environment.

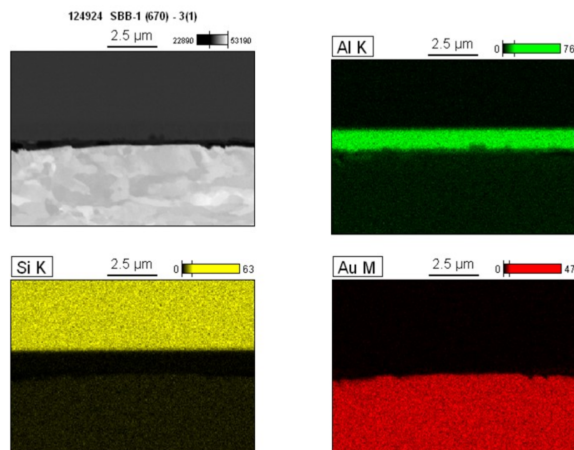

Figure 77 Elemental Mapping of bumped dice

The elemental mapping formed using EDX analysis suggested that no thermal diffusion occurred between adjacent sputtered metallic films (Figure 77).

3.3. Performance Analysis after Bend Test

The box-plots of the mean resistance measurements (via-to-via) of the embedded die packages are shown in the Figure 78. For 350x350 µm embedded die package, the average resistance measurement of bare die, bumped die and SBB die package is 1.83, 2.59 and 1.49 Ω respectively. For 670x670 µm die packages, the average resistance measurement of bare die, bumped die and SBB die package is 2.87, 3.06 and 1.90 Ω respectively. For the 1000x1000 µm die packages, the average resistance measurement of bare die, bumped die and SBB die package is 2.19, 3.36 and 2.00 Ω respectively. The average resistance values for different package types were analyzed statistically using one-way ANOVA which suggested significant difference because the p-value was zero. The Tukey test pair-wise comparison with 95% confidence interval revealed that all the mean resistance values were different. The individual confidence level turned out to be 98.09%. The performance measurement of the die packages suggests that SBB package shows the best performance, as shown in the Figure 79.

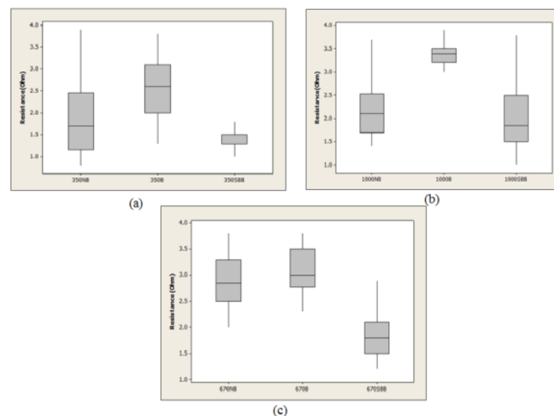

Figure 78 Box-plot of via-to-via resistance measurement of (a) 350x350 µm (b) 670x670 µm (c) 1000x1000 µm die package

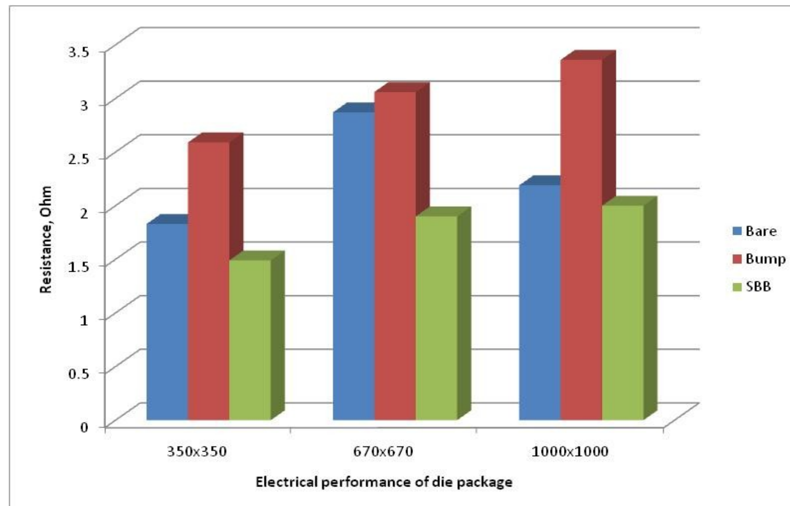

Figure 79 The performance comparison of the three embedded package types after bend test

External mechanical stress is extremely important for ultra-thin chips as they are used in flexible systems. The mechanical deformation effect on embedded dice and silver micron-sized paste filled trenches warrants detail investigation. When subjected to mechanical bending, the embedded packages undergo stress effect which results in important consequences; the electrical property of the system may change drastically due to crack propagation. There is a possibility to use the change to utilize in sensor applications. Due to small size and thickness, the embedded package should be measured with great caution. Embedding the chips inside the test package allow bending the chips without breaking them. A unique phenomenon was observed while the bend test was performed. The continuity of the packages improved after the bend test. The conductive trenches were PTFI-ed with silver micron-sized paste and cured to make them conducive. The mechanical bending actually helped to increase the contact area between silver particles and improved the conductivity, as shown in Figure 80. . This phenomenon can be attributed to the increment of the contacts between the largely spherical particles in the paste when subjected to local normal and tangential forces during bending. This mechanism, modeled by Lo and Tsai [265], is referred to as 'Junction growth'. Tabor [266] also presented an

explanation of the phenomenon. Junction growth can be explained by the requirement to maintain a constant von Mises stress at the contact points. Under a normal pre-load, the plastically yielded contact area increases with tangential loading to reduce mean contact pressure and contain shear stresses. According to Lo and Tsai [265], the condition for plastic flow at the contact is given by, $\rho^2 + \alpha\tau^2 = \alpha\kappa^2$; where ρ is the normal stress, τ is the shear stress, κ is the material flow strength in shear, and α is the junction growth coefficient. The junction growth coefficient increases with the increase of mean pressure, hence the spherical contact also increases. Under the effect of normal load, the critical value of normal stress falls below the mean pressure value required for a plastic flow due to shear stress. Under a constant normal load, the area of interface enlarges to maintain plasticity. The junction growth effect eventually leads to a lower resistance of the conductive paste.

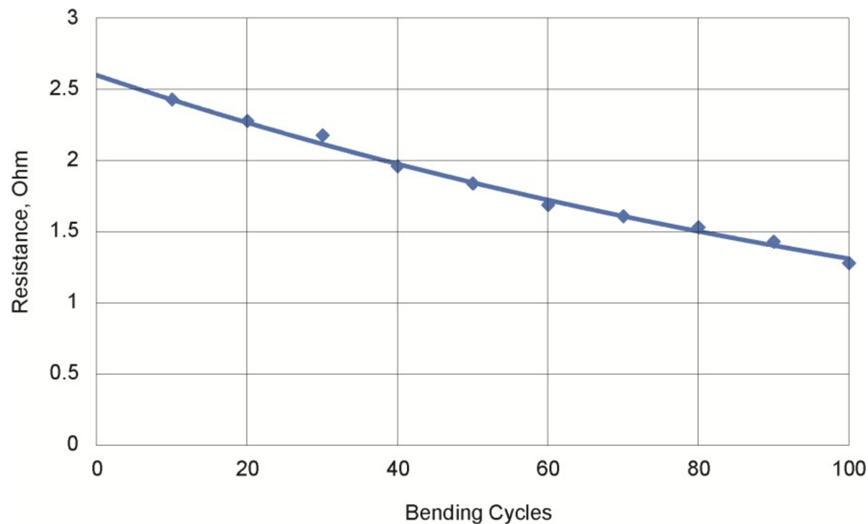

Figure 80 Resistance vs. bending cycle for a 350x350 µm SBB die package

After analyzing the electrical performance results of all packages, it was concluded that SBB package performed best. The stud bumps are resistant to oxidation due to unique material property of gold. The shape of the studs also helps to improve performance. The gold bumps

make an excellent connection with the Al seed layer and the tail, being 25 μm in diameter, helps the unobstructed flow of the silver micron-sized paste. The shape of the stud bumps prevents the package from delamination at the paste-bump interface. The contact surface of the stud bumps is larger than the bare die and electroplated bump package. The stud bump technology also offers reduced interconnect length, power consumption, inductance and signal loss. The stud bumps reduced the effect of strain, being located at the neutral plane of the package. If the location of the bumps is far away from the centroid of the package, the strain will be higher and the useful life will be shorter. The height of the bump is also very important as there is a quadratic relation exists between the bump height and fatigue endurance [267]. The current carrying capacity of the gold bumps is higher than solder alloys. The thermal conductivity is also better, hence providing better heat transfer [223]. The pad size also influences the electrical connection. In these packages, the seed layer was used as bonding pads which maximized the contact surface.

In case of electroplated bumps, the profile of the plated bumps and via created the obstruction for the free flow of silver micron-sized paste. The performance will be improved, if bumps with lower diameter can be plated. Still, the contact surface of the plated bumps is lower than that of stud bumps. The plated bumps were made of copper, which easily gets oxidized in the ambient temperature. The SEMs suggested delamination of paste along the bump profile. The lack of delamination in case of stud bumps is due to the better adhesion between gold and silver paste as opposed to oxidized copper and silver paste.

The sharp tail always ensured the good contact with the silver paste. For the bare die package, the delamination of the paste with the copper seed layer and oxidation of copper is considered responsible for the poor performance. The silver pastes suffered shrinkage and delamination was noticed at the contact surface of the ink and via walls.

CHAPTER 4. CONCLUSION

In this study, a novel embedding process of ultra-thin (below 50 µm) bumped die in the flexible LCP substrate was fully developed by optimization and integration of ultra-thin die preparation, die metallization, substrate preparation and assembly processes. In order to assess the reliability performance, embedded die packages were designed and assembled without any underfill and hereby established the cost effectiveness of the novel process. The reliability study revealed the importance of stud bumping the die to achieve better electrical performance. The better adhesion between gold studs and silver pastes and excellent bonding of the stud bumps to the seed layer played the major role behind better performance of the stud bumped packages.

A plasma-etch process was developed for thinning and dicing thinned Si wafers as a viable alternative to diamond saw dicing. The optimized process is capable of dicing thin Si wafers (25 µm) with high quality. Externally procured standard thickness wafer was thinned and singulated using DRIE and laser dicing. For the sputtered dice, singulation by DRIE method was developed in order to produce crack-free ultra-thin silicon tiles. As the blade dicing is not very suitable for the ultra-thin wafers due to warpage and use of coolants, singulation of plasma etching of silicon proved the advantage of the process. This process can successfully be applied in the microelectronic industry to singulated crack-free ultra-thin dice.

In order to avoid the die cracking while transferring and to increase the productivity, contactless thermo-mechanical selective laser assisted die transfer process (tmSLADT) was developed. Transferring the electronic components by blister formation using Nd:YVO_4 laser was demonstrated and successfully applied to fabricate flexible RFID tags. In some of the first experiments tens of dies were transferred at nearly a 100% transfer rate and with a very high precision.

A novel sensitizer was developed to increase the UV-absorption characteristics of off-the-shelf photopolymers that showed promising results for the fabrication of high density microstructures. The high resolution interconnects were fabricated using a low cost electroplating method that can be applied in flip chip wafer level assembly process. The optimized electroplating method resulted in uniform metallic bumps with excellent grain structures. These bumps, when formed on thinner ICs, can further improve the flexibility of the package. The stud bumping parameters were also optimized to create stud bumps on Al sputtered bare silicon. Wire bonding proved capable of fabricating up to 50 μm long Au studs. The concept of using the top surface of the die as a continuous pad helped to establish a continuously conductive path and improved the electrical performance.

CHAPTER 5. FUTURE WORK

The reliability performance of the electronic package is determined by running the thermal accelerating test for 1000 hours according to JEDEC standards. Once the thermal testing is completed, the failure modes need to be identified by analyzing the failed components. The failure model corresponding to the failure modes need to be developed to comprehend the failure mechanism and predict the fatigue life of the package. An optimization model to determine the optimum thickness of the silicon die is needed to be developed. The model to investigate the mechanical bending effect of silicon die on the electrical performance of the embedded package is also necessary and warrants special attention. Finite element analysis method can be utilized to predict the failure and deformation model of the stud bumps as a future work.

The contactless laser transfer process was developed and demonstrated, but was not integrated in fabricating the test packages. This method need to be incorporated in the fabrication process of the embedded packages. The die attach materials was not applied to fabricate the packages. The SEMs taken while investigating the failure modes suggests that die attach materials should be used to maintain the precision of the assembly. The PTFI process was completed manually which left a room for non-uniform filling of the conductive trenches. The automation of the PTFI process using screen printing method may solve the problem and should be pursued. The lamination of the dice was accomplished using Kapton® tapes which created occasional entrapped voids in the final structures. The automatic vacuum lamination process may alleviate this problem for good.

The developed bumped packaging technology can be utilized in the fabrication of high density flexible RFID antennas have a wide range of application in military grade bio-degradable health sensor system, and consumer level tracking system. Green substrate application, moisture

reliability and alternate metallic deposition may be suggested as the future work for improving commercial performance and extend their application.

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