CMOS PHASE SHIFTER FOR CONFORMAL PHASED ARRAY BEAMFORMER APPLICATIONS

A Thesis
Submitted to the Graduate Faculty
of the
North Dakota State University
Of Agriculture and Applied Science

By
Alarka Sanyal

In Partial Fulfillment of the Requirements
for the Degree of
MASTER OF SCIENCE

Major Department:
Electrical and Computer Engineering

April 2015

Fargo, North Dakota

North Dakota State University
Graduate School

Title

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MASTER OF SCIENCE

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ABSTRACT

A vector modulator based phase shifter is developed using 0.18um CMOS process at S-band frequency to be integrated into a conformal phased array antenna to recover the desired radiation pattern in the entire 360° range. The phase shifter has a variable gain amplifier integrated into the circuit in order to vary gain along with phase for precise control to correct the degraded radiation pattern due to the conformal shaping. The results show state-of-the-art performances including more than 7dB conversion gain with variable feature, a continuous phase rotation of 360° with steps as low as 11.25° and very low power consumption of 17mW, for the first time to the best of the authors' knowledge. The chip size including all pads is 1.5mm X 0.75mm.

ACKNOWLEDGEMENTS

Firstly, I would like to thank my academic advisor, Dr. Debasis Dawn for his continuous support, patience and guidance in helping me complete my research work.

I would also like to thank Alfonso Mendoza Radal for his support and guidance while working on my research work.

ND NASA EPSCoR has supported this project under the agreement FAR0020852. I would like to thank Prof. Benjamin D. Braaten of North Dakota State University, Fargo, ND, Dr. Neil F. Chamberlain of NASA JPL, Dr. Michael T. Reich of Center for Nanoscale Science and Engineering (CNSE) of North Dakota State University, Fargo, ND and Prof. Dimitris E. Anagnostou of Department of Electrical and Computer Engineering, South Dakota School of Mines and Technology, Rapid City, SD for their support and collaboration.

I am very grateful to all my committee members, Dr Scott C. Smith, Dr Gursimran S. Walia and my advisor Dr Debasis Dawn for their patience and support.

I would also like to thank all my colleagues at NDSU for their kind help and support during the course of my Master's program. I am really grateful to all these people and deeply appreciate the support offered by them.

DEDICATION

I would like to dedicate this thesis to *Ma* and *Baba* for their unconditional love and support.

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1. INTRODUCTION

Phase shifters are critical components of any phased array antenna system [1] which are of particular interest for NASA in wireless communications involving space suits worn by astronauts and is found to be very popular because it allow the scanning of the antenna beam electronically. The phase shifters can be used to change the angle of radiation of transmitted and received waveform signals, thus avoiding bulky arrangements for mechanical rotation of the antenna system. To get a broadside radiation pattern in a microstrip antenna array, all the antenna elements must be fed with same voltage phase.

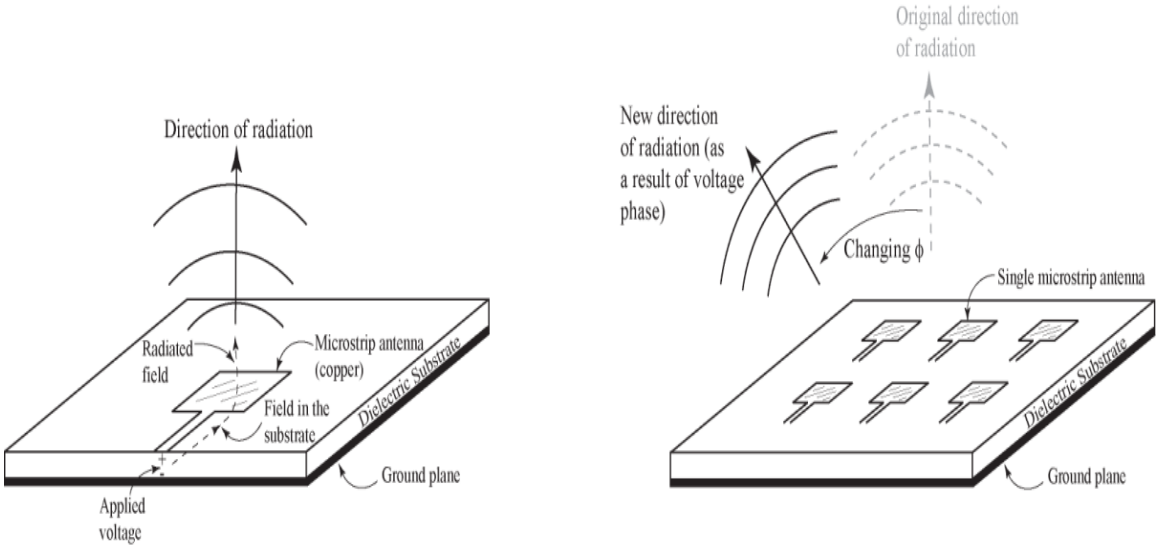

Figure 1: A single antenna element and an antenna array

However, when this antenna array is bent or placed on a conformal surface, the radiation pattern is changed from its broadside direction, and overall performances such as angle of radiation and gain are degraded. The amount of degradation depends upon the bending radius. In order to restore the original radiation pattern, appropriate phase compensation is required on each antenna array element [2]. The CMOS phase shifter described here can be integrated with a conformal phased array antenna to fully recover the radiation pattern through precise gain and phase control mechanism.

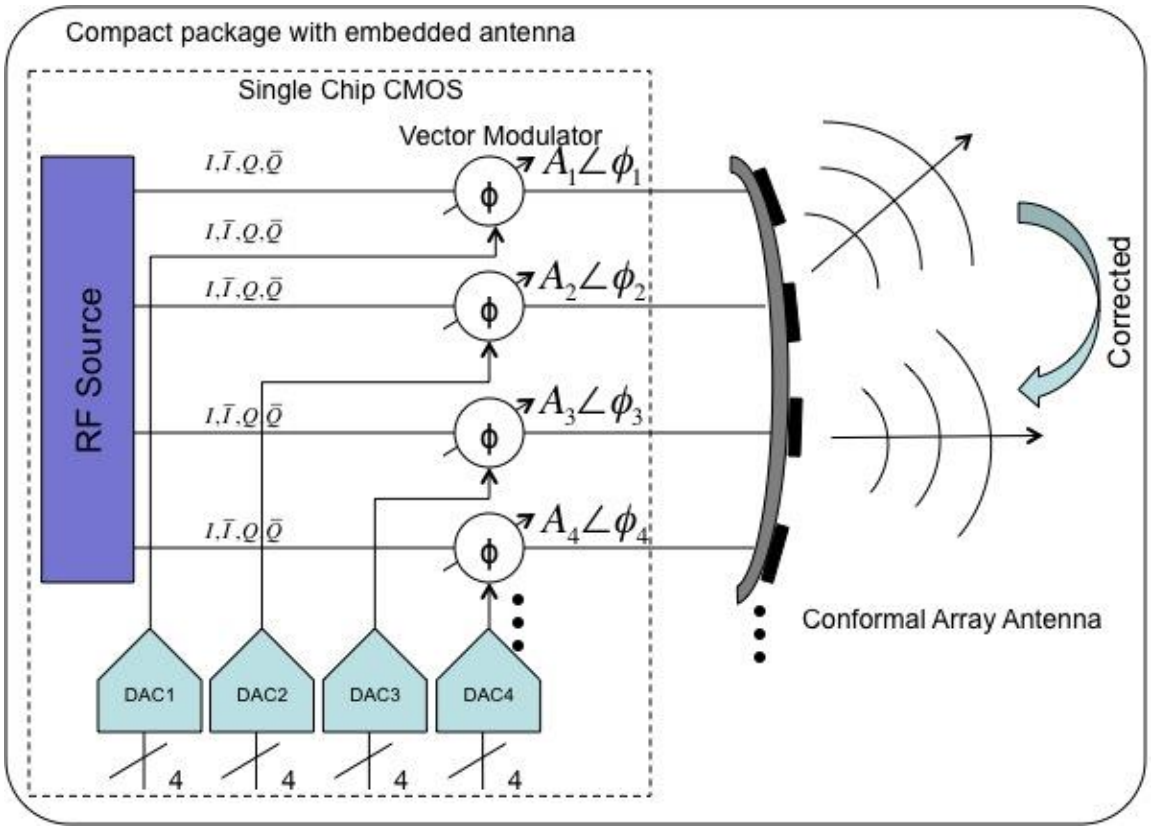

Figure 2: Integrated Beam Former with antenna array and phase shifters

Phase shifters can be classified into passive and active phase shifters [3], with the former having the disadvantage of signal attenuation, which can be overcome by using the active phase shifters [4]. Other way to classify the phase shifters is in analog and digital [5]; analog phase shifters provide continuous phase variation over a certain range and are controlled by a varying voltage. Digital phase shifters provide fixed phase steps that are selected using a binary coded input [5].

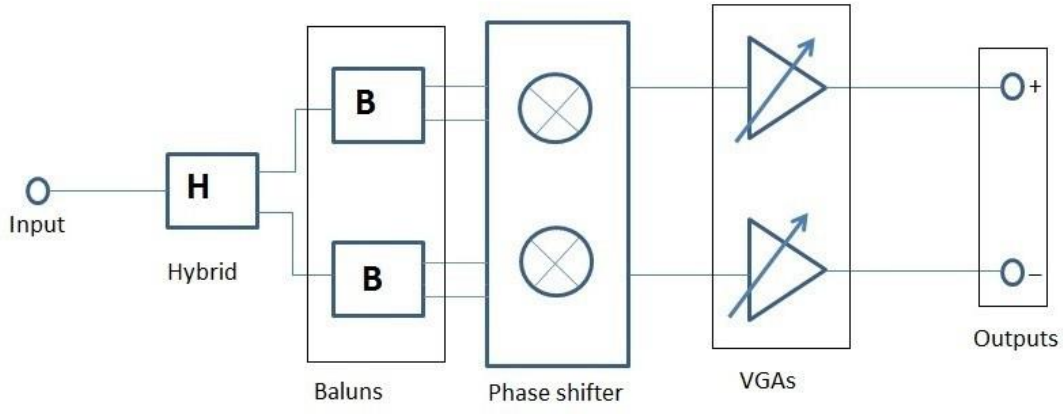

Figure 3: Integrated CMOS phase shifter with precise gain/phase control

For example, a 360^{o} digital phase shifter with 4 bits control can obtain discrete phase-shift steps of 22.5^{o}, whereas an analog phase shifter can produce a continuous phase-shift over the 360^{o} range. Phase shifters can be designed in different forms, namely switched line phase shifters [7], loaded-line phase shifters [8], and reflection-type phase shifters [9].

Due to the rapid scaling of the transistor lengths in the recent past, it has become possible to fully integrate large number of transistors with both analog and digital functionality into a single chip [6]. Especially CMOS RFIC (Radio Frequency Integrated Circuits) made possible towards

realization of system-on-chip (SOC) solutions where all analog and digital functionality can be integrated into a single process platform and analog radio can be controlled through digital circuitry with programs written on a computer. Smaller chip area also helps in energy consumption, as well as the cost reduction. The reduced power requirement opens the possibility for wide applications including portable electronics.

Here, we have proposed an integrated CMOS phase shifter, which can be operated at S-band frequency. The phase shifter consists of passive hybrid, active balun and a variable gain amplifier with buffer stages integrated into a single chip which can be integrated into a conformal phased array beamformer to achieve precise gain/phase control simultaneously. The phase shifter is designed in 0.18um CMOS process.

2. REVIEW OF LITERATURE

Phase shifters form a very important part of phased array systems [1]. Microwave phase shifters were previously implemented in III-V compound semiconductors for stringent performance requirements. With the current developments in fabrication technology, more and more monolithic microwave integrated circuits (MMICs) are now fabricated in CMOS technologies [16], [17], although the substrate losses and inferior Q-factors of the passive components still hinder the realization of CMOS phase shifters at microwave frequencies. To consider the hardware cost and system integration, it is desirable to implement high-performance microwave phase shifters using a standard CMOS process [15]. A change in the direction of transmission of an antenna array can be caused due to a various reasons. In order to compensate the change in direction or in to get the transmission of the radiating beam in a desired direction, a phase shift can be applied to the input signal of the antenna. This is where phase shifters come into play. The goal of designing a good phase shifter is to have a low insertion loss and also a gain in the output amplitude.

There are different architectures for implementing phase shifters such as reflection-type phase shifters [14], switched-line phase shifters [7], loaded-line phase shifters [8] and vector sum based phase shifters [11]. The phase shifters are chosen based on performance specifications like phase and amplitude imbalance, insertion loss, area, power, etc.

Shunt and series transmission lines together with reactive elements like varactors or diodes are used to design Passive phase shifters. The major advantages of this type of phase shifters are the simplicity of implementation and zero DC power consumption [3]. The major disadvantages

are higher insertion loss and obtaining more than 180° phase shift at mm-wave frequency using the low quality passive phase shifters of standard digital CMOS processes. One of these disadvantages of obtaining a phase shift over 180° is achieved by designing Active phase shifters which can obtain phase shifts over the entire 360° range. Active phase shifters consist of a quadrature generator along with a weighed I/Q summer called Vector Modulator (VM) and since the output is obtained by the addition of the quadrature signals, any arbitrary phase shift over the entire range of 360° can be obtained [3].

[18] implemented a distributed phase shifter with diode-loaded transmission line, which is widely used due to its low power consumption and low insertion loss, although the biggest drawback for this architecture is the considerably large chip area, especially for applications below 10 GHz frequency. To overcome this drawback of large circuit size, [13] implemented an ultra-compact phase shifter by using spiral inductors to replace the required transmission line sections, although it had its own set of drawbacks as it suffered from higher insertion loss and limited phase shift range.

The reflection-type phase shifter (RTPS), utilizing a 3-dB hybrid coupler and a pair of reflective termination circuits with impedance transformers is also widely used for its wide-band performance [14], [19]-[21], although the bulk silicon processes, the low inductor/varactor *Q* values and the limited varactor capacitance range produce high losses and small phase control ranges [22]. Another way of obtaining a broad-band phase shifter is by switching between a low-pass filter and a high-pass filter, which is called a switching-type phase shifter (STPSs). The low resistivity substrate and large on-state resistance in CMOS process will degrade the performance of the switching-type phase shifters [23]. The two types of phase shifters, RTPS and STPS can be cascaded for multibit operation, which increases their insertion losses and phase errors [19].

Compared to this, active phase shifters using vector sum method can provide continuous phase shift or multibit operation with low loss or gain [24]-[30].

[31] implements two K-band monolithic phase shifters, the Cartesian phase shifter and the hybrid polar phase shifter. The Cartesian phase shifter can achieve a 360° phase shift by using the vector sum of four orthogonal signals of which amplitudes can be varied over a wide dynamic range. It has a chip size of 0.95mm X 0.76mm, which was achieved by reducing the number of couplers and delay lines. It has a continuous phase shift and an insertion loss of 8 dB with a 37-dB dynamic range between 15-20 Ghz. The hybrid polar phase shifter on the other hand separates the input signal into two paths of which one can be placed anywhere in the first quadrant and the other one can cover the whole third quadrant, combining which, again a continuous phase shift can be achieved. It has an insertion loss of 16.2 dB with a 38.8-dB dynamic range from 15-20 GHz. The main drawbacks of these phase shifters are they have losses instead of gain in amplitude, limited output power and degraded noise figure due to the insertion loss and nonlinearity.

SiGe BiCMOS technology at 65-nm node and beyond is also ideally suited for highly integrated and low-power W-band phased arrays which helps in new system architectures based on electronic beam-forming and beam-steering [32]. These help in increased range, resolution and zooming functions for applications such as automotive and industrial sensors, active and passive imaging. [32] describes 70-77 GHz and 80-94 GHz phase shifters with 3-dB bandwidths. The phase shifters use the phase interpolation architecture consisting of a 90° hybrid which separates out the input signal into two equal-amplitude paths in quadrature and a phase rotator. The 77 GHz phase shifter uses BiCMOS technology whereas the 94 GHz phase shifter uses CMOS technology. Both the designs have VGAs, which are obtained by telescopic-cascode Gilbert cells and current

summer implemented as a differential-to-single-ended balun. The gain, isolation and bandwidth are maximized by applying the mm-wave signal at the gates of the common-source devices.

Even though the different distributed types of phase shifters like switched transmission lines [33]-[35], 90°-hybrid coupled lines [36]-[38], and periodic loaded lines [39]-[41] can achieve true time delay along the line sections, their physical sizes make them impractical for integration with multiple arrays in a commercial IC process, especially below K-band frequencies. The physical dimensions of phase shifters are reduced by the migrations from distributed networks to lumped-element configurations, such as synthetic transmission lines with varactors tuning [42]-[44], lumped hybrid-couplers with reflection loads [12], [22], [45] and the combined topologies of lumped low-pass filters and high-pass filters [46]-[48]. However, for fine phase quantization levels over wide operation bandwidth, the size of the lumped passive networks increases a lot, the main reason for which is the use of the various on-chip inductors, and is unsuitable for integrated phased array systems on a chip. Also, in most cases, there is a nonlinear relationship between the control signal (voltage or current) and output phase of the lumped passive phase shifters, which makes the design of the control circuits quite complex [49]. The passive phase shifters do not consume any DC power and still can achieve good linearity, but their large insertion loss requires an amplifier to compensate the loss, typically more than two stages at high frequencies (10 GHz), which offsets the major merits of good linearity and low power dissipation of the passive phase shifters. In comparison to the passive phase shifters, active phase shifters [50]–[51], [29], [31], [52]-[55] can achieve a high integration level with decent gain and accuracy along with a fine digital phase control with a required power budget where differential phases are obtained using transistors instead of passive networks. Different phase shifters like endless PS [50], a programmable PS [21], a Cartesian PS [31], or a phase rotator [52], the underlying principle for all cases is to interpolate

the phases of two orthogonal-phased input signals by adding the I/Q inputs for synthesizing the required phase. The different amplitudes between the I- and Q-inputs result in different phases. Thus, the basic function blocks of a typical active phase shifter are composed of an I/Q generation network, an analog adder, and control circuits which set the different amplitudes of I- and Q-inputs in the analog adder for the necessary phase bits [11].

A CMOS 4-bit active digital phase shifter is presented in [11] for X-, Ku-, and K-band frequencies. The phase shifters interpolate the phases of the quadrature input signals by adding two I/Q inputs. Excellent signal, precision, increased operating bandwidth and minimal loss are obtained by developing resonance-based differential quadrature networks.

3. THE PHASE SHIFTER

A double balanced Gilbert cell has been used for designing this phase shifter as shown in Figure 3 (block diagram) and in Figure 4 (circuit schematic). In the bottom part, we have the vector modulator circuit with the Variable Gain Amplifier (VGA) circuit in the center and the two buffer circuits on each side. Each small block of the vector modulator has two top transistors for passing the RF signal and a tail transistor at the bottom to pass the control voltages. The common gate and common source transistors connected in the cascade topology form each small block of the vector modulator. The control voltages applied at the bottom tail transistors of the vector modulator help in passing the RF signal, being fed to the top transistors, to the output of the vector modulator circuit, which is then passed on to the input of the VGA circuit. The VGA circuit also has a pair of top transistors, which are used as the input for the phase changed signals from the vector modulator circuit, and a tail transistor at the bottom to control the amplitude of the signal. By controlling and varying the control signal of the bottom transistor, we can vary the output amplitude of the RF signal. The output signal is then passed through the buffer circuits. The buffer circuits are meant for 50Ω output matching during measurements.

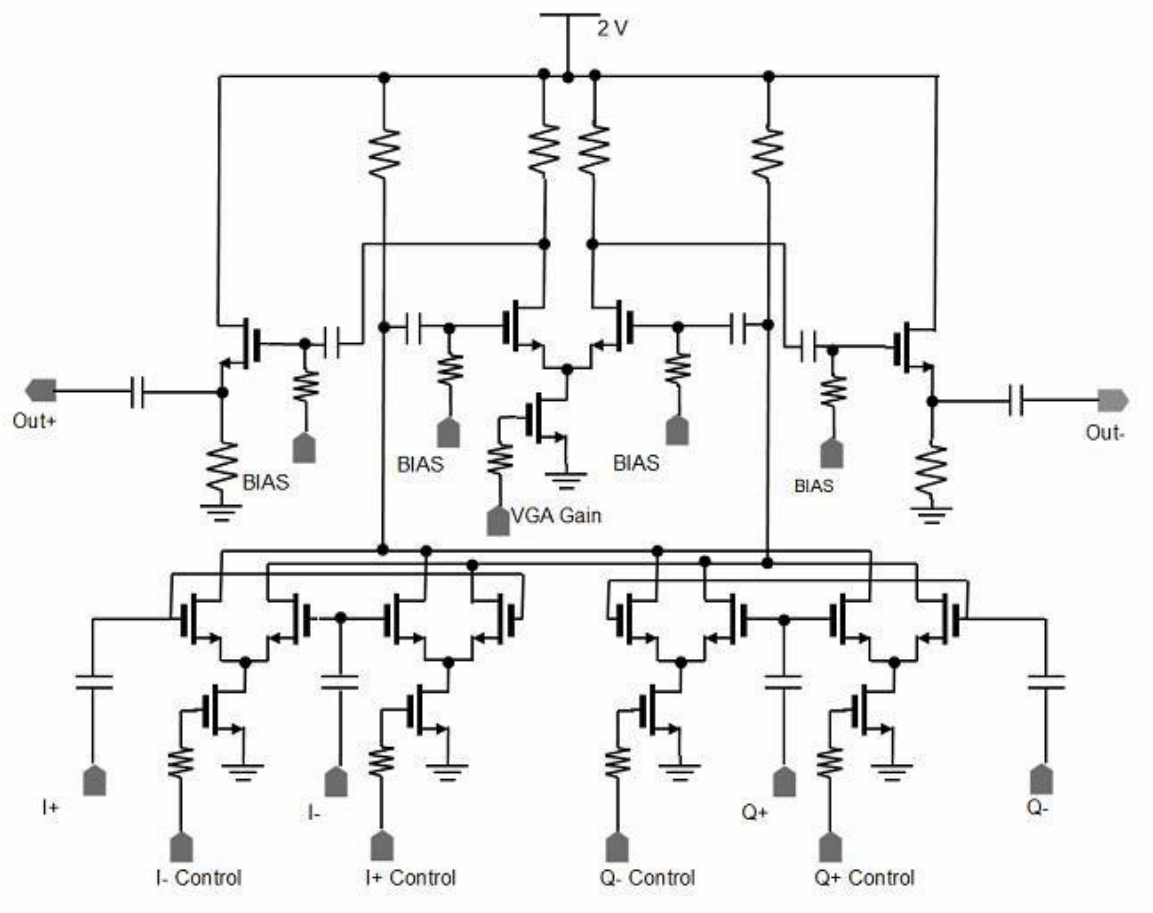

Figure 4: The circuit schematic of the Gilbert cell phase shifter integrated with the variable gain amplifier

This integrated phase shifter design is optimized through co-design method where each connecting block's input/output impedances are considered in the design, thus, maximizing the performance of the overall chip while minimizing power consumption. Figure 5 shows the principle of operation for the vector modulator based phase shifter.

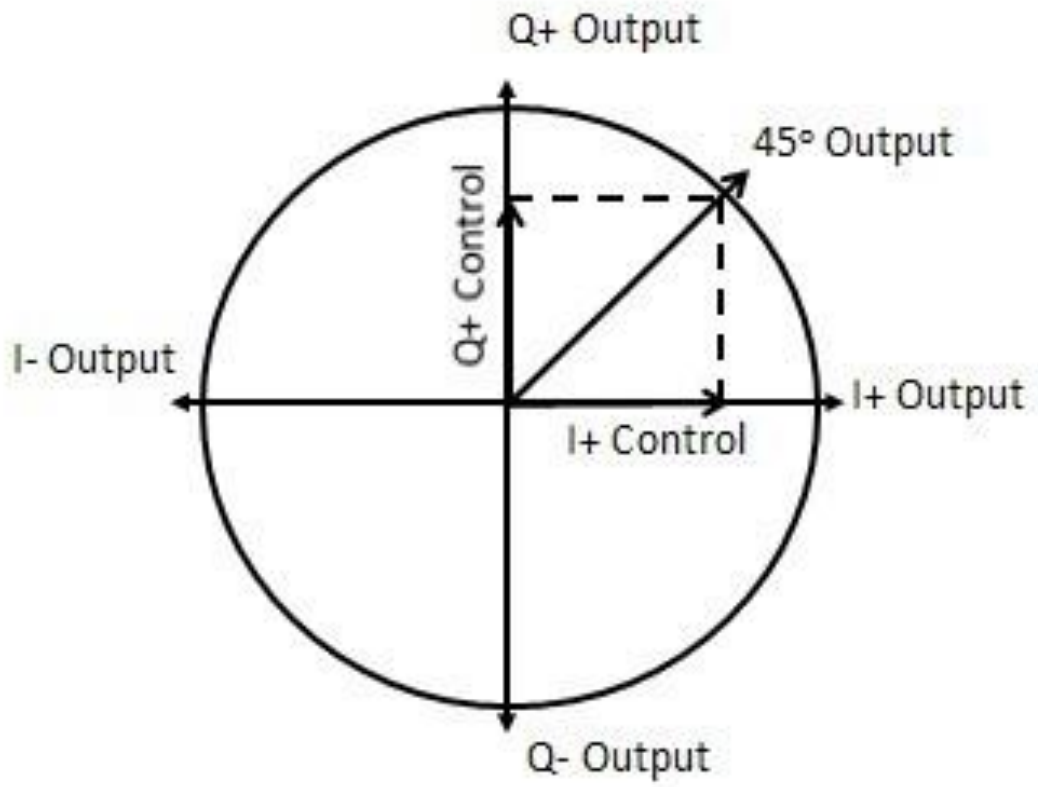

Figure 5: Phase control mechanism

Starting with 4 signals with phases of 0^o (I+), 90^o (Q+), 180^o (I-) and 270^o (Q-), the output signal with a specific phase is achieved by adding two of these input signals. By controlling the amplitude of each added signal, a continuous phase shift is possible. An on-chip passive hybrid (Figure 6) and an active balun circuitry (Figure 7) were included in the design to generate the required phases from the input RF signal.

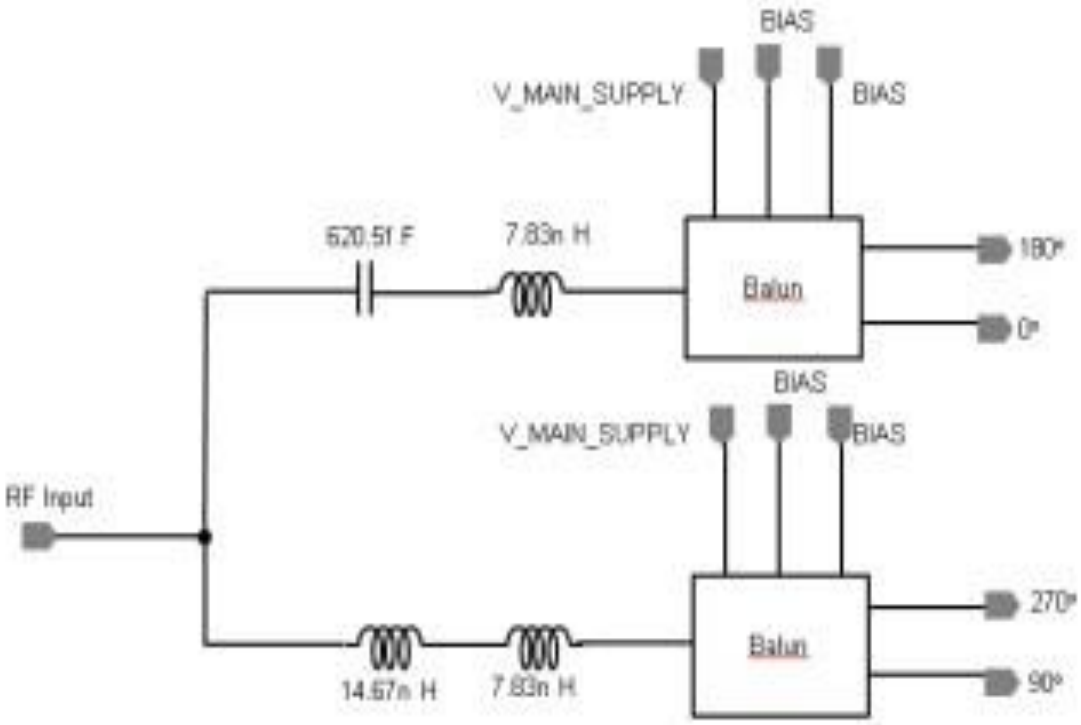

Figure 6: The circuit schematic of the passive hybrid

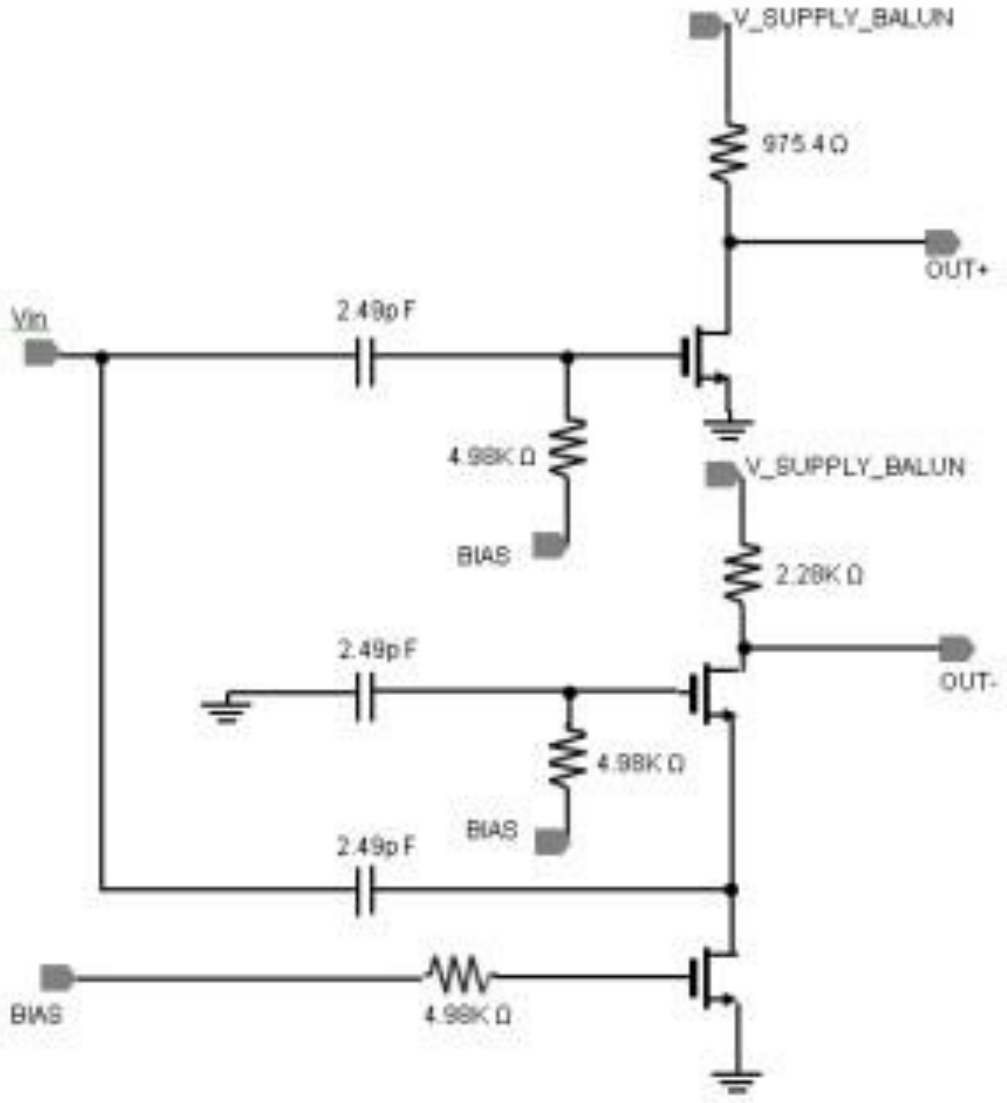

Figure 7: The circuit schematic of the active balun

The input RF signal is passed through a passive hybrid to produce I (in phase) and Q (quadrature) signals with a phase difference of 90^{o}. The inductors and capacitor of the hybrid circuit helps in achieving the two signals with the phase difference as mentioned. The hybrid being designed with passive elements produces a loss in the amplitude of the RF signal when passed through it. This I & Q signals are then fed to an active balun consisting of a common-

source/common-gate topology and cascade topology, producing differential signals from each input signal, thus producing four separate RF signals with 90^{o} phase difference between each. The active balun compensates the losses incurred in the passive hybrid and produces extra gain. The amplitude of the signals is adjusted by using the bias levels of the active balun. All four RF signals from the balun (I+, I-, Q+, Q-) are then fed to the double-balanced Gilbert cell vector modulator. The input signals are fed to the upper differential pair transistors of the vector modulator. The four controlling voltages are fed to the tail transistors in order to control the phases of the output signal. The control of the output phase is accomplished by applying the proper voltages to any two of the four controlling ports so that signals can be passed through any two of the small blocks of the vector modulator and we can do the vector sum of the passed signals to achieve the required phase shift in the output vector added signal. For example, in order to get a phase shift of 45^{o}, control voltage values must be given to the control ports I+ Control and Q+ Control, as shown in Figure 3. By varying all four-control voltage coefficients of these ports, any arbitrary phase shifts can be generated. The outputs of the Gilbert cell vector modulator are passed through a two stage VGA (Variable Gain Amplifier) in order to obtain an amplified output signal with variable gain capability. All the circuit blocks shown in Figure 3 are designed using the co-design methodology where input/output impedances are properly considered for RF matching ensuring the most efficient line-up performances with minimum chip size.

4. RESULTS AND PERFORMANCES

Simulation is carried out using CADENCE® Spectre® [10] simulator and layout is done using Virtuoso® tool. The input to the hybrid and the output buffers are matched to 50Ω. The performance summary of the phase shifter is shown in Table 1, which confirms state-of-the-art performances.

Table 1: Performance Summary

Technology	0.18um CMOS
Frequency	2 ~ 3 GHz
Phase Range	360^{o}
Gain	+7dB @ 2.2 GHz (variable)
Input Return Loss	< -25dB @ 2.2 GHz
Output Return Loss	< -11dB @ 2.2 GHz
Power Consumption	17.48mW
Chip Area	1.5mm X 0.75mm(with pads)

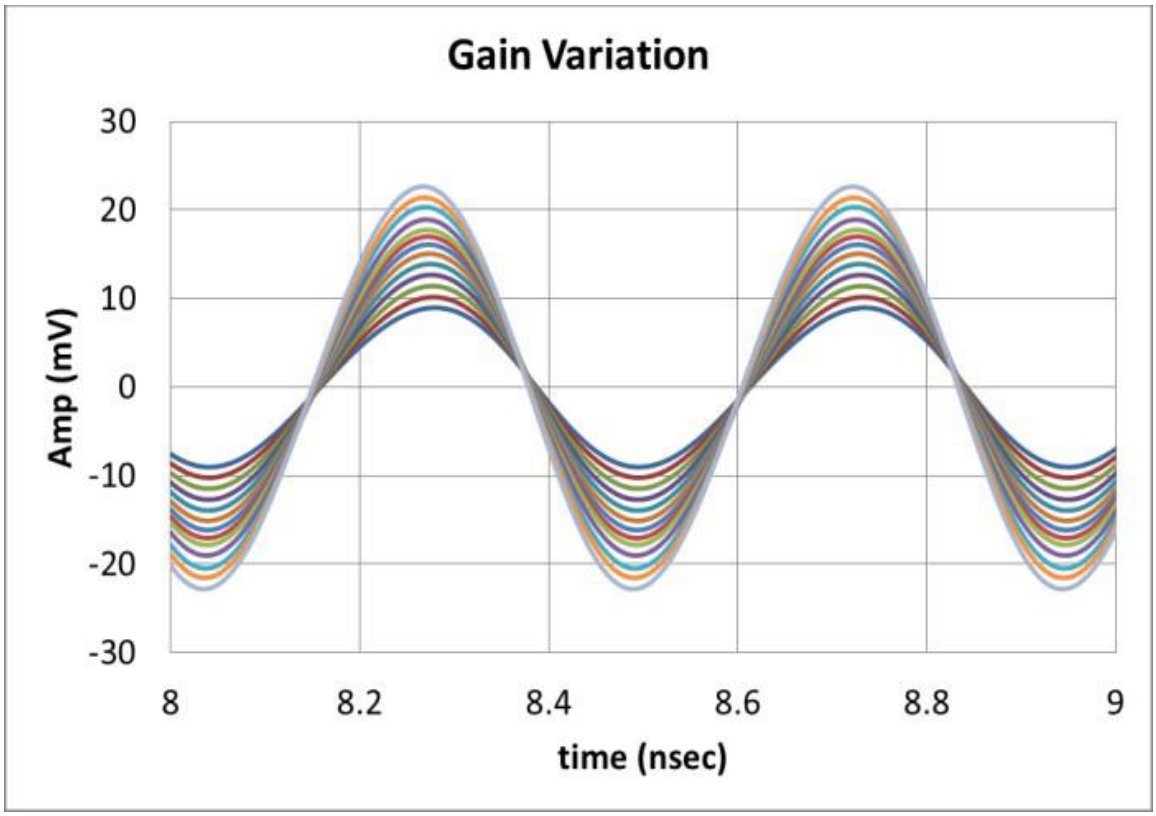

Figure 8: The gain variation of the circuit for single ended output with a particular phase setting

The circuit has been simulated with a 2.2GHz input RF signal at -30dBm (10mV peak) amplitude which gives a maximum amplified output signal of ~20mV peak for single ended output. We can also get the differential output from the two output ports from the two buffers of the circuit. From Figure 8, we can see that the circuit also produces ~ 40mV peak for differential output. The gain variation for single ended output has been shown in Figure 8, which also confirms the stability at the desired phase setting.

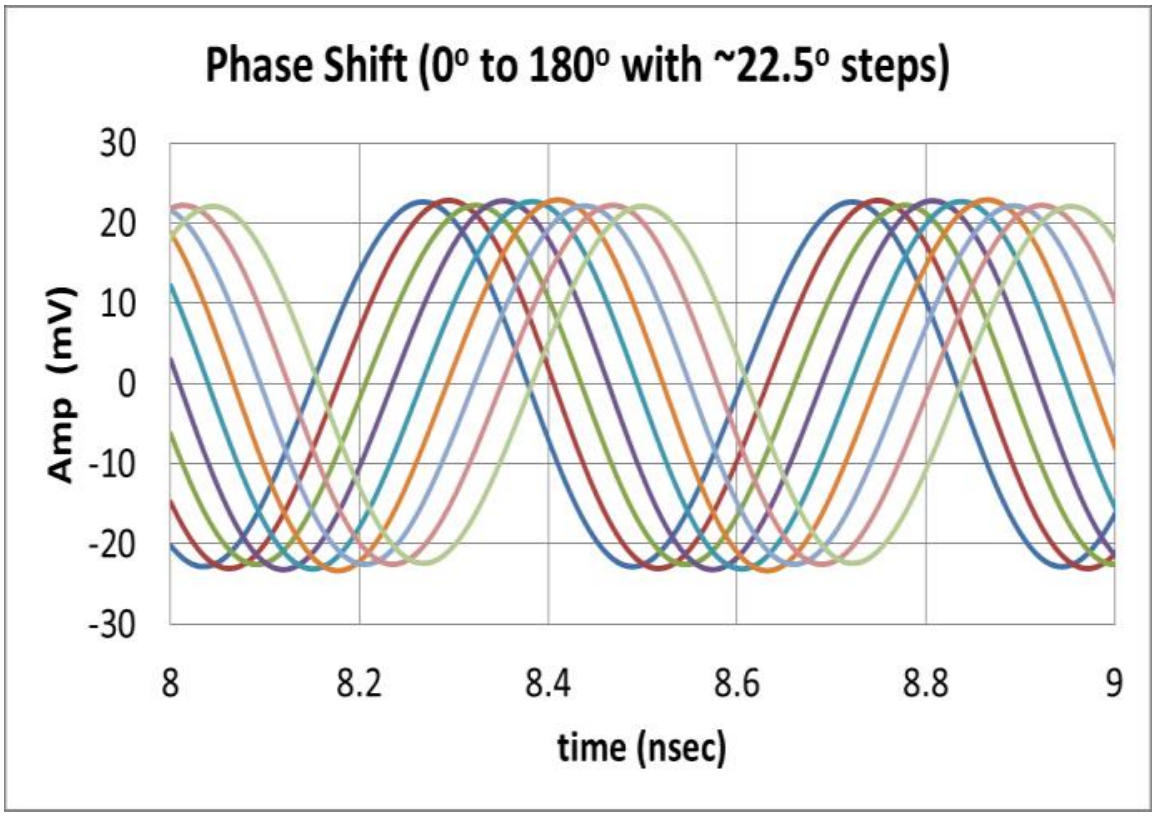

Figure 9: Phase shifting performance over 0° to 180° with 22.5° steps

Figure 9 shows the phase shift performance of the circuit from 0° to 180° with 22.5° steps while maintaining same amplitude. The phase shifter has the capability of continuously changing the phase in the 0° to 360° range, as shown in the frequency domain plot in Figure 10. Though this phase shifter can achieve any arbitrary value of phase shift, the 22.5° step is chosen to correlate the analog phase shifter performance through a digital bit control circuitry in terms of 2n relationship.

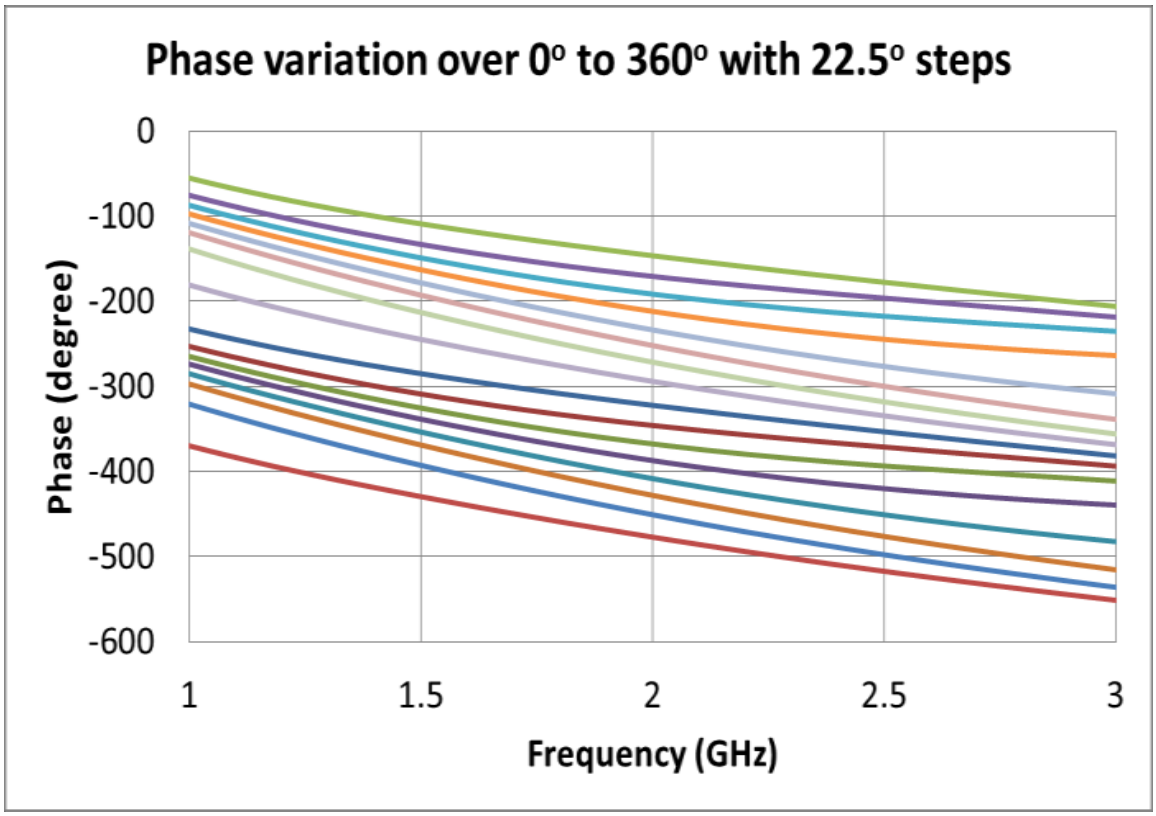

Figure 10: Frequency characteristics of phase variation in the entire 360° range

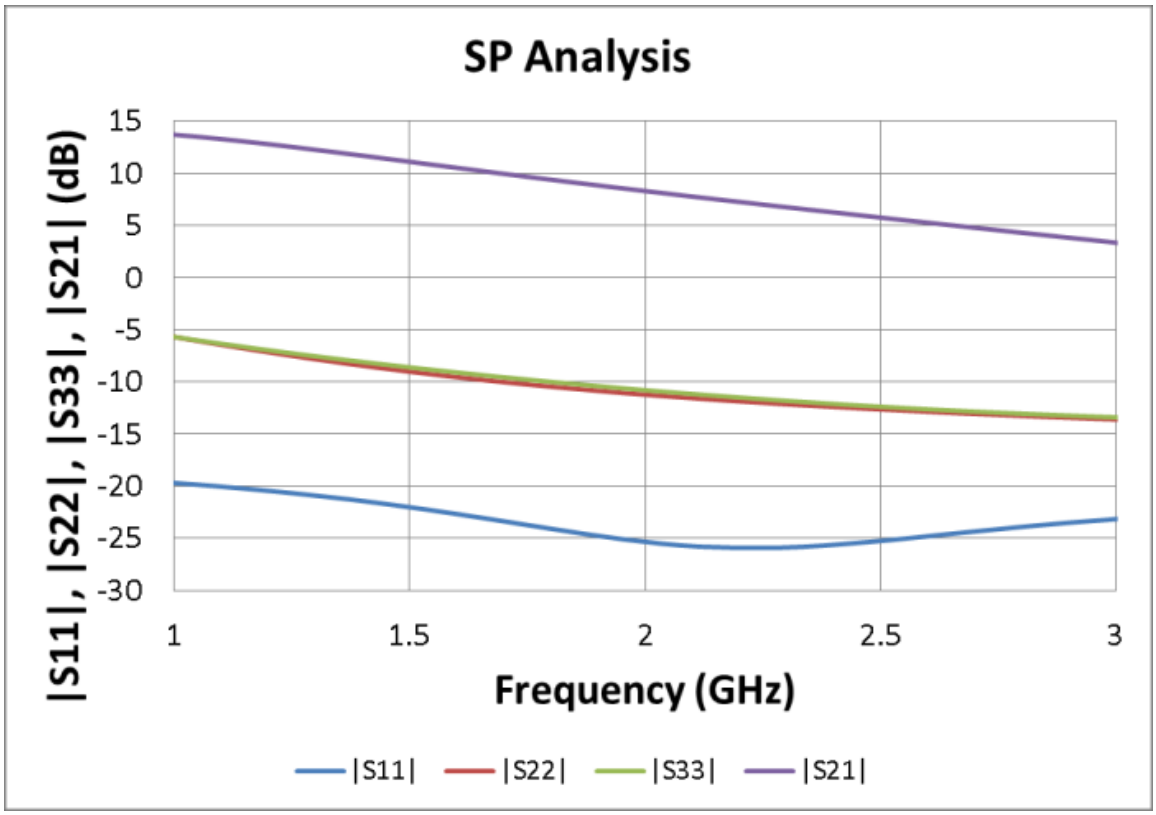

Figure 11: S-parameter analyses of conversion gain and return loss

The S-parameter simulation of the overall integrated phase shifter, with the input port (Port 1) in the passive hybrid and the two output ports (Port 2 and 3) in the two buffer circuits, is shown in Figure 11. We can see that the S-parameter analysis shows an input return loss (S11) better than -25dB, an output return loss (S22) better than -11dB in the 2~3GHz and conversion gain (S21) of 7dB achieved at 2.2GHz.

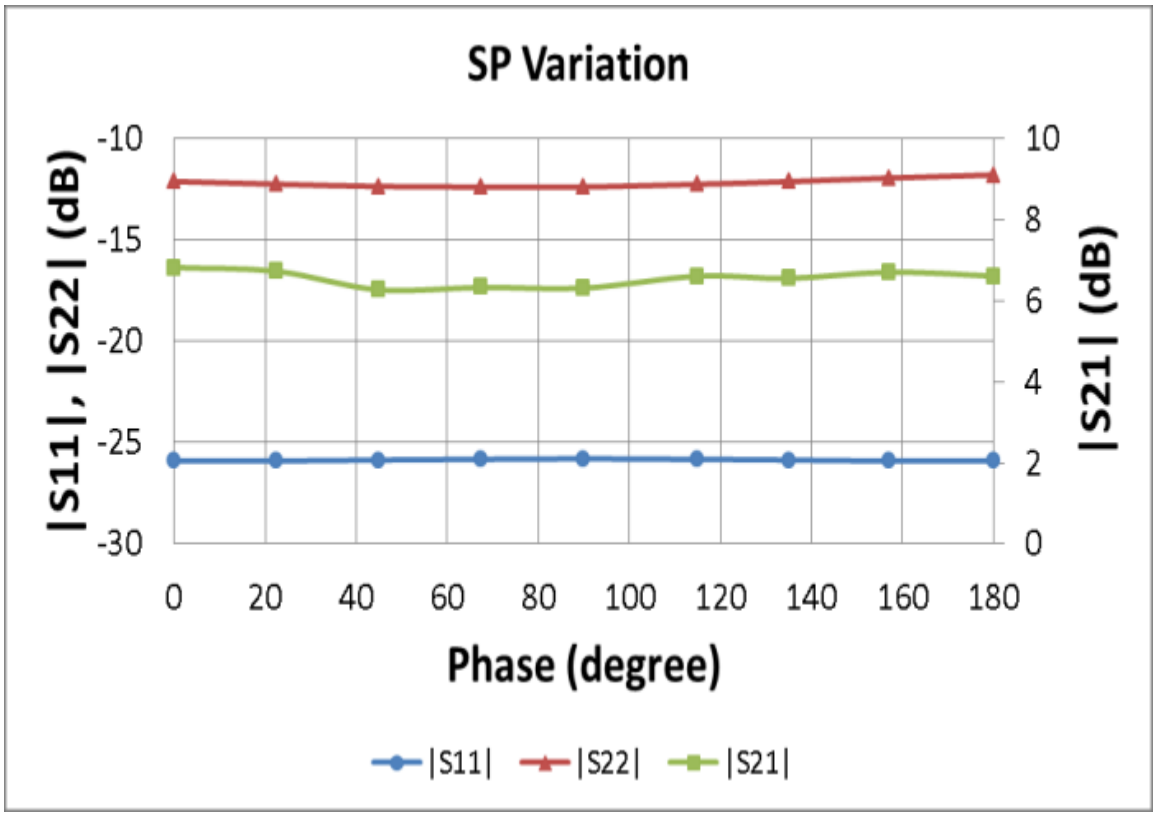

Figure 12: Stability of conversion gain and return loss over phase variation

Figure 12 shows very unique performances of this proposed CMOS integrated phase shifter where gain (S21) and input/output impedances (S11, S22) remain almost constant when phases are varied which is essential for simultaneous control of gain and phase variations without affecting each other. Large-signal performances are shown in Figure 13.

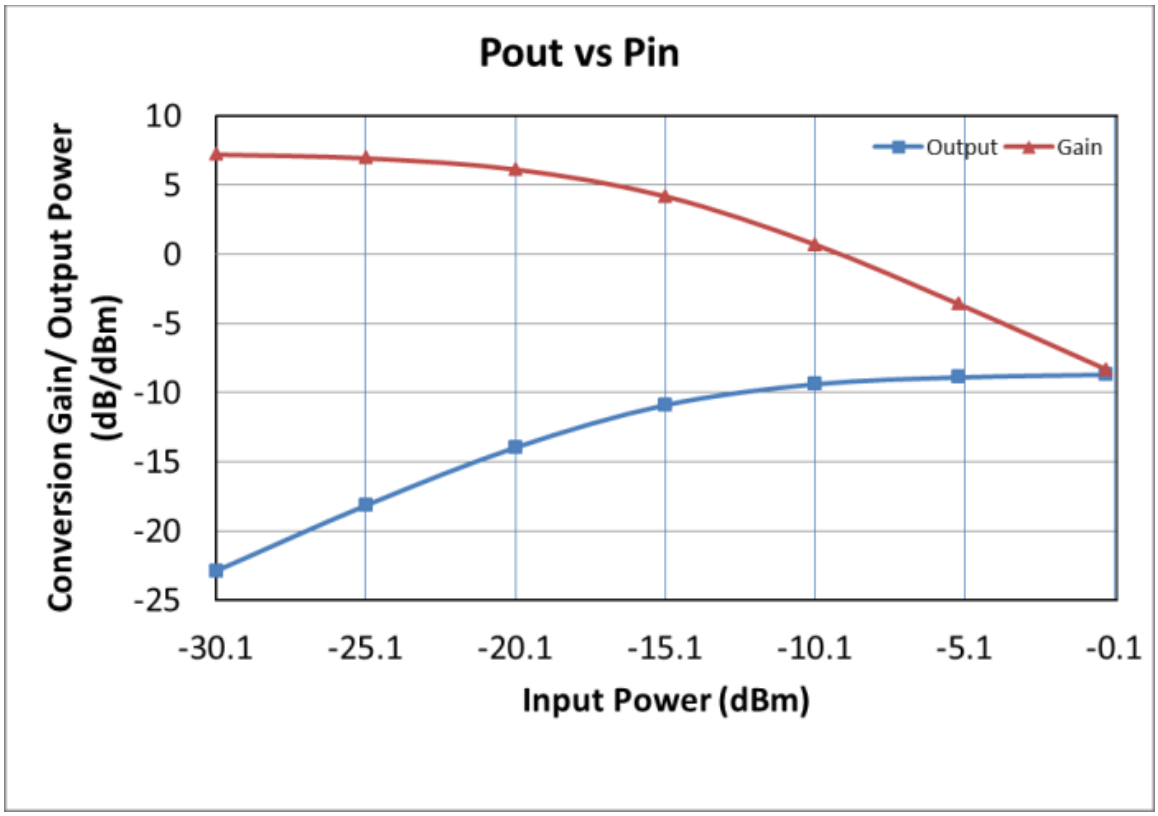

Figure 13: Large-signal performance showing compression of the integrated phase shifter

The 1-dB output compression power is found to be about -15dBm, which is sufficient for inclusion of this integrated phase shifter in the receiver circuitry and in the LO path of the transmitter circuitry. The layout of the integrated phase shifter with a size of 1.5mm X 0.75mm including all bond pads is shown in Figure 14. Table 2 shows the performance comparison of our work with other phase shifters using various process technologies.

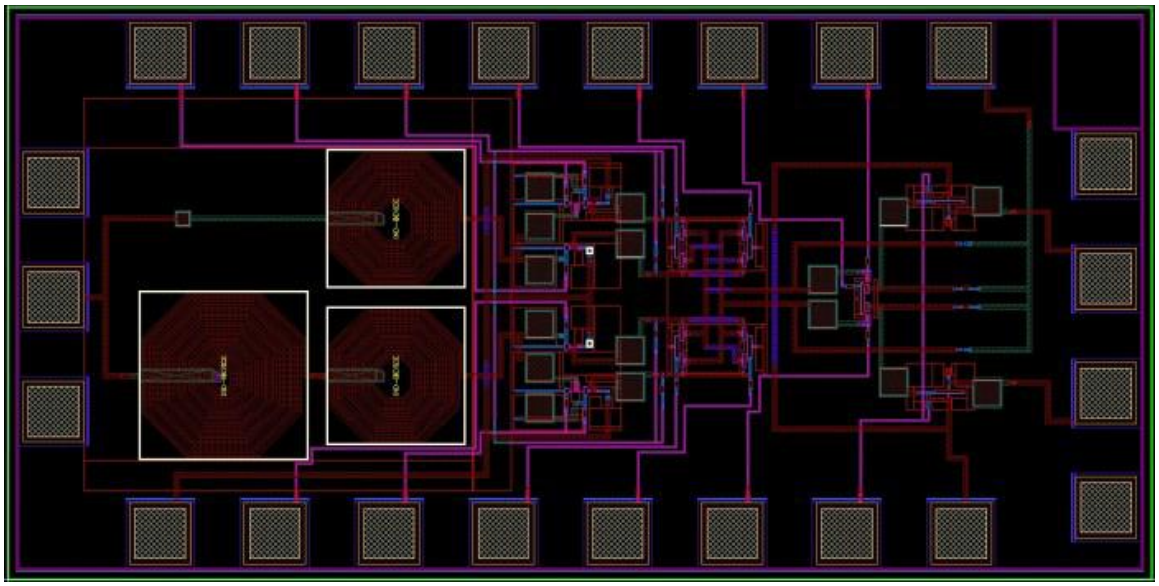

Figure 14: The layout of the phase shifter (1.5mm X 0.75mm)

Table 2: Performance Comparison

Ref	[7]	[11]	[12]	[13]	This work
Frequency (GHz)	11-15	15-26	5.15-5.7	4-6	1-3
Conversion Gain (dB)	-16.2	-3.8	-9	-2.2	+7.0 (variable)
Phase Range (^{o})	360	360	360	90	360
Area (mm^2)	4.34	0.15	0.9	0.5	1.125 (with pads)
Power (mW)	0	11.7	~0	~0	17.48
Process Technology	0.18um CMOS	.013um CMOS	0.6um GaAs MESFET	0.6um GaAs MESFET	0.18um CMOS

5. SUMMARY, CONTRIBUTIONS AND FUTURE WORK

5.1. Summary

A vector modulator based CMOS phase shifter has been designed using 0.18um CMOS process. This phase shifter is integrated with an on-chip passive hybrid and active balun and is capable of achieving both gain/phase controls. This has potential application in integrating into a conformal phased array beamformer for recovering the degraded radiation pattern due to conformal shaping through simultaneous precise control of gain and phase. The results show state-of-the-art performances including conversion gain of 7dB with variable feature for the first time to the best of author's knowledge. The simulation results, especially the plot of SP variation over the phase shift range over 360^o show that the gain (S21) and input and output impedances (S11, S22) remain fairly constant when there is a variation in phase which is essential for simultaneous control of gain and phase variations without affecting each other, within the range of 2-4GHz. The circuit can produce a continuous phase rotation of 360^o with steps as low as 11.25^o with total power consumption as low as 17mW.

5.2. Contributions

I proposed an integrated phase shifter architecture which is capable of controlling both phase and gain of the output signal. These two parameters are necessary to precisely restore the degraded radiation pattern of the conformal antenna array when it is being placed on a curved surface. The proposed architecture can keep constant phase when gain varies and keep constant

gain when phase varies. This is essential so that both parameters can be used to correct the radiation pattern without being dependent on each other. In order to minimize power consumption, this integrated phase shifter is designed with co-design methodology where complex input/output impedances of each individual block is considered instead of standard 50Ω termination.

5.3. Suggestions for Future Work

The next steps of this project would be to characterize the fabricated chip and do the measurements. Once these are done, then an array of phase shifters can be realized. As part of our future endeavors, we intend to design the next step of phase shifters which can be used in closed loop circuits, receive a feedback from the output of the antenna and decide how much phase changed RF signal should be fed to the antenna as input signal in order to get the desired direction of the radiating beam of the antenna and also work on enhancing the output signal amplitude.

PUBLICATIONS RESULTING FROM THIS WORK

[1] Alarka Sanyal, Alfonso Mendoza-Radal, Bilal Ijaz and Debasis Dawn, "CMOS Phase Shifter for Conformal Phased Array Beamformer Applications," presented at WiSEE 2013 IEEE International Conference.

[2] Bilal Ijaz, Alarka Sanyal, Alfonso Mendoza-Radal, Sayan Roy, Irfan Ullah, Michael T. Reich, Debasis Dawn and Benjamin D. Braaten, "Gain Limits of Phase Compensated Conformal Antenna Arrays on Non-Conducting Spherical Surfaces using the Projection Method," presented at WiSEE 2013 IEEE International Conference.

[3] Alarka Sanyal, Alfonso Mendoza-Radal and Debasis Dawn, "CMOS Integrated Beamformer with Conformal Phased Array Antenna for Wireless Communications," poster presentation at IMAPS/NDSU Microelectronics Technology Summit, 2013.

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