A VARIABLE HIGH GAIN AND HIGH DYNAMIC RANGE CMOS PHASE SHIFTER FOR PHASED ARRAY ANTENNA APPLICATIONS

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The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

MASTER OF SCIENCE

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ABSTRACT

Phase shifters can adjust phases electronically and hence is very popular for phased array antenna applications where radiation angle can be scanned electronically avoiding bulky mechanical rotation arrangement. In this research a variable gain phase shifter was investigated, capable of controlling precisely both phase and gain simultaneously. The phase shifter was fabricated using 0.18um CMOS process and the measured results showed continuous phase shift of 303^0 with 9-dB variable gain at 3.5 GHz. Based on the measured results, a modified phase shifter was proposed and designed which can achieve continuous phase rotation of 360^0 with small 22.5^0 steps, a low RMS phase error of 2^0 providing high resolution, a very high conversion gain of 14.2 dB with dynamic gain control range of 20 dB. These performances will create a potential future for smart communication radar applications where both beamforming and nulling can be achieved.

ACKNOWLEDGEMENTS

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DEDICATION

To *Maa* and *Baba*.

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1. INTRODUCTION

1.1. Background

A conformal surface changes its curvature with time and can be planar or non-planar. When an antenna system lies on a planar conformal surface, the field pattern of the antenna behaves normally. However, the radiation pattern of an antenna array gets changed from its regular radiation direction, if it is formed on a non-planar or curved surface, which results in comprehensive performances degradation such as radiation angle and amplitude. These performance degradations depend upon the bending radius of the antenna array [1].

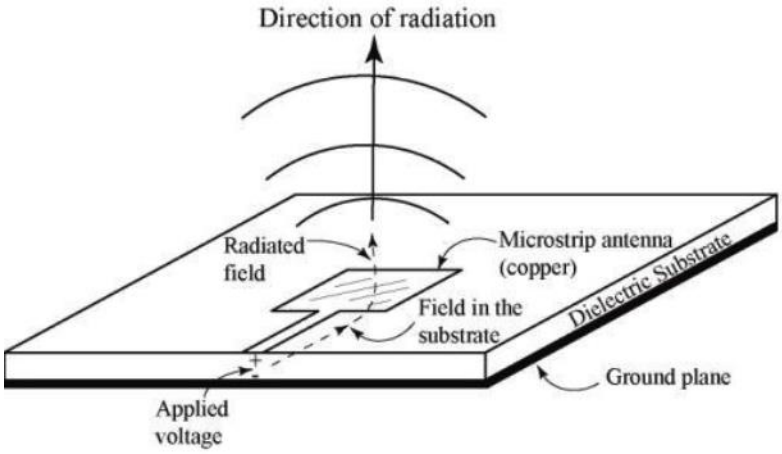

Fig. 1. A single antenna element.

Beam steering concept can be implemented to recover the field pattern of the antenna array by proper correction in relative phases between each antenna elements of the antenna array [2]. Thus, conformal phased array antenna systems have gained its popularity in wireless communications applications like aerospace designs, wearable antenna, spacesuit, mobile devices

etc. due to its capability of electronic beam steering and thus helping to avoid massive arrangement for involuntary rotation of the antenna system.

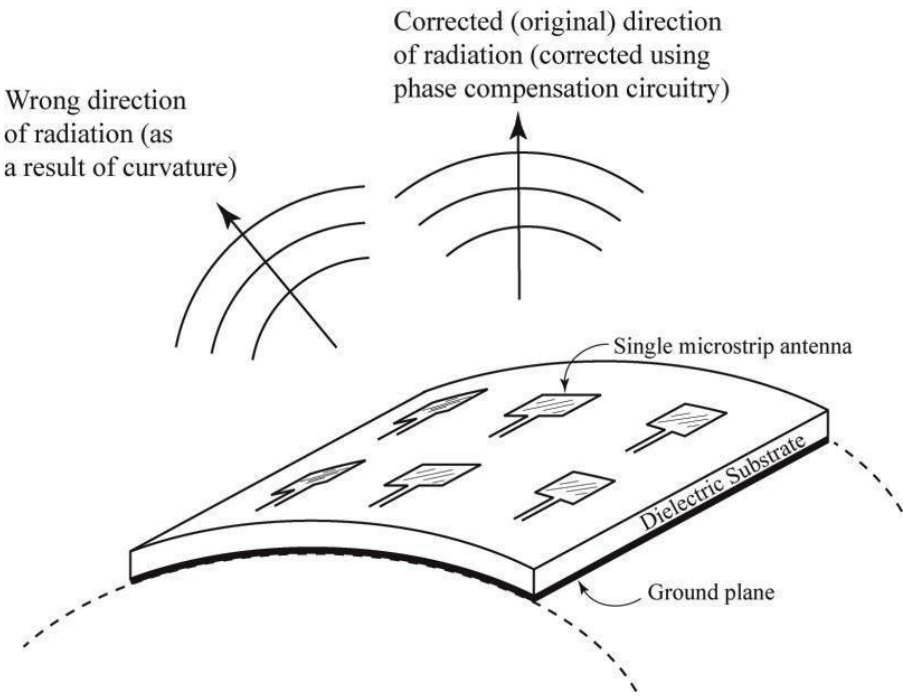

Fig. 2. An antenna array on a curved surface with direction of maximum radiation.

Phase shifter is an integral component of a phased-array system [3]. Proper phase restoration is needed on each element of antenna array to recover the indigenous pattern of antenna radiation. There are several classifications of phase shifters, like passive phase shifters, active phase shifters [4], analog and digital phase shifters [5], switched line phase shifters [6], loaded-line phase shifters [7] and reflection type phase shifters [8] among others. The passive phase shifter experiences signal attenuation, which can be recovered by active phase shifter. And, a continuous phase

rotation can be achieved by varying a control voltage in analog phase shifter, whereas using a binary coded input fixed phase states are achieved by a digitally controlled phase shifter.

In recent past years, silicon-based CMOS RFICs (Radio Frequency Integrated Circuits) has appeared to be an efficient and reasonable solution for phased array systems as a result of their potentiality of high integration density, yield and functionality on a single chip solution. As a result of accelerated scaling of the transistor lengths in the past, it is now practicable to accommodate sizable number of transistors in a single chip, which includes both analog and digital functionality [9]. Particularly CMOS RFIC made it feasible approaching system-on-chip (SOC) solutions, which helps to include analog and digital components into a single process platform and allows analog radio to be controlled through digital circuitry via the computer. Smaller chip size is a great way to reduce cost and power consumption. The low power criteria provide leverage for a range of applications such as portable electronics.

As phase shifter is an integral component of phased array systems, NASA has particular interest in the development of CMOS phase shifter for the phased array systems applications to tackle the radiation degradation problem of the antenna array when the array bends on a conformal surface. The frequency of interest is S-band, particularly 2~2.3 GHz, where transponders will be assigned frequencies for future human exploration missions for NASA. To handle this problem a variable gain CMOS phase shifter architecture has been proposed in [10] and [11], which can control both phase and gain of the phase shifter output. The phase shifter is a vector modulator based phase shifter, integrated with an on-chip passive hybrid, two active baluns and a variable gain amplifier (VGA). The simulated results of the phase shifter proved the validation of the concept and it gives the assurance that if the concept is implemented, the phase shifter can be embedded as smart electronics in phased array antenna systems.

1.2. Objectives

This research is targeting to develop a unit-cell variable high gain and high dynamic range CMOS phase shifter that will lead towards implementing digitally assisted single-chip arrays of phase shifter for phased array antenna applications as depicted in Fig. 3. In order to achieve this goal as a first step, the phase shifter architecture proposed and designed in [10] and [11] will be fabricated and characterized. After this, all measured results will be analyzed and based on the outcome, this research also aims to modify the phase shifter architecture to improve its overall performances including low power consumption in order to be more suitable in integrating multiple such phase shifters for phased array antenna applications.

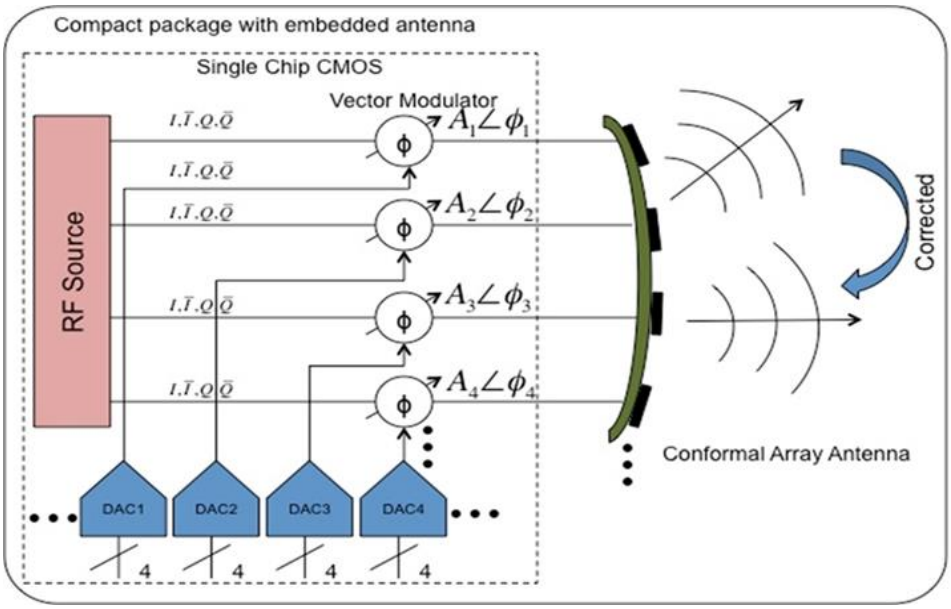

Fig. 3. CMOS integrated beamformer with conformal phased array antenna for wireless communications.

1.3. Organization

This thesis is organized with literature survey in section 2, the chip layout and fabrication in section 3 followed by characterization of the fabricated chip and discussions in section 4. Based on the measured results, a modified phase shifter is proposed and designed in section 5 and the simulation and results of the new proposed phase shifter are discussed in section 6 followed by summary, contributions and future work in section 7.

2. LITERATURE REVIEW

Previously, microwave phase shifter was realized with III-V compound semiconductors due to strict performance restrictions. Due to significant advancement in fabrication process and rapid technology scaling, monolithic microwave integrated circuits (MMIC) are now frequently fabricated in CMOS technology.

Three different active and passive phase shifters were reported for the first time using 90nm CMOS process in the 50-56 GHz frequency range in [4]. The passive phase shifter was designed based on shunt and series shunt lines, while the active phase shifters were designed based on vector modulator to compensate the phase rotation inability of the passive phase shifters in the entire 360^0 range. The passive phase shifters also experienced higher insertion loss compared to the active phase shifters.

A MMIC phase shifter was presented in [6], using 0.18 um CMOS process in the 11-15 GHz frequency range for satellite communications and radars. This phase shifter achieved phase range of 360^0 with literally no power consumption, but it showed high insertion loss and occupies a large chip area.

An mm-Wave CMOS phase shifter was presented in [7], which can be controlled digitally. 65nm CMOS technology was used to design the phase shifter and the phase shifter achieved 180^0 differential phase shift with 22.5^0 phase resolution and low chip area. The phase shifter was proposed for mm-Wave phased array systems. This was first ever reported digitally controlled phase shifter at 60 GHz.

Three CMOS phase shifters were presented in [12], which were 4-bit active digital phase shifter for X-, Ku-, and K-band phased array applications. The phase shifts were achieved by interpolating the quadrature input signals by adding two in-phase (I) and quadrature phase (Q)

inputs. Low insertion loss, very high phase precision were achieved along with very low chip area including all the digital control parts.

A Passive phase shifter with a very low phase step was implemented using 0.18 um CMOS technology in the S-band frequency [13]. This phase shifter demonstrated phase resolution as low as 5.625^0 along with very low RMS phase error and low insertion loss. Though the phase shifter consumed high DC power and occupied a large chip area, yet it demonstrated its potentiality for high precision beam steering application in phased array systems in the 2.5 - 3.2 GHz frequency range.

A K-band phase shifter was proposed in [14] using both 180^0 switch-type phase shifter (STPS) and 180^0 reflection-type phase shifter (RTPS). This phase shifter experienced very low insertion loss variation and occupied small area with no power consumption. Another K-band phase shifter was reported in [15], with low RMS phase error and low gain variation for phased array systems application. This phase shifter was a passive phase shifter based on vector-sum method in the 0.18 um CMOS technology.

A vector combining based active CMOS phase shifter was implemented in mm-Wave frequency for automotive radar applications [16]. This phase shifter demonstrated phase rotation performance in the whole 360^0 range with a decent gain of 4.3 dB and small chip area of 0.3 mm^2 excluding the digital control parts. An mm-Wave passive phase shifter with smallest chip area was reported for the first time at 60 GHz for mm-Wave beamforming applications [17].

A vector-sum based phase shifter was presented in [18], which used a variable gain amplifier (VGA) to control the gain and phase in the 0.5-6 GHz frequency for suitable wide band phased array systems applications. This phase shifter exhibited 360^0 phase shift performance with a high

gain of 8-10 dB and a relatively high power consumption of 27.5 mW compared to passive phase shifters.

Most of the works discussed above mostly concentrated on phase control and suffered from high insertion loss. In [16], [18], good conversion gain was achieved with 360^0 phase shift. None of the works achieved very high gain with dynamic gain controllability.

All the literature survey is summarized in Table 1.

Table 1: Summary of the literature review

Technology	Frequency (GHz)	Phase Shift (^{0})	Gain (dB)	Area (mm^2)	Power Consumption (mW)	Application	Reference
90nm CMOS	50-56	360	-4.9	0.18	23	Phased Array Systems	[4]
0.18um CMOS	11-15	360	-16.2	4.34	0	Satellite Communication and Radar	[6]
65nm CMOS	60	180 diff.	-9.4	0.2	~0	Phased Array Systems	[7]
0.13um CMOS	15-26	360	-3.8	0.15	11.7	Phased Array Systems	[12]
0.18um CMOS	2.5-3.2	360	-2.5	4.16	60	Phased Array Systems	[13]
0.18um CMOS	23	275	-12	0.45	0	Phased Array Systems	[14]
0.18um CMOS	22-26	360	-15.3	0.31	0	Phased Array Systems	[15]
65nm CMOS	76-81	360	4.3	0.3	~	Automotive Radar	[16]
65nm CMOS	57-64	360	-16.3	0.094	~0	mm-wave Beamforming	[17]
0.13um CMOS	0.5-6	360	8-10	1.21	27.5	Wide Band Phased Array Systems	[18]

3. CHIP LAYOUT AND FABRICATION

The layout of the phase shifter [10], [11] was carried out using Cadence virtuoso tool and sent to MOSIS for fabrication using 0.18um CMOS process. The completed layout of the CMOS phase shifter [10], [11], is shown in Fig. 4. The microphotograph of the fabricated CMOS phase shifter die is shown in Fig. 5. The dimensions of the fabricated die are 1.5 mm x 0.75 mm including all bond pads.

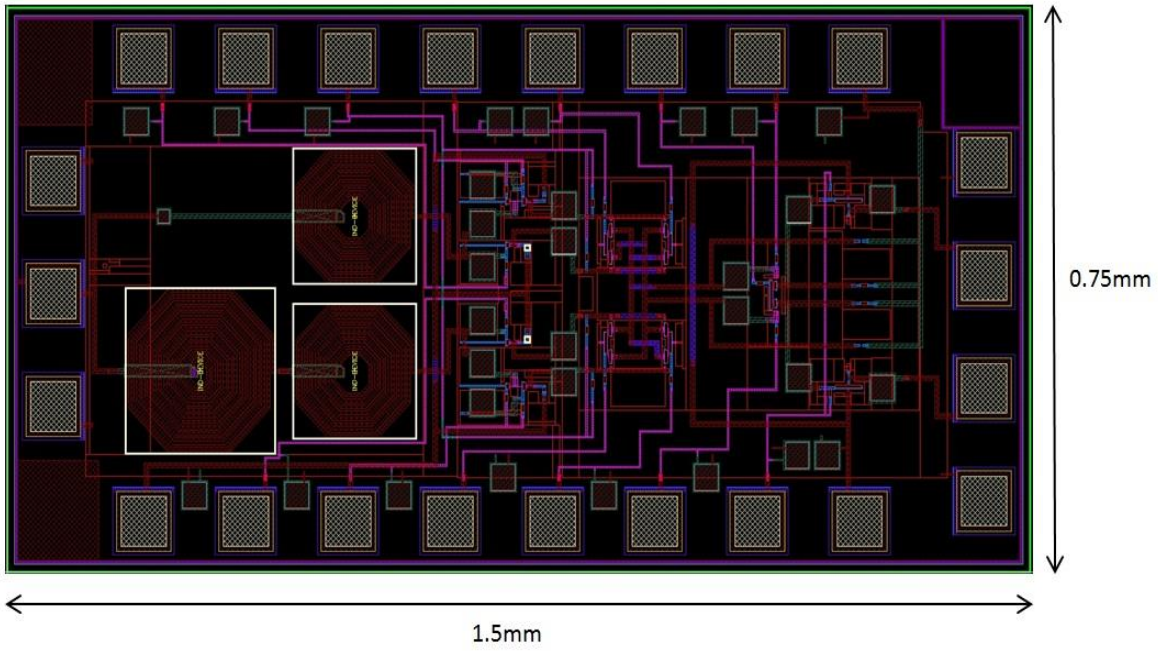

Fig. 4. Layout of the CMOS phase shifter (1.5 mm x 0.75 mm).

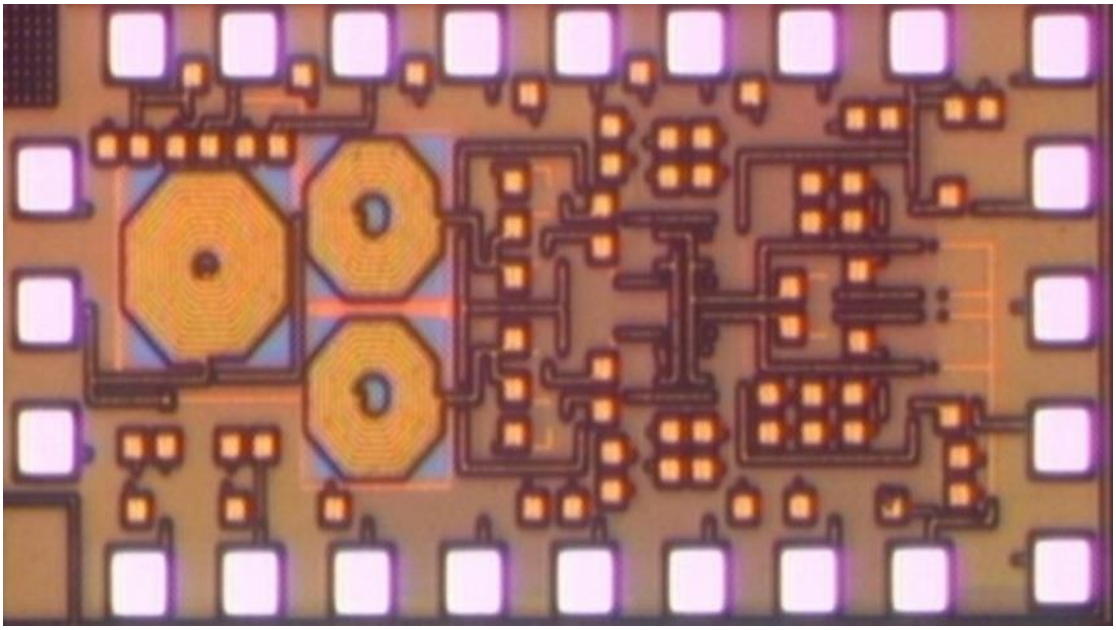

Fig. 5. Micrograph of the fabricated CMOS phase shifter die (1.5 mm x 0.75 mm).

4. CHARACTERIZATION OF THE FABRICATED CHIP AND DISCUSSIONS

The phase shifter was measured using an Agilent ENA E5071C network analyzer with frequency sweeping from 100 KHz to 8.5 GHz. Cascade Microtech probe station was used for probing the phase shifter die.

ACP (Air Co-planar) series GSG probes were used for probing the RF input and output of the phase shifter die. ACP probes are ideal for high power, can perform measurements up to 2000 C and can endure 5 A DC current [19]. An ACP series GSG probe is shown in Fig. 6.

Fig. 6. An ACP series RF GSG probe.

All the measurements were done with 2-port SOLT (Short, Open, Load, Thru) calibration to the ACP probe tips. Impedance Standard Substrate ISS 101-190 C was used as calibration substrate for calibration. The CalKit ISS 101-190 C was defined manually in the ENA E5071C network analyzer. Before doing the calibration, all the probes were planarized on the contact substrate inspecting the probe marks for even GSG contacts.

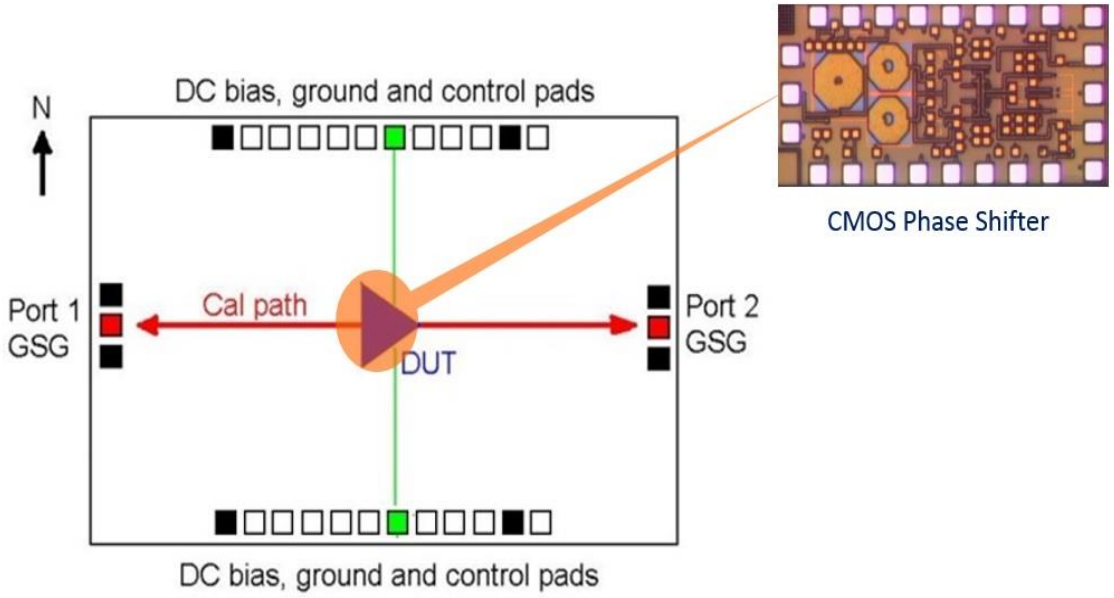

Fig. 7. Device pad layout for the phase shifter measurement.

The device pad layout for the phase shifter measurement is shown in Fig. 7, where the fabricated CMOS phase shifter die was the device under test (DUT). All pads were placed on the top surface and the recommended minimum pad size was ensured for ACP probes, which is 80 um x 80 um [19]. To avoid the cross-talk, 200 um separation between the RF probes was maintained and all the grounds were connected together.

As mentioned above, the phase shifter was measured using Agilent ENA E5071C network analyzer and all the measurements were done with SOLT calibration to the probe tips. Fig. 8 presents the measured phase response of the phase shifter over 2~3 GHz. The phase shifter demonstrated a continuous phase shift of 303^0 over the 2~3 GHz frequency. The phase shift was measured at the highest gain setting. The phase shifting characteristics were achieved by changing

the bias voltages of the tail transistors of the vector modulator of the phase shifter. The phase control principle of the phase shifter is discussed in section 5.

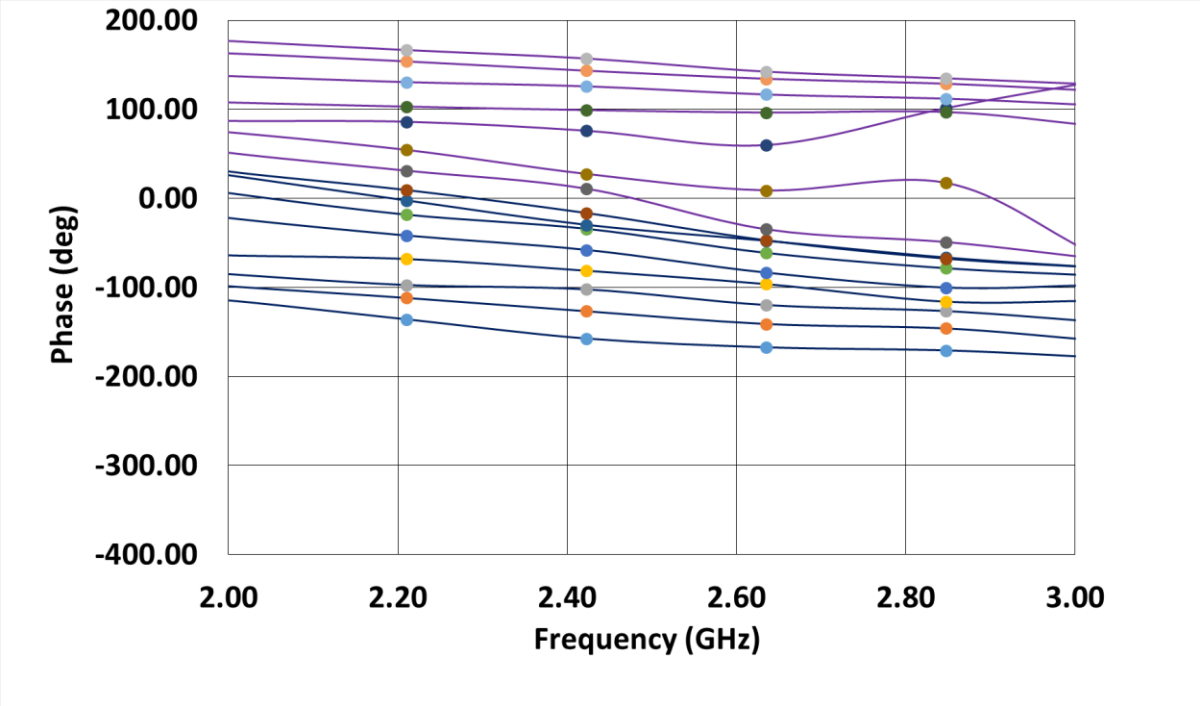

Fig. 8. Measured frequency characteristics of the phase variation of the CMOS phase shifter by changing phase control signals.

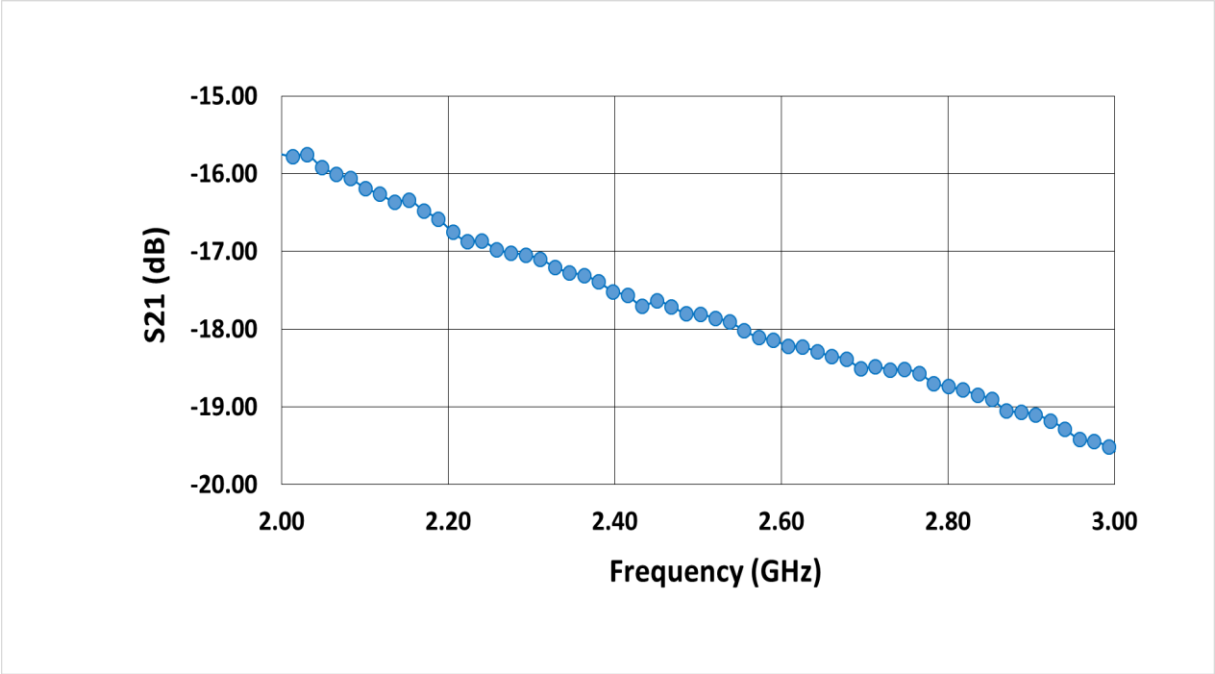

Fig. 9. Measured gain response of the phase shifter.

The measured gain response of the phase shifter is shown in Fig. 9. The phase shifter resulted in -16.8 dB of gain (S21) at 2.2 GHz. Fig.10 presents the measured input return loss and output return loss of the phase shifter. The phase shifter demonstrated an output return loss (S22) of -9.53 dB at 2.2 GHz and <-10 dB over 2.25-3 GHz frequency. And, the phase shifter exhibited an input return loss (S11) of less than -20 dB over 1.5-3 GHz frequency. The measured input and output return loss confirms that the phase shifter input and output were well matched to 50Ω.

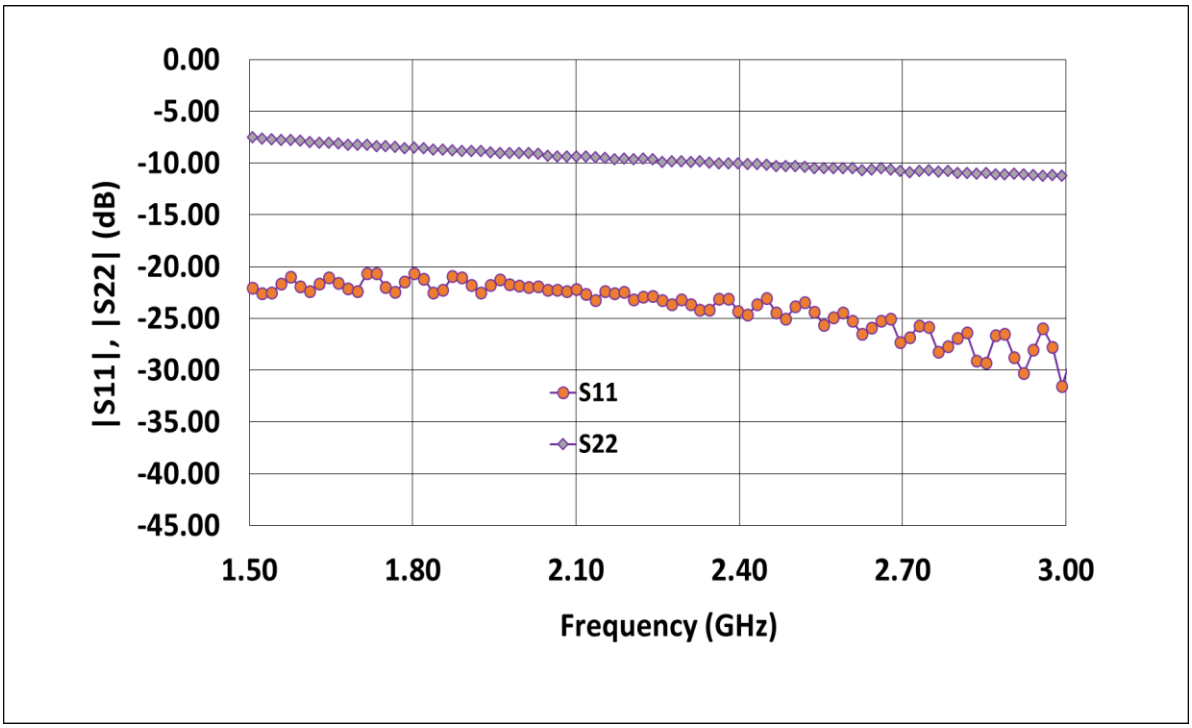

Fig.10. Measured input return loss and output return loss of the phase shifter.

Fig.11 features the characteristics of the measured gain variation at a particular phase setting of the phase shifter. The phase shifter achieved 9-dB of gain variation at a particular phase setting @3.5GHz. The gain variation of the phase shifter was measured at a particular phase setting by varying the tail transistor bias voltage of the variable gain amplifier (VGA).

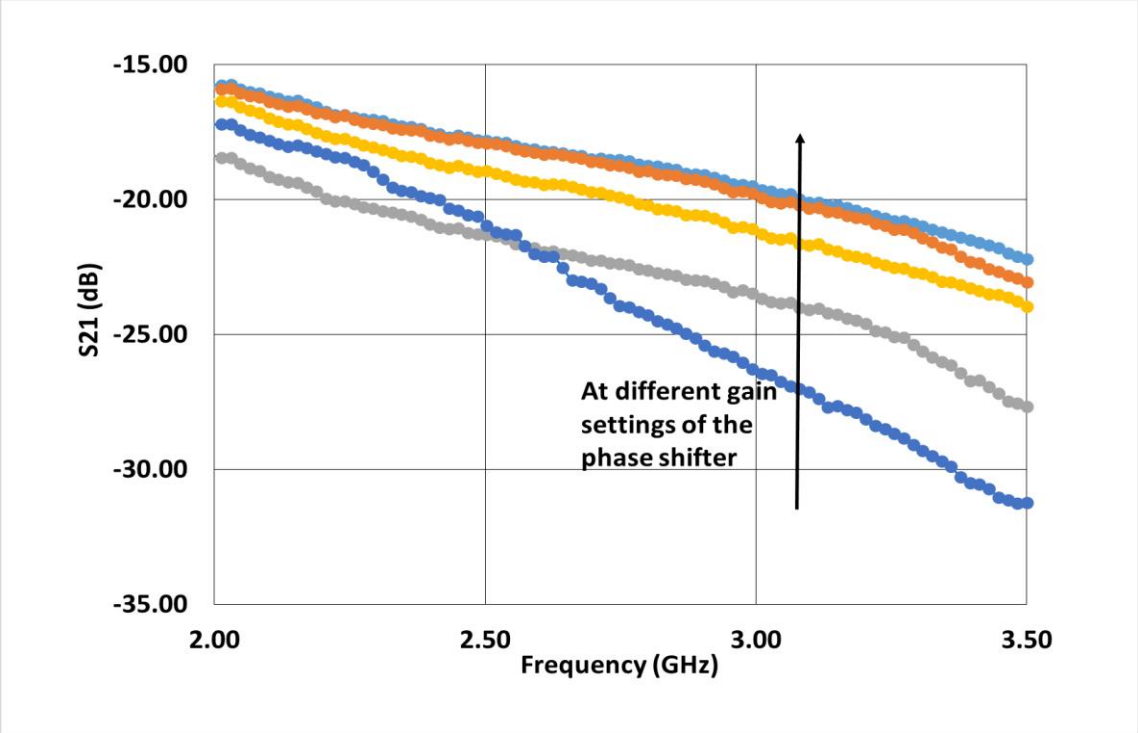

Fig. 11. Measured gain variation of the phase shifter at a particular phase setting.

The phase shifter consumed 34.2 mW of measured DC power. All the measurement results of the phase shifter are summarized in the Table 2.

Table 2: Summary of the measured results

Technology	0.18 um CMOS
Phase Range	303^0 (Over 2~3 GHz)
Gain (S21)	-16.8 dB @ 2.2 GHz
Input Return Loss	<-20 dB (Over 1.5~3 GHz)
Output Return Loss	<-10 dB (Over 2.25~3 GHz)
Gain Variation	9 dB @ 3.5 GHz
Power Consumption	34.2 mW
Chip Area	1.5 mm x 0.75 mm (including pads)

5. DESIGN OF THE NEW PHASE SHIFTER

From the measured results of the phase shifter in section 4, it is noticeable that the phase shifter [10], [11], achieved continuous phase rotation of 303^0 and a gain variation of 9-dB at 3.5 GHz. The phase shifter also demonstrated 16.8 dB of insertion loss at 2.2 GHz with very good input/output matching. Based on the measured results, a modified phase shifter was proposed and designed with a high gain active balun and a modified passive hybrid. The passive hybrid was changed to R-C from L-C, which helped to avoid bulky inductor and reduce the chip area without degrading the hybrid performance. The loading of the both vector modulator (VM) and variable gain amplifier (VGA) circuits were replaced by inductor for better RF performance at 2~3 GHz frequency. Block diagram of the proposed CMOS phase shifter is shown in Fig. 12.

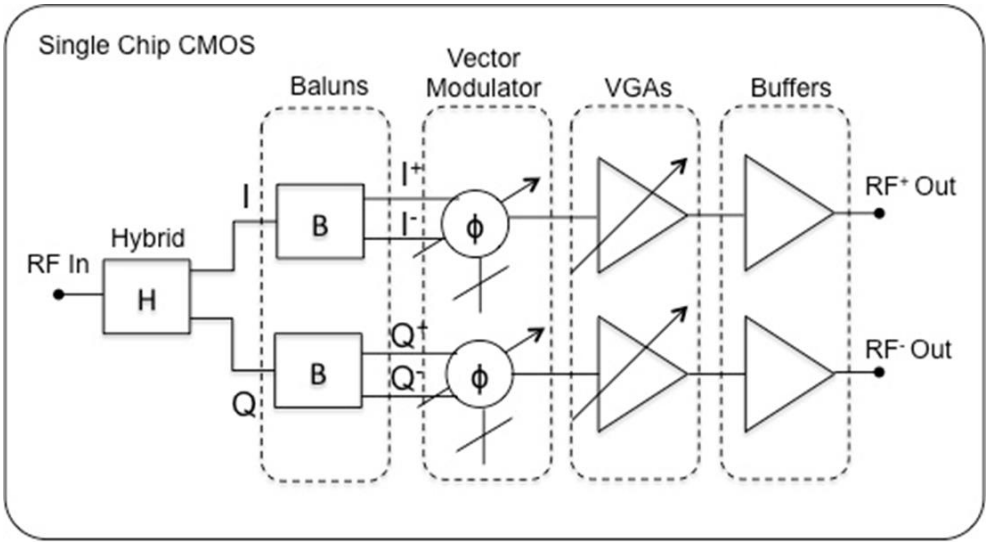

Fig. 12. Block diagram of the proposed single chip CMOS phase shifter.

Fig. 13 shows the modified vector modulator integrated with VGA and buffer stages for the new phase shifter. A double balanced Gilbert cell based vector-modulator circuitry was used as the phase rotator, which is shown in Fig. 13. Four RF signals with phases 0^0 (I+), 90^0 (Q+), 180^0

(I-) and 270^0 (Q-) respectively, were fed to the upper differential pair transistors of the Gilbert cell as shown in Fig. 13. To get an output signal with a particular phase shift, vector components of these RF signals needed to be added as shown in Fig. 14. To achieve the continuous phase shift, the amplitude of these RF signals needed to be controlled via control voltages through four tail transistors used as the control ports named as I- control, I+ control, Q- control and Q+ control respectively shown in Fig. 13. By applying appropriate control voltages to any of these control ports, it was possible to get any desired phase. The loading of the vector modulator was replaced by inductor (L1, L2) from resistors of previous design [10], [11] and the values were chosen L1 = L2 =2.6nH. Inductors were used to make the gain more frequency dependent and to achieve better phase linearity. Proper bias voltages through control ports of the vector modulator were chosen to get all the 16 phase steps with 22.5^0 of resolution from 0^0 to 360^0. While choosing the control voltages, it was also made sure that the upper transistors operate in saturation region, as it was noticed that if the upper transistors of the vector modulator were not in saturation region, it reduced the swing of the vector modulator output which caused the amplitude imbalance of the phase shifter with the change of phase from 0^0 to 360^0 at a particular gain setting.

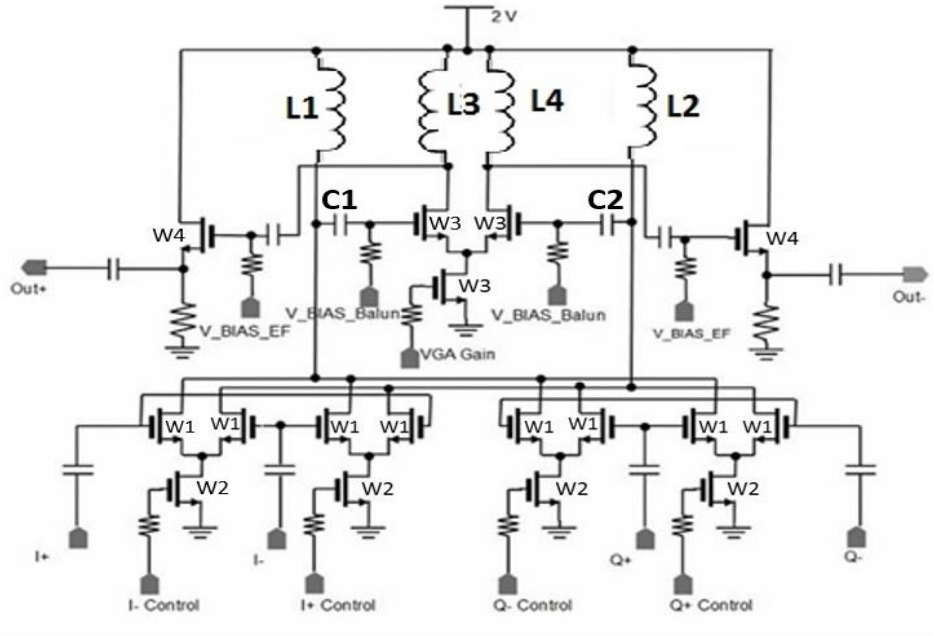

Fig. 13. Circuit schematic of the vector modulator integrated with VGA and buffer for new phase shifter design.

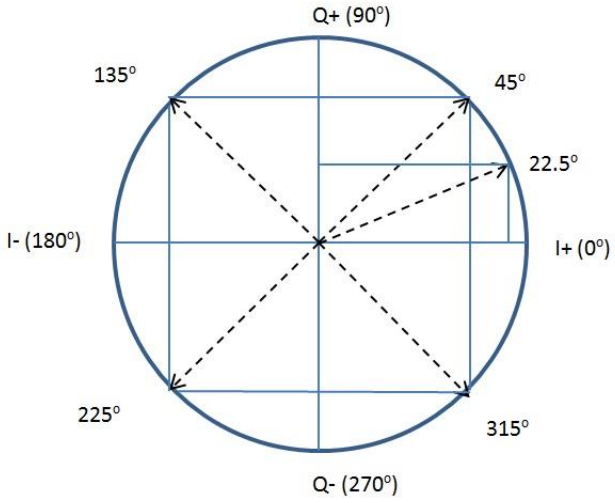

Fig. 14. Phase control diagram.

Now, to generate the four input RF signals that fed to Gilbert cell, a passive quadrature and two active baluns were used. The passive quadrature/hybrid was used to split the input RF signal

into two RF signals with the phase difference of 90^0 and thus, in phase (I) and quadrature (Q) signals were produced. The passive hybrid was designed with RC low pass and high pass filter shown in Fig. 15 with 3 dB loss. The quadrature/hybrid was designed in such a way that both of the arms matched to 100 Ω to terminate or match the hybrid input, that is, the phase shifter input to 50 Ω. The resistor value was chosen 71.18 Ω and the capacitor value was 1.02 pF to match each arm to 100 Ω at 2.2 GHz. This passive hybrid helped to reduce the overall chip size avoiding bulky inductors of previous design [10], [11]. The upper end (R-C end) of the hybrid contributed -45^0 phase and the lower end (C-R end) contributed $+45^0$ phase. Thus the passive quadrature produced two output signals of 90^0 phase difference with no phase mismatch.

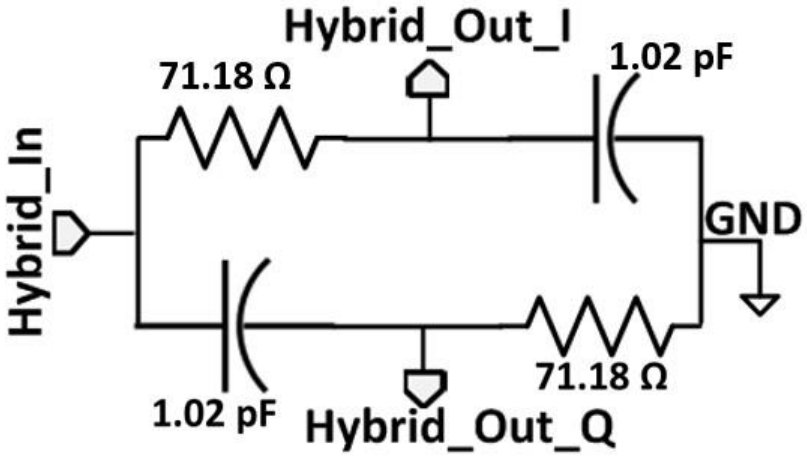

Fig. 15. Circuit schematic of passive hybrid.

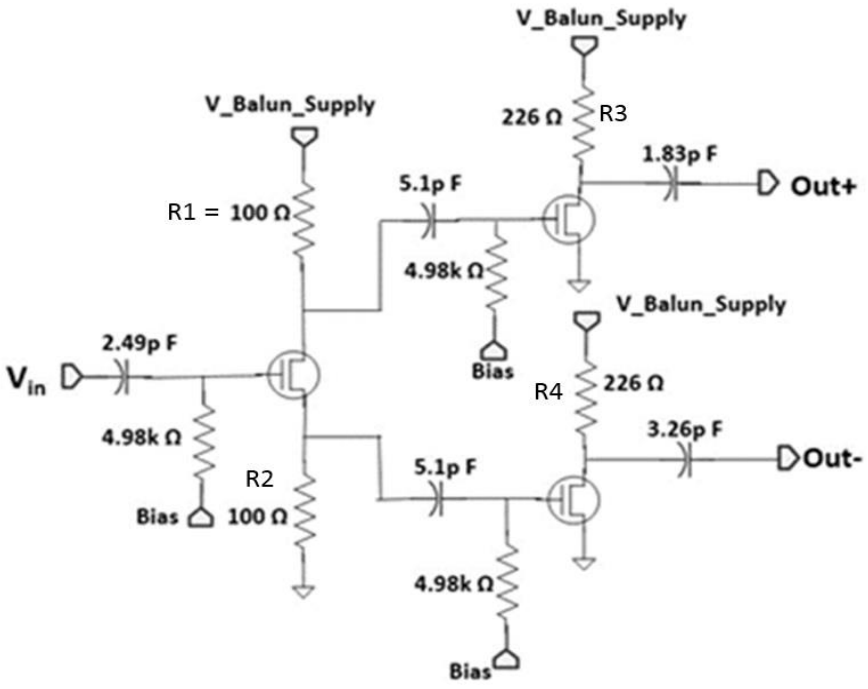

Fig. 16. Circuit schematic of active balun.

These I and Q signals were passed through active baluns to produce two out of phase signals from each input signal as shown in Fig. 16. The active balun was designed using common source and source follower arrangement to get two output signals of 180^0 out of phase. Both of the resistors were kept of same value (R1 = R2= 100Ω) to get output of similar amplitude from the balun. This active balun provided very low amplitude imbalance and phase mismatch between the two out of phase paths compared to the previous active balun design [10], [11]. This was because both of the paths of the balun were symmetrical and a single bias was used for the balun to control the phase and amplitude. The two out of phase signals were fed through identical CS amplifier stages to produce extra gain by compensating the 3 dB loss of passive hybrid. The resistors values of the amplifier stages were also kept same (R3 =R4) to maintain the same amplitude.

The variable gain amplifier (VGA), shown in Fig. 13, can vary gain by controlling the bias (VGA Gain) of the tail transistor. Vector modulator outputs were fed to the VGA to achieve gain variation. The vector modulator output and the VGA input impedances were matched such that phase and gain variation do not affect each block. The loading of the VGA (Fig. 13) was also replaced by inductors (L3, L4) for better RF performances. The values were chosen L3 = L4 = 19.6nH. The highest gain was tuned at the desired frequency (2~3 GHz) range with inductors loading, as inductor-capacitor circuit arrangement gives better tuning than the resistor-capacitor arrangement. The bias of the VGA tail transistor (VGA Gain in Fig. 13) was varied from 0.45 V to 1.2 V to vary the gain of the phase shifter and thus to achieve the dynamic gain control range. While designing the VGA, the looking impedance to VGA from vector modulator was kept very high compared to the looking impedance to vector modulator from VGA, to maintain the consistency of phase while varying the bias of VGA tail transistor at a particular phase setting. The values of C1 and C2 were chosen 2.08 pF to make sure $X_{L1} = X_{L2} = X_{C1} = X_{C2}$. This helped to maintain the phase consistent with the variation of gain at a fixed phase setup. Source follower buffer stages (Fig. 13) were used to match the phase shifter output to 50 Ω.

All the circuits were designed using co-design method considering the input and output impedances of the each block to ensure minimum power consumption.

All the transistor sizes are listed in the Table 3.

Table 3: Transistor sizes of the new phase shifter

Transistors	Width (um)	Length (um)
W1	20	0.18
W2	35	0.18
W3	35	0.18
W4	51	0.18

6. SIMULATION RESULTS OF THE NEW PHASE SHIFTER

CADENCE® Spectre® simulator [20] was used for simulating the whole circuit. The input and output of the integrated phase shifter circuit were matched to 50Ω.

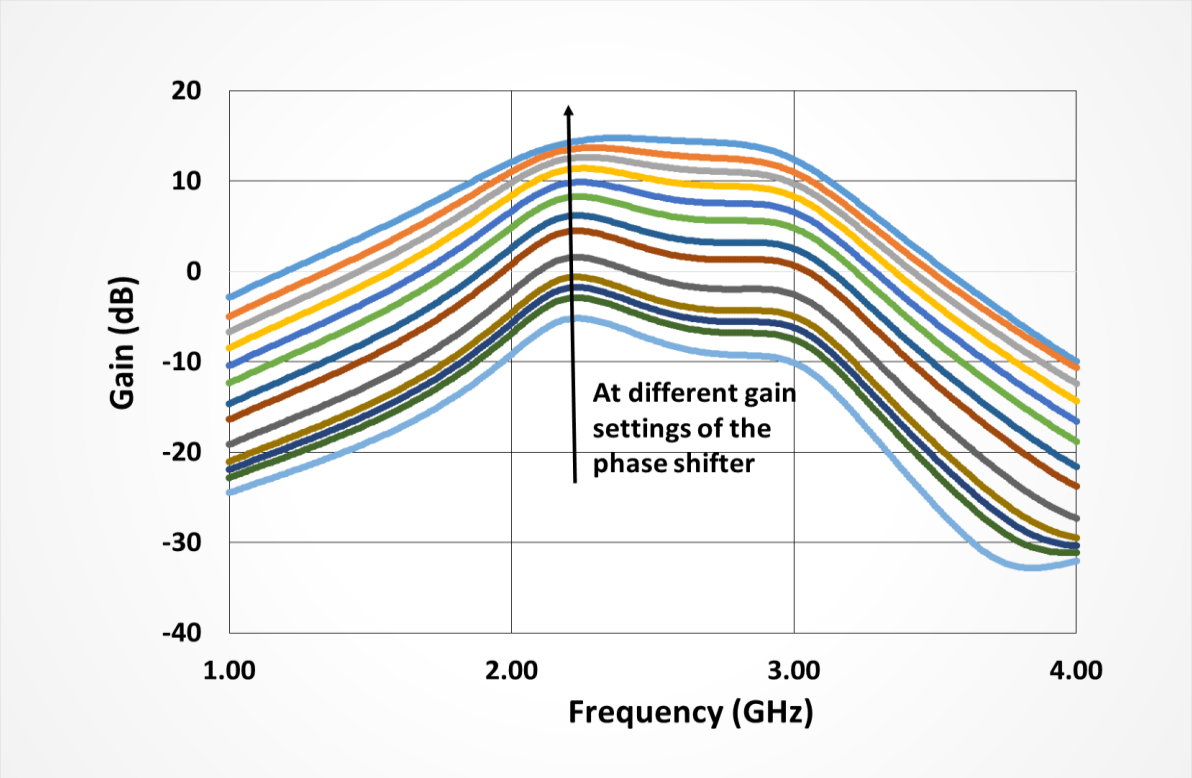

Fig. 17. Frequency characteristics of gain variation of the phase shifter at a particular phase setting.

Fig. 17 exhibits the frequency characteristics of the gain variation of the circuit at 0^0 phase setting. A very high gain control range of 20 dB was achieved over 2~3 GHz frequency, shown in Fig. 17, which ensured the high dynamic range of the proposed phase shifter. The gain variation was achieved by varying the tail transistor bias, VGA_Gain of the variable gain amplifier (VGA) shown in Fig. 13. The bias voltage was swept from 0.45 V to 1.2 V to achieve 20-dB of gain variation.

Fig. 18 demonstrates the frequency characteristics of the phase variation of the circuit from 0^o to 360^o with resolution of 22.5^o. The phase shifter was capable of rotating the phase in the entire 0^o to 360^o range on continuous basis. The phase shifting performances were achieved at highest gain setting. The phase shift in the entire 360^0 range was achieved by controlling the bias voltages of the control ports of the vector-modulator shown in Fig. 13.

The overall integrated phase shifter showed an input return loss better than 7.73dB, an output return loss better than 11dB for the 1-3 GHz frequency range. The total conversion gain of 14.2 dB was achieved at 2.2GHz as depicted in Fig. 19.

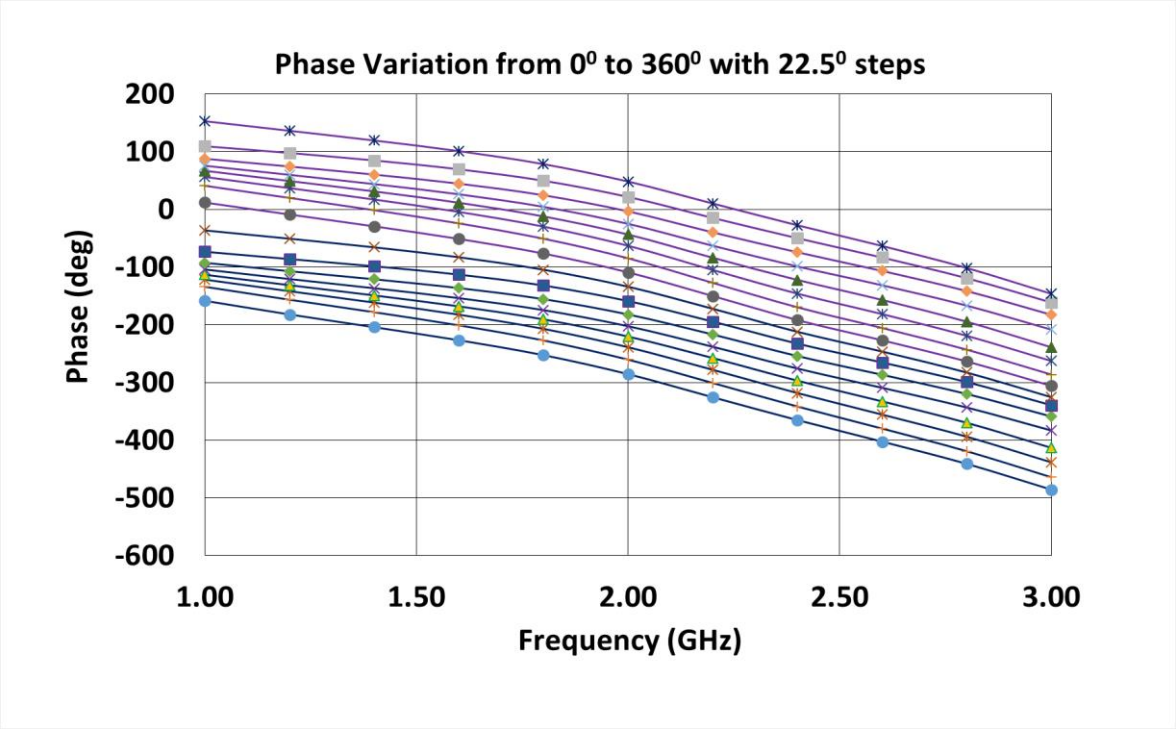

Fig. 18. Phase variation of the phase shifter in the entire 360^o range by changing the phase control signals of the phase shifter.

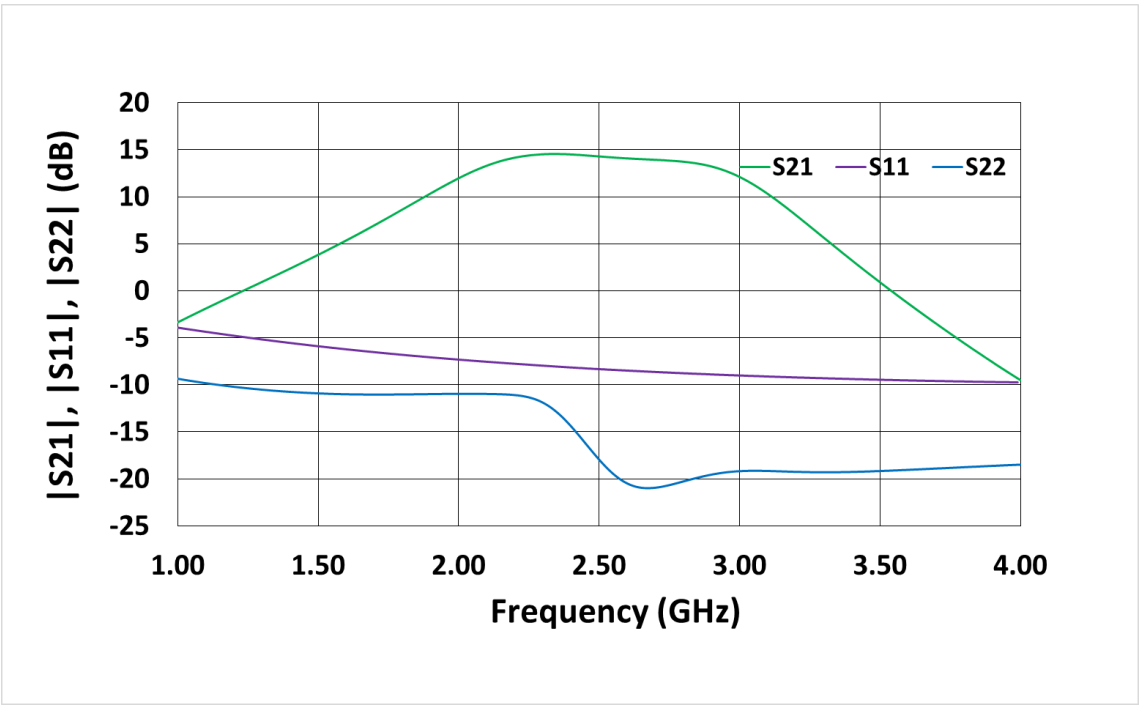

Fig. 19. Simulation results of the scattering parameters of the integrated phase shifter.

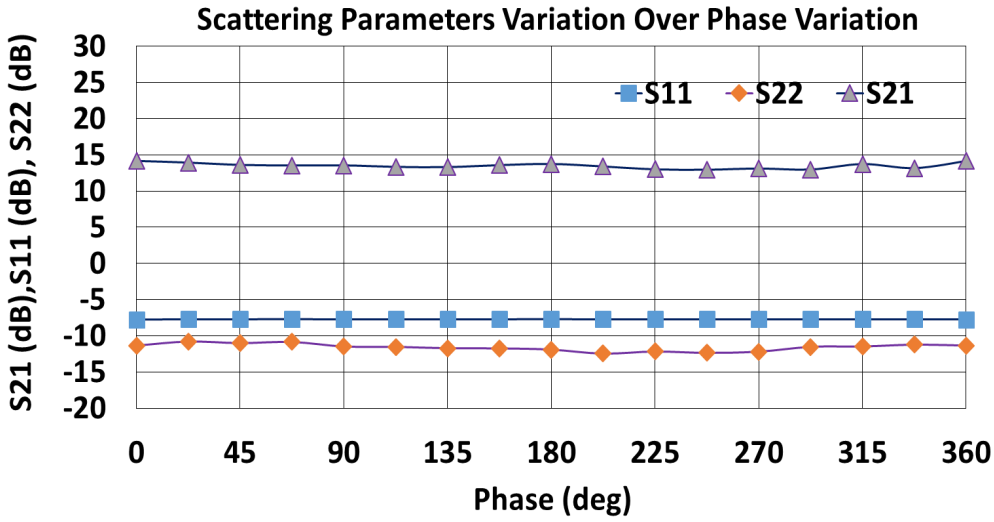

Fig. 20. Stability of conversion gain and return loss over phase variation.

The uniqueness of this proposed CMOS phase shifter was in demonstrating the constant input and output impedances with the continuous change of phase, which is shown in Fig. 20. The

gain characteristics showed a variation of less than 1-dB with the change of phase from 0° to 360°, which confirmed that the phase shifter was capable of controlling its phase without degrading its gain.

The RMS phase error was achieved 2^0 at 2.2 GHz, shown in Fig. 21. The RMS phase error was calculated by following:

$$RMS\ \ phase\ error = \sqrt{\frac{\sum_{k=i}^{n} \Delta\phi_k^{\,2}}{n}} \tag{1}$$

Where,

$\Delta\phi_k$ = Phase errors of the raw phase states

n = Number of the phase state

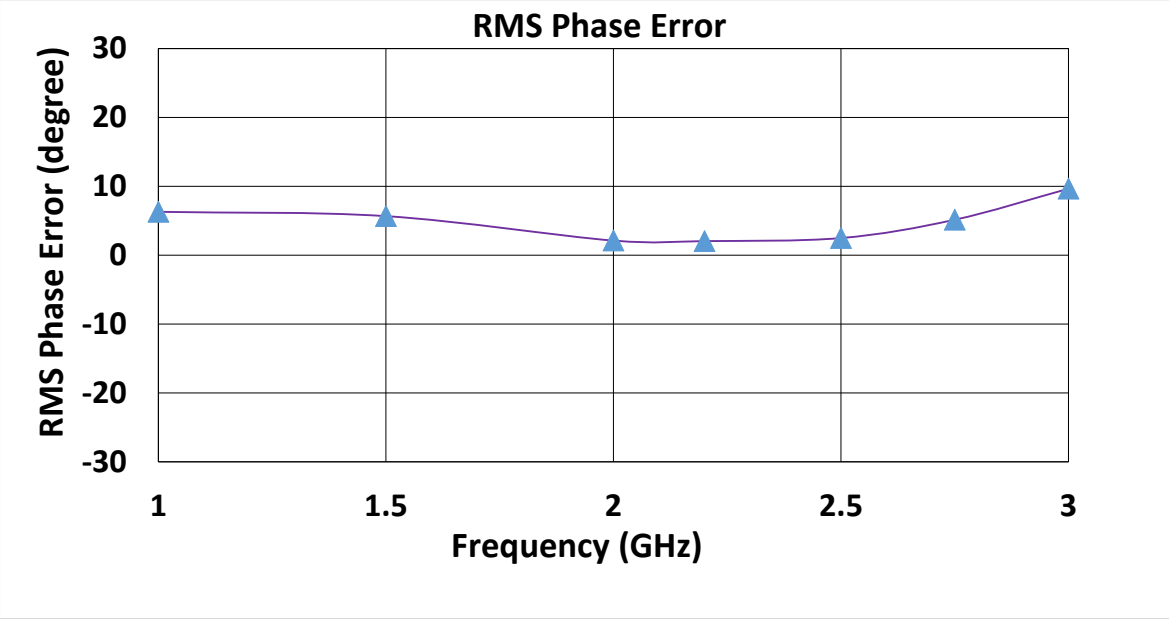

Fig. 21. RMS phase error.

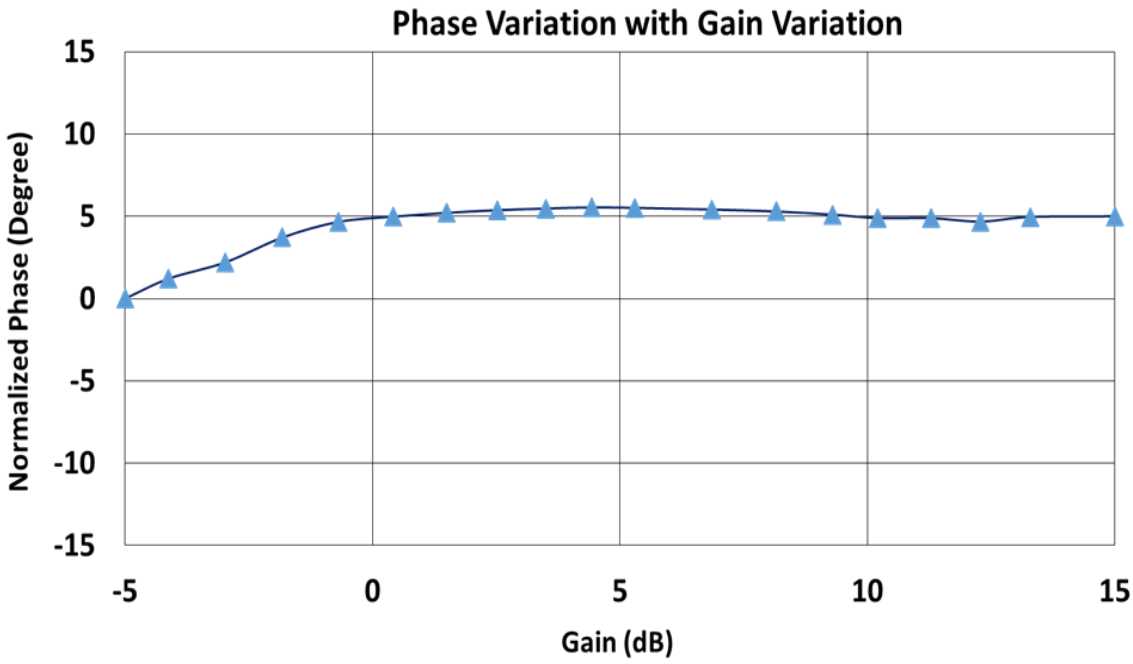

Fig. 22. Phase variation of the integrated phase shifter over gain variation.

Fig. 22 shows a small phase variation with the variation of gain at a particular phase setting. The phase changed up to 5^0 over the 20-dB gain variation, which confirmed the consistency of the phase of the phase shifter with the variation of gain at a particular phase setting.

Fig. 23 exhibits the large signal performances of the phase shifter. The 1-dB input compressed power was found to be -20 dBm. This amount of power is enough to include this proposed phase shifter circuit in the receiver and in the local oscillator path of a transmitter.The input third intercept point (IIP_3) of the circuit was achieved -10.4 dBm after adding 9.6 dB to 1-dB intput compression point.

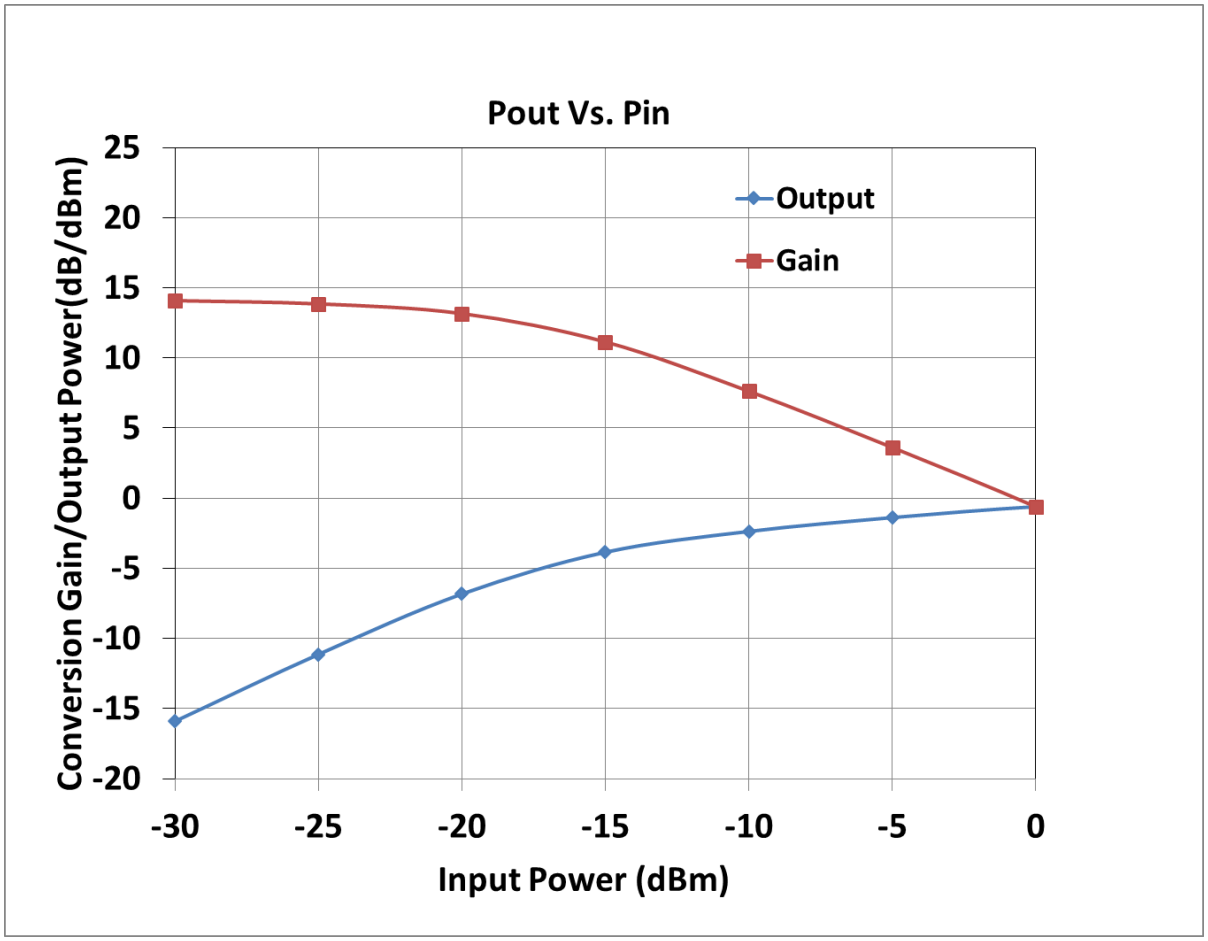

Fig. 23. Conversion gain and output power vs. input power of the integrated phase shifter.

The performance summary of the phase shifter is shown in Table 4, which confirms state-of-the-art performances of the phase shifter.

Table 4: Performance summary

Technology	0.18um CMOS
Frequency	1 ~ 3 GHz
Phase Control Range	360^{o} (continuous)
Conversion Gain	+14.2dB @ 2.2 GHz (variable)
Gain Control Range	20 dB over 2~3 GHz
Input Return Loss	< -7.73dB @ 2.2GHz
Output Return Loss	< -11dB @ 2.2GHz
1-dB Input Compressed Power	-20 dBm
Power Consumption	98.65mW

Table 5 shows the performance comparison of the proposed phase shifter with other state-of-the-art phase shifters using various process technologies.

Table 5: Performance comparison

Ref.	[6]	[12]	[13]	[18]	[21]	[22]	This work
Frequency (GHz)	11-15	15-26	2.5-3.2	0.5-6	5.15-5.7	4-6	1-3
Conversion Gain (dB)	-16.2	-3.8	-2.5	8-10	-9	-2.2	+14.2 (variable)
Gain Control Range (dB)	-	-	-	-	-	-	20 over 2~3 GHz
Phase Range (^{o})	360	360	360	360	360	90	360
DC Power (mW)	0	11.7	60	27.5	~0	~0	98.65
Process Technology	0.18um CMOS	0.13um CMOS	0.18um CMOS	0.13um CMOS	0.6um GaAs MESFET	0.6um GaAs MESFET	0.18um CMOS

7. SUMMARY, CONTRIBUTIONS AND FUTURE WORK

7.1. Summary

A vector modulator based variable gain CMOS phase shifter [10], [11], was fabricated and characterized. The phase shifter demonstrated measured continuous phase shifting characteristics of 303^0 and a gain variation of 9-dB at 3.5 GHz. It also resulted in 16 dB of insertion loss and input return loss better than 20 dB and output return loss better than 9.53 dB at 2.2 GHz frequency. Based on the measured results, a modified phase shifter was proposed using 0.18um CMOS with high gain and high dynamic gain control range. The proposed new design achieved phase rotation of 360^0 with 22.5^0 steps with a low RMS error of 2^0 at 2.2 GHz. It achieved a very high conversion gain of 14.2 dB, along with input return loss better than 7.73 dB and output return loss better than 11 dB at 2.2 GHz. A dynamic gain control range of 20 dB was achieved over 2~3 GHz by tuning the tail transistor bias of the VGA. The simulated results showed that the phase shifter experiences amplitude imbalance of less than 1-dB while changing the phase from 0^0 to 360^0 and a phase variation of less than 5^0 while varying the gain of the phase shifter. The phase shifter consumed 98.65 mW of DC power with 2 V supply. All these specifications of the proposed phase shifter make it very suitable for phased array antenna systems applications to restore both the phase and amplitude of the degraded radiation pattern due to its incident on conformal surface, where both beamforming and nulling can be achieved.

7.2. Contributions

The layout and fabrication of a variable gain CMOS phase shifter was done and the fabricated chip was characterized, which showed very good phase shifting characteristics along with very good gain variation. After analyzing and debugging the measured results, modified new

phase shifter was proposed and designed, which achieved a very high gain along with a high dynamic gain control range and capable of controlling both the phase and amplitude of the phase shifter output signal simultaneously and independent of each other. This independent controllability of both phase and gain gave the proposed phase shifter unique characteristics of restoring both phase and gain of the degraded radiation pattern of antenna array due to its incident on a conformal surface and showed a huge potential application of integrating the implemented phase shifter with phased array antenna systems and would create a potential future for smart communication radar applications like weather radar, surface ship radar, and some communication satellites, especially the radars used by NASA to communicate with space shuttle and the International Space Station. All the circuit blocks were designed using co-design method to terminate both input and output of the phase shifter to 50 Ω.

7.3. Future Work

The next research plan is to finish the layout of the proposed new phase shifter design and send it for fabrication in the next available tape out run. And once the fabricated chip come back, the single chip will be characterized to look at its real performances. As an extension of this work, there is a plan to develop a phase shifter array with a closed loop digital control system for taking care of dynamical changes of surface curvature of a conformal phased array antenna. The ultimate goal is to build the whole CMOS integrated beamformer with conformal phased array antenna shown in Fig. 3.

8. PUBLICATIONS RESULTING FROM THIS WORK

[1] **Dipankar Mitra**, Palash Roy & Debasis Dawn, "A Variable High Gain and High Dynamic Range CMOS Phase Shifter for Phased Array Beamforming Applications," presented at EiT 2016 IEEE International Conference.

[2] **Dipankar Mitra**, Alarka Sanyal, Palash Roy & Debasis Dawn, "A Variable Gain CMOS Phase Shifter for Phased Array Beamformer Applications," presented at 3rd International Conference on Foundations and Frontiers in Computer, Communication and Electrical Engineering, 2016.

[3] **Dipankar Mitra**, Palash Roy, Alarka Sanyal, and Debasis Dawn, "CMOS Integrated Beamformer with Conformal Phase Array Antenna for Wireless Communications," poster presentation at ND EPSCoR/IDeA 2015 State Conference.

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