

WIDE BAND-GAP SEMICONDUCTOR BASED POWER CONVERTER RELIABILITY  
AND TOPOLOGY INVESTIGATION

A Dissertation  
Submitted to the Graduate Faculty  
of the  
North Dakota State University  
of Agriculture and Applied Science

By  
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In Partial Fulfillment of the Requirements  
for the Degree of  
DOCTOR OF PHILOSOPHY

Major Department:  
Electrical and Computer Engineering

June 2020

Fargo, North Dakota

North Dakota State University  
Graduate School

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**Title**

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RELIABILITY AND TOPOLOGY INVESTIGATION

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## ABSTRACT

Wide band-gap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) have been widely investigated these years for their preferred operation at higher switching frequency, higher blocking voltage, higher temperature, with a compacter volume, in comparison with the traditional silicon (Si) devices. SiC MOSFETs have been utilized in photovoltaic systems, wind turbine converters, electric vehicles, solid-state transformers, more electric ships, and airplanes. GaN based transistors have also been adopted in the DC-to-DC converters in data centers, personal computers, AC-to-DC power factor correction converters for the consumer electronic adaptors, and DC-to-AC photovoltaic micro-inverters.

The first part of this dissertation is regarding the lifetime modeling and condition monitoring for the SiC MOSFETs. Since SiC-based devices have different failure modes and mechanisms compared with Si counterparts, a comprehensive review will be conducted to develop accurate lifetime prediction, condition monitoring, and lifetime extension strategies. First, a novel comprehensive online updated system-level lifetime modeling approach will be presented. Second, to monitor the SiC MOSFET ageing, the typical degradation indicators of SiC MOSFET gate oxide will be investigated. Third, to measure the junction temperature, the dynamic temperature-sensitive electrical parameters for the medium-voltage SiC devices will be studied.

The other part is the topology investigation of these emerging wide band-gap devices. A generalized topology that would leverage the advantages of the wide band-gap devices will be introduced and analyzed in detail. Following it is a new evaluation index for comparing different topologies with the consideration of the semiconductor die information. The topology and its derivatives will be utilized in the subsequent chapters for three applications. First, a 100 kW switched tank converter (STC) will be designed using SiC MOSFETs for transportation power

electronic systems. Second, an updated STC topology integrating with the partial-power voltage regulation will be introduced for electric vehicle applications. Third, two novel single-phase resonant multilevel modular boost inverters will be designed based on the voltage-regulated STC. These topologies will be validated through designed prototypes. As a result, the high power density and high efficiency will be realized by combining the well-suited topologies and the advantages of the WBG devices.

## ACKNOWLEDGEMENTS

First of all, I want to express my sincere gratitude to my advisor Dr. Dong Cao for offering me this Ph.D. opportunity, for his academic guidance, support, and help in the past four and a half years. Without the patient, enthusiastic, effective instructions from Dr. Cao, this dissertation would be impossible. The experience in the Sustainable Power Electronics and Electric Drive (SPEED) Lab at NDSU has intrinsically strengthened my understanding in power electronics and has also taught me to be a better person in many ways. I will cherish this period for my whole life. I would like to send my best wishes to him in both his career and life.

Also, I want to appreciate Dr. Om Prakash Yadav from IME department and Dr. Brij N. Singh from John Deere Electronic Solutions, for their support in the power electronics reliability project from 2016 to 2018 at NDSU. Dr. Yadav's Reliability Engineering class has systematically prepared me with the fundamentals in reliability analysis. Dr. Singh has provided valuable advice in the monthly project meetings. The interdisciplinary cooperation with the Center of Quality, Reliability and Maintainability Engineering (CQRME) at NDSU has been interesting and exciting.

I would like to acknowledge Dr. Rajesh Kavasseri and Dr. Di Wu for being my committee members. Their advice given in the preliminary and final exams has made the research structure more organized. Their rigorous academic attitude has helped improve this dissertation quality.

I would like to say my thanks to Dr. Xiaofeng Lyu, Dr. Yanchao Li, Mr. Jalen Johnson, Mr. Chengkun Liu, Ms. Mengxuan Wei, Mr. Aaron Niehaus, Mr. Boris Curuvija, and Mr. Khalid Abdelgadir in the SPEED lab for the time we have spent together on multiple projects. I have been so lucky to have met these friends at NDSU. I appreciate for those discussions, mutual encouragement, and afterwork gatherings that have been important for me to go through this unforgettable journey.

I want to appreciate Dr. Sheng Zheng, Dr. Madhu Sudhan Chinthavali and all the team members in the Electric Energy Systems Integration Group from the National Transportation Research Center at the Oak Ridge National Laboratory (ORNL). I appreciate the opportunity to work on the medium-voltage projects and investigate the device thermal monitoring. I want to thank Dr. Zheng for being my internship mentor and for his encouragement and assistance.

I would like to acknowledge Dr. Baoming Ge, Dr. Lihua Chen, and Mr. Boris Curuvija from the Ford Motor Company for the helpful technical discussions in the 100-kW DC-to-DC project. I also want to thank Mr. Derek Lehmann, Mr. Jim Baumgart and Dr. Long Wu at John Deere Electronic Solutions for the test platform coordination and testing assistance in this project. I would also like to thank Mr. Jeffrey Ericson in the ECE department. Jeff has assisted in many projects patiently regarding the component ordering and mechanical engineering assistance.

This research work has been supported in part by ND EPSCoR under Award no. FAR0029766, in part by NASA EPSCoR Research Cooperative Agreement under Award no. 80NSSC19M0081, in part by Ford Motor Company and in part by the National Science Foundation under Award 1810428. This research has also been supported in part by an appointment to the ORNL Advanced Short-Term Research Opportunity Program, sponsored by the U.S. Department of Energy and administered by the Oak Ridge Institute for Science and Education.

Last but not least, I want to send thanks to my family, especially my father Anlin Ni and my mother Chengying Liu. Their understanding, support, care, and love have always been providing me courage and strength to endeavor further in this life.

## TABLE OF CONTENTS

ABSTRACT .....	iii
ACKNOWLEDGEMENTS .....	v
LIST OF TABLES .....	xi
LIST OF FIGURES .....	xii
LIST OF ABBREVIATIONS.....	xviii
LIST OF SYMBOLS .....	xx
1. INTRODUCTION AND MOTIVATION .....	1
1.1. Research Background for the Reliability of Power Electronic Systems .....	4
1.2. The Impact of Wide Band-gap Devices on Topology.....	6
1.3. Structure of This Dissertation .....	7
2. SiC POWER CONVERTER LIFETIME MODELING.....	10
2.1. SiC MOSFET Failure Modes and Mechanisms.....	15
2.1.1. Chip-Level Failure Modes of SiC MOSFETs.....	15
2.1.2. Package-Level Failure Modes of SiC MOSFETs .....	20
2.1.3. Summary of Failure Modes of SiC MOSFETs .....	25
2.2. Offline Component-Level Lifetime Modeling.....	26
2.2.1. SiC MOSFET Accelerated Lifetime Tests and Indicators .....	26
2.2.2. Component-Level Lifetime Modeling Methods.....	30
2.2.3. Cycle Counting and Fatigue Damage Accumulation .....	40
2.3. System-Level Offline Lifetime Modeling.....	41
2.3.1. State-of-Art System-Level Lifetime Prediction Techniques.....	42
2.3.2. Discussion of the Applicability in SiC Power Converters .....	46
2.3.3. SiC Converter Lifetime Modeling Software .....	47
2.4. SiC Power Converter Condition Monitoring .....	49

2.4.1. Electro-Thermal Modeling of SiC Power Devices.....	51
2.4.2. Thermo-Mechanical Modeling of SiC Power Devices .....	53
2.4.3. Temperature-Related Health Indicators .....	54
2.4.4. Non-thermal Health Indicators .....	58
2.4.5. Challenging Online Measurement Techniques .....	59
2.5. System-Level Lifetime Extension .....	63
2.6. Summary for This Chapter .....	69
<b>3. SIC MOSFET GATE OXIDE DEGRADATION INVESTIGATION .....</b>	<b>73</b>
3.1. Theory of Miller Plateau Shift With Gate Oxide Electric Field .....	75
3.2. Theory and Simulation Verification of Miller Plateau Shift With Temperature .....	76
3.3. Gate Oxide Accelerated Lifetime Test.....	78
3.3.1. High Electric Field Stress Accelerated Lifetime Test .....	78
3.3.2. Positive Bias Temperature Stress Accelerated Lifetime Test .....	79
3.4. Indicator Verification Test and Analysis .....	80
3.4.1. Miller Plateau Shift Verification and Analysis .....	81
3.4.2. Threshold Voltage Verification Test and Analysis .....	85
3.4.3. Gate Resistor Turn-on Energy Verification and Analysis.....	88
3.5. Comparison and Analysis Among The Three Investigated Indicators .....	93
3.6. Summary for This Chapter .....	94
<b>4. SIC MOSFET TEMPERATURE-SENSITIVE ELECTRICAL PARAMETER STUDY .....</b>	<b>96</b>
4.1. Theoretical Dynamic TSEP Analysis.....	100
4.1.1. Turn-on Miller Plateau Amplitude .....	100
4.1.2. Current Switching Rate .....	102
4.1.3. Voltage Switching Rate.....	104
4.1.4. Internal Gate Resistance and Gate Current .....	105

4.1.5. Turn-off Delay Time .....	109
4.1.6. Turn-on Delay Time .....	110
4.2. Design of the Testing Platform Enabling Thermal Dependence Characterization .....	112
4.3. Test Results and Comparison .....	114
4.3.1. Turn-on Miller Plateau Amplitude .....	114
4.3.2. Current Switching Rate .....	116
4.3.3. Voltage Switching Rate .....	119
4.3.4. Internal Gate Resistance and Gate Current .....	120
4.3.5. Turn-off Delay Time and Total Turn-off Time .....	123
4.3.6. Turn-on Delay Time and Total Turn-on Time .....	127
4.4. Summary for This Chapter .....	130
5. A GENERALIZED TOPOLOGY LEVERAGING WBG DEVICE ADVANTAGES .....	136
5.1. Circuit Structure and Operation Principle .....	137
5.2. Total Semiconductor Loss Index (TSLI) .....	144
5.3. Summary for This Chapter .....	150
6. SIC MOSFET DC-TO-DC CONVERTER WITH 100-KW POWER RATING .....	151
6.1. Topology Comparison .....	153
6.1.1. Semiconductor Loss Index Breakdown Analysis .....	156
6.1.2. TSLI as a Reflection of Different Output Power .....	158
6.1.3. TSLI as a Reflection of Switching Frequency .....	160
6.1.4. TSLI as a Reflection of Different Number of Cells for N-cell STC .....	160
6.2. Design of Devices and Passive Components .....	162
6.2.1. Design of Devices .....	162
6.2.2. Design of Heatsink .....	165
6.2.3. Design of Resonant Capacitor .....	165

6.2.4. Design of Resonant Inductor .....	169
6.2.5. Design of DC Capacitors .....	177
6.3. Simulation and Experiment Results .....	179
6.4. Thermal Performance Comparison Between One-cell and N-cell STC.....	188
6.5. Summary for This Chapter .....	191
7. GAN BASED STC WITH PARTIAL-POWER VOLTAGE REGULATION .....	192
7.1. Operation Principles of Proposed STC with Partial-Power Voltage Regulation .....	195
7.1.1. 1:6 STC as the Unregulated Stage.....	197
7.1.2. Buck Converter as the Voltage-Regulated Stage .....	199
7.2. Evaluation of the STC with Partial-Power Voltage Regulation.....	201
7.3. Power Loss Breakdown and Efficiency Estimation .....	207
7.4. Simulation Results.....	210
7.5. Prototype, Test Platform, and Experiment Results .....	211
7.6. Summary for This Chapter .....	214
8. GAN BASED MULTILEVEL BOOST INVERTERS DERIVED FROM STC .....	215
8.1. Research Background of Applying the STC-Derived Topologies into PV Inverters .....	215
8.2. Working Principle of the Resonant Multilevel Modular Boost Inverter with an Unfolder .....	218
8.3. Working Principle of the Differential-Mode Resonant Multilevel Modular Boost Inverter .....	221
8.4. Simulation, Analysis and Comparison .....	222
8.4.1. Simulation and Analysis.....	223
8.4.2. Actual Simulation, Prototype and Test Results.....	225
8.5. Summary for This Chapter .....	231
9. CONCLUSION AND RECOMMENDATION .....	233
REFERENCES .....	236

## LIST OF TABLES

<u>Table</u>	<u>Page</u>
1.1. Material Properties of Si, 4H-SiC, and GaN.....	2
2.1. Failure Locations, Causes, and Indicators of SiC MOSFETs.....	25
2.2. Comparison of Different Accelerated Lifetime Tests.....	27
2.3. Summary of Linear and Nonlinear Data-driven Models .....	37
2.4. Summary of SiC MOSFET Component-Level Lifetime Models .....	39
2.5. Comparison of Reliability Indexes Between Two System Structures .....	42
2.6. Summary of System-Level Lifetime Models.....	46
2.7. Summary of SiC MOSFET Electro-Thermal and Thermo-Mechanical Modeling .....	54
2.8. Summary of TSEPs of SiC MOSFETs .....	55
2.9. Summary of the Active Thermal Control Strategies.....	64
3.1. Comparison Among Three Investigated Indicators .....	93
4.1. Temperature Sensitivity Summary of the Investigated TSEPs.....	133
6.1. Comparison Among Prospective Capacitors .....	168
6.2. Steady-state Temperature at 50 kW Operation.....	184
7.1. Key Components of Designed 4-kW 1200-V Output Converter.....	208

## LIST OF FIGURES

<u>Figure</u>	<u>Page</u>
1.1. Specific on-resistance vs. blocking voltage of Si and wide band-gap semiconductors .....	1
1.2. Summary of Si, SiC, and GaN material properties .....	3
1.3. Application ranges in terms of the output power and switching frequency .....	3
1.4. Classification and statistical analysis of the referenced papers .....	4
1.5. Paper percentage in the four main categories of this reliability research .....	5
1.6. Amount of the included SiC MOSFET based papers by the year .....	6
2.1. Online and offline system lifetime modeling summary for power converters .....	13
2.2. An up-to-date typical SiC MOSFET chip-level structure.....	16
2.3. Mechanism of threshold voltage increase at continuous positive gate bias.....	19
2.4. SiC MOSFET package-level structure.....	21
2.5. Condition monitoring method classification.....	50
2.6. Two types of RC thermal networks .....	52
2.7. Typical 3-D thermal network.....	53
3.1. SiC MOSFET turn-on waveforms with Miller plateau region highlighted .....	75
3.2. SiC MOSFET Miller plateau shift with different ambient temperature .....	78
3.3. HEF acceleration test (a) circuit, (b) platform .....	79
3.4. Positive bias temperature stress test platform: (a) power supplies (b) thermal chamber.....	80
3.5. SiC MOSFETs under tests inside the thermal chamber.....	80
3.6. Double pulse test (a) circuit schematic, (b) platform, and (c) board .....	81
3.7. Miller plateau shift with different $V_{GS}$ stress after 100-hour duration .....	82
3.8. Miller plateau shift with the different duration of 40V $V_{GS}$ stress .....	83
3.9. Miller plateau shift with gate resistance after 100-hour 40-V $V_{GS}$ stress.....	84

3.10.	$V_{GS}$ of the normal MOSFET and those after positive bias temperature stress tests.....	84
3.11.	Threshold voltage measurement circuit .....	85
3.12.	Experimentally tested $V_{GS} - I_D$ curves of three normal SiC MOSFETs.....	86
3.13.	Tested $V_{GS} - I_D$ curves for devices with various $V_{GS}$ stress (a) amplitude (b) duration .....	86
3.14.	Threshold voltage shift with different $V_{GS}$ stress (a) amplitude and (b) duration.....	87
3.15.	Threshold voltage shift results after the positive bias temperature stress tests.....	88
3.16.	The voltage of turn-on gate resistor vs. $V_{GS}$ stress (a) amplitude (b) duration .....	90
3.17.	Gate resistor turn-on energy vs. $V_{GS}$ stress (a) amplitude, and (b) duration .....	91
3.18.	Turn-on gate resistor energy verification after the positive bias temperature stress.....	92
3.19.	Comprehensive comparison among the three investigated health indicators .....	94
4.1.	Four typical sources of stress for electronic equipment.....	96
4.2.	Ideal turn-on, turn-off transients to demonstrate the dynamic TSEPs.....	101
4.3.	Physics of Miller plateau amplitude temperature dependence .....	102
4.4.	Physics of current switching rate temperature dependence .....	103
4.5.	Physics of turn-off voltage switching rate temperature dependence .....	105
4.6.	Internal gate resistance vs. $T_j$ for SiC MOSFETs and Si IGBTs .....	106
4.7.	Gate charge equivalent circuit and simplified first-order form .....	107
4.8.	Physics of gate current peak temperature dependence .....	108
4.9.	Physics of gate current plateau temperature dependence .....	109
4.10.	Physics of turn-off delay time temperature dependence.....	110
4.11.	Physics of turn-on delay time temperature dependence .....	111
4.12.	The power stage schematic with parasitic parameters included .....	112
4.13.	The medium-voltage device temperature dependence characterization platform .....	113
4.14.	Turn-on waveforms of (a) $V_{GS}$ and (b) $V_{GE}$ .....	115
4.15.	Turn-on Miller plateau thermal dependence for SiC and Si devices .....	116

4.16.	Thermal coefficient of Miller plateau amplitude for SiC and Si devices .....	116
4.17.	Waveforms of the turn-on (a) $I_{DS}$ and (b) $I_{CE}$ .....	117
4.18.	Temperature dependent trend of the turn-on $dI_{DS}/dt$ and $dI_{CE}/dt$ .....	118
4.19.	Temperature coefficient comparison of turn-on $dI_{DS}/dt$ and $dI_{CE}/dt$ .....	118
4.20.	Turn-off waveforms of (a) $V_{DS}$ and (b) $V_{CE}$ .....	119
4.21.	Temperature dependent trend of turn-off $dV_{DS}/dt$ and $dV_{CE}/dt$ .....	120
4.22.	$I_{g(pk)_{off}}$ temperature dependence of (a) SiC MOSFET, (b) Si IGBT.....	121
4.23.	$I_{g(p)}$ temperature dependence of (a) SiC MOSFET, (b) Si IGBT .....	123
4.24.	Waveforms indicating turn-off delay of a) SiC MOSFET (b) Si IGBT .....	124
4.25.	SiC MOSFET, Si IGBT turn-off delay time at different $V_{DC}$ , $I_{DS} / I_{CE}$ ( $10 \Omega R_{g_{ext}}$ ).....	125
4.26.	(a) $t_{d_{off}}$ vs. dc voltage $V_{DC}$ , (b) $t_{d_{off}}$ vs. external gate resistance $R_{g_{ext}}$ .....	126
4.27.	Thermal coefficients of $t_{d_{off}}$ for SiC MOSFETs and Si IGBTs .....	126
4.28.	Temperature coefficient summary of the three TSEPs in the turn-off transient.....	127
4.29.	SiC MOSFET, Si IGBT turn-on delay time at different $V_{DC}$ and $I_{DS} / I_{CE}$ .....	128
4.30.	(a) $t_{d_{on}}$ vs. DC voltage $V_{DC}$ , (b) $t_{d_{on}}$ vs. external gate resistance $R_{g_{ext}}$ .....	128
4.31.	Temperature coefficients of the turn-on delay time.....	129
4.32.	Temperature coefficients of the three TSEPs in the turn-on transient.....	130
4.33.	Summary of the detection approaches for the investigated dynamic TSEPs.....	134
5.1.	Generalized $N$ -cell STC topology with voltage transfer ratio $1:(N+1)$ .....	138
5.2.	One-cell STC and equivalent circuits of the two switching modes .....	140
5.3.	Theoretical waveforms of the one-cell switched tank converter .....	140
5.4.	The 2-cell STC topology.....	141
5.5.	Two switching modes for the 2-cell STC .....	141
5.6.	Operation waveforms of the 2-cell STC .....	142
5.7.	Conventional and proposed STC topologies with 1:4 conversion ratio .....	143

5.8.	Specific on-resistance versus the breakdown voltage and junction temperature.....	146
6.1.	Total semiconductor loss index comparison.....	156
6.2.	Semiconductor loss index breakdown of (a) Boost converter, and (b) One-cell STC.....	158
6.3.	TSLI vs. total die area and output power for (a) boost converter and (b) one-cell STC.....	159
6.4.	TSLI vs. total die area, switching frequency for (a) boost converter, (b) one-cell STC.....	161
6.5.	TSLI as a function of total die area and number of cells for $N$ -cell STC.....	161
6.6.	Total MOSFET power loss comparison among different MOSFETs.....	163
6.7.	Thermal resistance circuit.....	164
6.8.	Thermal performance comparison among five 1200 V SiC modules.....	164
6.9.	Capacitance density per unit volume comparison.....	167
6.10.	Capacitor evaluation based on required inductance and total volume.....	168
6.11.	Voltage derating curves for HC and LC series capacitors.....	168
6.12.	(a) One-turn and multiple-turn winding. (b) AC busbar 3D model and assembly.....	171
6.13.	Core loss density comparison at 100 kHz frequency.....	172
6.14.	(a) E core dimensions. (b) Equivalent magnetic paths.....	173
6.15.	Core temperature rise and core volume trade-off.....	175
6.16.	The relationship between (a) flux density and core cross-section area. (b) core cross-section area and air gap length.....	176
6.17.	Investigation of DC capacitors from major manufacturers.....	178
6.18.	Trade-off between temperature rise and total volume for DC capacitors.....	178
6.19.	Simulation results at 300 V – 600 V with 100-kW output power.....	179
6.20.	The designed and assembled 100 kW one-cell STC.....	180
6.21.	The test platform schematic for the assembled 100-kW prototype.....	180
6.22.	300 V – 600 V test results at (a) 50 kW and (b) 100 kW.....	181

6.23.	Tested gate-source and drain-source waveforms .....	182
6.24.	Selected SiC module half bridge pin diagram and parameter measurement details .....	183
6.25.	Tested thermal performance at 50 kW continuous operation .....	183
6.26.	The tested baseplate temperature and calculated junction temperature .....	185
6.27.	Tested efficiency and power loss breakdown for the assembled prototype.....	185
6.28.	(a) DC busbar power loss vs. $P_o$ . (b) AC copper loss vs. $P_o$ .....	186
6.29.	Comparison between the theoretical and tested TSLIs.....	187
6.30.	TSLI in the designed prototype and optimized solution .....	188
6.31.	Resonant capacitor temperature rise vs. number of STC cells .....	189
6.32.	Core temperature rise vs. the number of the STC cells .....	190
6.33.	The relationship between junction temperature and the number of cells .....	190
7.1.	A typical high-power high-voltage power electronic system in an electric vehicle .....	192
7.2.	Differential power converters modeled as a controlled current source .....	193
7.3.	Generalized composite structure for regulated DC-to-DC converters.....	193
7.4.	Two typical composite structures for regulated DC-to-DC converters .....	194
7.5.	Two isolated forms of the unregulated stage .....	194
7.6.	Generalized STC integrated with partial-power processed voltage regulator .....	196
7.7.	STC integrated with a buck converter with 1 : (5+D) conversion ratio.....	198
7.8.	Two switching states of the proposed 1 : 6 STC .....	199
7.9.	Timing graph of the 1 : (5+D) regulated STC .....	200
7.10.	TSLI evaluation for the proposed STC with PPVR.....	203
7.11.	TSLI evaluation with different output power operation .....	204
7.12.	TSLI of boost converter and STC with PPVR under different switching frequency .....	205
7.13.	TSLI versus total die area with different conversion ratio .....	206
7.14.	Percentage of the power processed by buck converter versus conversion ratio .....	207

7.15.	Power loss breakdown of the STC with PPVR.....	208
7.16.	Power loss comparison of the STC and the partial-power voltage regulator .....	209
7.17.	Efficiency estimation of STC with PPVR .....	209
7.18.	Simulation results of 350-V-to-1200-V 4-kW STC with PPVR .....	211
7.19.	Tested prototype and control boards.....	212
7.20.	The 200 V – 1200 V 1 kW overall test platform .....	212
7.21.	The testing waveforms of 200-V-to-1200-V 1-kW STC.....	213
7.22.	The testing waveforms of 1:4.8 368-W STC with PPVR.....	213
8.1.	Three types of step-up transformerless PV inverter topologies.....	216
8.2.	Proposed resonant multilevel modular boost inverter with a full-bridge unfold.....	219
8.3.	Control logic of the resonant 8-level modular boost inverter with an unfold.....	220
8.4.	Control waveforms of the resonant 8-level modular boost inverter with an unfold .....	221
8.5.	Proposed differential-mode resonant multilevel boost inverter.....	222
8.6.	Control waveforms of the differential-mode resonant 8-level modular boost inverter .....	224
8.7.	Simulation results of the resonant 16-level modular boost inverter with an unfold .....	225
8.8.	Simulation results of the resonant 16-level differential-mode boost inverter.....	226
8.9.	The tested 6-level boost inverter prototype schematic .....	227
8.10.	Control signal waveforms in the simulation .....	227
8.11.	Current and voltage waveforms in the simulation with 35-V input voltage.....	229
8.12.	Overall perspective of the test platform .....	229
8.13.	Bird's-eye view of the test platform.....	230
8.14.	Tested control signals of the STC switches .....	230
8.15.	Tested current and voltage results.....	231

## LIST OF ABBREVIATIONS

AC	.....	alternate current.
ALT	.....	accelerated lifetime test.
BN	.....	Bayesian network.
CTBN	.....	continuous-time Bayesian network.
CTE	.....	coefficient of thermal expansion.
DBN	.....	dynamic Bayesian network.
DC	.....	direct current.
DCB	.....	direct copper bonding.
DFTA	.....	dynamic fault tree analysis.
DPWM	.....	discontinuous pulse width modulation.
DRBD	.....	dynamic reliability block diagram.
DTBN	.....	discrete-time Bayesian network.
DUT	.....	device under test.
EKF	.....	extended Kalman filter.
EMI	.....	electromagnetic interference.
ESR	.....	equivalent series resistance.
FCMC	.....	flying capacitor multilevel converter.
FTA	.....	fault tree analysis.
GaN	.....	gallium nitride.
HEF	.....	high electric field.
HTGB	.....	high temperature gate bias.
HTRB	.....	high temperature reverse bias.
IGBT	.....	insulated-gate bipolar transistor.
KF	.....	Kalman filter.

MC .....Markov chain.

MLCC .....multi-layer ceramic capacitor.

MOSFET.....metal-oxide-semiconductor field-effect transistor.

MTTF .....mean time to failure.

PC.....power cycling.

PF .....particle filter.

PoF .....physics-of-failure.

PPVR.....partial-power voltage regulation.

PV .....photovoltaic.

PWM.....pulse width modulation.

RBD .....reliability block diagram.

RMS .....root mean square.

RUL.....remaining useful lifetime.

Si .....silicon.

SiC.....silicon carbide.

STC .....switched tank converter.

TC .....temperature cycling.

TDDB.....time-dependent dielectric breakdown.

THD .....total harmonic distortion.

TS .....thermal shock.

TSEP .....temperature-sensitive electrical parameter.

TSLI .....total semiconductor loss index.

WBG .....wide band-gap.

ZCS .....zero current switching.

ZVS.....zero voltage switching.

## LIST OF SYMBOLS

$A_e$	.....	core cross-section area.
$B_{PK}$	.....	peak flux density.
$C_{DS}$	.....	drain-source capacitor / capacitance.
$C_{GD}$	.....	gate-drain capacitor / capacitance.
$C_{GS}$	.....	gate-source capacitor / capacitance.
$C_{iss}$	.....	intrinsic input capacitor / capacitance.
$C_{oss}$	.....	intrinsic output capacitor / capacitance.
$C_{OX}$	.....	oxide capacitor / capacitance.
$\delta$	.....	skin depth.
$dI_{CE}/dt$	.....	collector-emitter current switching rate.
$dI_{DS}/dt$	.....	drain-source current switching rate.
$dV_{CE}/dt$	.....	collector-emitter voltage switching rate.
$dV_{DS}/dt$	.....	drain-source voltage switching rate.
$\Delta B$	.....	flux density swing.
$\Delta \epsilon_p$	.....	plastic strain change in thermal cycles.
$\Delta T$	.....	temperature range in the entire thermal cycle.
$\Delta T_0$	.....	elastic temperature range.
$\Delta T_j$	.....	junction temperature swing.
$\Delta T_{on}$	.....	turn-on time duration.
$\epsilon_s$	.....	bond wire strain.
$\epsilon_p$	.....	bond wire plastic strain.
$E_a$	.....	activation energy.
$f_{sw}$	.....	switching frequency.
$I_d$	.....	drain-source current.

$I_{DSS}$ .....	drain leakage current.
$I_{G(p)}$ .....	gate current plateau.
$I_{G(pk)}$ .....	gate current peak.
$I_{GSS}$ .....	gate leakage current.
$k_b$ .....	Boltzmann's constant.
$l_g$ .....	air gap length.
$L_S$ .....	solder crack length.
$LT(V_{normal})$ .....	lifetime of components under normal use.
$LT(V_{stressed})$ .....	lifetime of components under voltage stress.
$\lambda_C$ .....	channel length modulation factor.
$\lambda_i$ .....	failure rate of the $i^{th}$ individual component.
$\lambda_{max}$ .....	maximum failure rate among all components.
$\Lambda$ .....	system failure rate.
$\mu_N^*$ .....	electron mobility.
$N_f$ .....	number of cycles to failure.
$P_{V(core)}$ .....	core loss density per volume.
$R_{DS\_ON}$ .....	drain-source on-state resistance.
$R_{g\_int}$ .....	internal gate resistance.
$R_{on}$ .....	body diode on-resistance.
$R_{th(j-c)}$ .....	junction-case thermal impedance.
$R(t)$ .....	system reliability.
$t_{d\_off}$ .....	turn-off delay time.
$t_{d\_on}$ .....	turn-on delay time.
$t_f$ .....	fall time.
$t_{off}$ .....	total turn-off time.

$t_{on}$ .....total turn-on time.  
 $t_r$  .....rise time.  
 $T_{GS(p)}$ .....gate-source voltage Miller plateau time duration.  
 $T_j$ .....junction temperature.  
 $T_{j\_max}$ .....maximum junction temperature.  
 $T_{j\_mean}$  .....average junction temperature.  
 $V_B$  .....blocking voltage.  
 $V_{CE}$ .....collector-emitter voltage.  
 $V_{CE\_ON}$ .....on-state collector-emitter voltage.  
 $V_{CE(p)}$ .....collector-emitter voltage Miller plateau amplitude.  
 $V_{core}$  .....core volume.  
 $V_{DS}$ .....drain-source voltage.  
 $V_{DS\_ON}$ .....on-state drain-source voltage.  
 $V_F$  .....body diode forward voltage.  
 $V_{GS}$ .....gate-source voltage.  
 $V_{GS(p)}$ .....gate-source voltage Miller plateau amplitude.  
 $V_{normal}$  .....normal voltage amplitude.  
 $V_{stressed}$  .....stressed voltage amplitude.  
 $V_{TH}$ .....threshold voltage.

## 1. INTRODUCTION AND MOTIVATION

Wide band-gap (WBG) semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have drawn extensive research efforts for the power conversion applications. Figure 1.1 presents the specific on-resistance (on-resistance times die area  $R_{DS\_ON} \cdot A_{die}$ ) versus blocking voltage  $V_B$  of the conventional silicon (Si) and six typical wide band-gap semiconductors [1]. As can be seen, at the same blocking voltage, wide band-gap semiconductors achieve much smaller on-resistance with the same die area. Correspondingly, the device conduction loss is smaller. It can also be concluded that it is more feasible for them to achieve compacter chip sizes with the same on-resistance. This further results in smaller intrinsic capacitances and lower stray inductances.

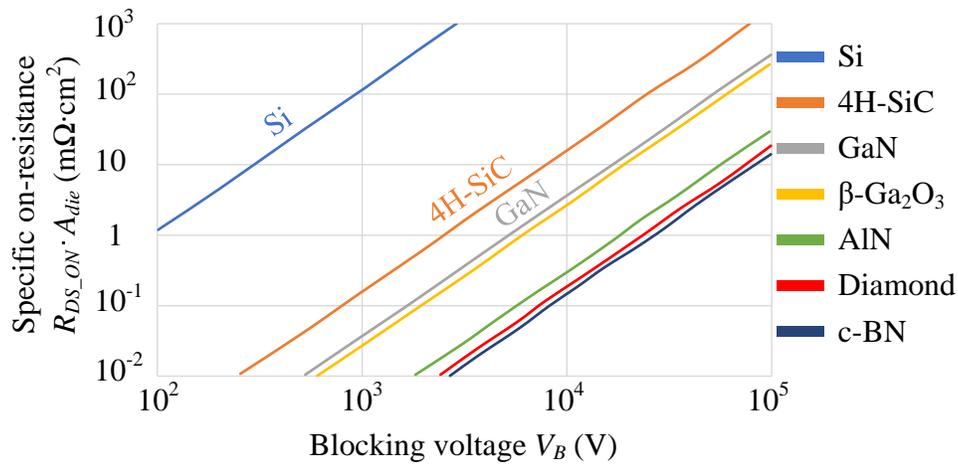


Figure 1.1. Specific on-resistance vs. blocking voltage of Si and wide band-gap semiconductors

Table 1.1 shows the material properties of silicon, 4H-SiC, and GaN. The peak saturated electron velocity [2] is an indicator of the operated switching frequency. When this parameter is larger, the switching frequency can be designed to be higher. So, the volume of the passive components would be decreased. Energy band gap [3] and electric field [3] for breakdown are two parameters to be correlated to the operated voltage capacity. Higher critical electric field enables

thinner, more highly doped voltage-blocking layers with smaller on-resistance [4]. Both the larger band gap and higher electric field for breakdown result in higher voltage rating. Besides, the melting point and the thermal conductivity [3][5] can be related to how high temperature these semiconductors can sustain.

Table 1.1. Material Properties of Si, 4H-SiC, and GaN

Substance	Si	4H-SiC	GaN
Peak saturated electron velocity ( $\times 10^7$ cm/s)	1	2	2.7
Energy band gap (eV)	1.12	3.25	3.44
Electric field for breakdown (MV/cm)	0.3	3.18	3.5
Melting point ( $\times 10^3$ K)	1.687	3.1	2.77315
Thermal conductivity ( $\times 10^2$ W/m-K)	1.3	7	1.1

To make the comparison more illustrative, Figure 1.2 further summarizes the major properties of the Si, 4H-SiC, and GaN semiconductors. As can be concluded from this figure, both the GaN and 4H-SiC can achieve much higher operated voltage capability. GaN enables the highest switching frequency, while Si exhibits the lowest frequency range. 4H-SiC demonstrates its much better thermal performance compared with other two semiconductors.

Figure 1.3 further shows the application ranges in terms of the output power and switching frequency for these three semiconductors. The Si semiconductor is normally used at relatively lower switching frequency range compared with the other two. Although it covers a wide range of the applications, there are some areas where it is not a preferred candidate. With the switching frequency required to be higher, GaN is a better choice because of their obviously lower output charge, gate charge, and reverse recovery charge. The corresponding applications include servers, telecoms, adapters, and wireless charging. Due to their inferior thermal performance in comparison with SiC, they are not desirable for the high-current, high-power applications. As the output power

becomes higher, SiC is preferred owing to their superior thermal performance and higher switching frequency capability.

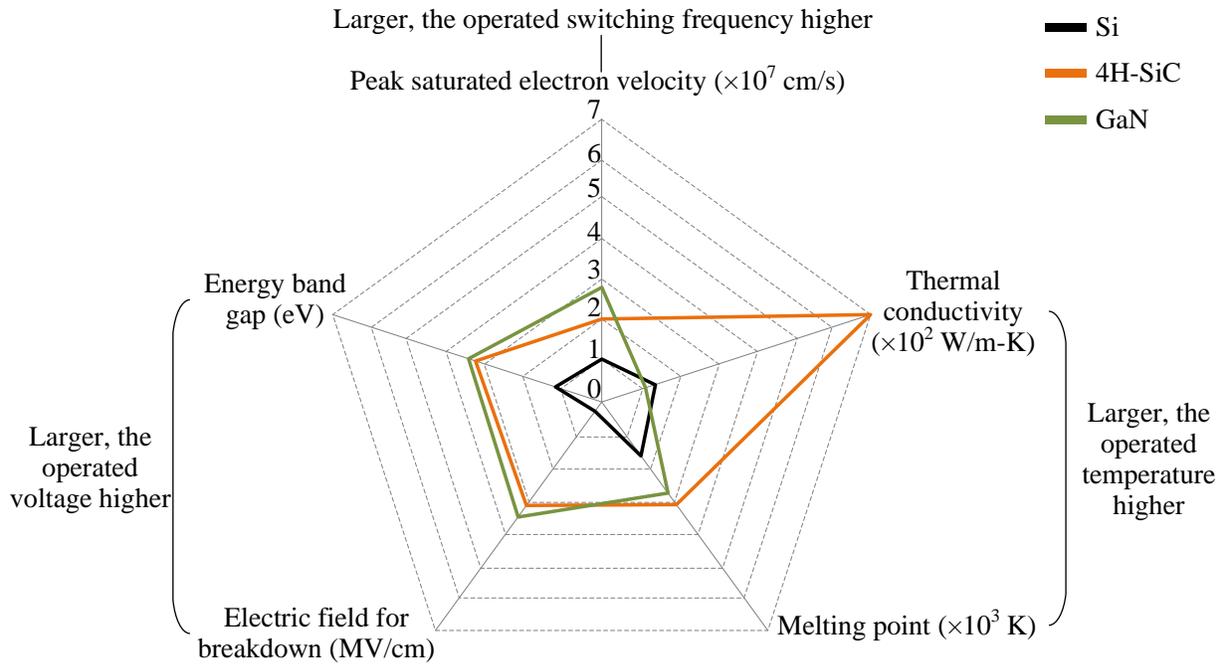


Figure 1.2. Summary of Si, SiC, and GaN material properties

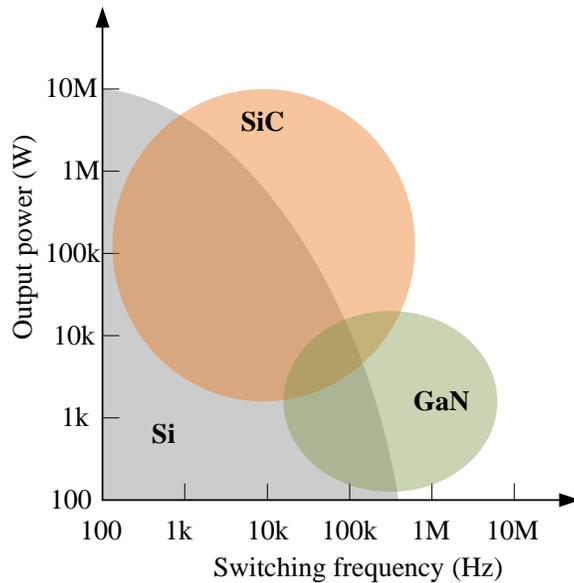


Figure 1.3. Application ranges in terms of the output power and switching frequency

But these emerging-semiconductor-based devices bring in the challenges in the reliability issues, since they have different physical failure mechanisms, compared with the conventional silicon devices. Also, the most suitable topologies need to be investigated to fully utilize their specific characteristics. These two concerns form the basic foundations of this dissertation.

In this research work, there will be two main parts to address the above mentioned challenges that accompanies the wide band-gap semiconductor devices. First, from the perspective of the reliability, the lifetime modeling and condition monitoring approaches should be studied based on the specific physical failure mechanisms and individual device characteristics. Second, in terms of the efficiency and power density in the energy conversion, the suitable topologies need to be proposed to leverage the advantages of these wide band-gap devices.

### 1.1. Research Background for the Reliability of Power Electronic Systems

To make the state-of-the-art lifetime research more illustrative, a statistical analysis has been made. Figure 1.4 shows the percentage of the papers in each investigated category. The papers

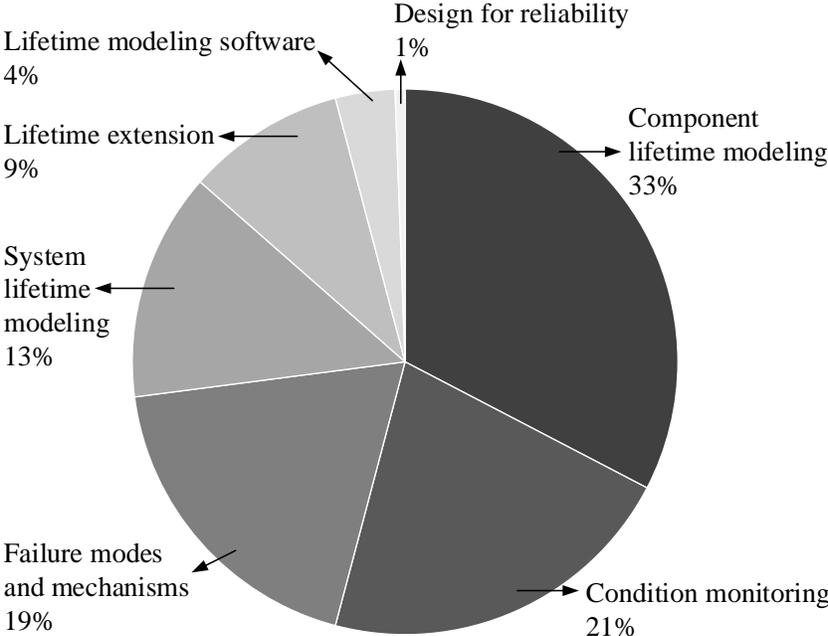


Figure 1.4. Classification and statistical analysis of the referenced papers

concerning the component lifetime modeling takes the largest proportion, which is 33% among all the categories. In areas of condition monitoring as well as failure modes and mechanisms, the percentage is 21% and 19%, respectively. Papers regarding the system lifetime modeling takes about 14%.

Figure 1.5 further classifies the four main categories into detailed sub-category percentage. Figure 1.5 (a) shows that in this overview, the papers regarding the physics-of-failure (PoF) models contribute most to the component lifetime modeling domain. From Figure 1.5 (b), in the

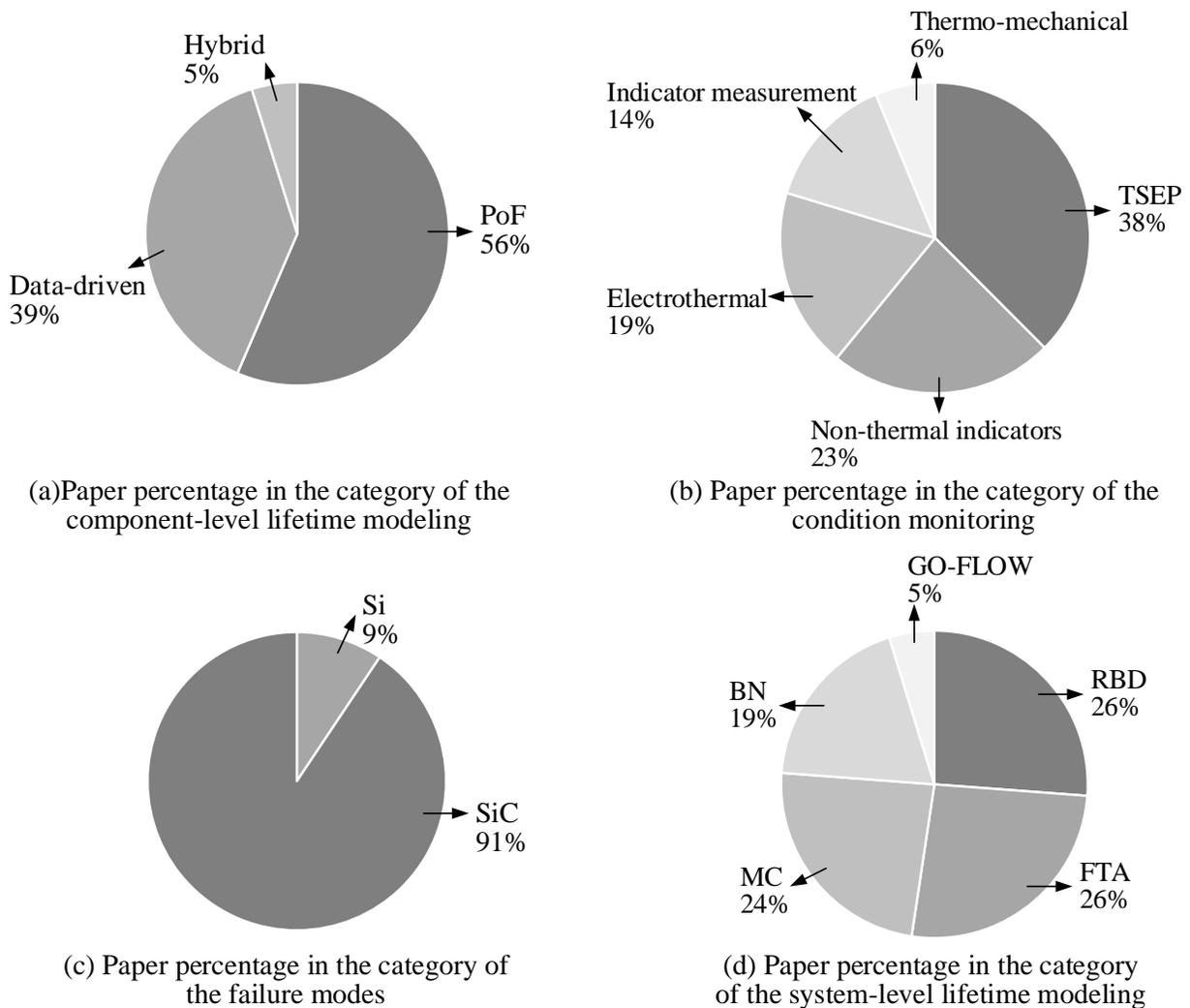


Figure 1.5. Paper percentage in the four main categories of this reliability research

condition monitoring area, about 38% and 23% of this research focuses on temperature-sensitive electrical parameters (TSEPs) and non-thermal indicators, respectively. Figure 1.5 (c) presents around 91% of the cited papers in the failure mode domain are related to the SiC MOSFETs. In Figure 1.5 (d), regarding the system lifetime modeling, the mostly cited papers are related to reliability block diagram (RBD), failure tree analysis (FTA) and Markov chain (MC).

Furthermore, from the literature review, the main reliability domains based on SiC MOSFETs, such as failure modes, accelerated lifetime tests (ALTs), PoF models, and TSEPs have not been investigated extensively compared with the Si counterparts. Therefore, Figure 1.6 lists the amount of the SiC MOSFET based papers included in this overview by the year. It shows an increasing trend of the number of SiC MOSFET based papers these years, especially in the areas of failure modes and TSEPs.

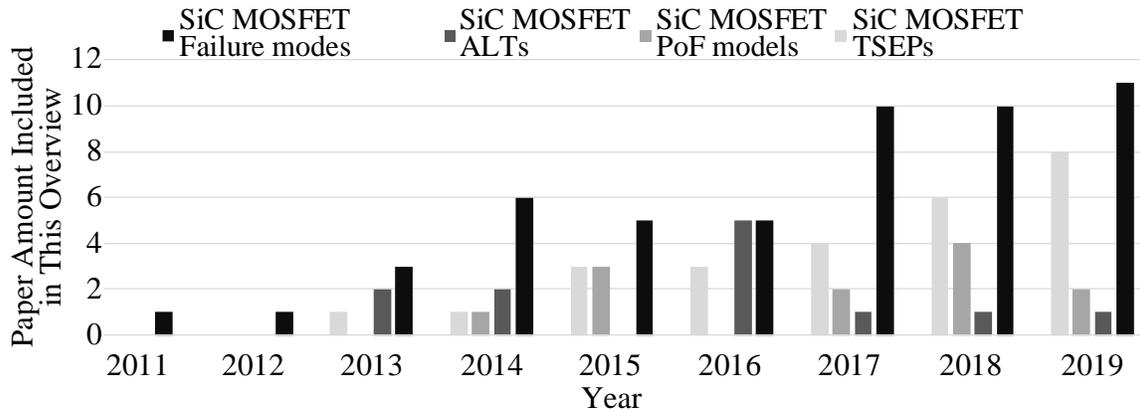


Figure 1.6. Amount of the included SiC MOSFET based papers by the year

## 1.2. The Impact of Wide Band-gap Devices on Topology

Based on the semiconductor property analysis at the beginning of this chapter, a further investigation of the impact of the WBG semiconductor on the topology is conducted. SiC MOSFET can achieve 40 ~ 100 times higher capability in terms of the blocking voltage times switching frequency in comparison with Si IGBT [6]. As a result, simple topologies are enabled

with SiC MOSFETs in medium- or high-voltage applications at high switching frequency. At low-voltage level, the low channel mobility in SiC MOSFET inversion channel requires higher electric field to realize smaller channel resistance. But the high electric field is undesirable for gate oxide reliability. Therefore, there exists a trade-off between the small on-resistance and reliable gate oxide. Due to these considerations, GaN heterojunction FETs (HFETs) are more superior in the low voltage ranges from 30 V to 600 V [7]. To leverage the benefits of currently available low-voltage-rating GaN devices with high switching frequency capability, the suitable topologies are needed to achieve high power conversion efficiency and high power density.

Therefore, below summarizes the wish list for the for the topologies fitted to WBG devices. First, they should enable low-voltage-rating GaN transistors to achieve high-voltage applications at high switching frequency. Second, they also need to enable high-current-rating SiC modules to achieve high-power application at high switching frequency. Third, the soft switching strategies need to be achieved. Fourth, they should enable the design of the high-efficiency and high-power-density passive components. Fifth, the compact heatsink design needs to be enabled, even at high-temperature operation. Sixth, they are supposed to enable voltage regulation at a wide input voltage range. Finally, high reliability needs to be realized by these topologies.

### **1.3. Structure of This Dissertation**

In the first part including Chapter 2 through Chapter 4, the dissertation will present a detailed investigation into the wide band-gap semiconductor device reliability. Above all, Chapter 2 will present the basic physics-of-failure mechanisms in these emerging devices at the beginning. The comparison with the silicon counterparts will be made. It will continue to propose the component-level and system-level lifetime modeling strategies. Consequently, a system-level lifetime extension discussion will be conducted. Secondly, based on the failure mechanism

analysis in the previous content, Chapter 3 will select one specific location in the SiC MOSFET to investigate the relationship between the internal ageing extent and the external electrical parameters. The gate oxide will be focused upon because it has been reported to be a relatively fragile location that is more susceptible to the gate-source voltage stress and temperature stress, compared with the counterpart in silicon devices. After exploring three health indicators, the Miller plateau will be recognized to be a potential parameter to indicate the gate oxide degradation extent. The findings in this project would provide helpful insight into the degradation monitoring and lifetime modeling in terms of both the component level and system level. Third, Chapter 4 will address the condition monitoring challenges through the junction temperature detection. Since the thermally relevant device failure takes a major percentage among all the failure causes, temperature measurement will be paid essential attention to. Multiple methods have been utilized to detect the temperature of the internal chip junction. The thermal modeling, external temperature-detection tool utilization, and negative-thermal-coefficient thermistor application have been well studied. But they bring in additional efforts in the computational resources, obviously extra costs, and manufacturing issues. Therefore, Chapter 4 will put much effort into the temperature-sensitive electrical parameters (TSEPs), which can be integrated into the gate drives. Most of these investigated parameters have well linked linear relationship with the junction temperature. The contributions in this project have been exploring the individual characteristics of the TSEPs in the medium-voltage, low-current devices. The presented work would be useful to the development of the junction monitoring circuits for the wide band-gap devices.

The other major part of this dissertation has been regarding the topological improvements that would leverage the advantages of the emerging wide band-gap devices. Chapter 5 serves as a transitional part to bring in a proposed generalized switched tank converter (STC) circuit topology

that would fully adapt the WBG devices to efficient and compact applications. Also, a novel evaluation index is analyzed, which will be utilized to compare different topologies in the following three chapters. In Chapter 6, based on this proposed topology, a 100-kW, 300-V-to-600-V DC-to-DC converter will be built by using the SiC MOSFET power modules. Chapter 7 will further investigate more capabilities of this generalized STC concept by utilizing the GaN devices. To achieve the voltage regulation efficiently, a buck converter will be included into the original structure. This project will be a good reference for the DC-to-DC power conversion stage in the electric vehicle applications. Other than the DC-to-DC applications, Chapter 8 will further explore the application boundaries of this proposed structure in the DC-to-AC inverters. Two novel multilevel inverter topologies will be disclosed based on the generalized switched tank cells. The simulation and testing results will be presented to emphasize their conspicuous advantages in power density and overall efficiency when the GaN devices are applied.

Finally, a conclusion will be drawn in Chapter 9. Also, the recommendations for future work will be presented for further investigation needs.

## 2. SiC POWER CONVERTER LIFETIME MODELING

Power converters are the key power processing components for many emerging applications including renewable energy generation and storage systems, electric or hybrid electric vehicle drives, solid-state transformers, more electric ships, and airplanes, etc. To reduce the total design and maintenance cost, guarantee the uninterrupted power delivery system operation and the human safety, two generalized approaches have been extensively studied. One is from the perspective of the design for reliability [8] through integrating the reliability and durability analysis into the design period. Most recent research in this area has adopted artificial intelligence methods such as artificial neural network to optimize the balance between design parameters and reliability indexes [9]. Another more widely researched method is regarding the accurate remaining useful lifetime (RUL) prediction of power converters, which can help prevent unwanted failures and generate better maintenance plans. This work will focus on the second one. The reliability and lifetime prediction of silicon (Si) semiconductor device based power converters have been commonly investigated [10]–[18]. Over the past decade, power converters based on silicon carbide (SiC) semiconductor devices such as SiC MOSFETs have demonstrated superior performance in terms of efficiency and power density [19]–[22]. Compared with Si devices, SiC MOSFETs feature higher withstand voltage, higher operating temperature, higher switching frequency, and smaller on-state resistance [23]–[26]. Nevertheless, SiC MOSFETs are facing new reliability challenges compared with Si devices [27][28]. Therefore, to design more reliable SiC power converters, an understanding of additional SiC MOSFET failure modes, lifetime prediction approaches, and online monitoring strategies is needed for real-time lifetime prediction.

SiC MOSFETs have the chip-level and package-level failure modes. The chip-level failure modes are mainly related to gate oxide and body diode. Compared with Si devices, the gate oxide

of SiC MOSFETs has a higher probability of time-dependent dielectric breakdown (TDDB) according to the following three aspects. First, higher electric field is normally used to achieve lower channel resistance. Second, higher temperature operation is preferred to shrink the cooling systems. Third, higher Fowler-Nordheim tunneling current exists due to smaller conduction band offset between SiC and SiO<sub>2</sub> [29]–[32].

The body diode failure of SiC MOSFETs is primarily caused by stacking faults. Most of the package-level failure modes appear at bond wires and solder layers. The bond wires between the SiC die and the direct copper bonding (DCB) are less reliable compared with those in Si-based devices, due to worse flexibility caused by about 10 times hardness of SiC material [33]. Besides, both the bond wires and solder layers in SiC devices are more possibly subjected to thermo-mechanical degradation caused by coefficient of thermal expansion (CTE) mismatch during commonly higher temperature operation. Therefore, the SiC MOSFET failure modes, mechanisms, and indicators are essential to developing the component-level lifetime models.

Traditionally, to generate a lifetime prediction, offline lifetime models are developed. These models need statistical methods like Monte Carlo analysis for the parameter estimation [10][11][13][14]. To verify the validity of the lifetime models, accelerated lifetime tests (ALTs) to stress certain failure modes should be performed [13][14][17]. The lifetime prediction of power converters could be investigated from the component level to the system level. The main components of power converters include active switches, capacitors, and inductors. The lifetime models of these components have been developed based on physics-of-failure, data-driven and hybrid methods. They are verified by ALTs [34]–[39]. Based on component-level lifetime models, the system-level lifetime models could be developed by reliability block diagram (RBD), failure tree analysis (FTA) and Markov chain (MC) [11]–[18][40]. However, the offline system lifetime

model accuracy is limited since it cannot be dynamically adjusted during the system operation. A more accurate real-time lifetime model with data updating features is needed through condition monitoring. How to combine the monitored degradation indicator information and the ALT-based statistical models is the major challenge.

The semiconductor device reliability has been reviewed systematically [41]. Failure mechanisms and lifetime prediction techniques have also been summarized in [42]. But these papers have not covered the RUL estimation modeling methods of the power converter systems. Besides, the RUL estimation models have been thoroughly analyzed in [43]–[45]. But they are presented in a generally statistical way. Therefore, it can be concluded that there is no dedicated overview on system-level RUL estimation and extension for SiC power converters.

This chapter intends to address these challenges and provide a comprehensive overview of the real-time lifetime prediction and extension strategies for SiC MOSFET based power converters. Figure 2. shows the organization of this overview. Due to the space limitation in this figure, only typical ageing indicators and online monitored parameters have been included. More health indicators will be explained further. As shown in this figure, lifetime modeling can be conducted either offline or online. By combining the static offline lifetime models with real-time data through online monitoring, it is possible to generate a more accurate real-time estimation method for RUL. This real-time SiC power converter lifetime prediction methodology could be explained in the following four steps.

#### 1) Health Indicator Monitoring and Calculation

Both the chip-level and the package-level failure indicators could be monitored online. By measuring these parameters, the lifetime models derived from the ALTs could be updated, and the corresponding real-time lifetime models could be developed. For example, the on-state device

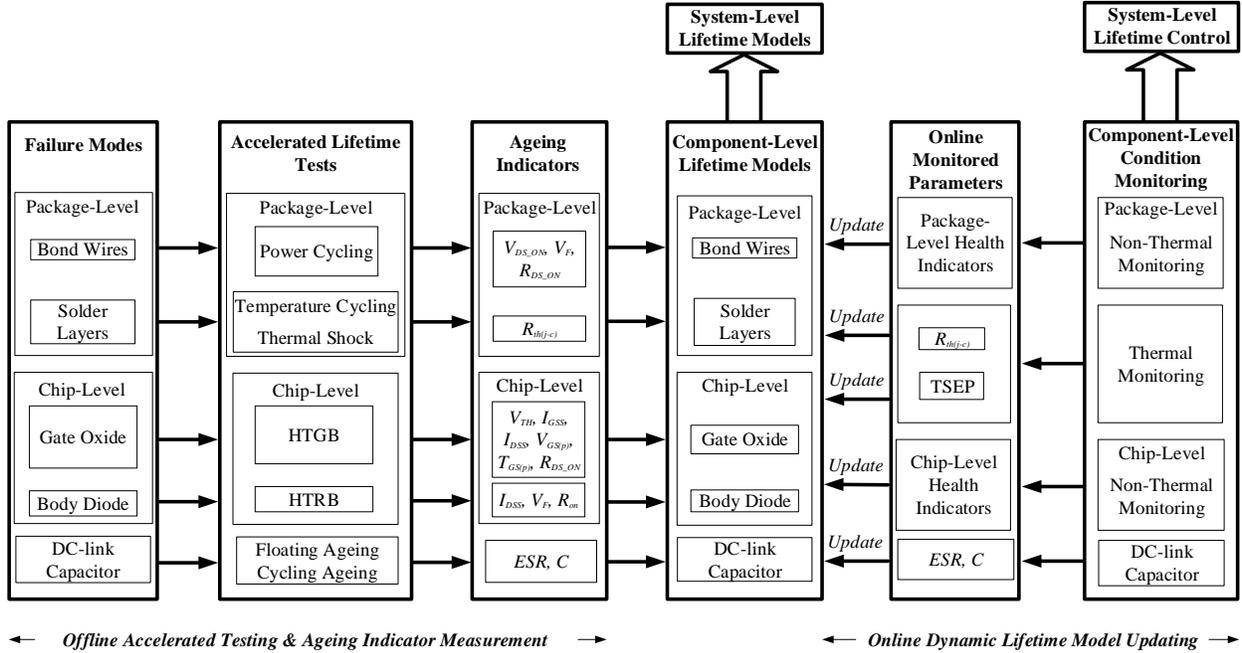


Figure 2.1. Online and offline system lifetime modeling summary for power converters

voltage has been measured in real time to reflect the package-level degradation such as the bond wire lift-off [46][47]. The Miller plateau amplitude has been measured to detect gate oxide ageing [48]. Equivalent series resistance (ESR) and capacitance have been monitored to tell the dc-link capacitor health condition [49]. Section 2.1 will be dedicated to more detailed health indicators.

To estimate the model parameters in the lifetime models of each component, algorithms such as the Kalman filter (KF), the extended Kalman filter (EKF), and the particle filter (PF) could be used. Section 2.2 will analyze more in this modeling part.

## 2) Component Health Indicator Integration

Since a component could have more than one health indicator, an integration should be conducted for each component. In this procedure, all the monitored health indicators of each component are integrated to reflect the health condition for this specific component. For example,

eleven health indicators have been collected and processed through principal component analysis to detect unsupervised degradation in the SiC MOSFETs [50].

### 3) Component Interdependence Consideration

Different failure indicators can be the cause and result of each other. For instance, the negative bias temperature stress results in negative shift of  $V_{TH}$ , which induces the increase of  $I_{DSS}$  [51]. Besides, when solder fatigue happens, the thermal impedance increases, which causes  $T_j$  to rise. This in turn results in an increase of  $V_{DS\_ON}$ , which indicates another failure mode – bond wire lift-off. Likewise, bond wire lift-off induces uneven current distribution, which generates higher power loss and corresponding higher junction temperature. As a result, more thermal stress is put onto the solder layers [52]. Thus, the failure mode interdependence among different components in the system should be included in this procedure.

### 4) System-Level RUL Prediction

Based on the widely investigated system-level lifetime modeling techniques, the SiC power converter system-level lifetime modeling can be further made, and the lifetime prediction can be conducted in real time more accurately. Further details in this part will be presented in Section 2.3.

The online monitored data could be further used for active lifetime extension. A tradeoff between reliability improvement and system performance has to be cautiously considered [53]–[56]. Section 2.5 will summarize these techniques.

This chapter will be organized as follows. Section 2.1 reviews the failure modes, mechanisms of SiC MOSFETs, and the corresponding aging indicators. Section 2.2 first covers the ALTs relevant to the presented specific indicators. Component-level static RUL models are then presented. The cycle counting and fatigue damage accumulation approaches are also analyzed as necessary procedures of deriving lifetime models. Section 2.3 summarizes system-level static

lifetime modeling, and also lists the component-level and system-level lifetime modeling software. Section 2.4 gives a comprehensive analysis of the SiC power converter real-time condition monitoring methods and the corresponding parameters. These online measured parameters could be utilized to make the models more accurate through dynamically updating the initial system-level models. Section 2.5 reviews the system-level lifetime extension strategies to actively improve the RUL. Finally, Section 2.6 provides the conclusion and recommendations for future research opportunities in the area of the SiC power converter lifetime prediction and extension.

### **2.1. SiC MOSFET Failure Modes and Mechanisms**

To derive the lifetime models, the failure modes, and mechanisms of SiC MOSFETs should be investigated first. This physical understanding would lay the foundation for identifying the indicators of various failure modes. Furthermore, the failure criteria could be developed based on these indicators.

The frequently encountered failure modes of SiC MOSFETs are located at the gate oxide, body diode, bond wire, chip-substrate solder layer, and substrate-baseplate solder layer [57]. Among them, the gate oxide and the body diode are considered to be chip-level, while the bond wire, chip solder-substrate layer, and substrate-baseplate solder layer are considered as package-level. These chip-level and package-level failure modes are challenging to be monitored directly due to their inaccessible locations. In the following paragraphs, these two groups of failure modes and mechanisms as well as the corresponding indicators will be summarized.

#### **2.1.1. Chip-Level Failure Modes of SiC MOSFETs**

Figure 2.2 shows an up-to-date typical chip-level SiC MOSFET trench structure [58] with low on-state resistance and improved gate oxide reliability especially at the bottom of the gate

trench [59][60]. The most common chip-level failure modes of SiC MOSFETs occur at the gate oxide and body diode.

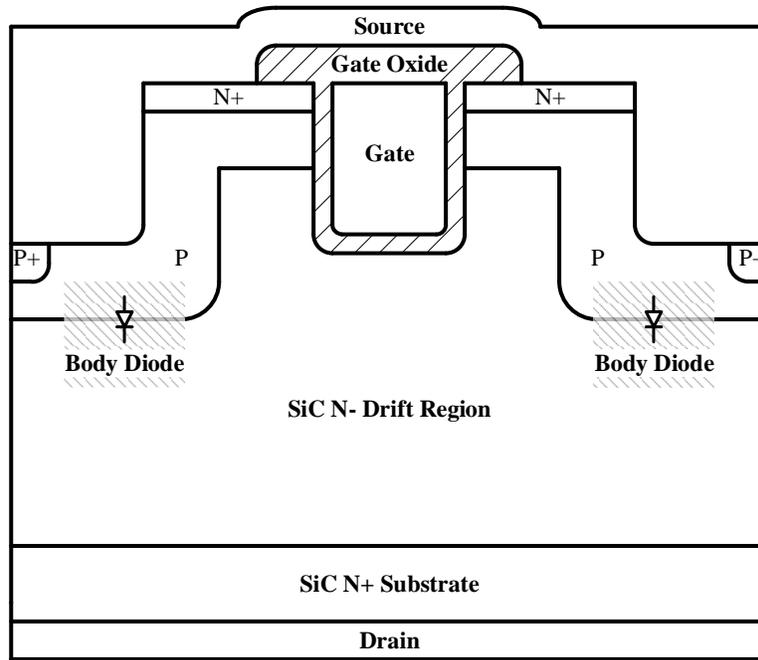


Figure 2.2. An up-to-date typical SiC MOSFET chip-level structure

Gate oxide degradation failure is basically caused by the tunneling current into the gate oxide layer [61]. Two stresses contribute to the gate oxide degradation, i.e. high electric field stress and high temperature stress. Compared with Si devices, three aspects have counteracted the gate oxide reliability of SiC MOSFETs, as shown in the following.

- (1) SiC MOSFETs have lower inversion channel mobility [30]. As a result, higher electric field is needed to realize smaller channel resistance. So, a tradeoff exists between smaller on-state resistance and better gate oxide reliability.
- (2) Higher interface state density occurs at SiC-SiO<sub>2</sub> interface [30][62], which brings in lower barrier height. Thus, more mobile hot carriers are injected from doped SiC to oxide.

Therefore, it is more likely for the carrier non-equilibrium to induce the gate oxide dislocation.

- (3) Smaller conduction band offset between SiC and SiO<sub>2</sub> [31] introduces higher Fowler-Nordheim tunneling current at similar gate electric field and temperature. Hence, there is higher probability of TDDB. In sum, the more possibly degraded gate oxide in SiC MOSFETs would further lead to the failures such as short circuit [63].

The intrinsic body diode failure is normally due to the recombination-induced stacking fault mechanism [64]. The forward voltage bias stress has been reported to be the primary cause of the body diode degradation [23][64][65].

#### **2.1.1.1. Gate Oxide**

There are two main failure mechanisms for SiC MOSFET gate oxide. One is the TDDB, which is caused by high temperature and high electric field stress [31]. Compared with Si counterparts, SiC MOSFETs are more often applied with higher  $V_{GS}$  and higher temperature to achieve lower on-state resistance and smaller heatsink. This would make the gate oxide more vulnerable [66]. The other is the avalanche breakdown, which is caused by high electric field stress [66][67]. The most extensively studied indicators of gate oxide degradation include Miller plateau voltage amplitude [68][69], Miller plateau time duration [69], drain leakage current [70], threshold voltage [51], gate leakage current [70], and on-state resistance [69].

- (1) Miller plateau voltage amplitude  $V_{GS(p)}$  increases with the  $V_{GS}$  stress and is identified as a more obvious indicator than threshold voltage  $V_{TH}$  for Si MOSFET gate oxide degradation [68]. In SiC MOSFETs,  $V_{GS(p)}$  is verified to be an indicator of gate oxide degradation by high electric field stress test and positive bias temperature stress test [71]. As shown in (Eq.2.1), with higher electric field stress, the  $\mu_N^*$  decrease caused by electron scattering

[72] and the  $V_{TH}$  increase caused by the electrons confined to the SiC-SiO<sub>2</sub> interface [73] will lift up  $V_{GS(p)}$ . The second stress of the miller plateau shift is caused by the temperature dependence of  $V_{TH}$  and electron mobility [66].

$$V_{GS(p)} = \sqrt{\frac{2 \cdot I_{DS} \cdot L_{Gate}}{\mu_N^* \cdot C_{OX} \cdot W_{Gate} \cdot (1 + \lambda_C \cdot V_{DS})}} + V_{TH} \quad (\text{Eq.2.1})$$

where  $\mu_N^*$  is the electron mobility.  $C_{OX}$  is the oxide capacitance.  $W_{Gate}$  is the gate width.  $L_{Gate}$  is the gate length.  $\lambda_C$  is the channel length modulation factor.

- (2) Miller plateau time duration  $T_{GS(p)}$  has been shown to have a larger positive shift in Si MOSFETs compared with  $V_{GS(p)}$  and  $V_{TH}$  under the high electric field test [69].
- (3) Both the drain leakage current  $I_{DSS}$  and threshold voltage  $V_{TH}$  tend to increase with stress time under the high temperature gate bias (HTGB) test [51][70][74]. The change of  $I_{DSS}$  and threshold voltage  $V_{TH}$  fundamentally appears together due to the same shift mechanism [75]. Their shift is mainly caused by high electric field stress and high temperature stress [51][76]–[78]. When a continuous positive gate-source voltage is applied, the electrons close to the conduction band edge are attracted to the gate oxide area and gradually trapped at SiC-SiO<sub>2</sub> interface [66]. This phenomenon can be seen clearly in Figure 2.3. As a result, a negative bias is formed between gate and source. Therefore, a higher  $V_{TH}$  is needed to have the drain current flowing through the device. This results in an increase in  $V_{TH}$ . Contrarily, with a continuous negative  $V_{GS}$ , the holes are trapped at the SiC-SiO<sub>2</sub> interface, which causes  $V_{TH}$  to decrease [79]. This  $V_{TH}$  instability issue is mainly caused by the active charge traps in the near-interfacial region in the gate oxide [80]. Besides, due to a larger portion of the capture and emission in the holes and electrons, the  $V_{TH}$  hysteresis effect has been measured and verified to be more obvious in SiC MOSFETs compared with Si counterparts [81].

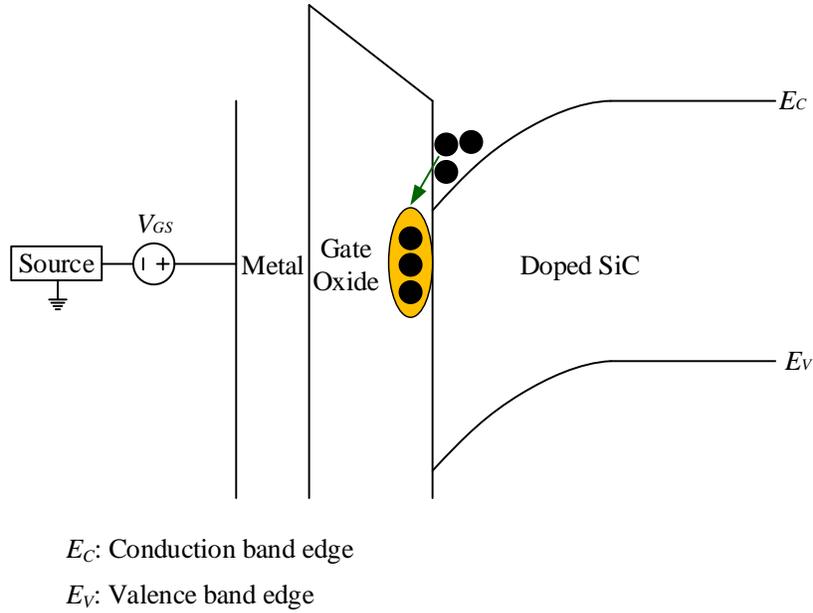


Figure 2.3. Mechanism of threshold voltage increase at continuous positive gate bias

- (4) Gate leakage current  $I_{GSS}$  increases with stress time under the high temperature reverse bias (HTRB) test [70]. Under the operating condition of the high electric field and high temperature, the localized heat stresses the polycrystalline silicon gate metal. As a result, the voids are formed and cracks appear in the gate metal, through which  $I_{GSS}$  flows between the source and gate. Thus,  $I_{GSS}$  could be an indicator of SiC MOSFETs gate oxide breakdown. Since SiC MOSFETs have thinner gate oxide layer compared with Si counterparts for the sake of a desirably lower  $V_{TH}$  value [82], they are more easily affected by large variations of  $V_{DS}$  and  $T_j$ . So, there is higher probability to induce larger  $I_{GSS}$  for SiC MOSFETs [74].
- (5) On-state resistance  $R_{DS\_ON}$  is an indicator for Si MOSFET gate oxide degradation [69][74][83][84], although it has been mostly used to indicate the package-related failures. SiC  $R_{DS\_ON}$  mainly consists of the channel resistance due to mobile carriers, the resistance in the  $N^+$  source layer, the resistance in source and drain electrodes, and the resistance in

the  $N^-$  drift region between two adjacent wells of P-type semiconductor [85]. Higher electric field stress increases the oxide charge density and further enlarges the overall  $R_{DS\_ON}$ . So,  $R_{DS\_ON}$  could indicate the SiC MOSFET gate oxide degradation.

#### **2.1.1.2. Body Diode**

Formed by the  $N^-$  drift region and the well of P-type semiconductor, the SiC MOSFET body diode degradation is caused by the forward voltage bias stress [23][64][65] owing to the stacking fault mechanism [64][86]. The continuous forward current flowing through SiC MOSFET P-N junction results in accumulated hole-electron recombination energy [23][65], which forms the stacking fault extended at the body diode. Since the forward current pathway is blocked by these faults, both the on-resistance and forward voltage of the body diode would rise [87]. The larger body diode on-resistance brings in the thermal design challenges. The increase of forward voltage drop could degrade the blocking voltage. Therefore, in the topologies with current commutation occurring at the body diode, such as full bridge inverters, these stacking faults play a significant role in reducing the system lifetime.

Three indicators of the body diode degradation have been the body diode on-resistance  $R_{on}$  [23], forward voltage  $V_F$  [88], and drain leakage current  $I_{DSS}$  [66]. They are fundamentally attributed to the high-density basal plane dislocation in the lightly doped  $N^-$  drift layer [64][89].  $V_F$  of body diode has been demonstrated to be influenced by the forward stress duration [64][65][89] based on the ALT results.  $I_{DSS}$  has been shown to increase with the forward stress duration as well [64].

#### **2.1.2. Package-Level Failure Modes of SiC MOSFETs**

From the perspective of package-level failure modes, most literature focuses on Si IGBT modules. SiC MOSFET package-level failure modes have not been well studied. Figure 2.4 shows

one typical SiC MOSFET power module package with bond wires. It is mainly composed of three parts, i.e. the SiC chip die, the direct copper bonding (DCB), and the baseplate. DCB is composed of two layers of substrate conductors and a substrate insulator layer in between. The substrate conductor is usually made of copper. Substrate insulator could be made of ceramics by using  $\text{Al}_2\text{O}_3$ ,  $\text{AlN}$  or  $\text{Si}_3\text{N}_4$  [90]–[92]. Bond wires connect the SiC die and the DCB. The chip die and the DCB, as well as the baseplate and the DCB, are commonly attached by solder. The baseplate could be made of copper or  $\text{AlSiC}$  [91][92].

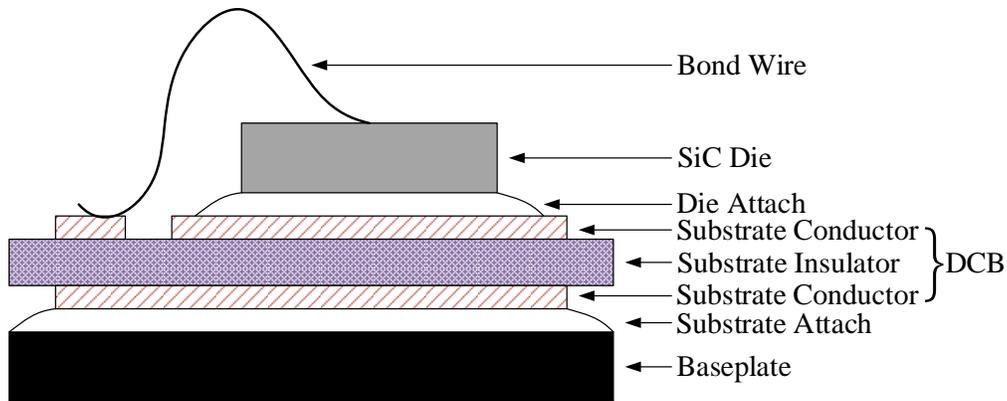


Figure 2.4. SiC MOSFET package-level structure

Compared with that of the Si counterparts, the package-level reliability of the SiC MOSFETs is not so promising. It will be analyzed in detail from three perspectives regarding the semiconductor fabrication, mechanical and material properties.

- (1) From the semiconductor fabrication perspective, SiC based dies have smaller active die areas compared with Si based ones assuming the same current rating [93]. It means that SiC dies have higher current density than Si ones. As a result, the electromigration would be more likely to occur in SiC devices [94]. Hence, there is higher probability for the electromigration to generate more internal voids inside the bond wires [94]. These voids would increase the imbalanced current density among the bond wires and strengthen the

unequal self-heating effect [95]. The electromigration could also generate more solder voids and induce worse interconnect failures [96]. In summary, at the same temperature and the same current rating, higher current density in SiC devices induces higher probability of degradation at both bond wires and solder layers. One way of alleviating this issue is to have more bond wires in parallel, thereby relieving stresses caused by high current density [94].

(2) From the mechanical property perspective, SiC is stiffer and has much larger Young's Modulus than Si [97]. It would bring in higher stress on the interface between the SiC die attached solder and the substrate conductor during power cycling. Larger Young's Modulus would also result in more significant accumulated creep strain and creep energy concentration on the interface between SiC die solder and the substrate conductor at the same junction temperature [98]. Correspondingly, for SiC MOSFETs, the crack initiation would be more likely to occur on the interface between the SiC die solder and substrate conductor compared with Si counterparts.

(3) From the material property perspective, SiC has higher thermal conductivity than Si. Correspondingly, the larger temperature variation has been reported in SiC devices compared to Si ones at the same current [93][99]. This higher temperature swing could increase the stress on the interface between SiC die solder and substrate conductor.

The detailed package-level failure will be discussed further as follows. Bond wires and solder layers are the two mostly studied package-level failure locations of SiC MOSFET modules [100]. Package-level failures are mainly caused by three stresses. First, thermo-mechanical stress is induced by the CTE mismatch among different materials. The resulted temperature swing results in solder fatigue, crack growth, and bond wire failures [52][101]–[103]. Second, relative humidity

stress intensifies the effects of mechanical stresses, which reduces the metal atom bonding energy. Thus, the atom corrosion increases the crack growth rate at the tail of the bond wire [104]. Third, high current density stress caused by the relatively small SiC die size could accelerate electromigration related degradation [94][104].

#### **2.1.2.1. Bond Wires**

Two types of failure mechanisms have been identified in the bond wires [105]. One is the bond wire fracture at the interface between bond wire and DCB upper surface. The other one is the bond wire lift-off at the interface between bond wire and SiC die. The bond wire fracture is caused by its alternate heating and cooling [50][106]. The temperature cycling leads to repeated expansion and contraction on bond wires. When the thermo-mechanical deformation is accumulated to a certain extent, the cracks would occur. As a result, the fracture is identified at the bond wire tail interfaced with the DCB upper surface. The other type of failure is the bond wire lift-off caused by the CTE mismatch between the bond wire copper and SiC, as well as ohmic self-heating effects [94]. The thermo-mechanical stress changes the surface structure through the chip metallization [107]. When the chip surface structure change is accumulated to separate bond wires from the SiC die, the bond wire lift-off occurs. Furthermore, due to the parasitic resistance and high SiC current density, the internal voids and cracks would also gradually induce the bond wire lift-off [94].

Bond wire fracture happens more slowly than its lift-off [108]. Thus, the bond wire lift-off has been investigated more extensively. Five indicators have been studied for the bond wire lift-off as shown in the following. First, the on-state voltage has been identified to indicate bond wire lift-off as thermal cycles accumulate [109][110]. Second, the SiC MOSFET on-state resistance  $R_{DS\_ON}$  increases with the thermal cycles [111]. Third, the voltage between the kelvin-source and

power-source has been used to reflect the online SiC MOSFET bond wire lift-off [112]. Fourth, the bond wire resistance increases when SiC MOSFET bond wire lift-off deteriorates [94]. Fifth, the eddy current in bond wires generated by pulsed electromagnetic induction heating has been used as an indicator of the IGBT bond wire lift-off [95], which could be employed to monitor SiC MOSFETs in the induction heating related applications.

#### **2.1.2.2. Solder Layers**

Solder layers include the die attach between SiC die and DCB as well as substrate attach connecting DCB and baseplate [57][113]. Due to the CTE mismatches between the SiC and solder material, between the DCB upper layer copper and solder material, shear stress gradually generates the cracks and voids in the solder layer [114]. These cracks and voids reduce the effective heat conduction area between the die and DCB copper. As a result, the thermal resistance of the chip die-to-DCB solder increases, which leads the die-attach temperature to rise. As the voids grow, this localized die-attach heating process accelerates the chip damage [115]–[117]. Two indicators have been studied in the SiC MOSFET solder layer degradation. First, the junction-case thermal impedance has been shown to increase with the degradation of die-DCB solder layer [118], substrate-baseplate solder layer [109] in the Si IGBTs and SiC MOSFETs [119]. Second, the solder layer resistance has been verified to be related to the SiC MOSFET solder fatigue [113]. As analyzed in the chip-level failure modes,  $V_{TH}$  shifts as SiC gate oxide degrades. To exclude this degradation from solder fatigue evaluation, the body diode could be utilized to conduct the load current. With this approach, the die-attach solder layer resistance increase is not associated with SiC die degradation.

### 2.1.3. Summary of Failure Modes of SiC MOSFETs

The typical failure locations, causes, and indicators of SiC MOSFETs are summarized in Table 2.1. Failure locations show where the corresponding failure modes occur. Two chip-level and two package-level failure modes are summarized. Failure causes list the stresses of different failure modes. Indicators are the external electrical parameters reflecting the corresponding internal failure modes. The indicators are identified to determine the number of cycles to failure in ALTs when the indicator values reach to the defined failure criteria [120].

Table 2.1. Failure Locations, Causes, and Indicators of SiC MOSFETs

Failure location	Failure Cause	Failure Indicator
Gate oxide	High electric field, high temperature	Gate leakage current $I_{GSS}$ [70][82]
		Threshold voltage shift $\Delta V_{TH}$ [51][76]–[78][122][123]
		Drain leakage current $I_{DSS}$ [122][121]
		Miller Plateau $V_{GS(p)}$ [71]
Body diode	Forward bias [64][65][89]	Drain leakage current $I_{DSS}$ [66]
		Body diode forward voltage $V_F$ [88]
Bond wires	Thermo-mechanical stresses	On-state drain-source voltage $V_{DS\_ON}$ [110]
		Drain-source on-state resistance $R_{DS\_ON}$ [111]
		Voltage between Kelvin, power sources [112]
		Bond wire resistance [94]
Solder layers		Thermal resistance $R_{th(j-c)}$ [119]
		Solder layer resistance [113]

For the gate oxide failure, the two causes are related to high electric field and high temperature. Higher electric field results in more localized heat, which generates more polycrystalline silicon voids between the gate and source [70]. As a result, the gate leakage current  $I_{GSS}$  [70][82] would increase. Double the nominal value of  $I_{GSS}$  has been used as a gate oxide degradation criterion [70]. Higher electric field and temperature stresses also result in more charge trapping at the SiC-SiO<sub>2</sub> interface [121]. It leads to the increase of both the threshold voltage shift

$\Delta V_{TH}$  [51][76]–[78][122][123] and drain leakage current  $I_{DSS}$  [122][121]. The 20% higher than the initial  $V_{TH}$  [122], or 5 times the initial  $I_{DSS}$  [121] have been applied as the failure criterion. Higher electric field and temperature stresses also lead to the increase of both the fixed charge of the gate oxide and the charge in interface states, which uplifts the  $V_{GS(p)}$  [68][69].

For the body diode failure, the forward bias is the main stress. It induces expansion of basal plane dislocations in the SiC epitaxial layer [64][65][89], which further causes forward voltage  $V_F$  and drain leakage current  $I_{DSS}$  to increase. Thus, the body diode  $V_F$  [88] and  $I_{DSS}$  [66] have been used as indicators.

For the bond wire and solder layer failures, the thermo-mechanical stresses are the main contributors to the failure. It causes high junction temperature in bond wires, which further leads to the increase of on-state parameters  $V_{DS\_ON}$  and  $R_{DS\_ON}$ . Thermo-mechanical stresses also cause crack propagation in the solder, which increases thermal impedance  $R_{th(j-c)}$ . Thus,  $R_{th(j-c)}$  could be used as an indicator of the solder layer failures [120].

## **2.2. Offline Component-Level Lifetime Modeling**

To obtain the component-level lifetime models, it is necessary to conduct the accelerated lifetime tests (ALTs) first. Then, the component-level SiC MOSFET lifetime estimation models are extrapolated using the information obtained from the ALTs. To analyze the irregular thermal cycles in ALT results, cycle counting techniques are applied. After that, the fatigue accumulation approaches need to be used to consider the accumulative stress effect based on the mission profiles.

### **2.2.1. SiC MOSFET Accelerated Lifetime Tests and Indicators**

To acquire reliability and lifetime data efficiently, ALTs are commonly adopted. In SiC MOSFET based ALTs, gate oxide, solder layer, and bond wire have been subjected to higher-than-normal accelerated temperature stress and voltage stress. The test results are further applied to

lifetime prediction at normal use conditions. The widely-used reliability test methods for SiC MOSFETs are high temperature gate bias (HTGB) [124][125], high temperature reverse bias (HTRB) [124][125], power cycling (PC) [111][126][127], temperature cycling (TC) [128] and thermal shock (TS) [106]. Their test conditions, locations, and failure indicators are summarized in Table 2.2.

Table 2.2. Comparison of Different Accelerated Lifetime Tests

Test	Test condition		Test location	Failure indicator
HTGB	$V_{GS}$ stressed to maximum voltage at maximum $T_j$		Gate oxide	$I_{GSS}$
				$V_{TH}$
HTRB	$V_{DS}$ reversely biased to the maximum voltage at maximum $T_j$		Edge channel structure and solid-state junction surface	$I_{DSS}$
PC	The device is heated and cooled by pulses		Bond wire	$V_{DS\_ON} / V_F$
				$V_{TH}$
				$R_{DS\_ON}$
				$I_{GSS}$
	$C_{DS}$			
TC	External heat and cooling	Short cycle time	Solder joint, bond wire	$R_{DS\_ON}$
TS		Long cycle time	Interface between DCB and baseplate	$R_{th(j-c)}$

(1) HTGB test is designed to detect the gate oxide degradation caused by the random oxide defects and the ionic oxide contamination [124][129]. In this test, the gate oxide is subjected to the maximum positive or negative  $V_{GS}$  stress at the maximum operating junction temperature  $T_{j\_max}$  for a long enough period, such as 1000 hours [130]. The drain and source are shorted. Gate leakage current  $I_{GSS}$  [106], threshold voltage  $V_{TH}$  [124][125][131] have been used for indicating the gate oxide degradation. The HTGB test is regarded to be passed when  $I_{GSS}$  or  $V_{TH}$  shift is within twice the initial value [124]. Considering the bias temperature instability in SiC MOSFETs, the  $V_{TH}$  shift occurs due to

the device self-heating in the HTGB test. By measuring the body diode forward voltage with a small drain current flowing through it, the self-heating related  $V_{TH}$  shift is avoided [132]. So, more accurate ageing condition is indicated.

(2) HTRB test is used to evaluate the stability and integrity of the edge channel structure and solid-state junction surface [124][131]. The drain-to-source junction is reversely biased [129] by stressing  $V_{DS}$  at 80% ~ 100% maximum voltage rating at  $T_{j\_max}$  for a sufficiently long period, such as 1000 hours [124]. The gate and source are shorted. The drain leakage current  $I_{DSS}$  is used as the indicator [130]. HTRB test is regarded to be passed when  $I_{DSS}$  is within twice the initial value [124].

(3) PC test is intended to detect the degradation of bond wires [106]. Power cycling test can be classified into DC and AC tests based on different heating sources [133]. The heating of DC power cycling tests is from only conduction power loss  $P_{cond}$ . The device under test (DUT) in AC power cycling tests is heated by both the conduction loss  $P_{cond}$  and switching loss  $P_{sw}$ . In this test, the gate is triggered either continuously or alternately, so that the DUT is heated with load current flowing through the junction. Then the DUT is cooled down shortly by turning off the power and using external cooling such as typically chosen water cooling. Threshold voltage  $V_{TH}$  [127], on-state resistance  $R_{DS\_ON}$  [111][127][134], gate leakage current  $I_{GSS}$  [127], drain-source capacitance  $C_{DS}$  [127], on-state voltage  $V_{DS\_ON}$  [127][129] and body diode forward voltage  $V_F$  [106] can be used for the indicators. One criterion for the pass is that  $V_{DS\_ON}$  or  $V_F$  should be within +5% the initial value [106]. As temperature rises, for either Si or SiC MOSFETs, the decrease of mobility in the drift region [135] results in an increase of drift region resistance. For SiC MOSFETs, the channel mobility increase leads to channel resistance decrease [136]. This would

counteract the increase of the drift region resistance. As a result,  $R_{DS\_ON}$  is less temperature relevant [137][138], and thus is not an ideal indicator in SiC MOSFET power cycling test. Also, due to smaller die size in SiC and resulted less apparent change of Miller capacitance compared with Si devices, the discharge time of Miller capacitor is not so sensitive to be an indicator in SiC power cycling tests [139][140]. Considering these constraints, the TSEPs for the SiC MOSFETs have been explored. One promising DC power cycling TSEP is identified as body diode's voltage drop at low current and negative gate bias, which is shown to be independent of the ageing effect [141][142].

- (4) TC test is also used for the acceleration of the packaging interconnection degradation. But the heating and cooling sources are from the external hot plate or thermal chamber. Compared with PC test, TC test is able to achieve more precise temperature control of  $T_{j\_max}$ ,  $T_{j\_mean}$ , and  $\Delta T_j$ .
- (5) TS test is similar to TC test, but with longer thermal cycling time. The DUT is heated in one chamber for a sufficient time and then cooled in another chamber for another enough period. The time should be long to guarantee the DUT has a uniform temperature distribution. The transfer time between these two chambers does not contribute to the accelerated ageing in this test, and thus should be short.

The above ALTs could also be combined with other characterization tests to realize specific functions. A double pulse test has been integrated with a PC test platform to acquire multiple health indicators in real time [143][144].

Commonly adopted reliability test standards for power devices have been published by Joint Electron Device Engineering Council (JEDEC) [145], Automotive Electronics Council (AEC) [121][146], International Electrotechnical Commission (IEC) [51] and Military Standard

(MIL STD) 750 [146]. The transfer characteristics is sensitive to both the measurement sweep speed and direction for SiC MOSFETs [146]. However, none of the existing standards has considered this issue. Besides,  $V_{TH}$  shift in SiC MOSFETs tends to recover when the temperature rapidly decreases under a positive bias thermal stress [129]. The minimum uninterrupted bias duration in the MIL-STD-750F standard [147] is defined as 8 hours [148]. The maximum interrupted bias duration in the JEDEC JESD22-A108D standard [43] is regulated as 96 hours for devices working at the voltage larger than 10 V, or 168 hours for all other devices. Nevertheless, these minimum uninterrupted and maximum interrupted bias durations need to be reconsidered for SiC MOSFETs. JEDEC is now working on JC-70.2 standards to clarify the qualification procedures, characterization methods for SiC MOSFETs [148].

### **2.2.2. Component-Level Lifetime Modeling Methods**

Lifetime models are used to estimate the reliability under normal operating conditions based on the failure data obtained from ALTs. Every acceleration model has its own application conditions [108]. The component-level statistical models have been reviewed in [149]. The data obtained from ALTs are discrete numbers. To use them in the fully parametric RUL estimation, extrapolation is typically conducted based on physics-of-failure (PoF) models, data-driven models and hybrid models for both chip-level and package-level RUL modeling.

#### ***2.2.2.1. Physics-of-Failure Models***

The PoF models are based on the physical parameters reflecting corresponding failure mechanisms. They use statistical methods for parameter identification, which requires experiments and tested data. The PoF models are classified based on different failure modes, such as gate oxide failure, bond wire fracture and lift-off, and solder fatigue.

Gate oxide failure could be caused by voltage stress related to high electric field. The corresponding lifetime model is based on stressed and normal voltage [104][123] as shown in (Eq.2.2). It has advantages in predicting long-term damage behaviors due to their damage accumulation mathematical description.

$$LT(V_{Stressed}) = (V_{Stressed}/V_{normal})^{\beta_1} \cdot LT(V_{normal}) \quad (\text{Eq.2.2})$$

where,  $V_{stressed}$  and  $V_{normal}$  are the stressed and normal voltage amplitude, respectively.  $LT(V_{stressed})$  and  $LT(V_{normal})$  are the lifetime of the component under voltage stress and under normal use conditions, respectively.  $\beta_1$  is a negative constant depending on the acceleration test results.

Gate oxide degradation could also be associated with the high temperature stress. A Weibull-Arrhenius model shown in (Eq.2.3) has been used to model the SiC MOSFET failure rate in terms of the junction temperature [150]. Gate leakage current has been monitored to indicate the ageing extent.

$$\lambda(t, T_j) = \left[ \beta_2 / \left( c_1 \cdot e^{E_a/(k_b \cdot T_j)} \right) \right] \cdot \left[ t / \left( c_1 \cdot e^{E_a/(k_b \cdot T_j)} \right) \right]^{\beta_2 - 1} \quad (\text{Eq.2.3})$$

where,  $\lambda$  is the instantaneous failure rate.  $t$  is the time.  $E_a$  is activation energy.  $k_b$  is Boltzmann's constant.  $\beta_2$  is the form factor.  $c_1$  is a constant related to the material.

With a simplified form, the above SiC MOSFET gate oxide time to failure could also be represented by the (Eq.2.4) [151].

$$\tau_{BD} = \tau_0 \cdot e^{-\gamma \cdot E_{ox}} \cdot e^{-E_a/(k_b \cdot T_j)} \quad (\text{Eq.2.4})$$

where,  $\tau_{BD}$  is time to break down for SiC MOSFET gate oxide.  $\tau_0$  is the constant dependent on accelerated tests.  $\gamma$  is the electric field acceleration factor.  $E_{ox}$  is gate oxide electric field.

Bond wire fracture is caused by the alternate expansion and contraction at the wire interfaced with DCB upper surface. (Eq.2.5) shows the Schafft model to analyze the relationship

between  $N_f$  and wire bending stress [148][152]. Thus, the fracture related bond wire lifetime could be predicted.

$$N_f = a_1 \cdot (\varepsilon_s)^{n_1} \quad (\text{Eq.2.5})$$

where,  $\varepsilon_s$  is the bond wire strain,  $a_1$  and  $n_1$  are constants based on the bond wire material.

PoF lifetime models of bond wire lift-off and solder fatigue are based on the fundamental form of the Coffin-Manson model [114][153]–[155] in (Eq.2.6). The SiC MOSFET bond wire lifetime has also been estimated with this model [156][157].

$$N_f = a_2 \cdot (\Delta T - \Delta T_0)^{-n_2} \quad (\text{Eq.2.6})$$

where,  $N_f$  is the number of cycles to failure.  $\Delta T$  is the temperature range in the entire thermal cycle.  $\Delta T_0$  is the elastic temperature range, which is normally regarded as insignificant.  $a_2$  and  $n_2$  are defined by the database of power cycling tests.

However, it fails to consider the impact of the average junction temperature  $T_{j\_mean}$  on cycles to failure. By Arrhenius approach [114][152][158], more accurate Coffin-Manson based lifetime model for bond wire lift-off and solder fatigue is improved [36][159], as shown in (Eq.2.7).

$$N_f = a_3 \cdot (\Delta T_j)^{-n_3} \cdot e^{\frac{E_a}{k_b \cdot T_{j\_mean}}} \quad (\text{Eq.2.7})$$

A bond wire lifetime comparison between the Si IGBT and SiC MOSFET has been conducted using the above model [160]. With  $R_{DS\_ON}$  as the degradation indicator in thermal cycling tests, SiC MOSFETs are shown to achieve more cycles to failure than Si IGBTs, especially at low junction temperature swing.

By further considering other parameters such as power-on time  $t_{on}$ , current flowing through the wire  $I_w$ , blocking voltage  $V_B$ , and wire diameter  $D_w$ , the bond wire lifetime model is improved in the Bayerer model in (Eq.2.8) [154][161]–[164].

$$N_f = a_4 \cdot (\Delta T_j)^{-\beta_2} \cdot e^{\beta_3/(T_j+273)} \cdot t_{on}^{\beta_4} \cdot I_w^{\beta_5} \cdot V_B^{\beta_4} \cdot D_w^{\beta_7} \quad (\text{Eq.2.8})$$

It has been verified to predict the lifetime of SiC MOSFETs under thermal cycling mission profiles [165].

The bond wire lift-off could also be modeled from the perspective of material science. (Eq.2.9) shows a plastic strain based Coffin-Manson model, which can illustrate the physical failure process caused by the CTE mismatch between the bond wire copper and SiC [166][167].

$$N_f = c_2 \cdot (\Delta \varepsilon_p)^{-c_3} \quad (\text{Eq.2.9})$$

where,  $\varepsilon_p$  is the plastic strain put on the bond wire.  $c_2$  and  $c_3$  are defined by the thermal test results.

Solder fatigue is caused by the CTE mismatch. The PoF lifetime models can be based on stress, plastic strain, creep strain, stress-strain hysteresis energy, and crack propagation damage [168]. The Coffin-Manson model based on plastic strain [169] is shown in (Eq.2.10). Norris-Landzberg model [168][170] leads to more precise lifetime estimation by further considering cycling frequency and maximum temperature.

$$N_f = L_S / \left[ a_5 \cdot (\Delta \varepsilon_p)^{n_4} \right] \quad (\text{Eq.2.10})$$

where,  $L_S$  is solder crack length.  $\Delta \varepsilon_p$  is plastic strain change in thermal cycles.  $a_5$  and  $n_4$  are decided by thermal cycling tests.

(Eq.2.11) presents a SiC MOSFET solder layer lifetime model based on the exponential relationship between the lifetime and creep strain energy accumulated in one cycle [98].

$$\Delta W_c = W_f \cdot (2N_f)^m \quad (\text{Eq.2.11})$$

where,  $\Delta W_c$  is the creep energy accumulated in one cycle.  $W_f$  is the fatigue energy coefficient of solder material.  $m$  is the fatigue energy index.

$R_{DS\_ON}$  has been measured to reflect the overall RUL of the SiC MOSFET based on power cycling test results [171]. The corresponding lifetime model is shown in (Eq.2.12).

$$\Delta R_{ds\_on}(t) = \theta_1 \cdot e^{\theta_2 \cdot t} + \theta_3 \quad (\text{Eq.2.12})$$

where  $\theta_1$ ,  $\theta_2$  and  $\theta_3$  are the model parameters dependent on the specific prognostic algorithms.

To estimate the model parameters in the PoF models, algorithms such as the particle filter (PF) [168][172][173], the Kalman filter (KF) [172], and the extended Kalman filter (EKF) [173] have been used. These algorithms are based on Bayesian inference to generate probability density function. Since the posterior distributions of PF algorithm parameters are expressed by particles and weights, it is more suitable for the prognostics of the nonlinear systems with non-Gaussian noise compared to KF and EKF methods [174]. The correlation between the parameters and the noise in the sensor data needs to be considered in the model parameter identification process.

PoF models have a direct physical meaning. But it is difficult to obtain accurate models in real systems considering the different failure modes [43]. Besides, as the model becomes more complex, laborious experiments are needed to identify the model coefficients. Thus, PoF models are not universally applicable to different types of power converter systems.

#### **2.2.2.2. Data-Driven Models**

Data-driven models estimate the RUL based on available data without need of any physics mechanisms [43][175]. The uncertainty margins are large by using this method. Thus, it is not suitable to predict long-term lifetime [176]. The data can be collected from either recorded failure data or real-time condition monitoring. Considering relatively scarce failure events, condition monitored data is a more realizable source. This real-time data can either directly reflect or indirectly indicate the system health status. For the former case, the RUL estimation is regarded as the prediction of the condition monitored data to reach a predefined threshold level. For the

latter case, failure event data is probably needed along with the condition monitored data for RUL estimation [43]. This chapter only focuses on the former case. Both a threshold and a model to represent the monitored data are required to determine the RUL. The decision of the threshold is normally based on the engineering experience and related standards.

Data-driven models are dependent on observed data in both healthy and faulty states [177][178]. RUL is estimated normally in a form of probability density functions [179]. They include the models based on regression, Wiener process, Gamma process, Markov chain and artificial intelligence. The models based on Wiener, Gamma, and Markov chain are related to stochastic processes capturing degradation dynamics. Thus, these three models are suitable to model the lifetime of the power inverters with multiple steady states. Further discussions are presented in the following.

- (1) Regression based models are most commonly used. By using this method, the system health condition is reflected by the monitored variables. Hence, the RUL is estimated by modeling these variables with a predefined threshold.
- (2) Modeling through Wiener process or Brownian motion with drift [43] is appropriate when the degradation develops bi-directionally over the time with Gaussian noises.
- (3) Gamma process [180] based models are applicable for the cases in which the degradation occurs gradually over time in a sequence of small positive increments. These models have relatively straightforward mathematical calculations. Besides, they take the temporal variability into consideration.
- (4) Markov chain based models assume that the future degradation state depends only on the current degradation state, and the system state can be reflected directly by observed data.

(5) Artificial intelligence based methods have mostly applied machine learning to estimate the RUL of power devices and converters, such as relevance vector machines [177], artificial neural networks [174][181], deep learning algorithms [179][182], genetic algorithms [183][184], and supervised learning [185]. A relevance vector machine has been utilized to train the power MOSFET ageing data to obtain representative vectors [177], which are fitted by a degradation model to predict the RUL. A time-delay neural network failure model has been combined with the probabilistic function by using the maximum likelihood method for IGBT model optimization [179]. A recurrent neural network scheme has been applied in the system prognostics [174]. A deep learning algorithm based on stacked long short-term memory (LSTM) has been used to conduct the training and inference for Si MOSFETs and corresponding power converters by detecting  $R_{DS\_ON}$  change [179][182]. It derives a more accurate lifetime model compared to Kalman filter and particle filter methods. A genetic algorithm has been adopted to select the valuable principal components for GaN device behavioral modeling [184]. Supervised learning has assisted in predicting the switching voltage and current waveforms so that a GaN RUL model is built to realize better device lifetime prediction [185].

From another perspective, the parameter estimation could be conducted through different mathematical methods based on the data derived from thermal cycling tests. Therefore, the data-driven models could also be classified into the linear and nonlinear groups as shown in Table 2.3.

(a) *Linear data-driven models*: The maximum likelihood estimation is the most basic linear data-driven modeling method [185]. The least square approximation has been used to predict the gate oxide lifetime as a function of  $V_{GS}$  stress based on the HTGB test data [174]. However, the estimation accuracy is discounted due to the outliers present in the beginning part of the data [185].

To address this issue, some ideas in other disciplines could be applied. Random sample consensus is a way to remove the data outliers and improve estimation accuracy [186]. But the nonlinearity in the initial part of the data still remains.

Bayesian interference is another way to improve accuracy by considering prior knowledge into estimation [168]. Furthermore, Kalman filter has been used to minimize the mean square errors by estimating the posterior state [34][187].

Table 2.3. Summary of Linear and Nonlinear Data-driven Models

Model group	Parameter estimation method	Monitored component / location	Failure indicator
Linear model	Bayesian Interference [186]	Power MOSFETs / Solder layers	$R_{DS\_ON}$
	Bayesian Interference [187]	Discrete IGBTs / Solder layers	$V_{CE\_ON}$
	Random sample and consensus [188]	Si Power MOSFETs and IGBTs / Gate oxide	$V_{TH}$
	Kalman Filter with least square fitting [124]	Power MOSFETs / Bond wires, solder layers	$R_{DS\_ON}$
Nonlinear model	Extended Kalman Filter [174]	SiC MOSFETs / N/A	$R_{DS\_ON}$
	Exponential model [184][185]	Si MOSFETs / N/A	$R_{DS\_ON}, V_{TH}$
		Si IGBTs / N/A	$V_{CE\_ON}$

(b) *Nonlinear data-driven models:* Bayesian tracking algorithms such as extended Kalman filter and exponential models are commonly adopted for the nonlinear data-driven techniques [186]. First, Extended Kalman filter nonlinear algorithm has been applied in SiC MOSFET junction temperature estimation. This is based on a state space model describing the relationship between  $R_{DS\_ON}$  and  $T_j$  [174]. The experiment result shows the robustness to load change. Second, Extended Kalman filter could also be utilized together with other techniques such as particle filter to model the RUL. The battery RUL estimation has been conducted with relevance vector machine by combining these two approaches [175][189]. Extended Kalman filter is shown to be robust but

suffers from fast divergence [190]. The particle filter is presented to improve the estimation accuracy. But resampling of the particles is carried out in each iteration, which increases the computation burden [13]. Third, Exponential models have been applied to relate the on-state resistance and Si device lifetime [184][185]. The exponential lifetime model could also be utilized in the  $V_{TH}$  related degradation [185]. Furthermore, the matrix-vector based exponential lifetime model has been used to create a connection between the lifetime and on-state device voltage [184].

*(c) Data-driven models in both linear and nonlinear systems:* Some models can be applied in either linear or nonlinear circumstances. Monte Carlo simulation method [43] is especially useful when analytical approaches are not feasible. Since it performs stochastic iterations of the independent component variables [34] to conduct the simulation, a weighted average value is normally used to calculate the lifetime. So, it cannot generate an exact prediction [191]. Besides, machine learning is an alternative in either linear or nonlinear cases by applying the statistical techniques such as least square approximation [43] or Bayesian inference [44]. But the RUL probability density function is unavailable in this method [44].

### ***2.2.2.3. Hybrid Models***

The hybrid models could combine the physics of failure and data-driven models [192][193]. They could leverage the benefits of different types of models. The PoF based models reflect the real physical mechanisms with the model parameters estimated by the measured data. The challenge in this group of models is that it is more difficult to represent the prognostics uncertainty compared with the other two models [194].

Table 2.4 further presents a summary of all the above three component-level lifetime models.

Table 2.4. Summary of SiC MOSFET Component-Level Lifetime Models

Model Categories	Failure Modes	Model Descriptions	Features	
Physics-of-failure models	Gate oxide breakdown	Stressed & normal voltage based	Suitable for long-term damage behavior prediction	
		Weibull-Arrhenius exponential model and its derivatives	Capable of modeling temperature stress	
	Bond wire fracture	Schafft Model	Capable of modeling wire bending stress	
	Bond wire lift-off	Coffin-Manson model	Fails to consider the impact of $T_{j\_mean}$	
		Coffin-Manson model by Arrhenius approach	Shows SiC MOSFETs achieve more cycles to failure than Si IGBTs, especially at low $\Delta T_j$	
		Bayerer model	Includes power-on time $t_{on}$ , current $I_w$ , blocking voltage $V_B$ , and wire diameter $D_w$	
		Plastic strain based Coffin-Manson model	Capable of modeling CTE mismatch between the bond wire copper and SiC	
	Solder fatigue	Coffin-Manson model by Arrhenius approach	Capable of including the impact of $T_{j\_mean}$	
		Plastic strain based Coffin-Manson model	Capable of modeling CTE mismatch between the DCB-die solder attach and SiC	
		Norris-Landzberg model	Considers temperature cycling frequency and maximum temperature	
		Creep strain energy	Shows exponential relationship between lifetime and creep strain energy in a cycle	
	Failure modes indicated by $R_{DS\_ON}$	Exponential function for $R_{DS\_ON}$	Covers more than one failure mode	
Data-driven models	Not specific failure modes	Regression based models	Most commonly used data-driven method	
		Wiener process	Suitable for the bi-directionally developing degradation	
		Gamma process	Relatively straightforward calculations with temporal variability	
		Markov chain	Memoryless	
		Artificial intelligence	Relevance vector machines	Representative vector extraction
			Artificial neural networks	Model optimization by combination with maximum likelihood method
			Deep learning algorithms	More accurate lifetime model compared to Kalman filter, particle filter methods
			Genetic algorithms	Valuable principal component selection
			Supervised learning	Voltage, current waveform prediction
		Hybrid models	Not specific failure modes	Combination of two or more above models

### 2.2.3. Cycle Counting and Fatigue Damage Accumulation

To efficiently count the random thermal cycles, many counting algorithms have been proposed, such as level-crossing counting, peak counting, simple-range counting, and rainflow counting [195]. Among them, the rainflow counting algorithm is the most well-known [17][196]. It has been applied to reduce the stress spectrum into simple values for the cyclic accumulated bond wire damage when the amplitude and frequency of the thermal cycles are not repetitive [99]. The extreme points are counted to extract the amplitude [197][198], mean value [199] and cycling period [200]. Traditional rainflow methods output half cycles that are difficult to be integrated into reliability algorithms. Counting small cycles within larger ones helps this integration [17]. Besides, to overcome inefficient data storage, real-time minimum or maximum temperature could be counted by stack-based recursive programming [201].

Once the component-level RUL estimation model is created, the fatigue damage accumulation is conducted by either linear or nonlinear approaches. Thus, the stress accumulation with the mission profile characteristics could be reflected.

The linear damage accumulation method based on the Palmgren-Miner's law [202] is mostly accepted in damage evaluations. However, it is independent of the loading levels [203], which reduces the lifetime prediction accuracy. Besides, it assumes a constant damage accumulation rate during the lifetime. However, more damage would lead to increased stresses, and thus cause additional physical mechanisms. This would result in a different damage accumulation rate. For example, as the crack propagates,  $R_{th(j-c)}$  increases due to more power loss, which accelerates the damage accumulation rate in the bond wires and solder layers. Therefore, lifetime predicted by linear methods is impractically longer.

The nonlinear damage accumulation approach reflects the accumulation rate change in different stress levels. For instance, the method based on the double linear damage law [204] allows each phase of the loading to be analyzed by the Palmgren-Miner linear damage rule. But it ignores the mutual interaction among different stresses. Manson Halford model [205] considers both stress sequences and interaction by modifying the exponent parameter in double linear damage model. Besides, nonlinear approaches consider the damage accumulation rate change by putting proper weights onto the affected physical parameters. To determine these weights, detailed experimental data are needed, which makes these methods not generally applied.

### **2.3. System-Level Offline Lifetime Modeling**

The lifetime models based on the ALT approaches are static because no dynamic real-time RUL estimation is conducted to update initial models. Statistically, most system-level lifetime has been modeled by the Weibull probability distribution functions. It has been adopted in the system-level lifetime prediction for a fuel cell DC-to-DC power stage [13], a LED source and capacitor system [206], and an onboard DC-to-DC converter for more electric aircraft [207]. For the systems with an irregular cumulative distribution function, the maximum entropy probability distribution has been presented to be more suitable compared with the Weibull distribution [208].

In this section, five static system-level lifetime modeling methods will be reviewed, including the combinatorial reliability techniques, such as reliability block diagram, fault tree analysis, GO-FLOW, and Bayesian networks, as well as the state-based modeling techniques, such as Markov chain. In this section, the state-of-art system-level lifetime prediction techniques are first summarized. Then a discussion regarding their applicability in SiC power converters is presented.

### 2.3.1. State-of-Art System-Level Lifetime Prediction Techniques

#### 2.3.1.1. Reliability block diagram (RBD)

RBD system lifetime modeling technique can be applied in the distributions with either constant or inconstant failure rates [14][16][205][209]. It allows to evaluate concepts in the early design period. This is useful to implement the design for reliability. It is a success oriented system analysis method [210]. Both in-series and in-parallel systems could adopt it. One issue with RBD is that some big systems have to be modeled with complex series or parallel combinations [211]. Table 2.5 compares the typical reliability indexes including system reliability, failure rate and mean time to failure (MTTF) for in-series and in-parallel systems. Here, a constant failure rate is assumed. In the table,  $\lambda_i$  is the failure rate of individual components.  $\lambda_{max}$  is the maximum failure rate among all the in-series components. RBD cannot model the time-dependent failures, the sequences among failures, or system dynamics. Dynamic reliability block diagram (DRBD) has been proposed to resolve these issues. But more complexity is introduced.

Table 2.5. Comparison of Reliability Indexes Between Two System Structures

Reliability Index	In-parallel System	In-series System
System reliability $R(t)$ [17][206][212]	$e^{-\sum_{i=1}^n \lambda_i t}$	$1 - \left(1 - e^{-\lambda_{max} t}\right)^n$
System failure rate $\lambda$ [16][205][212][213]	$\sum_{i=1}^n \lambda_i$	$\lambda_{max}$
System $MTTF$ ( $\int_0^{\infty} R(t) dt$ ) [14][214]	$1 / \sum_{i=1}^n \lambda_i$	$\frac{1}{\lambda_{max}} \sum_{i=1}^n \frac{1}{i}$

- A paralleled inverter lifetime has been modeled by the RBD approach, considering the constant failure rate [17]. A dynamic power distribution control has been adopted to optimize both the reliability and the cost on the system level.

- A multilevel converter lifetime has also been estimated with RBD, considering the constant failure rate [215].
- This method can also be applied in the systems with inconstant failure rates. A fuel cell DC-to-DC converter lifetime has been modeled by RBD with time-dependent failure rate [212].

### **2.3.1.2. Fault Tree Analysis (FTA)**

Developed by Bell Telephone Laboratories in 1962, FTA is a deductive, top-down method conducted in failure space to analyze the effect of initial faults on a complex system [205][214][216]. FTA only focuses on the failure combination. This approach has been applied to analyze the lifetime models following the distribution with constant failure rate such as in the fuel cell lifetime modeling application [214]. It has also been used in the circumstances with the inconstant failure rate. In [216], an electric vehicle drive system lifetime has been modeled with the time-dependent failure rate. However, there are some issues with the FTA approach. First, both the dependence among different degradations and the fault sequences [214][217] have not been modeled in this method. Second, it could be used to evaluate complex systems by analyzing the probabilities of combined failures [211]. But it must model the relationship among all individual failures [210]. Thus, the failure mechanisms of each component are required. So, with this method, the computational burden is heavy for complex systems [218].

To solve the above problems, the extended FTA techniques for dynamic and complex systems are necessary. Below summarizes three typical extended FTA methods.

- Dynamic FTA (DFTA) defines specific gates to represent failure dependence, redundancy and sequence relationships [219]. To solve the fault trees, it is conventionally translated into MCs. But Markov model becomes complicated for large

systems. A hybrid Bayesian network inference algorithm has been used instead to solve the fault trees [220]. Neither numerical integration nor conditional probability table is needed. So, this approach is suitable for the complex systems.

- Pandora temporal fault trees introduce temporal gates to describe event sequences and allow qualitative analysis of temporal fault trees [221]. This method applies Bayesian networks to solve fault trees to analyze dynamic dependability.
- Repairable fault trees further extend system lifetime by applying different repair strategies into the model [222].

### **2.3.1.3. GO-FLOW**

This system analysis technique is success-oriented [223]. It is an alternative to FTA method and is effective to estimate the lifetime of complex time-dependent systems with multiple states [224]. But it is hard to model the dynamic behavior characteristics. To overcome this, an extended GO integrated with DBN has been used to model the system dynamics [224].

### **2.3.1.4. Bayesian Network (BN)**

The Bayesian network technique could be regarded as a general version of FTA. Dependence among failures could be represented with this method [225]. It is relatively suitable for the complex system lifetime modeling because it performs the factorization of joint probability distribution for conditionally dependent variables [226]. It could be used to represent interdependency among components and include uncertainty in modeling [227]. The derivatives of BN are summarized below.

- Dynamic Bayesian network (DBN) models the temporal sequence of the variables. It is a generalization of the hidden Markov models and Kalman filters [228][229].

- By integrating the genetic algorithm into DBN, the system reliability has been regarded as a parameter in design stages to promote the design for reliability [230].
- Both the standard and dynamic BN methods repeat the random variable probability distribution calculation at every time interval and increase the model complexity. To address this issue, a discrete-time BN (DTBN) method assumes that each event happens at most once [231]. This is especially applicable for the non-repairable systems.
- The continuous-time BN (CTBN) generalizes the DTBN framework [232]. The main advantage of a CTBN over a DTBN is that it provides a closed-form solution for the system lifetime. Besides, CTBN also saves memory, because the probabilities are described in terms of parametric functions rather than multi-dimensional tables in DTBN.

#### **2.3.1.5. Markov Chain (MC)**

The Markov chain approach is a random process with the next state depending only on the present state [214]. It is time independent and focuses on either successful or failed combination. It saves the computational effort in the lifetime calculation of systems with fault sequence [210]. MC and its derivatives are suitable to solve dynamic systems with component interactions [233]. However, the Markov model expands its state space exponentially with the number of components. Thus, it is difficult to apply MC into large, complex systems. Besides, MC is not suitable in systems with time-dependent failure rates [210][217]. Some applications of the MC methods into the power converter area are listed in the following. An interleaved DC-to-DC boost converter lifetime has been modeled by applying this MC method, considering the constant component failure rates [15]. Besides, an induction motor drive lifetime modeling has also been conducted

with the MC analysis [234]. Furthermore, a proton exchange membrane fuel cell power plant lifetime has been estimated by the MC technique as well, with the continuous state transitions [40].

### 2.3.2. Discussion of the Applicability in SiC Power Converters

Table 2.6 summarizes the above system-level lifetime models and their derivatives. Overall speaking, based on the six evaluated indexes, DRBD and DBN could achieve a relatively wide application range. Secondly, the component failures such as gate oxide breakdown, body diode degradation, bond wire fracture, and lift-off as well as solder fatigue are all time dependent. Since the classical RBD, FTA and MC cannot model the time-dependent failures, they are not applicable in the SiC power converter lifetime prediction. Third, if one failure mechanism occur after the other one, the RBD, FTA are not suitable for this sequence order modeling in the SiC converter

Table 2.6. Summary of System-Level Lifetime Models

Modeling methods	Time dependent failure modeling	Event sequence modeling	Applicable to the fixed / variable failure rate	Dynamic behavior modeling	Complex system lifetime modeling	Success- / failure-oriented
				<ul style="list-style-type: none"> <li>• Component interdependency modeling</li> <li>• Customizable redundancy modeling</li> <li>• Load sharing modeling</li> </ul>		
RBD	No	No	Either	No	Difficult	Success
DRBD	Yes	Yes	Either	Yes	Yes	Success
FTA	No	No	Either	No	Difficult	Failure
DFTA	Yes	Yes	Either	Hard / Impossible	Yes	Failure
GO-FLOW	Yes	Yes	N/A	No	Yes	Success
Extended GO-FLOW	Yes	Yes	N/A	Yes	Yes	Success
BN	No	Yes	Either	Yes	Suitable	N/A
DBN	Yes	Yes	Either	Yes	Suitable	N/A
MC	No	Yes	Fixed	N/A	Difficult	Either

lifetime prediction. Fourth, for the components with inconstant failure rate, MC is not a promising option to predict the SiC converter system lifetime. Fifth, regarding the dynamic behavior modeling, such as component interdependence in SiC MOSFET failure mechanisms, redundancy modeling in the multilevel converters, and load sharing modeling in the paralleled devices, RBD, FTA, GO-FLOW are not applicable. Although DFTA has improved the dynamic capability, it is still hard compared with the DRBD, extended GO-FLOW, and BN techniques. This is decided by the adopted inference algorithm. Sixth, for the complex systems consisting of various components such as the three-port SiC converter consisting of an interleaved boost converter, an interleaved bidirectional flyback converter, and a three-phase voltage source inverter [235], it takes considerable computational resources to utilize the RBD, FTA and MC techniques in the converter lifetime prediction.

The system lifetime modeling has been conducted in the Si IGBT based inverters following exponential distribution with constant failure rate [16][17]. SiC MOSFET based power converter lifetime models following the Weibull distribution with inconstant failure rate could be investigated. Furthermore, system RUL estimation could be based on multiple indicators using techniques such as principal component analysis [50].

### **2.3.3. SiC Converter Lifetime Modeling Software**

Both the academia and industry have developed component-level and system-level simulation tools to analyze and predict the lifetime of the SiC converters. These software uses different random number generation methods and lifetime modeling strategies to derive the component or system lifetime in the form of statistical probability distributions.

### ***2.3.3.1. Component-Level Lifetime Modeling Software***

One of the component-level lifetime modeling software is the finite element analysis tool developed by the ANSYS. It has been used to simulate solder layer lifetime with energy-based and creep-strain-based methods [236]. The other one is the finite element analysis software by the COMSOL Multiphysics. The lifetime of the die-attach solder layer has been modeled with thermo-mechanical physical analysis [98].

### ***2.3.3.2. System-Level Lifetime Modeling Software***

Both the academic and commercial system-level lifetime modeling software has been developed by using different modeling categories mentioned in Section 2.3.

In the academics, three system-level lifetime modeling software has been well known. First, Galileo tool [237] by the University of Virginia. It is specifically designed to model and analyze the dynamic fault trees. It can be edited in a web-based graphical environment. Second, the Symbolic Hierarchical Automated, Reliability and Performance Evaluator (SHARPE) [238] by Duke University could model the system-level lifetime by integrating the information from each component time-dependent degradation and the system structure. It supports RBD, FTA and MC modeling methods. It generates lifetime results statistically in the form of a probability distribution function. Third, the DFTCalc [239] by the University of Twente. It translates each top-level failure event into an input-output interactive Markov chain. The failure probability of a dynamic fault tree is calculated by composing these chains one by one. It could be used to output the system mean time to failure.

Besides, six commercial system-level lifetime modeling software is also summarized in the following. First, the Isograph [240] provides two tools to model the SiC converter system-level lifetime in a graphical format, including the Reliability Workbench tool and the Availability

Workbench tool. Both of them offer RBD and FTA modeling approaches. The former tool is useful when there is need to refer to the standards such as MIL-STD 1629 and IEC 61508. Second, the RAM Commander [241] could utilize the RBD, FTA and MC techniques to model the system-level lifetime. Third, ReliaSoft [242] offers four tools to model the system lifetime. BlockSim tool provides RBD and FTA to model the system-level lifetime for both repairable and non-repairable systems in a graphical interface. Besides, Weibull++ tool is used to analyze lifetime data using Weibull distribution. Furthermore, ALTA tool could analyze the quantitative lifetime data from accelerated tests. Also, Lambda Predict tool could estimate the system lifetime based on the standards such as MIL-HDBK-217F. Fourth, the Windchill RBD (formerly Relx OpSim) [243] supports series, parallel, and hybrid RBD configurations. It can be used to calculate the expected number of failures, the failure rate, MTTF for non-repairable systems, and mean time between failures (MTBF) for repairable systems. Fifth, the Fault Tree Analyzer [244] is an open-source tool. It could do static FTA in a web-based graphical environment. Sixth, the ITEM ToolKit [245] could be utilized to analyze the RBD, FTA and MC modeling techniques in lifetime prediction. Seventh, the AGENARISK [246] could be used to predict the SiC power converter lifetime with the up-to-date techniques from Bayesian artificial intelligence and probabilistic reasoning. It integrates the real-time degradation data with the knowledge about component causal relationship and interdependence.

#### **2.4. SiC Power Converter Condition Monitoring**

To update the static system lifetime model based on the results of ALTs, the summary of the component-level lifetime models, and the extrapolation of statistical lifetime modeling in Section 2.3, the identified degradation indicators are further measured in real time. Condition monitoring is a passive method to online indicate the degradation of power devices

[114][247][248], capacitors [39][249], and overall systems [114]. Figure 2.5 classifies condition monitoring into component and system levels. Component-level condition monitoring includes direct and indirect methods. Since thermally induced failure takes a significant percentage of 55% among all sources of failures [250][251], most of power electronic condition monitoring has been focused on temperature related failure.

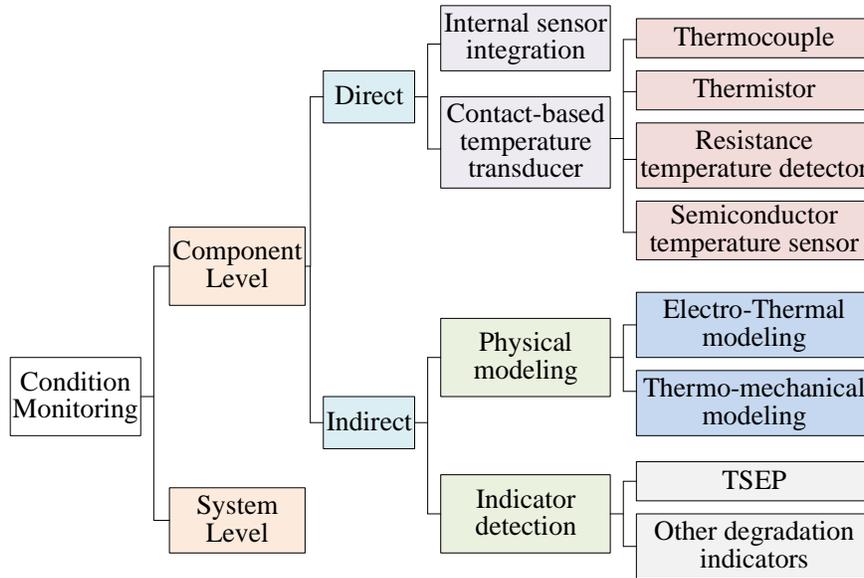


Figure 2.5. Condition monitoring method classification

1) Direct condition monitoring

Direct condition monitoring is realized by using internal sensors and contact-based temperature transducers. Device packaging and internal design are essential in the internal sensor integration method. Based on the thermistor principle, a temperature sensor is integrated into the SiC power MOSFETs to measure  $T_j$  [252]. More common direct condition monitoring is conducted by applying contact-based temperature transducers such as thermocouples, thermistors, resistance temperature detectors, and semiconductor temperature sensors [253]. However, high-bandwidth temperature sensors are not cost-effective. Another extensively employed contact-based

temperature sensors have focused on the negative thermal coefficient (NTC) thermistor. The thermal impedance between the SiC die and the integrated NTC thermistor has been modeled in a Foster thermal network to estimate  $T_j$  [254].

## 2) Indirect condition monitoring

Indirect condition monitoring is carried out by either physical modeling or detecting parameters indicating internal degradation. Physical modeling can be further classified into electro-thermal modeling and thermo-mechanical modeling. The indicator detection includes the monitoring of the TSEPs and other degradation indicators reflecting the degradation of the gate oxide, the body diode, bond wires and solder layers.

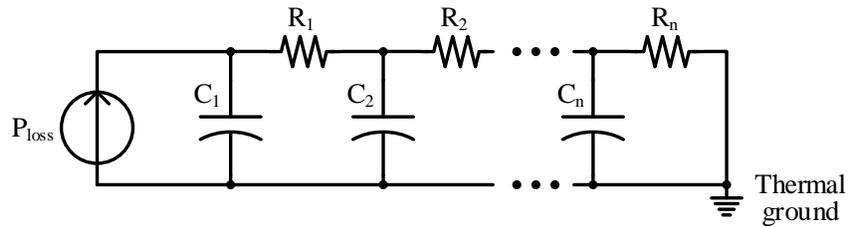
## 3) System condition monitoring

System-level condition monitoring has not been explored enough compared with component-level counterpart. It is commonly performed by comparing the responses in real time and under normal operations [114]. The difference between the two responses is used to evaluate system health condition.

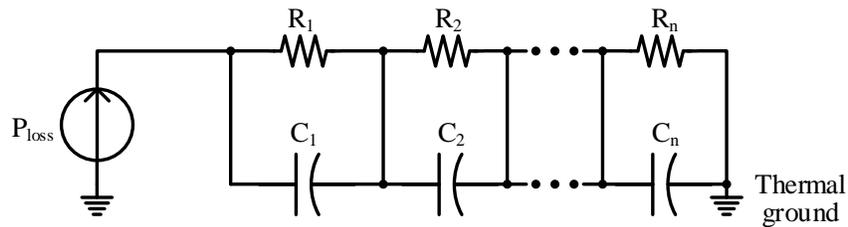
### **2.4.1. Electro-Thermal Modeling of SiC Power Devices**

Electro-thermal modeling is normally concerned with the SiC device model, power loss model, and thermal model. Temperature swing [255] and average junction temperature [159] are targeted by electro-thermal simulation including power loss calculation. Compared with other temperature estimation methods, electro-thermal modeling is more cost-effective. However, it is difficult to model the electro-thermal system accurately. One challenge is to consider uneven temperature distribution among the chips, layers, and different points on the chip inside the power module due to thermal coupling. Another challenge is to model mission profiles and thermal dynamics, which are closely related to device lifetime.

Two electro-thermal modeling methods have been studied, i.e. 1-dimension (1-D), 3-dimension (3-D) thermal networks. Both approaches can be realized by either Cauer or Foster thermal networks [256] as shown in Figure 2.6. Cauer grounded-capacitor ladder thermal network is based on heat physics. It is more accurate but computation extensive. Foster non-grounded-capacitor ladder thermal network is not physically based and thus mathematically more convenient [257].



(a) Cauer Thermal Network



(a) Foster Thermal Network

Figure 2.6. Two types of RC thermal networks

1-D lumped RC thermal networks are based on manufacturer datasheets [258][259]. They are convenient to be realized in circuit simulation [258] and thus fast. They are suitable for a rough estimation of junction temperature. But they basically estimate the average junction temperature of the chip area and intrinsically disregard thermal coupling among chips or different layers beneath chips [260]. Most of the 1-D RC thermal modeling is conducted in the time domain and fails to consider the boundary conditions including nonlinear heating and cooling systems [261]. To fix this issue, an electro-thermal co-simulation is conducted based on 1-D time-domain RC

thermal network by including boundary conditions [262]. Also, a frequency-domain 1-D thermal network [263] considers the impact of boundary conditions of nonlinear cooling system on thermal impedance. A low pass filter has been adopted to model the loss behavior of thermal grease and heat sink so that the junction temperature can be estimated more accurately.

Another electro-thermal modeling method is based on 3-D lumped RC thermal network as shown in Figure 2.7. It is more accurate than 1-D network due to the consideration of thermal coupling and dynamics. Differential thermal analytical equations using finite difference method [260], finite element method [264] have been used to derive both the steady-state and transient temperature profiles (junction temperature swing  $\Delta T_j$  and maximum junction temperature  $T_{j\_max}$ ). But they are limited with time-consuming calculation [265]. Thus, owing to both the high cost and possible divergence, they are not efficient to analyze long-term mission profiles. To improve the execution speed, the thermal boundary conditions can be transformed from the finite element method to circuit simulation [266].

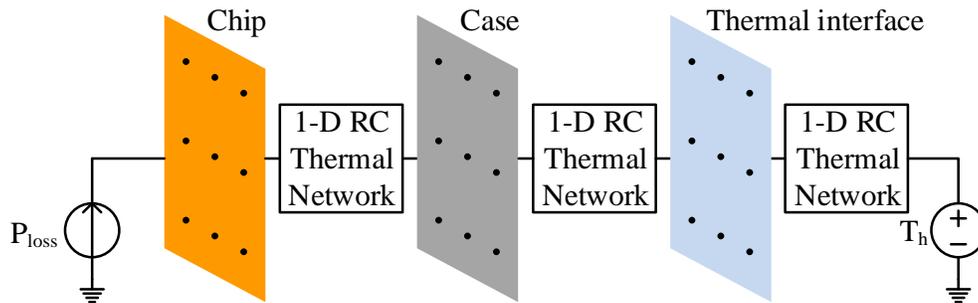


Figure 2.7. Typical 3-D thermal network

#### 2.4.2. Thermo-Mechanical Modeling of SiC Power Devices

Thermo-mechanical modeling is derived from the thermo-mechanical stress at the bond wires and solder layers. It can be used to diagnose the health condition of these package-level locations. The IGBT module bond wire 3-D thermo-mechanical degradation modeling has been

studied in [267]. The thermo-mechanical creep behavior of solder layers has been analyzed in [268]. Since the package-level failure mechanisms between SiC MOSFETs and Si IGBTs are similar based on the review in Section 2.1, these thermo-mechanical modeling methods have also been applied to the SiC MOSFETs [170]. For example, in the SiC power modules, the stress and strain response to thermal loading has been modeled and simulated [166]. The difference between Si and SiC devices regarding this thermo-mechanical modeling is a potential domain to be further investigated. A summary of SiC MOSFET electro-thermal and thermo-mechanical modeling techniques has been shown in Table 2.7.

Table 2.7. Summary of SiC MOSFET Electro-Thermal and Thermo-Mechanical Modeling

Model Categories	Descriptions	Features
Electro-thermal modeling	One-dimension thermal networks	Convenient to be realized in circuit simulations quickly
		Suitable for a rough estimation of $T_j$
		Disregards thermal coupling among chips or various layers beneath chips
	Three-dimension thermal networks	More accurate by thermal coupling consideration
		Time-consuming calculation
		Not efficient to analyze long-term mission profiles
Thermo-mechanical modeling	Stress and strain response to thermal loading	N/A

### 2.4.3. Temperature-Related Health Indicators

Two groups of the temperature-related health indicators have been well studied for the component-level thermal condition monitoring. One of them is the junction-case thermal impedance  $R_{th(j-c)}$ . It has been utilized as the indicator of solder fatigue through temperature cycling tests or thermal shock tests [106].

Another one is associated with measuring the case temperature and junction temperature, which has been more extensively investigated. First, the relationship has been disclosed between the case temperature and the degradation of substrate-baseplate solder as well as bond wire [269]. Second, the TSEPs have been widely reviewed for the  $T_j$  monitoring of power devices [270]–[273]. On-state resistance [274][275], turn-on current switching rate [139][276], turn-on gate current plateau [139], turn-on voltage switching rate [277], turn-off discharge time of Miller capacitance [139], turn-off delay time [278], integral of the turn-on gate current over turn-on time [279], turn-on peak output current [279], shoot-through current magnitude [140], and drain current for a low gate voltage [143] have been used as the TSEPs of SiC MOSFETs. Table 2.8 presents a brief summary of these parameters.

Table 2.8. Summary of TSEPs of SiC MOSFETs

<b>TSEPs of SiC MOSFETs</b>	<b>Positive / Negative Temperature Relevance</b>
Turn-on current rate $dI_{DS}/dt$ [139][276]	Positive
Turn-off current rate $dI_{DS}/dt$ [276]	Negative
Turn-on gate current plateau [139]	Positive
Turn-on voltage rate $dV_{DS}/dt$ [281]	Negative
The discharge time of Miller capacitance during turn-off [139][282]	Positive
Turn-off delay time [278]	Positive
Integral of gate drive turn-on output current over turn-on time [279]	Positive
Gate drive turn-on peak output current [279]	Positive
On-state resistance $R_{DS\_ON}$ [275]	Positive
Shoot-through current magnitude [140]	Positive

To begin with, the current rate  $dI_{DS}/dt$  has been identified as the SiC MOSFET TSEP [139][276] because it increases with temperature during the turn-on transient and decreases with temperature during the turn-off process [280]. Negative temperature coefficient of the  $V_{TH}$  is the reason behind the positive temperature coefficient of both  $dI_{DS}/dt$  and  $I_{G(p)}$  during SiC MOSFET

turn-on. Both two TSEPs can be integrated with gate drive. There is also a tradeoff between switching loss and temperature sensitivity for both  $dI_{DS}/dt$  and  $I_{G(p)}$  during turn-on. They are not suitable for fast switching due to the obvious interference of the parasitic inductance. Their temperature dependency is sensitive to die size and gate resistance. Decoupling is needed since turn-on  $I_{G(p)}$  would also be affected by the temperature-irrelevant parameters such as load current.

Besides, the turn-on voltage rate  $dV_{DS}/dt$  has a negative temperature dependency for SiC MOSFETs [281]. This is mainly caused by the negative temperature coefficient of the threshold voltage, which is caused by the positive temperature relevance of the intrinsic carrier concentration.

Third, the discharge time of Miller capacitance  $C_{GD}$  during turn-off process has been utilized as another TSEP for SiC MOSFETs [139]. Due to smaller intrinsic capacitances at the same current rating, it takes shorter time for this capacitor to be discharged. As a result, this TSEP is less manifest and thus less temperature-sensitive for SiC MOSFETs compared with Si IGBTs.

Fourth, the turn-off delay time has been integrated into the gate drive with adjustable gate resistance [278]. But its temperature dependency is sensitive to the dc-link voltage, load current, and gate resistance. Thus, a decoupling mechanism needs to be included in this TSEP monitoring circuit design.

Fifth, the peak value of the gate drive turn-on output current has been detected to indicate the junction temperature inside the chip. The issue with this TSEP is that the gate drive detecting circuit is relatively complex [279]. Also based on this output current, the integral of this gate drive turn-on output current has been further verified to be an effective TSEP for SiC MOSFETs. But its temperature dependency is sensitive to both the dc-link voltage and the load.

Furthermore, the drain-source on-state resistance  $R_{DS\_ON}$  has been shown as the SiC MOSFET TSEP [275]. However, As discussed in Section 2.2.1,  $R_{DS\_ON}$  is less temperature dependent in SiC MOSFETs compared with Si devices [138]. Besides, SiC MOSFET  $R_{DS\_ON}$  is highly dependent on the  $V_{GS}$  [283]. So,  $R_{DS\_ON}$  is not a promising TSEP for SiC MOSFETs.

Finally, the shoot-through current has been applied as a TSEP [140]. The amplitude of the shoot-through current caused by the crosstalk is less temperature-sensitive for SiC MOSFETs than Si IGBTs. This is mainly attributed to the relatively smaller Miller capacitance in SiC MOSFETs. This TSEP is based on the crosstalk and thus is intrusive to the normal operation.

Below are some discussions about the above TSEPs:

- Due to higher interface state traps and fixed oxide traps in SiC MOSFETs, the bias temperature instability results in more significant  $V_{TH}$  drift [284]. This would reduce the  $T_j$  estimation accuracy, based on  $R_{DS\_ON}$ , body diode forward voltage  $V_F$ , turn-on switching rates  $dI_{DS}/dt$  and  $dV_{DS}/dt$  [285].
- Both the statistic and dynamic SiC MOSFET TSEPs have been verified to be affected by the ageing effect in DC power cycling tests [286]. Thus, to make the junction temperature estimation more precise, a decoupling between the junction temperature change and the ageing degradation needs to be conducted to exclude the ageing impact on the junction temperature estimation results.
- In some cases, more than one TSEP could be combined with each other to optimize the estimation. For instance, both the square root of the device saturation current and the threshold voltage have been integrated into the junction temperature measurement to make the estimation more precise [287].

#### 2.4.4. Non-thermal Health Indicators

Other than the temperature related indicators, there is another group of non-thermal parameters that are dedicated to reflecting the ageing effect corresponding to different failure mechanisms of SiC MOSFETs. Below summarizes these health indicators that have been identified for specific failure modes. They could quantify the degradation extent, and further be used to derive corresponding offline lifetime models through ALTs.

- On-state drain-source voltage  $V_{DS\_ON}$  and body diode forward voltage  $V_F$  have been used as the indicators of bond wire lift-off failure through power cycling tests [106].
- Threshold voltage  $V_{TH}$  [51][76][77][122][123][288]–[290], gate leakage current  $I_{GSS}$  [106][291][292], drain leakage current  $I_{DSS}$  [122][121], and Miller plateau voltage  $V_{GS(p)}$  [48][68][69] have been adopted as the indicators of gate oxide failure through high temperature gate bias (HTGB) tests.
- Gate leakage current  $I_{GSS}$  [293] and forward voltage  $V_F$  [64][65][89] have been applied as the indicators of body diode failure through high temperature reverse bias (HTRB) tests.
- The turn-on time has been analyzed as an ageing indicator for SiC MOSFETs in [294]. But no specific package or chip failure has been clarified regarding this indicator.
- The gate-source impedance has been verified as an ageing indicator in [295]. A spread-spectrum time-domain reflectometry hardware has been added to sense this impedance change. So, the degradation could be indirectly detected. But this work does not specify which failure mode it is related to.

Besides, for the dc-link capacitors, the ESR and capacitance [39] have been applied as the indicators of capacitor degradation through floating or cycling aging tests [296][297].

#### 2.4.5. Challenging Online Measurement Techniques

For SiC MOSFETs, the measurement of some parameters is sensitive and requires special implementation techniques. Therefore, a detailed review of these measurement methods is essential for the practical testing regarding the health indicators.

The indicator measurement of SiC MOSFETs generally features the following challenges. The signal amplitude is small, which is hard to detect. The parameter resolution is required to be high enough to fit the fast switching speed. Also, they are susceptible to high-frequency noise. Besides, the inference from other parameters could generate false alarms. In the result analysis, the propagation delay of extra circuits needs to be considered. Furthermore, the interdependence among different physical mechanisms needs to be decoupled to analyze individual physical mechanism. Finally, the implement complexity should be evaluated to select a proper indicator.

To address these challenges, seven approaches have been generally employed. They will be summarized below in detail.

##### 1) Signal Amplifying

To make the small signal more detectable, most techniques have used the operational amplifiers. In the drain leakage current measurement,  $I_{DSS}$  is microampere-level at nominal blocking voltage [74]. Due to aging,  $I_{DSS}$  could reach to milliampere-level [298]. To make  $I_{DSS}$  more detectable, it could be measured at a higher  $V_{DS}$  than the nominal blocking voltage [74]. In the gate leakage current measurement,  $I_{GSS}$  is negligible in normal condition. But the milliampere-level gate current could occur in aged devices [298]. A difference amplifier with an enough bandwidth at designed switching frequency range has been utilized to measure  $I_{GSS}$  by detecting turn-on gate resistance voltage drop. This voltage is then compared to a predetermined threshold voltage to monitor the degradation.

## 2) High Resolution Consideration

The detection resolution and accuracy need to be high enough due to SiC MOSFET typically high switching frequency. An microcontroller unit high resolution capture peripheral with resolution of few hundred picoseconds has been used to measure the nanosecond-level turn-on delay time [294]. In a turn-off delay time measurement, the propagation delay mismatch and jitter of the signal isolator and gate drive IC would adversely affect the measured turn-off delay resolution [299]. This undesirable effect has been alleviated by increasing the gate resistance. In a drain leakage current measurement, the high-resolution requirement cannot be affected by the nominal switching drain-source current [298]. In the gate leakage current measurement, the measurement accuracy of voltage on the gate resistance has been included into the design [298].

## 3) Immunity to High-Frequency Noise

The impact of high-frequency  $dV_{DS}/dt$  overshoot and ringing noise on the measurement accuracy needs to be minimized [300]. Take the peak gate current measurement as an example. The transient noise could be induced by the high-frequency electromagnetic interference, and the switching transient from the gate drive power supply or the current peak detector [279]. To resolve these unexpected issues, additional circuits such as a filter and an amplifier with high common-mode rejection ratio have been utilized. In the measurement of peak gate current, an output filter has been applied to reduce the high-frequency noises at the outputs of the peak current detector and integrator. In the turn-on delay time measurement, to alleviate noise interference, an RC filter has also been designed. The input impedance has been increased with additional paralleled capacitors, high bandwidth buffer circuits [294]. In the turn-off delay time measurement, a series-parallel RC circuit has been included to filter high frequency noise as well [301]. In the gate

leakage current measurement, the amplifier with high common-mode rejection ratio at high switching frequency has been applied to counteract the undesirable noise effect [298].

#### 4) False Alarm Avoidance Due to Other Parameters

Since the detected health indicators interact with other parameters with similar electrical properties in the circuit, it is essential to prevent them from being contaminated by these signals. Hence, a false alarm should be avoided. In the measurement circuit of  $I_{GSS}$ , the amplifier input bias current rating and input offset voltage rating should be small enough in case that it would contaminate the real  $I_{GSS}$ . It has been suggested that input bias current should be at least one order of magnitude smaller than gate leakage current, and the input offset voltage should be at least one order of magnitude smaller than the minimum ageing threshold voltage [298]. Also,  $I_{GSS}$  could be mixed with gate charging current during switching transients, or the current flowing through extra gate-source resistor, protection-purpose Zener diode. To address this issue, a Zener diode with a small leakage current at gate voltages could be used. In the peak gate current measurement, the switching transient properties of SiC MOSFETs are sensitive to the gate bias voltage [279], which would also induce false alarm.

#### 5) Propagation Delay Consideration

Almost every reviewed health indicator circuit involves adding extra analog circuits. As a result, the corresponding propagation delay would impact the detected signal itself. Thus, including this delay time into the final indicator judgment should be noticed. In the turn-on delay time measurement, a propagation delay time of the voltage comparison circuits has been considered in the testing result analysis [294].

## 6) Decoupling Among Different Physical Mechanisms

Some indicators are dependent on more than one physical mechanism. To individually analyze the impact of a certain effect on a specific parameter, a decoupling strategy is normally required. It could be done by either identifying new indicators or developing new measurement methods.

Both the junction temperature rise, and the die ageing could cause the commonly applied TSEPs such as  $R_{DS\_ON}$  to change. Therefore, the real  $T_j$  of the chip cannot be reflected. The body diode's voltage drop at low current and negative  $V_{GS}$  has been utilized as a novel TSEP to decouple the ageing effect and the practical junction temperature rise [141]. On the other hand, if SiC MOSFET degradation needs to be monitored separately, the  $T_j$  effect should be excluded. The  $R_{DS\_ON}$  in saturation region has been measured to reflect the device ageing. And a low  $V_{GS}$  at start-up is applied to decouple the heating effect [302].

The decoupling could also be realized through the improvement of measurement methods. To decouple the self-heating effect at high-current high-voltage region from the real turn-off delay time measurement, this health indicator has been derived by online measuring the intrinsic on-state SiC MOSFET capacitance characteristics extracted from their S-parameters [303]. Another example is the decoupling of the package and chip degradation. As mentioned in Section 2.1, both of these two mechanisms could impact  $V_{DS\_ON}$ . Through utilizing a Kelvin source and drain to measure the chip voltage drop and detecting the bond wire voltage separately, these two failure modes have been monitored individually [290].

## 7) Measurement Complexity Evaluation

For some health indicators, the measurement involves more than one parameter.  $V_{TH}$  is such an example. The measurement of  $V_{TH}$  normally requires a high sensing speed and high

resolution for both drain current and gate-source voltage [294]. As a result, from the perspective of realization complexity, this indicator is not preferred as an ageing indicator.

## 2.5. System-Level Lifetime Extension

The degradation indicator information obtained from online condition monitoring can be applied to not only passively update but also actively control the system lifetime.

Table 2.9 summarizes the active thermal control strategies from the perspectives of topological and control improvement. No SiC MOSFETs have been included in this table because most of the literature has been focusing on the Si based components. The approaches applied to these Si devices could be good references for SiC MOSFET based converter lifetime extension. Two inherent issues exist in this method. Additional thermal control loops are needed. There is a compromise between thermal reliability and overall performance indices such as efficiency, cost, and volume. Active thermal control is normally conducted separately from the lifetime estimation. It can also be conducted together with system lifetime estimation by integrating lifetime and damage accumulation models into active thermal control algorithm [321]. Basically, the control of instantaneous junction temperature  $T_j$  [306], junction temperature swing  $\Delta T_j$  [304], maximum junction temperature  $T_{j\_max}$  [305], average junction temperature  $T_{j\_mean}$  [159], case temperature  $T_C$  [187][269], and heatsink temperature [187] have been targeted. Controlling  $T_{j\_mean}$  and  $\Delta T_j$  together has better lifetime improvement compared with the control of individual parameters [255]. But the hybrid control requires more computational resources. Thus, there exists a tradeoff between the microprocessor capability and control preciseness.

Table 2.9. Summary of the Active Thermal Control Strategies

Groups	Control methods	Devices	Realization details		
			If	Then	
Topology	Adaptive gate drive	GaN HEMT [304]	$T_C \uparrow$	$V_{GS}$ first-step duration $\uparrow \rightarrow P_{loss} \uparrow \rightarrow T_j \uparrow \rightarrow \Delta T_j \downarrow$	
		Si IGBT [305]	Load current $\downarrow$	$R_g \uparrow \rightarrow P_{sw} \uparrow \rightarrow T_j \uparrow \rightarrow \Delta T_j \downarrow$	
		Si MOSFET [306]	$R_{DS\_ON} \uparrow$	$V_{GS}$ amplitude $\downarrow \rightarrow T_j \downarrow$	
Control	Switching frequency control	Si IGBT [255][307][308]	Load current $\uparrow$	$f_{sw} \uparrow \rightarrow P_{sw} \uparrow \rightarrow \Delta T_j \downarrow$	
	Active cooling control	Si IGBT [309]	$T_j \uparrow$	Open-loop feed-forward control of $P_{loss}$ and $\Delta T_a$	
			$\Delta T_j \uparrow$	Close-loop feed-back control of temperature	
	PWM control modification	Si IGBT [310]	$P_o \uparrow$	DPWM clamping angle $\uparrow \rightarrow P_{loss} \downarrow \rightarrow T_j \downarrow$	
		Si IGBT [18]	$T_j \uparrow$	$V_{dc\_link} \downarrow$	$\rightarrow P_{sw} \downarrow \rightarrow T_j \downarrow$
				DPWM	$T_j \downarrow$
		Si IGBT [311]	$T_j \uparrow$	Optimize redundant switching states $\rightarrow P_{loss} \downarrow \rightarrow T_j \downarrow$	
		Si MOSFET [312]	Phase current $\uparrow$	Duty cycle $\downarrow \rightarrow P_{cond} \downarrow \rightarrow T_j \downarrow$	
		Si IGBT [313]	Device current $\uparrow$	Optimize redundant space voltage vectors $\rightarrow P_{loss} \downarrow \rightarrow T_j \downarrow$	
	Si IGBT [314]	$P_o \uparrow$	Duty cycle $\downarrow \rightarrow P_{loss} \downarrow \rightarrow T_j \downarrow$		
	Turn-off delay time control	Si IGBT [315]	$\Delta T_j \uparrow$	$R \downarrow$ or $C \downarrow$ in RC snubber circuit $\rightarrow P_{off} \downarrow \rightarrow \Delta T_j \downarrow$	
	Hybrid control	Si IGBT [316]	$T_j \uparrow$ or $\Delta T_j \uparrow$	$f_{sw} \downarrow \rightarrow P_{sw} \downarrow$	
				Duty cycle $\downarrow \rightarrow P_{cond} \downarrow$	
				$f_{sw} \downarrow$	
	Si MOSFET [317][318]	$T_{j\_mean} \uparrow$ or $\Delta T_j \uparrow$	Load current $\downarrow$		
$f_{sw} \downarrow$					
Si IGBT [319]	$T_j \uparrow$	Load current $\downarrow$			
System-level control	Si IGBT [320]	$\Delta T_j \uparrow$	Reactive power injection $\rightarrow \Delta T_j \downarrow$		

From the perspective of the topological improvement, most lifetime extension strategies have been focused on the adaptive gate drives, which are configured with either analog or digital circuits. In spite of the lower cost, the analog circuits have intrinsic weakness of adjusting control parameters and realizing fast switching [322]. The switching frequency is kept constant in this method. Below are some examples related to this approach. First, the case temperature changing rate has been controlled to adjust the turn-on transient duration, which is related to switching loss [304]. But there exists delay time between the change of junction and case temperature. Second, the load current has been controlled to adjust the gate resistance [305]. Both the  $T_{j\_max}$  and  $\Delta T_j$  have been reduced without  $T_j$  measurement. But the impact of parameter variation has not been analyzed. Third, the gate resistance has been changed to reduce both the  $T_{j\_max}$  and  $\Delta T_j$  [305]. Fourth, the  $V_{GS}$  amplitude has been adjusted to decrease the  $T_j$  by tracking  $R_{DS\_ON}$  change [306].  $V_{GS}$  increase causes smaller  $R_{DS\_ON}$ , compensating  $R_{DS\_ON}$  increase due to temperature rise. Thus, the efficiency has been improved.

From the perspective of control methods, the switching frequency control, active cooling control, active power control, PWM control modification, turn-off delay time control, hybrid control, and system-level control have been studied. The detailed demonstration for each of these methods will be presented in the following parts.

- 1) Switching frequency  $f_{sw}$  control

The switching frequency  $f_{sw}$  control has been carried out either separately or with other parameters. It is independent of the load cycles. The switching loss increases with higher  $f_{sw}$ , while the peak current per switching cycle rises with lower  $f_{sw}$  [314]. Thus, there is a trade-off between the efficiency and the device current stress. The  $f_{sw}$  has been changed through a hysteresis controller [159][255][307][308][323].  $\Delta T_j$  is derived from power loss modeling and used as the

input of the controller. Besides, the  $f_{sw}$  has also been controlled together with the load current to adjust  $T_j$  [316][317][319].

## 2) Active cooling control

This approach has been conducted without estimating junction temperature [309]. Feed-forward open-loop power loss and ambient temperature control are carried out to improve the dynamic response. Feedback closed-loop baseplate temperature control is intended to reduce the temperature swing. Although the temperature stress of devices could be decreased, two additional control loops make it relatively complex.

## 3) Active power control

Active power control has been applied to limit the maximum photovoltaic (PV) output power [324]. Thermal loading is reduced by combining active power control and maximum power point tracking. However, PV panel degradation has not been included [325]. Therefore, the long-term overall reliability evaluation is not accurate.

## 4) PWM control modification

Most PWM modification techniques have been conducted in Si IGBTs. They could induce issues such as the distorted output waveforms with high THD. To improve the quality of the output waveform, DPWM is applied with variable dc-link voltage control [18]. However, it suffers from unstable input voltage. Below lists the state-of-art literature regarding this PWM control modification method.

- The clamping angle of DPWM has been controlled to reduce the switching loss and corresponding thermal stresses of power devices in a cascaded H-bridge converter [310]. But it suffers from high output THD at the light load.

- Different from conventional PWM control, two modulation waveforms have been adopted in the improved DPWM scheme to realize active thermal control [326].
- DPWM1 method has been implemented in a hysteresis controller to decrease the thermal cycle amplitude [323].
- Improved carrier phase-shift algorithm has been used to optimize the gate switching sequence so that both the  $T_j$  and  $\Delta T_j$  thermal stresses of the switches are alleviated [311]. But neither the THD nor the cost has been well designed.
- Space vector pulse width modulation (SVPWM) has been adopted to reduce the loss in multilevel topologies [313]. One issue with this method is that the loss control and neutral point voltage control cannot be conducted simultaneously.
- Duty cycle has been used as the control parameter to decrease the power loss of devices in the isolated converter [314]. Although this method has fast response and simple implementation, there is a tradeoff between cost and efficiency.
- Switching states of submodules in modular multilevel converter have been controlled according to the temperature to achieve the thermal balancing among submodules [327]. The submodule capacitor temperature could also be regulated by controlling the capacitor voltage [328]. But this method suffers from a small thermal adjustment range constrained by the constant total arm voltage requirement.
- Improved PWM method has been used in Si MOSFETs to adjust the switch thermal stress in DC-to-DC and dc-ac interleaved converters [312]. Although only one control loop is needed, the cost is increased due to full-scale components.

#### 5) Turn-off delay time control

The turn-off delay time control has been conducted in Si IGBTs by introducing a turn-off trajectory adjustment circuit [315]. Individual thermal control is achieved. The turn-off loss is adjusted by the IGBT turn-off trajectory so that the  $\Delta T_j$  is decreased. It is useful in controlling the individual power loss of each device. However, the volume and cost are increased. Overall efficiency is discounted due to the additional circuit.

#### 6) Hybrid control methods

The technique combining two or more of the previous control strategies has also been extensively investigated. First, PWM selection between SVPWM and DPWM is done accompanying with the switching frequency modification to decrease the power loss [329]. However, there is a tradeoff between the output current waveform quality and the device lifetime. Second, the control of switching frequency, PWM method, load current has been conducted at the same time in [316]. Although this method is cost effective, it suffers from complex control. Third, the switching frequency and duty cycle are both controlled in [317][318]. But  $T_j$  is not strictly adjusted due to parameter drift with temperature. Fourth, the switching frequency and load current are both controlled in [319] to optimize the torque and efficiency at the same time. But the variability of load current is required to achieve this optimization.

#### 7) The system-level active thermal control

The system-level active thermal control has been implemented through the reactive current control in an individual converter or load sharing control among multiple converters. First, the reactive current control has been conducted to stabilize the device  $\Delta T_j$  in a three-level neutral-point-clamped inverter [320]. But the reactive current brings in additional thermal imbalance

issues. Second, the active power is controlled between two paralleled three-phase PWM inverters [330]. The average switch thermal stresses have been balanced.

According to the above summarization, some opportunities could be further explored in the active thermal control domain concerning the SiC MOSFET based power converters.

- Most of the active thermal control is based on the Si MOSFETs and Si IGBTs. Since temperature dependent characteristics of SiC MOSFET electrical parameters are different as analyzed in the previous sections, the active thermal control methods should be further investigated. For example, due to less temperature dependent on-state resistance in SiC MOSFETs, adjusting on-state resistance to compensate for the shift caused by temperature rise could be considered.
- Qualitative improvement has been extensively analyzed in the state-of-art active thermal control literature by observing the temperature decrease. It is necessary to make a quantitative comparison of both the lifetime improvement and the efficiency sacrifice for SiC power converters in the further research concerning lifetime modeling.

## **2.6. Summary for This Chapter**

A literature overview of the lifetime prediction and extension for SiC MOSFET based power converters is presented. SiC MOSFET chip-level, package-level failure modes, and mechanisms are summarized. Based on the individual failure indicators, the accelerated lifetime tests are discussed. Component-level RUL estimation is conducted including PoF lifetime models, data-driven lifetime models and hybrid models. Also, component-level cycle counting algorithms and fatigue damage accumulation approaches are reviewed. System-level lifetime estimation methods are further investigated. The component-level and system-level lifetime modeling software has been summarized based on the state-of-the-art academic and commercial

development. Online monitoring techniques concerning junction temperature related parameters and other non-thermal degradation indicators are analyzed. Finally, the system-level lifetime extension strategies are compared. By online updating the ALT-based static lifetime model, the overall system lifetime estimation accuracy could be improved. Based on the above analysis, some recommendations are made for future possible research directions in the SiC power converter lifetime prediction and extension area.

- The SiC MOSFET failure criteria of some emerging indicators have not been well studied. For instance, the Miller plateau amplitude and time duration for gate oxide breakdown, as well as the drain leakage current and forward voltage for body diode degradation have not been covered regarding the failure thresholds in the existing ALT standards. Besides, the failure criteria of the on-state voltage and on-state resistance for bond wire lift-off, as well as the thermal resistance for solder fatigue are also needed concerning SiC MOSFETs in corresponding standards. These regulations would help institutions and manufacturers conduct the fair reliability comparison among different SiC products.
- SiC MOSFET ALT designs need to be investigated due to their individual failure indicator shifting mechanisms.
- Most published physics-of-failure lifetime models for SiC MOSFETs are based on Si IGBT power modules. Considering the differences in the failure mechanisms between Si and SiC, the PoF lifetime models including SiC reliability characteristics would lead to more accurate lifetime prediction.
- Most published power electronic lifetime research has done detailed parameter estimation by using the Monte Carlo statistical extrapolating method. The statistical strategies such as

reviewed extended Kalman filter, particle filter and artificial intelligence are to be further compared with the Monte Carlo technique in the SiC MOSFET power converters.

- Palmgren-Miner's Law has been widely used in fatigue damage accumulation. Rather than sticking with this linear method, the nonlinear damage accumulation methods such as the Manson Halford model is to be investigated in the SiC MOSFET power converters. The fair comparison among different accumulation approaches is useful to improve the accuracy of lifetime prediction, especially considering the loading level dependence in SiC MOSFET power converters.
- Much system lifetime modeling has been conducted in the Si IGBT based inverters by using a reliability block diagram or Markov chain. SiC MOSFET based lifetime models following Weibull distribution with the inconstant failure rate could be studied. Also, the comparison by using different system lifetime models would help optimize the system-level lifetime prediction accuracy in SiC MOSFET power converters.
- Package-level thermo-mechanical modeling for the SiC MOSFETs has not been given enough attention to. The thermo-mechanical modeling difference between SiC MOSFETs and Si devices is necessary to improve the SiC MOSFET lifetime prediction accuracy and further provide design directions to enhance their package-level reliability.
- How to optimally apply the monitored parameter information to update the initial ALT-based statistical lifetime models would be further investigated for SiC power converters.
- Although both of the thermal and non-thermal health indicators have been well studied for SiC MOSFETs, they are still in a relatively emerging domain and could be further explored. For example, the Miller plateau time duration has only been studied in the Si

IGBT degradation. The output voltage harmonics have been used to indicate Si IGBT module solder fatigue and could be investigated in SiC MOSFETs as well.

- In the condition monitoring area, seldom literature has explored the system-level condition monitoring of SiC MOSFET based power converter. This technique plays an essential part in an accurate system-level lifetime prediction and thus should be investigated further.
- Controlled parameters in SiC MOSFET based power converter active thermal control could unfold other research opportunities, considering the TSEP temperature-dependent characteristics are different from Si devices.
- Instead of resting on the qualitative analysis, further quantitative comparison among different active thermal control approaches is necessary to make a reasonable tradeoff among lifetime, efficiency, and power density for the gradually widespread applications of SiC power converters.

### 3. SiC MOSFET GATE OXIDE DEGRADATION INVESTIGATION

SiC MOSFETs have been widely used in the applications with high power density [331] [332], high temperature [333] and high efficiency [333]. SiC Schottky diodes have been applied to reduce switching losses and increase the system efficiency due to negligible reverse recovery [334]. However, SiC device gate oxide reliability problem still remains to be investigated, which has been widely researched these years [30], [31], [61], [335]. Although improvements have been well studied in the design, modeling, and fabrication of SiC MOSFETs [336] and SiC Schottky diodes [337] [338], there are still two critical issues about the SiC-SiO<sub>2</sub> interface [25]. The first issue is related to the low inversion layer mobility caused by the poor quality of SiC-SiO<sub>2</sub> interface. The second one is the susceptibility of gate oxide to rupture caused by the high electric field within gate oxide.

Compared with the gate oxide of Si devices, naturally formed oxide in SiC devices faces poorer inversion channel mobility and higher interface state density in the SiC-SiO<sub>2</sub> interface [30], which reduces the barrier height between SiC and SiO<sub>2</sub>, especially at high temperature [31]. As a result, the carrier injection in the oxide increases and the resultant carrier non-equilibrium causes gate oxide dislocation. Besides, the smaller conduction band offset between SiC and SiO<sub>2</sub> induces higher leakage current and lower breakdown field in SiC MOSFET gate oxide [31]. Thus, gate oxide in SiC MOSFET has intrinsic lower reliability compared with that of Si devices. Two stresses have been widely studied because of their contribution to the degradation of SiC MOSFET gate oxide. On one hand, the temperature stress plays an important role in the SiC MOSFET gate oxide degradation. This is because the Time Dependent Dielectric Breakdown of SiC MOSFET gate oxide is closely related to temperature [31]. On the other hand, the gate oxide of SiC MOSFET

is more susceptible to electric field stress than Si counterparts. It results from the fact that SiC has higher critical electric field for avalanche breakdown compared with Si [66].

Most extensively researched gate oxide degradation indicators are threshold voltage, drain leakage current and gate leakage current [339]. Threshold voltage [51], [76], [77], [122], [123], [288], [289] and drain leakage current [122] [121] are commonly detected with the tested switch interrupted from normal operation [75], which makes them difficult for online monitoring. As to the gate leakage current, the  $\mu\text{A}$ -level amplitude makes it challenging to be detected [70] [82].

Miller plateau width has been proved to increase with junction temperature of a half-bridge IGBT module [282]. Thus, it has been used as a TSEP for the online monitoring of IGBT junction temperature. Furthermore, Miller plateau shift in a Si power MOSFET has been shown to have more correlation with the HEF stress in gate oxide than the gamma irradiation induced stress [68]. However, the relationship between ambient temperature and Miller plateau shift is not mentioned. Besides, the experiment is only based on Si MOSFET.

In this chapter, the Miller plateau shift with ambient temperature and HEF stress will be highlighted in SiC MOSFET. The Miller plateau shift with gate oxide electric field is first analyzed theoretically. After that, the relationship of Miller plateau at switching transients and ambient temperature is simulated and theoretically explained. Besides, HEF ageing tests and double pulse tests are done to verify the relationship between Miller plateau and gate oxide electric field stress with different  $V_{GS}$  stress amplitude applied for different stress duration. Following it are the comparison and analysis among three indicators, i.e. Miller plateau, threshold voltage and gate resistor turn-on energy. Finally, the conclusion and future opportunities in this area are given.

### 3.1. Theory of Miller Plateau Shift With Gate Oxide Electric Field

In Figure 3.1, the SiC MOSFET turn-on waveforms are captured at the second pulse rising transient in the double pulse test with the DC-link voltage  $V_{DC}$  equal to 300 V. To magnify the Miller plateau region for further evaluation and comparison, both the turn-on and turn-off gate resistors are selected with the resistance of  $33 \Omega$ .

As shown in in Figure 3.1, during  $t_1$  period, the gate-source capacitor  $C_{GS}$  is charged. And when  $C_{GS}$  is charged to the threshold voltage  $V_{TH}$ , drain current begins to flow through drain and source. During  $t_2$  period,  $C_{GS}$  continues to be charged until the drain current reaches designed current and stays constant while the drain-source voltage  $V_{DS}$  starts to fall. During  $t_3$  period, MOSFET operates in saturation region. Miller plateau starts when  $I_D$  reaches the peak and  $V_{DS}$  begins to drop. It ends when gate-drain capacitor or the miller capacitor  $C_{GD}$  is fully charged and  $V_{DS}$  comes to zero.

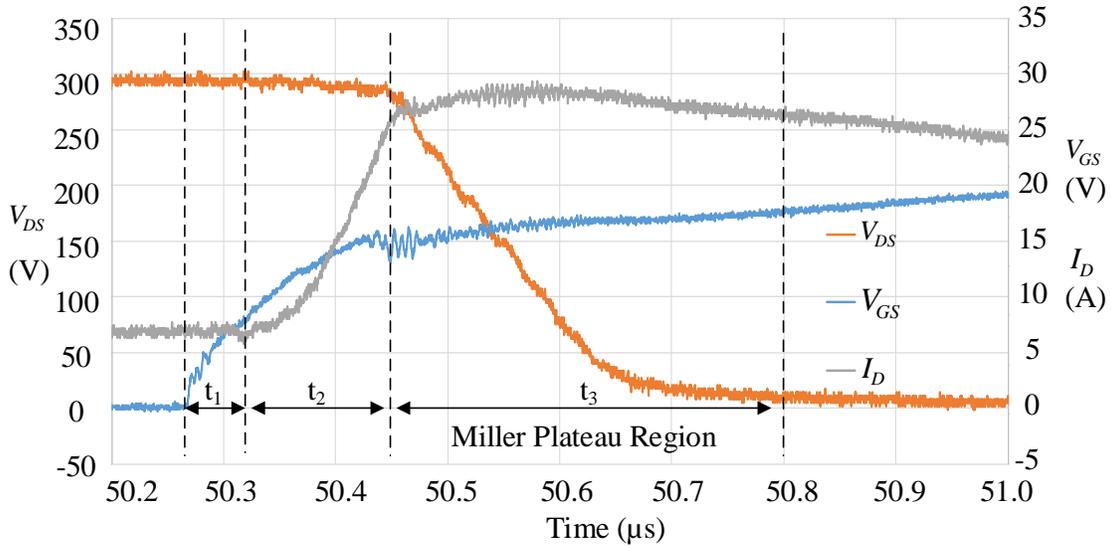


Figure 3.1. SiC MOSFET turn-on waveforms with Miller plateau region highlighted

According to MOSFET quadratic model [72], considering the channel length modulation of SiC MOSFET [73], improved saturated drain current  $I_D$  can be shown in (Eq.3.1).

$$I_D = \mu_N^* \cdot C_{OX} \cdot \frac{W}{2L} \cdot (V_{GS\_MP} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS}) \quad (\text{Eq.3.1})$$

where,  $\mu_N^*$  is the electron mobility.  $C_{OX}$  the oxide capacitance.  $W$  and  $L$  are the gate width and length, respectively.  $V_{GS(p)}$  is the miller plateau voltage.  $V_{TH}$  the threshold voltage.  $\lambda$  the channel length modulation factor. From (Eq.3.1),  $V_{GS(p)}$  is further derived in (Eq.3.2).

$$V_{GS(p)} = \sqrt{\frac{2 \cdot I_D \cdot L}{\mu_N^* \cdot C_{OX} \cdot W \cdot (1 + \lambda \cdot V_{DS})}} + V_{TH} \quad (\text{Eq.3.2})$$

As  $V_{GS}$  stress increases, the gate oxide electric field is strengthened, which causes electrons to be confined to the SiC-SiO<sub>2</sub> interface. Thus, the electron scattering is increased at the interface and the electron mobility  $\mu_N^*$  is decreased. From (Eq.3.2), the  $V_{GS(p)}$  will increase correspondingly. Therefore, the above analysis provides necessary theoretical support for the Miller plateau shift with the gate oxide electric field.

### 3.2. Theory and Simulation Verification of Miller Plateau Shift With Temperature

The relationship between Miller plateau and temperature can be analyzed based on two temperature dependent parameters, i.e. threshold voltage  $V_{TH}$  and electron mobility  $\mu_N^*$ .

On one hand, as illustrated in [279],  $V_{TH}$  can be affected by junction temperature  $T_j$ . Besides,  $V_{TH}$  is a function of the temperature-dependent ionized acceptor concentration  $N_A^-$  [66]. (Eq.3.3) gives a physical description of threshold voltage.

$$V_{TH} = \frac{\Phi_{GS}}{q} - \frac{Q_F}{C_{OX}} - \frac{Q_{IT}(\psi_S = 0)}{C_{OX}} + \frac{2KT}{q} \cdot \ln\left(\frac{N_A^-}{n_i}\right) + V_S + \frac{1}{C_{OX}} \cdot \sqrt{2q \cdot \epsilon_S \cdot N_A \cdot \left[ \frac{2KT}{q} \cdot \ln\left(\frac{N_A^-}{n_i}\right) + V_S \right]} \quad (\text{Eq.3.3})$$

where,  $\Phi_{GS}$  is gate-semiconductor work function.  $Q_F$  is fixed charge density.  $Q_{IT}(\psi_S=0)$  is charge density of interface states at flat band.  $\psi_S$  is the surface potential.  $N_A^-$  is ionized acceptor concentration.  $N_A$  is the total acceptor concentration.  $n_i$  is intrinsic carrier concentration.  $\epsilon_S$  is

dielectric constant of the semiconductor.  $q$  is elementary charge constant.  $V_S$  is the potential of MOSFET source.

The ionized acceptor concentration  $N_A^-$  decreases as temperature goes up. Considering stronger impact of  $N_A^-$  compared with the temperature itself [340], based on (Eq.3.3),  $V_{TH}$  is negatively temperature-dependent.

On the other hand, the electron mobility  $\mu_N^*$  is inversely proportional to the total scattering rate. According to Matthiessen's rule [66],  $\mu_N^*$  can be described in (Eq.3.4).

$$\frac{1}{\mu_N^*} = \frac{1}{\mu_B} + \frac{1}{\mu_{SP}^*} + \frac{1}{\mu_C^*} + \frac{1}{\mu_{SR}^*} \quad (\text{Eq.3.4})$$

where,  $\mu_B$  is the mobility of electrons due to bulk phonon scattering in the bulk semiconductor;  $\mu_{SP}^*$  the phonon-limited mobility due to surface phonon scattering;  $\mu_C^*$  the mobility due to Coulomb scattering;  $\mu_{SR}^*$  the mobility due to surface roughness scattering.

As temperature increases, bulk phonon scattering rate  $1/\mu_B$  and surface phonon scattering rate  $1/\mu_{SP}^*$  also increase, while the Coulomb scattering rate  $1/\mu_C^*$  and surface roughness scattering rate  $1/\mu_{SR}^*$  decrease. Since the increase of bulk phonon scattering rate is more obvious than the other scattering rates [66], the total scattering rate  $1/\mu_N^*$  slightly increases with temperature. Therefore, the overall electron mobility  $\mu_N^*$  decreases with temperature.

Thus, based on the negative temperature dependence of both  $V_{TH}$  and  $\mu_N^*$ , from (Eq.3.2),  $V_{GS(p)}$  is associated with temperature. To further investigate whether the temperature dependence of Miller plateau is negative or positive, the thermal simulation has been carried out by using the SPICE models of SiC MOSFET SCT2120AF from Rohm and SiC Schottky Diode C3D08060A from Cree based on the double pulse test simulation platform in LTSpice. In Figure 3.2, Miller plateau decreases as ambient temperature increases. From (Eq.3.2), the negative temperature

dependence of  $V_{GS(p)}$  can be explained when the electron mobility  $\mu_N^*$  has weaker temperature-dependent effect on Miller plateau than threshold voltage  $V_{TH}$ .

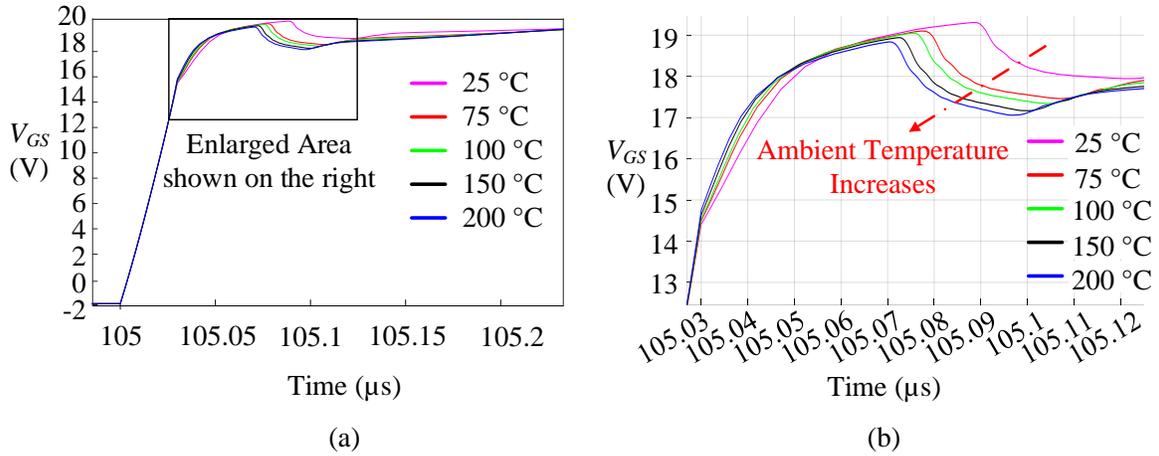


Figure 3.2. SiC MOSFET Miller plateau shift with different ambient temperature

### 3.3. Gate Oxide Accelerated Lifetime Test

As discussed in Section 2.2.1, the high temperature gate bias test is normally adopted to accelerate the degradation of the gate oxide. In this part, two accelerated tests will be conducted based on this approach. One is the high electric field stress test, which applies a higher-than-normal  $V_{GS}$  to the gate and source pins. The other one further takes the temperature impact into the consideration, which brings in not only the  $V_{GS}$  stress but also the temperature stress. The test platform design and set-up will be presented in the following.

#### 3.3.1. High Electric Field Stress Accelerated Lifetime Test

To accelerate gate oxide degradation, HEF ageing test is done with the circuit [68] [341] and platform shown in Figure 3.3 (a) and (b), respectively. In Figure 3.3 (b), from left to right,  $V_{GS}$  with amplitude of 25V, 30V, 35V, 40V has been used to stress SiC MOSFETs. In our experiments, 20 groups of tests have been designed. In each group, 5 SiC MOSFETs from the same batch are stressed. And 10, 40, 70, 85, 100 hours have been applied for different stress duration needs. The

positive maximum rating of  $V_{GS}$  in SCT2120AF is + 22V [342]. From the test results, when  $V_{GS}$  is between 40V and 45V, the gate and source have been shorted and gate oxide has probably been broken once the voltage has been applied. Similar HEF tests have been conducted in [68] based on Si MOSFET IRF520 from Vishay Intertechnology, whose positive maximum rating of  $V_{GS}$  is +20V [343]. From [68], the  $V_{GS}$  stress can reach up to 65V for 10 hours without breaking down the gate oxide of Si MOSFET. This is consistent with the intrinsic lower reliability of the gate oxide in SiC MOSFETs compared with Si MOSFETs, considering these two devices share similar  $V_{GS}$  absolute maximum ratings.

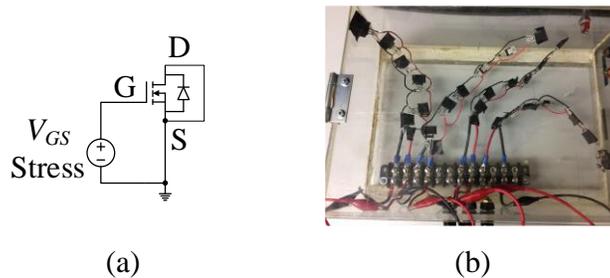


Figure 3.3. HEF acceleration test (a) circuit, (b) platform

### 3.3.2. Positive Bias Temperature Stress Accelerated Lifetime Test

Other than the HEF stress, the thermal stress is another aspect that would affect the gate oxide lifetime. In this part, the positive bias temperature stress testing will be conducted. The SiC MOSFETs under test have been stressed at 35 V and 40 V  $V_{GS}$  voltage for about 190 hours. Figure 3.4 (a) shows the voltage power supplies outside the thermal chamber, which provide the gate-source voltage to the inside devices under test. Figure 3.4 (b) presents the ESX-2CA thermal chamber. The tested SiC MOSFETs inside the chamber are shown in Figure 3.5.

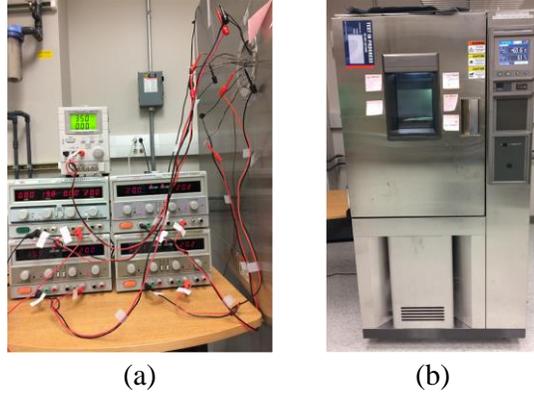


Figure 3.4. Positive bias temperature stress test platform: (a) power supplies (b) thermal chamber

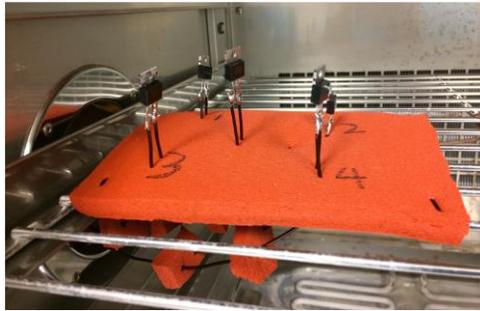


Figure 3.5. SiC MOSFETs under tests inside the thermal chamber

### 3.4. Indicator Verification Test and Analysis

After ageing test, the stressed devices are put into double pulse platform for dynamic performance tests. The double pulse test circuit and designed double pulse test board are shown in Figure 3.6 (a) and (b), respectively. In Figure 3.6 (a), SCT2120AF from Rohm has been used as SiC MOSFET, which has the voltage rating 650V and the pulsed drain current 72 A. C3D08060A from Cree has been selected as the SiC Schottky Diode, which has the voltage rating 600 V and non-repetitive peak forward surge current 71 A. The inductance has been calculated by (Eq.3.5).

$$L \geq \frac{V_{DC} \cdot t_{sw}}{\Delta I_L} = \frac{300V \cdot 25\mu s}{30A} = 250\mu H \quad (\text{Eq.3.5})$$

where  $V_{DC}$  is the DC input voltage.  $t_{sw}$  is the switching time, which is the high level duration of the pulses. In the tests, this duration is set in the Code Composer Studio C-code editor by using TI MSP430 microcontroller. Here,  $25 \mu s$  has been applied to  $t_{sw}$ .  $\Delta I_L$  is the variation of inductor current from the test waveforms. Based on (Eq.3.5), a  $270 \mu H$  air core inductor has been wound.

To avoid the transient  $V_{DS}$  overshoot, the parasitic series inductance current path composed of clamp ceramic capacitors, SiC MOSFET, SiC Schottky diode and the power ground has been minimized. The double pulse test platform is shown in Figure 3.6 (c).

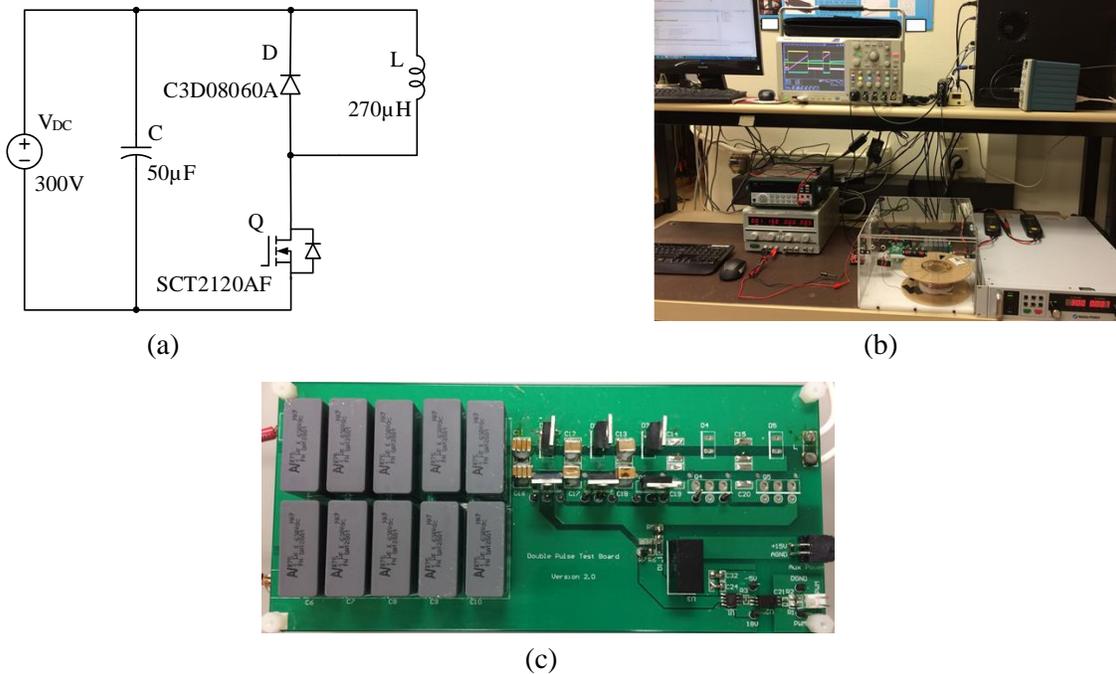


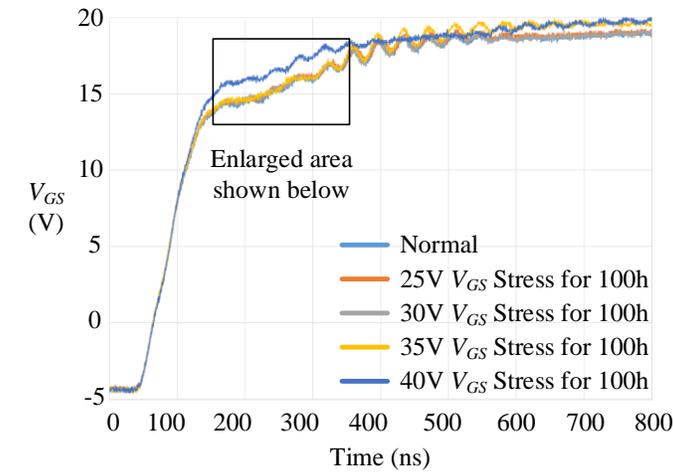
Figure 3.6. Double pulse test (a) circuit schematic, (b) platform, and (c) board

### 3.4.1. Miller Plateau Shift Verification and Analysis

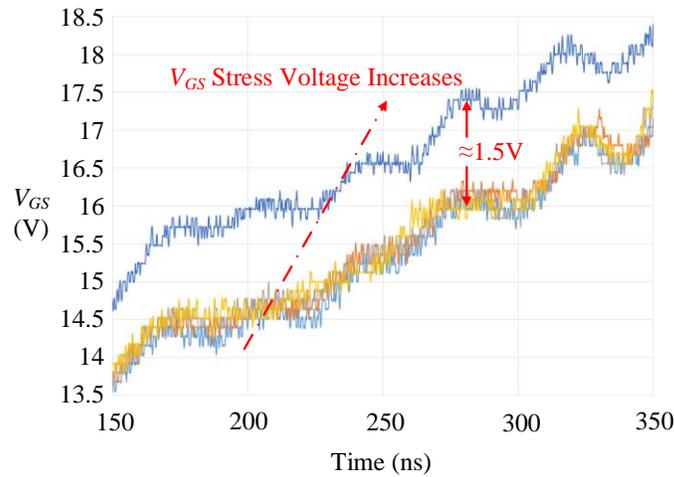
In Figure 3.7, under 300 V DC-link voltage, the double pulse test results show the Miller plateau rises with  $V_{GS}$  stress amplitude. From Figure 3.7, the Miller plateau increase is not proportional with the change of the stress amplitude. As the stress amplitude becomes larger, the Miller plateau shows a more significant shift. In Figure 3.8, the test results illustrate that the Miller

plateau also rises with  $V_{GS}$  stress duration. After 100-hour HEF tests with 40 V  $V_{GS}$  stress, the maximum Miller plateau shift is about 1.5 V. These test results match the theoretical analysis of Miller plateau shift with gate oxide electric field in Part 3.2.

In Figure 3.7 and Figure 3.8, both the turn-on and turn-off gate resistance is 33  $\Omega$ , which is larger than the usually used. By applying a larger gate resistance, smoother Miller plateau with longer duration can be captured, which is helpful for the comparison. In order to clarify this, the Miller plateau shift with gate resistance needs to be further explored.

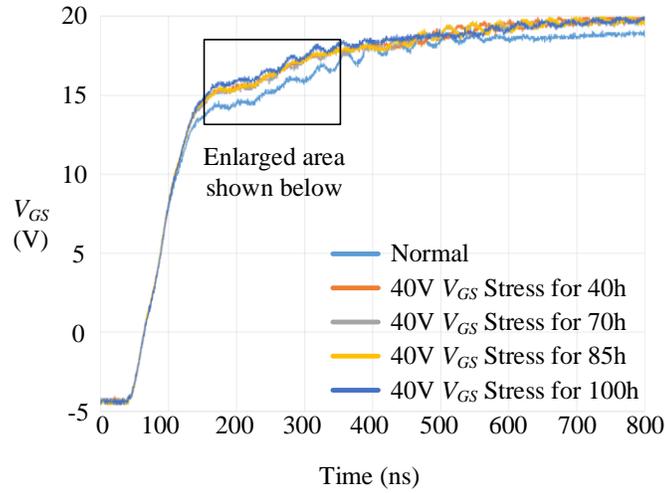


(a)

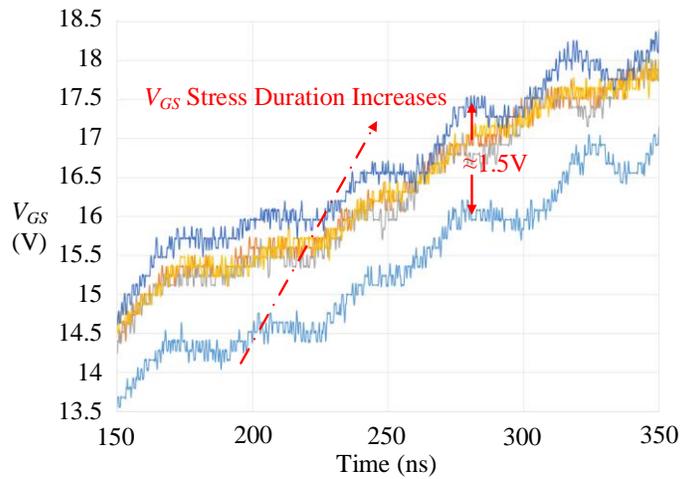


(b)

Figure 3.7. Miller plateau shift with different  $V_{GS}$  stress after 100-hour duration



(a)



(b)

Figure 3.8. Miller plateau shift with the different duration of 40V  $V_{GS}$  stress

In Figure 3.9, tested with devices having experienced 100-hour 40 V  $V_{GS}$  stress, the Miller plateau shift with 3  $\Omega$ , 10  $\Omega$ , 33  $\Omega$  external gate resistance  $R_{g\_ext}$  is shown. The Miller plateau shift decreases as  $R_{g\_ext}$  increases. And the Miller plateau difference between 3  $\Omega$  and 33  $\Omega$   $R_{g\_ext}$  applications is about 5 V. As the gate resistance increases, the gate charging current flowing through the Miller capacitor would decrease. Therefore, it takes longer time to charge  $C_{GD}$ . The resultant Miller plateau is wider and smoother with larger gate resistance, which causes the

amplitude to be smaller. Besides, larger gate resistance would alleviate the unexpected resonance among the MOSFET internal  $C_{GD}$ ,  $C_{GS}$ , parasitic inductance, and gate resistance, which also contributes towards a smoother Miller plateau.

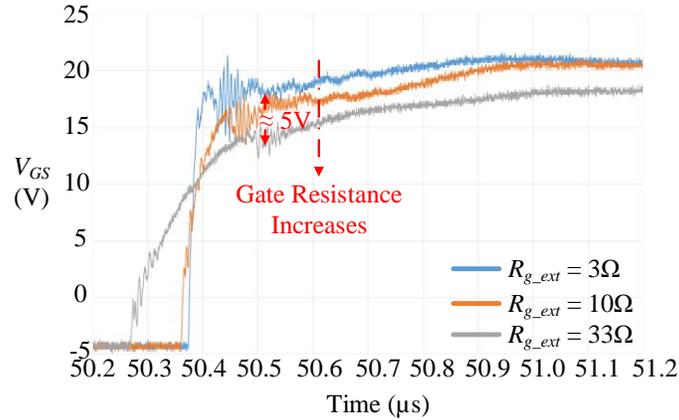


Figure 3.9. Miller plateau shift with gate resistance after 100-hour 40-V  $V_{GS}$  stress

The impact of the positive bias temperature stress on the Miller plateau amplitude has also been verified through the double pulse test platform. Figure 3.10 presents the gate-source voltage of the normal MOSFET and those after 35-V  $V_{GS}$  stress lasting for 189 hours. It can be seen that the temperature stress has relatively small impact on the  $V_{GS}$  shifting, compared with the  $V_{GS}$  stress.

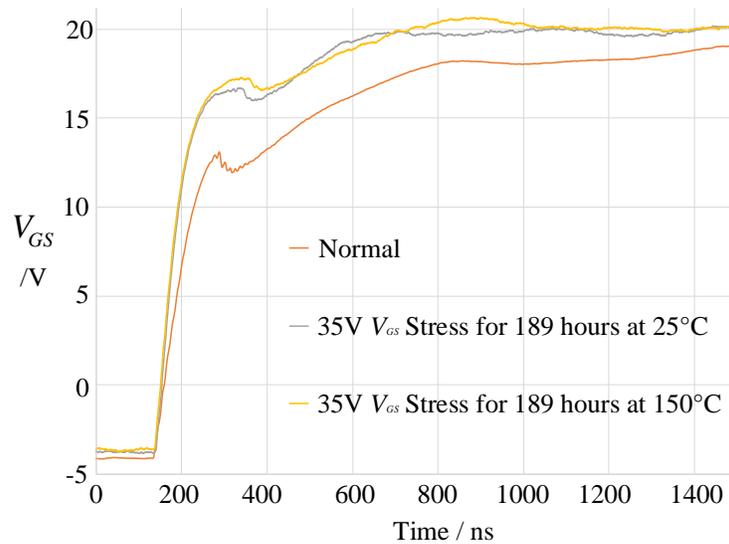


Figure 3.10.  $V_{GS}$  of the normal MOSFET and those after positive bias temperature stress tests

### 3.4.2. Threshold Voltage Verification Test and Analysis

The extraction of threshold voltage can be conducted with the MOSFETs operating in the linear region or saturation region [75]. A widely used method in industry is based on the  $I_D - V_{GS}$  curve of MOSFETs operating in the linear region. The corresponding  $V_{TH}$  measure circuit is shown in Figure 3.11 [342] [125]. In this method, the drain and gate are shorted. An adjustable DC voltage source is put between gate and source. A current meter is placed between the source and negative terminal of the voltage source. In this project, threshold voltage is extracted by using this method.

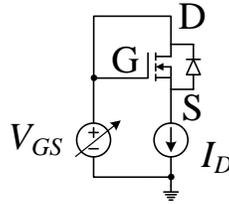


Figure 3.11. Threshold voltage measurement circuit

Based on the tested  $V_{GS}$  and  $I_D$  values, the discrete data points are fitted by the curve fitting function in MATLAB. To exclude the impact of the differences among the tested SiC MOSFETs themselves on the test results, three randomly selected normal SiC MOSFETs are tested with the circuit in Figure 3.11. According to the test results shown in Figure 3.12, when  $I_D$  is 3.3 mA, the maximum  $V_{TH}$  difference is smaller than 0.1 V. To show the impact of different  $V_{GS}$  stress amplitude and duration on  $V_{TH}$  shift, two clusters of experimentally measured  $V_{GS} - I_D$  curves are put in Figure 3.13 (a) and (b), respectively. Similarly, the threshold voltage can be observed when the drain current  $I_D$  is 3.3mA. From Figure 3.13 (a), when stress duration is 100 hours, as the  $V_{GS}$  stress amplitude increases, threshold voltage also rises. From Figure 3.13 (b), threshold voltage increases with the stress duration at a fixed stress amplitude 40 V.

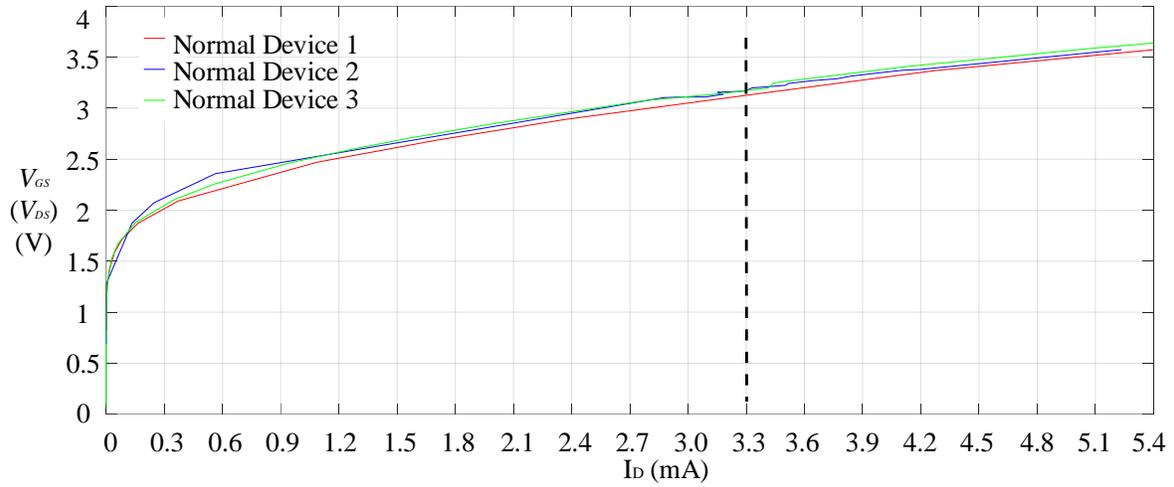


Figure 3.12. Experimentally tested  $V_{GS} - I_D$  curves of three normal SiC MOSFETs

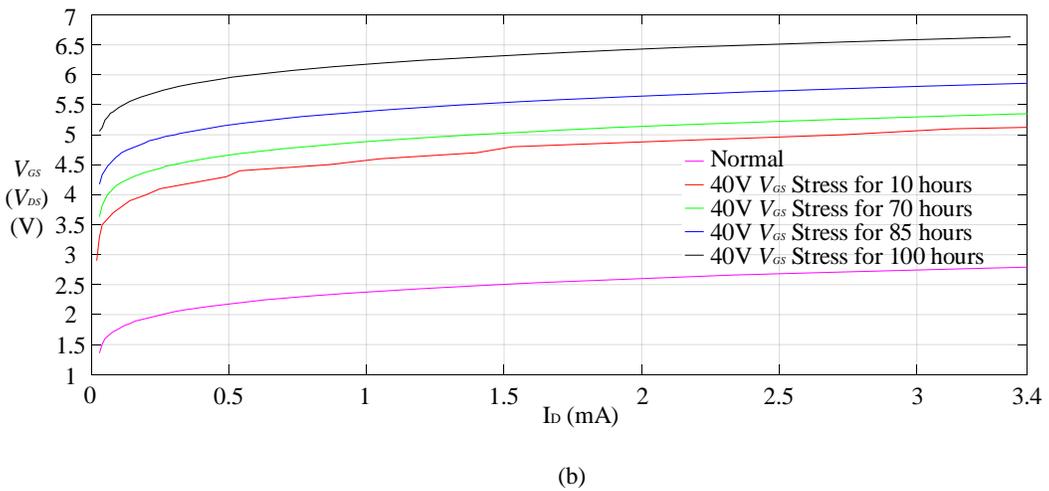
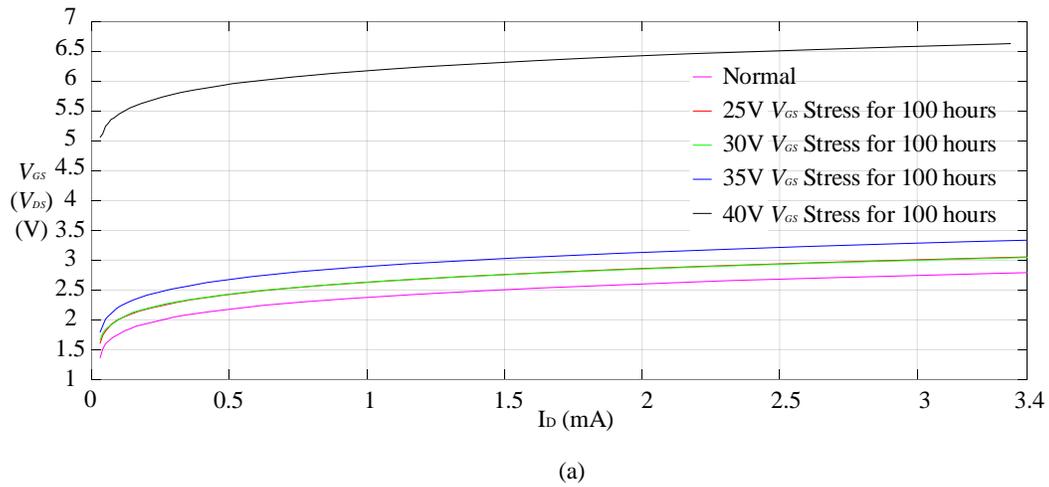
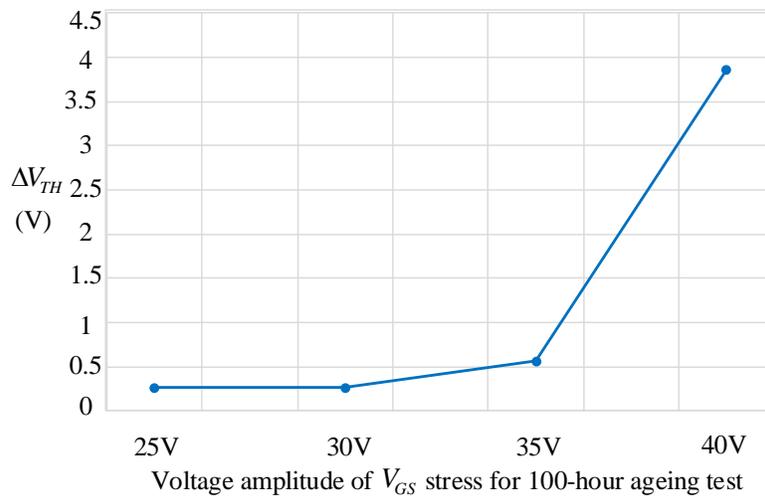
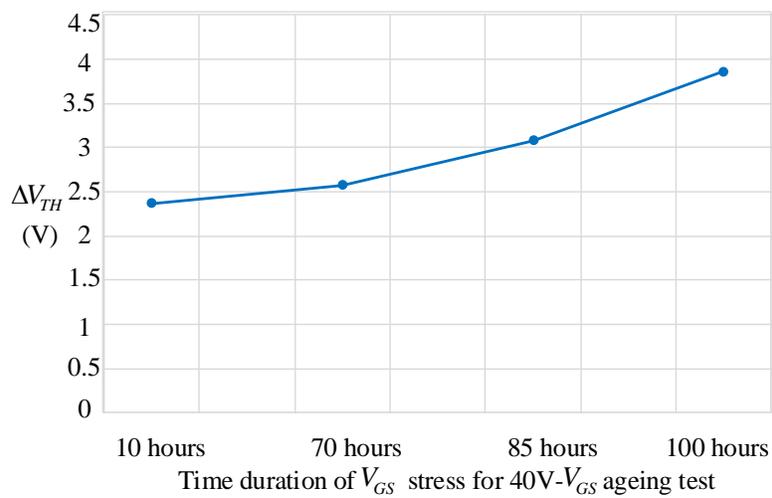


Figure 3.13. Tested  $V_{GS} - I_D$  curves for devices with various  $V_{GS}$  stress (a) amplitude (b) duration

According to the measured results in Figure 3.13 (a) and (b), the threshold voltage shift  $\Delta V_{TH}$  is derived by subtracting the  $V_{TH}$  of the stressed devices from that of the normal ones. In Figure 3.14 (a) and (b), the  $V_{TH}$  shifts with  $V_{GS}$  stress amplitude and duration are presented, respectively. According to the changing trend,  $V_{TH}$  rises with both the stress amplitude and duration. Maximum  $V_{TH}$  shift is about 3.86 V. What should be noticed is that from both Figure 3.13 and Figure 3.14, the  $V_{TH}$  increase is not proportional with the stress amplitude and duration change. With the stress amplitude and duration larger, the  $V_{TH}$  shift appears to be more obvious.



(a)



(b)

Figure 3.14. Threshold voltage shift with different  $V_{GS}$  stress (a) amplitude and (b) duration

The threshold voltage shift with  $V_{GS}$  stress can be explained below. When the positive gate bias is larger, due to the high charge density of interface states near the conduction band edge, more electrons are injected to the conduction band edge. Meanwhile, with larger positive gate bias, due to the high charge density of interface states near the oxide traps, more electrons are trapped in oxide traps in SiC MOSFET structures. As a result, with more severe electron injection and trapping, the threshold voltage positive shift increases with the gate bias voltage stresses [66].

Furthermore, the threshold voltage verification tests have also been conducted for those MOSFETs that have experienced the positive bias temperature stress tests. Figure 3.15 (a) shows that the threshold voltage shift increases with the temperature stress at 35-V  $V_{GS}$  stress lasting for 189 hours. To present a clear description for the above analysis, Figure 3.15 (b) further summarizes the threshold voltage testing results with different voltage stress and temperature stress.

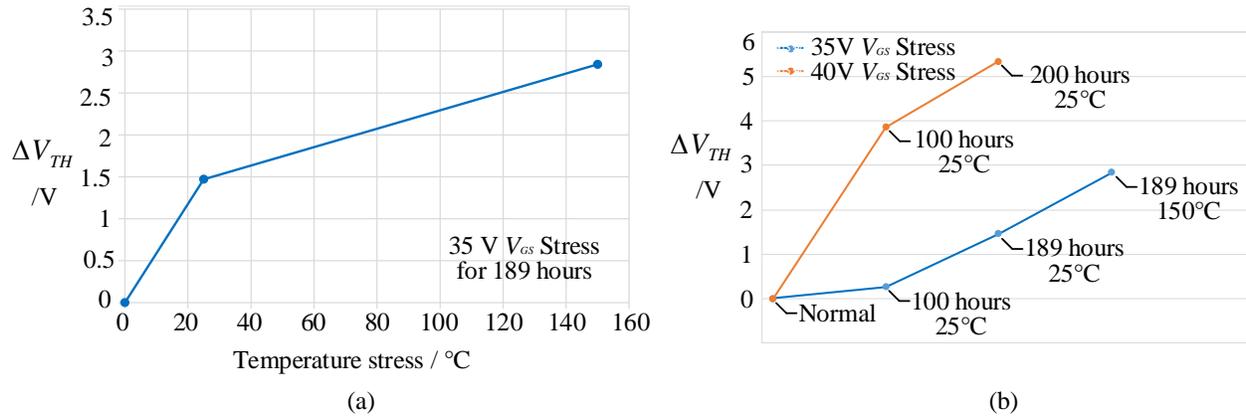


Figure 3.15. Threshold voltage shift results after the positive bias temperature stress tests

### 3.4.3. Gate Resistor Turn-on Energy Verification and Analysis

As presented in Figure 3.7 (a) and Figure 3.8 (a), when the  $V_{GS}$  stress amplitude and duration increase, the increasing slope of  $V_{GS}$  becomes sharper. Thus,  $V_{GS}$  stress amplitude and duration have effect on the  $V_{GS}$  changing rate. By analyzing  $C_{GD}$  and  $C_{DS}$  charging process, gate resistor current  $I_G$  is dependent on  $dV_{GS}/dt$  [344], according to (Eq.3.6).

$$I_G = (C_{GS} + C_{GD}) \frac{dV_{GS}}{dt} \quad (\text{Eq.3.6})$$

where,  $C_{GS}$  and  $C_{GD}$  are input gate-source capacitor and gate-drain capacitor, respectively. In [345], leakage gate current has been used for the diagnosis of gate oxide degradation, which further shows the relationship between the gate resistor current  $I_G$  and gate oxide degradation. Besides, the gate-source capacitor charging duration  $t_1+t_2$  is associated with the Miller plateau, as shown in (Eq.3.7).

$$t_1 + t_2 = R_G (C_{GS} + C_{GD}) \cdot \ln \left( \frac{1}{1 - \frac{V_{GS\_MP}}{V_{GS}}} \right) \quad (\text{Eq.3.7})$$

where,  $R_G$  is the sum of internal gate resistance  $R_g$  and external resistance  $R_{g\_ext}$ . Besides, Miller capacitor charging time  $t_3$  is also related to Miller plateau as can be seen in (Eq.3.8).

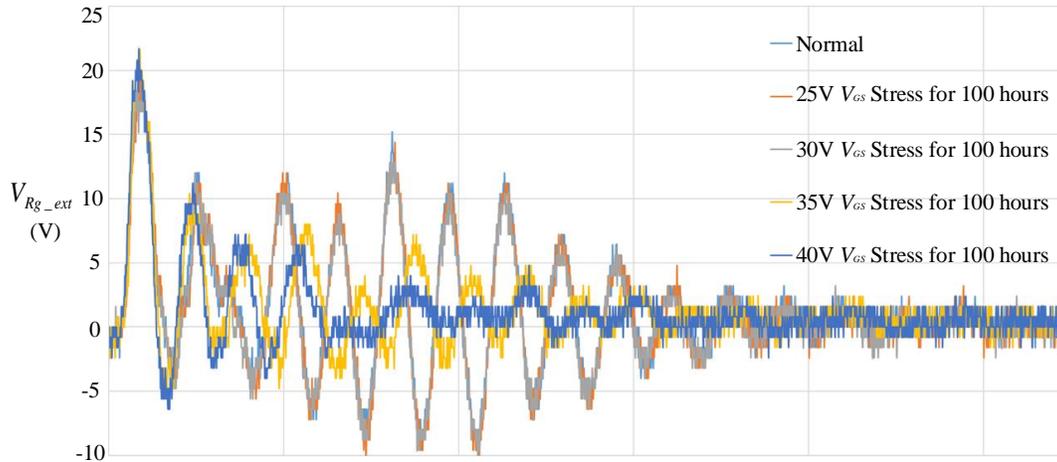
$$t_3 = R_G C_{GD} \cdot \frac{V_{DS}}{V_{GS} - V_{GS\_MP}} \quad (\text{Eq.3.8})$$

Hence, the turn-on switching time is a function of Miller plateau [344]. Based on the relationship between  $I_G$  and  $V_{GS}$  changing rate and between turn-on time and Miller plateau, the gate resistor switching energy can be another possible indicator for oxide degradation. In Figure 3.16 (a) and (b), the voltage of turn-on gate resistor  $V_{R_{g\_ext}}$  measured at the second pulse rising transient is shown for the stressed devices with different  $V_{GS}$  stress amplitude and duration, respectively.  $3 \Omega$  turn-on and turn-off gate resistance are used. By integrating  $(V_{R_{g\_ext}})^2/R_{g\_ext}$  over the turn-on switching time, the gate resistor turn-on energy  $E_{R_{g\_ext}}$  is derived as shown in (Eq.3.9).

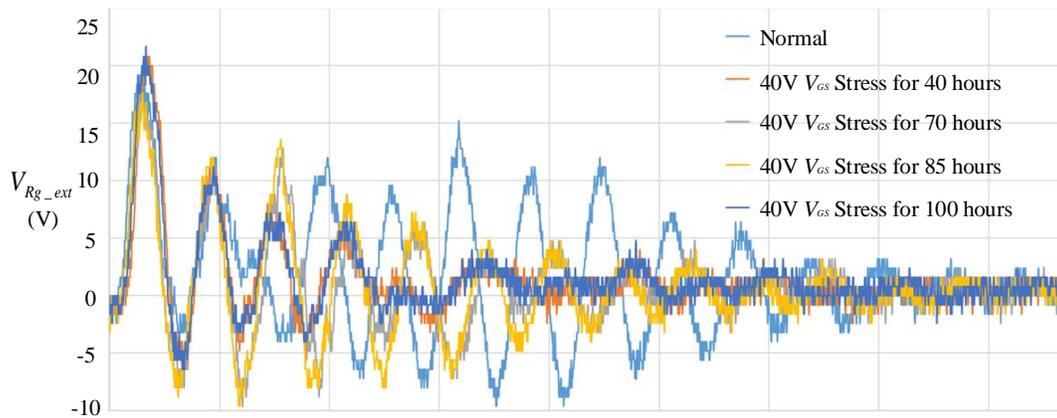
$$E_{R_{g\_ext}} = \int_0^{t_1+t_2+t_3} I_G^2 R_{g\_ext} dt = \int_0^{t_1+t_2+t_3} \frac{(V_{R_{g\_ext}})^2}{R_{g\_ext}} dt \quad (\text{Eq.3.9})$$

The integral interval has been selected to be long enough to cover the full range of the gate-source voltage fluctuation. As displayed in Figure 3.16,  $V_{R_{g\_ext}}$  amplitude swing experiences a less

obvious oscillations as the  $V_{GS}$  stress amplitude and duration rise. In other words, the integral of  $(V_{Rg\_ext})^2/R_{g\_ext}$  over the turn-on switching time tends to be smaller with the increase of  $V_{GS}$  stress amplitude and duration.



(a)



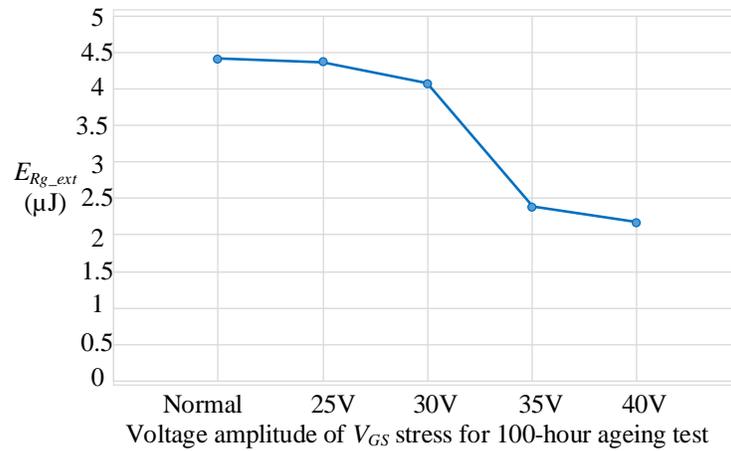
(b)

Figure 3.16. The voltage of turn-on gate resistor vs.  $V_{GS}$  stress (a) amplitude (b) duration

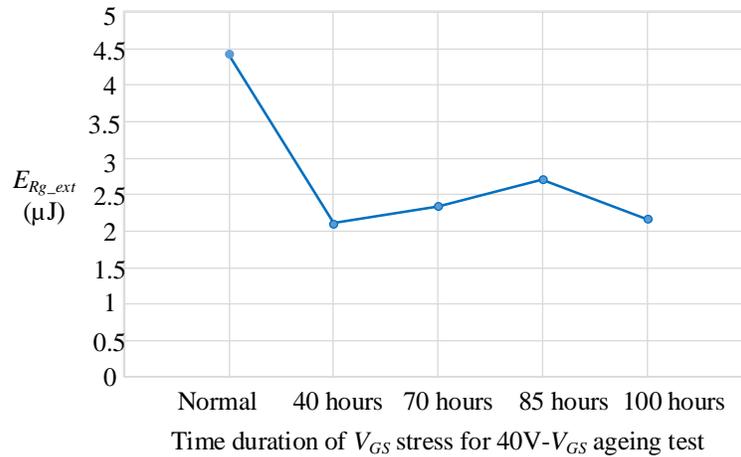
From the calculated results shown in Figure 3.17 (a), the turn-on resistor energy decreases as  $V_{GS}$  stress amplitude increases when the stress duration lasts for 100 hours. In Figure 3.17 (b), although some minor inconsistency occur at the devices having experienced 40 V  $V_{GS}$  stress with 40-hour and 70-hour stress duration, the overall trend is that the turn-on resistor energy decreases with the  $V_{GS}$  stress duration when the stress amplitude fixed at 40 V. Therefore, as  $V_{GS}$  stress

amplitude and duration increase, gate resistor energy tends to decrease. Maximum turn-on resistor energy change is about 2.24  $\mu\text{J}$ .

According to Figure 3.7 and Figure 3.8,  $dV_{GS}/dt$  increases with the  $V_{GS}$  voltage stress amplitude and duration. Besides, based on the test results in Part 3.3,  $V_{GS(p)}$  also rises as either the amplitude or duration of the  $V_{GS}$  voltage stress increases. Thus, considering (Eq.3.6) – (Eq.3.9), both  $dV_{GS}/dt$  and  $V_{GS(p)}$  contribute to the increase of turn-on resistor energy when the  $V_{GS}$  stress amplitude and duration go up.



(a)



(b)

Figure 3.17. Gate resistor turn-on energy vs.  $V_{GS}$  stress (a) amplitude, and (b) duration

Therefore, the decrease of the gate resistor turn-on energy can be explained by the decrease of the Miller capacitance with the  $V_{GS}$  stress amplitude and duration. This makes sense since the Miller capacitance is a nonlinear function of  $V_{GS}$ , and decreases with increasing  $V_{GS}$  [346]. Furthermore, combining the test results and (Eq.3.6) – (Eq.3.9), the Miller capacitance plays a more significant role in impacting the turn-on resistor energy compared with  $dV_{GS}/dt$  and  $V_{GS(p)}$  when either the amplitude or duration of the  $V_{GS}$  stress changes.

Moreover, the gate resistor turn-on energy verification has also been conducted for those MOSFETs after experiencing the positive bias temperature stress tests. Figure 3.18 (a) shows the waveforms of the external turn-on resistor voltage for both the normal devices and those after the positive bias temperature stresses. Based on these data, the energy that is consumed by the turn-on gate resistor has been further calculated. The results are presented in Figure 3.18 (b). It can be seen that the temperature stress plays a less obvious role in affecting the turn-on gate resistor energy, in comparison with the gate-source voltage stress.

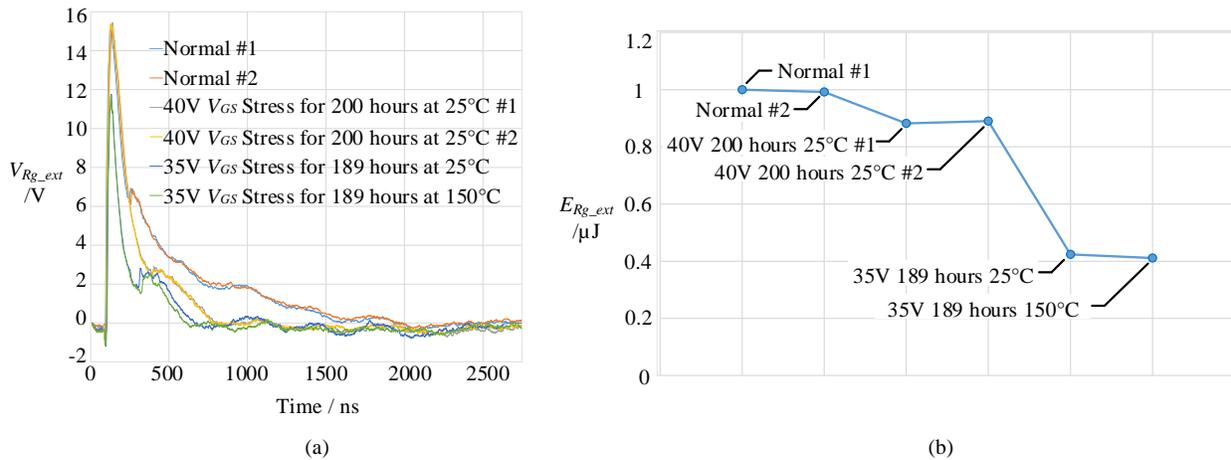


Figure 3.18. Turn-on gate resistor energy verification after the positive bias temperature stress

### 3.5. Comparison and Analysis Among The Three Investigated Indicators

As summarized in Table 3.1, among the three investigated indicators for SiC MOSFET gate oxide degradation, threshold voltage shift is the most obvious. However, it is difficult to realize online monitoring due to the small drain leakage current [75]. Similar to the gate charge test circuit [346], gate resistor turn-on energy  $E_{Rg\_ext}$  test can be realized online and integrated with the gate drive. But the integral calculation is needed, which adds additional cost. Besides, as can be seen from the gate resistor turn-on voltage waveforms shown in Figure 3.16, just like gate charge,  $E_{Rg\_ext}$  is also susceptible to the current oscillations flowing through the gate resistor. Due to inaccuracies introduced by a large number of smaller numbers being added instead of fewer large numbers [347], the unexpected effect of the current oscillation would be enlarged, which would impact the evaluation preciseness of  $E_{Rg\_ext}$  as an indicator of SiC MOSFET gate oxide degradation.

Table 3.1. Comparison Among Three Investigated Indicators

Indicators	Normal value	Maximum/Minimum value after stress	Maximum shift	Max. relative shift percentage
$V_{GS(p)}$	15.25 V	16.75 V	1.5 V	+9.84%
$V_{TH}$	2.74 V	6.60 V	3.86 V	+140.88%
$E_{Rg\_ext}$	4.41 $\mu$ J	2.17 $\mu$ J	2.24 $\mu$ J	-50.79%

Miller plateau is detected without interference with the normal operation since  $V_{GS}$  is directly measured from the gate and source [282]. And it has better ability to resist the interference from the gate current oscillations compared with turn-on resistor energy. Although its shifted extent is not so obvious compared with that of threshold voltage and gate resistor turn-on energy, Miller plateau is enough to be detected and further online monitored. Thus, Miller plateau is a promising robust indicator for SiC MOSFET gate oxide degradation with the potentials of further

online monitoring and gate drive integration. As an illustrative summary, Figure 3.19 presents a comprehensive comparison among these three health indicators.

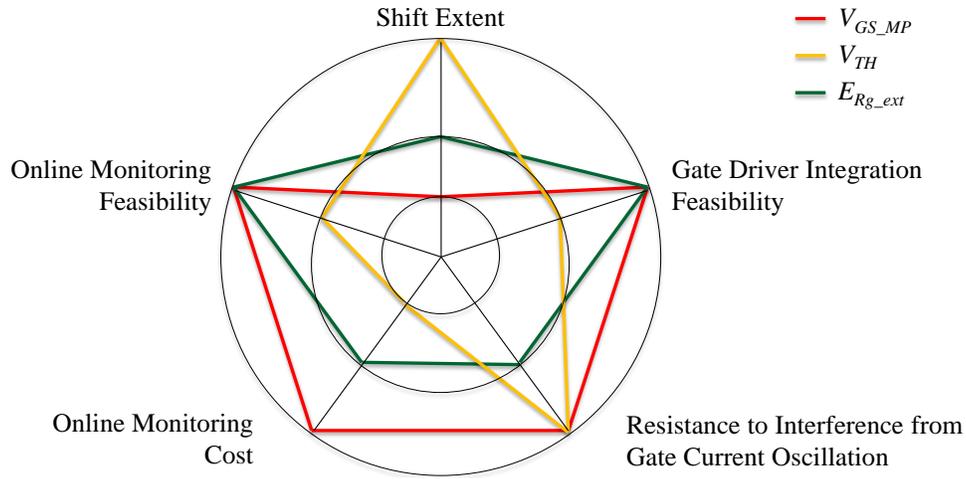


Figure 3.19. Comprehensive comparison among the three investigated health indicators

### 3.6. Summary for This Chapter

This section has explored the feasibility of Miller plateau as an indicator of SiC MOSFET gate oxide degradation from the perspectives of the temperature and the electric field relevance. By using the SiC MOSFET and SiC Schottky Diode device SPICE model, electro-thermal simulation has shown the negative temperature dependence of Miller plateau. Besides, the relationship between Miller plateau and High Electric Field (HEF) stress of gate oxide has been investigated by 20 groups of acceleration tests and double pulse tests with 5 identical SiC MOSFETs in each group. The positive bias temperature stress test has also been conducted and its impact on the investigated indicators has been analyzed. As  $V_{GS}$  stress amplitude and duration increase, Miller plateau rises with maximum shift about 1.5 V. Miller plateau is also compared with commonly used threshold voltage and the gate resistor turn-on energy which has the similar shifting mechanisms. It has advantages of inherent gate drive integration and online monitoring realization. Besides, there are no concerns caused by the current oscillations flowing through the

gate resistor when Miller plateau is measured. The disadvantage is the relatively small shift. Overall speaking, Miller plateau is a potential indicator for SiC MOSFET gate oxide HEF and high temperature induced degradation, especially for low-cost, in-situ oxide degradation detection.

#### 4. SIC MOSFET TEMPERATURE-SENSITIVE ELECTRICAL PARAMETER STUDY

As demonstrated in Figure 4.1, the temperature related failures take a considerable percentage of 55% among various sources of failures [250][251]. Thus, the thermal condition monitoring is critical for the long-term operation of power converters. In this area, the junction temperature has been extensively investigated. One way to measure the junction temperature is based on the electrothermal models. This approach has been reported to be dwarfed by low estimation accuracy [348]. Hence, to improve the estimation accuracy of the junction temperature, the temperature-sensitive electrical parameters (TSEPs) have been explored [349]. Considering the integration into gate drives, the dynamic TSEPs identified in the switching transient are more feasible compared with the static ones such as the on-resistance and on-state drain-source (collector-emitter) voltage.

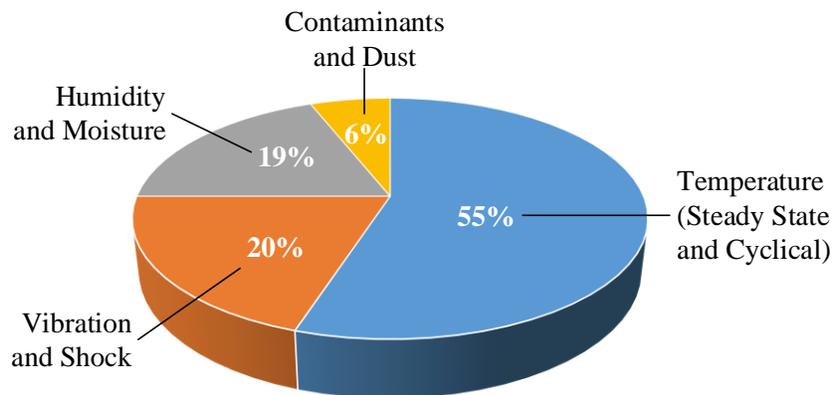


Figure 4.1. Four typical sources of stress for electronic equipment

The temperature coefficients and measurement ranges of the dynamic TSEPs have been widely studied for low-voltage Si IGBTs. The indexes such as sensitivity and linearity have been utilized to evaluate their effectiveness [271]. For the 650 V low-voltage Si IGBTs, the turn-on and turn-off delay time, current switching rate, tail current, diode reverse recovery charge, Miller plateau amplitude, and threshold voltage have been investigated [350]. The turn-on delay time has

been reported to present better linearity compared with turn-on current switching rate and turn-off time for low-voltage Si IGBTs [351].

There are also several studies that are focused on the low-voltage SiC MOSFET dynamic TSEPs. The current switching rate, threshold voltage, gate current peak have been utilized to estimate the junction temperature of SiC MOSFETs [352]. Among them, it has been found out that the current switching rate exhibits less temperature sensitivity and worse linearity over a wide operating range compared with the other dynamic TSEPs for low-voltage SiC MOSFETs [353]. Furthermore, the transconductance has been shown to be negatively temperature-dependent for 1.2 kV SiC MOSFETs [354]. But no theoretical mechanisms and physical analysis are provided.

Recently, with higher blocking voltage, medium-voltage wide band-gap devices have been characterized for different applications [355][356]. The advantages of this increased device blocking voltage could be demonstrated in two perspectives. First, the devices with higher blocking voltage are instrumental in less complex topologies thanks to the feasibility of fewer components. As a result, the decrease of the number of the devices, bond wires inside power modules, gate drives, and passive components would simplify the design and improve the system reliability. Second, the body diode forward voltage drop is smaller with one high-blocking-voltage device compared with multiple low-blocking-voltage devices in series, due to the minority injected conductivity modulation in the drift region. Correspondingly, the power loss would be reduced in the topologies that require the body diode conduction.

Compared with the devices with higher current rating, the low-current devices typically have smaller die area. On the one hand, this would lead to smaller intrinsic capacitances and less switching duration at the same switching frequency. Thus, the total switching loss would be

reduced. On the other hand, at higher switching frequency, the smaller device output capacitance  $C_{oss}$  helps the realization of the ZVS owing to shorter discharging and charging time.

Therefore, considering the above two positive aspects caused by both the medium voltage and low current ratings, these devices are preferred in the applications with higher voltage and higher frequency. One example is the high-voltage cascaded inverters with a step-up transformer, such as the isolated cascaded multistage dc-ac inverter [355]. In this topology, the secondary-side current is smaller than the primary-side current. The utilization of the 3.3 kV rather than 1.7 kV devices on the secondary side achieves less body diode voltage drop, smaller switching loss, higher switching frequency, and could save all but half of the total device number. Thus, the adoption of the medium-voltage, low-current devices in these applications would simplify the circuit and control design, as well as cut down the overall cost.

However, the junction temperature estimation for these devices has not been well explored yet. To address this problem, the unique physical characteristics of medium-voltage devices should be first examined. On the one hand, the bipolar degradation occurs with higher probability in the devices with larger blocking voltage when the body diodes experience forward bias [357][358]. This forward stress results in the stacking fault, which could lead to the increase of both body diode on-resistance and leakage current [359]. On the other hand, the drift region is thicker and more lightly doped at a higher blocking voltage. This would increase the on-resistance [360][361]. The drift-layer resistance increases with the blocking voltage ( $V_B$ ) in proportion to  $(V_B)^{2.3\sim 2.5}$  and is the main factor that determines the total on-resistance of the power devices [360].

Furthermore, in terms of dynamic characteristics, compared with Si devices, SiC counterparts feature the following characteristics. First, the channel mobility of Si MOSFETs decreases with temperature while that of SiC MOSFETs increases with temperature [362]. Second,

SiC devices typically have smaller active die areas compared with Si counterparts at similar current rating [93]. This would impact the intrinsic capacitance and other dynamic parameters. Third, SiC devices are normally switched faster, especially at the turn-on transient [363]. This higher switching speed would magnify the effect of the parasitic parameters. Thus, measuring the switching characteristics of SiC devices is more challenging. Due to these characteristics, it is necessary to conduct a detailed comparison of the typical TSEPs between these two types of devices in the emerging medium-voltage, low-current scenario.

The TSEPs for these medium-voltage low-current devices have not been well investigated. With high blocking voltage, the conventionally studied TSEPs would exhibit different temperature dependence. Besides, due to the low-current rating, the typical dynamic TSEPs are much harder to be detected. Therefore, for each TSEP, the related temperature-dependent parameters need to be explored in more detail. Furthermore, in spite of the extensive research regarding the dynamic TSEPs, the impact of parasitic parameters has not been analyzed, which plays an important role in an accurate junction temperature estimation, especially for the devices with low current rating. Moreover, the TSEP comparison between the medium-voltage Si IGBTs and SiC MOSFETs has not been conducted. It is significant to highlight the semiconductor material difference in terms of the medium-voltage device TSEPs.

This chapter offers an investigation of the typical dynamic TSEPs for the medium-voltage, low-current SiC MOSFETs and Si IGBTs considering the impact of junction temperature, dc voltage, drain current, and external gate resistance. The influence of the parasitic parameters is analyzed. In Section 4.1, the theoretical mechanisms are illustrated in detail. Section 4.2 provides the platform design for this temperature dependence characterization. The dynamic TSEP testing results and comparison are presented in Section 4.3. Finally, the conclusion is given in Section 4.4.

## 4.1. Theoretical Dynamic TSEP Analysis

Six groups of the typical dynamic TSEPs are theoretically analyzed in this section. Figure 4. demonstrates the definition of these parameters highlighted in red, in the ideal switching transients. They include the turn-on gate voltage Miller plateau amplitude  $V_{GS(p)}$  ( $V_{CE(p)}$ ), the current switching rate  $dI_{DS}/dt$  ( $dI_{CE}/dt$ ), the voltage switching rate  $dV_{DS}/dt$  ( $dV_{CE}/dt$ ), the internal gate resistance  $R_{g\_int}$  related TSEPs including the gate current peak  $I_{G(pk)}$  and the gate current plateau  $I_{G(p)}$ , the turn-off delay time  $t_{d\_off}$  and total turn-off time  $t_{off}$ , as well as the turn-on delay time  $t_{d\_on}$  and total turn-on time  $t_{on}$ . This figure is based on the SiC MOSFETs. Si IGBTs share these definitions. The physical mechanisms and the impact of the parasitic parameters on the temperature dependence of these dynamic TSEPs will be analyzed in the following sections.

### 4.1.1. Turn-on Miller Plateau Amplitude

The turn-on Miller plateau amplitude  $V_{CE(p)}$  has been proven to exhibit negative temperature coefficient in a 650 V, 200 A Si IGBT chip [364]. (Eq.4.1) shows the gate-source voltage Miller plateau amplitude description. It is derived from the MOSFET quadratic model [72], considering the channel length modulation of SiC MOSFET [73]. The corresponding derivative to junction temperature  $T_j$  is presented in (Eq.4.2).

$$V_{GS(p)} = V_{TH} + \sqrt{\frac{2 \cdot I_{DS} \cdot L_G}{\mu_n \cdot C_{OX} \cdot W_G \cdot (1 + \lambda_C \cdot V_{DS})}} \quad (\text{Eq.4.1})$$

$$\frac{\partial V_{GS(p)}}{\partial T_j} = \frac{\partial V_{TH}}{\partial T_j} + \sqrt{\frac{2 \cdot I_{DS} \cdot L_G}{C_{OX} \cdot W_G \cdot (1 + \lambda_C \cdot V_{DS})}} \cdot \left(-\frac{1}{2}\right) \cdot (\mu_n)^{-3/2} \cdot \frac{\partial \mu_n}{\partial T_j} \quad (\text{Eq.4.2})$$

As can be seen, the temperature characteristics of the Miller plateau amplitude is decided by the extents of the two temperature-sensitive parameters, i.e. the threshold voltage  $V_{TH}$  and the electron mobility  $\mu_n$ . The threshold voltage decreases with increasing temperature because of the positive temperature dependency of the intrinsic carrier concentration [365]. The electron mobility

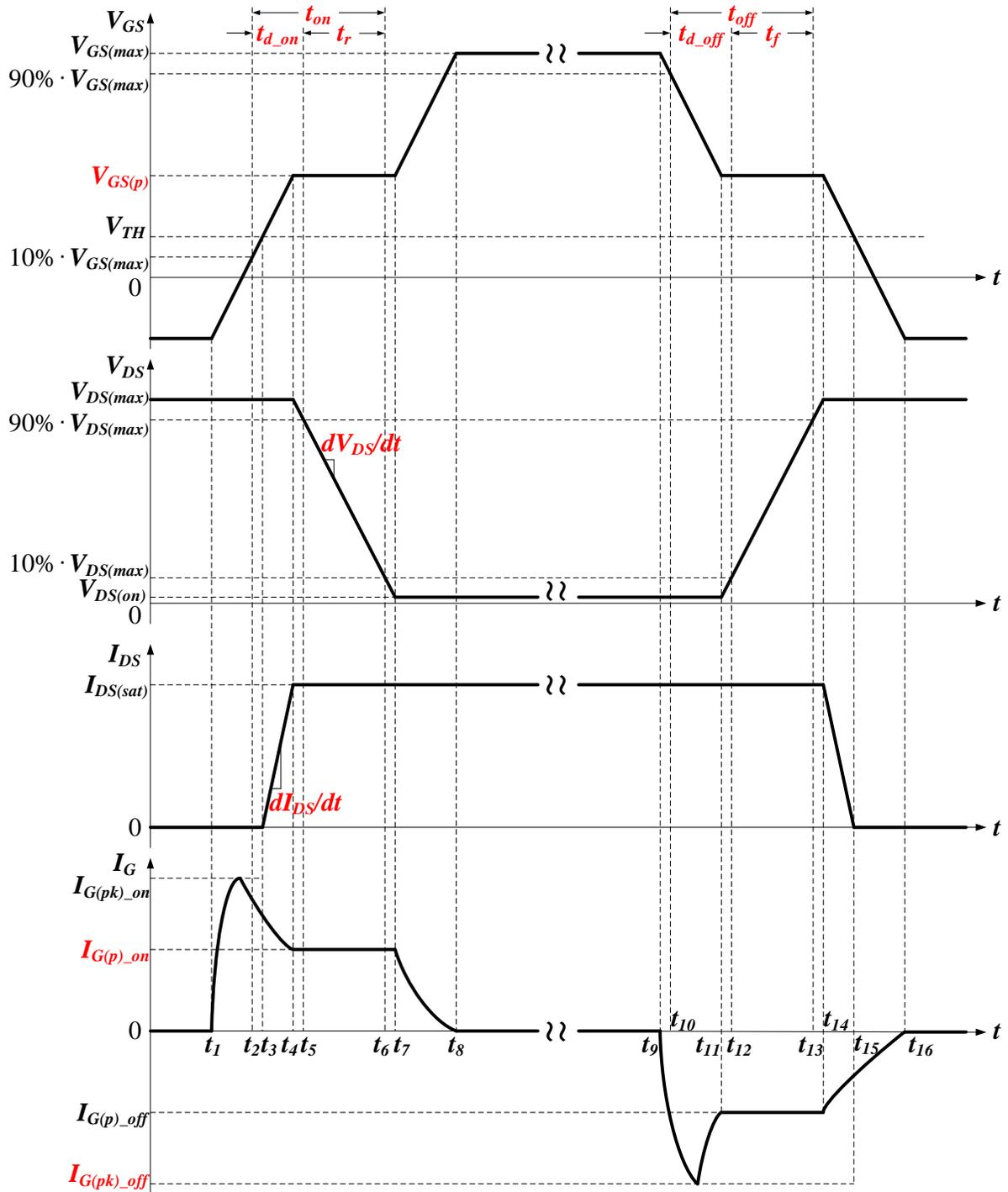


Figure 4.2. Ideal turn-on, turn-off transients to demonstrate the dynamic TSEPs

also decreases with  $T_j$  mainly due to the increased bulk phonon scattering [366][280]. From (Eq.4.2), these two parameters have the opposite impacts on the Miller plateau temperature

relevance, which is thus a combining result of them. Figure 4.3 shows the physical description of the Miller plateau amplitude temperature dependence. The two “minus” symbols indicate more negative impact on the TSEP than one “minus”, while the two “plus” symbols mean more positive impact than one “plus”. Because the threshold voltage exhibits stronger temperature dependence compared with the electron mobility for SiC MOSFETs, the Miller plateau amplitude typically presents a negative temperature coefficient. Since the electron mobility  $\mu_n$  is much larger in Si than in SiC [367], the impact of the negative temperature dependence of  $\mu_n$  would be larger for Si IGBTs. Therefore, the  $V_{GE(p)}$  of the Si IGBT exhibits less negative thermal dependence than the  $V_{GS(p)}$  of the SiC MOSFET.



Figure 4.3. Physics of Miller plateau amplitude temperature dependence

#### 4.1.2. Current Switching Rate

The drain-source current and its derivative are presented in (Eq.4.3) and (Eq.4.4), respectively. In this part, the analysis is based on the SiC MOSFETs. The Si IGBTs share these physical equations when the current switching rate is utilized as a TSEP.

$$I_{DS} = \mu_n \cdot C_{OX} \cdot (W_G/L_G) \cdot (V_{GS} - V_{TH})^2 / 2 \quad (\text{Eq.4.3})$$

$$\frac{dI_{DS}}{dt} = \frac{\mu_n \cdot W_G \cdot C_{OX} \cdot (V_{GS} - V_{TH})}{L_G} \cdot \frac{dV_{GS}}{dt} \quad (\text{Eq.4.4})$$

Since in the turn-on process the input capacitors  $C_{iss}$  are charged with the time constant of  $C_{iss} \cdot \sum R_G$ , the gate-source voltage during the turn-on transient can be presented in (Eq.4.5).

$$(V_{GS})_{ON} = V_{GG} \cdot \left( 1 - e^{\left( \frac{-t}{C_{iss} \cdot \sum R_G} \right)} \right) \quad (\text{Eq.4.5})$$

Substitute the derivative of the above equation into the (Eq.4.4), the turn-on current switching rate can be further shown in (Eq.4.6).

$$\left( \frac{dI_{DS}}{dt} \right)_{ON} = \frac{\mu_n \cdot W_G \cdot C_{OX} \cdot (V_{GS} - V_{TH}) \cdot V_{GG}}{L_G \cdot C_{iss} \cdot \sum R_G} \cdot e^{-t/(C_{iss} \cdot \sum R_G)} \quad (\text{Eq.4.6})$$

where,  $\sum R_G$  represents the total resistance in the gate charging / discharging loop. It could be regarded as the sum of internal gate resistance  $R_{g\_int}$ , external gate resistance  $R_{g\_ext}$  and gate current shunt resistance  $R_{shunt\_Ig}$ .

Figure 4.4 presents the physical relationships between the turn-on current switching rate and  $T_j$  for these two types of devices, with the thermal dependence of each intermediate physical parameter highlighted.

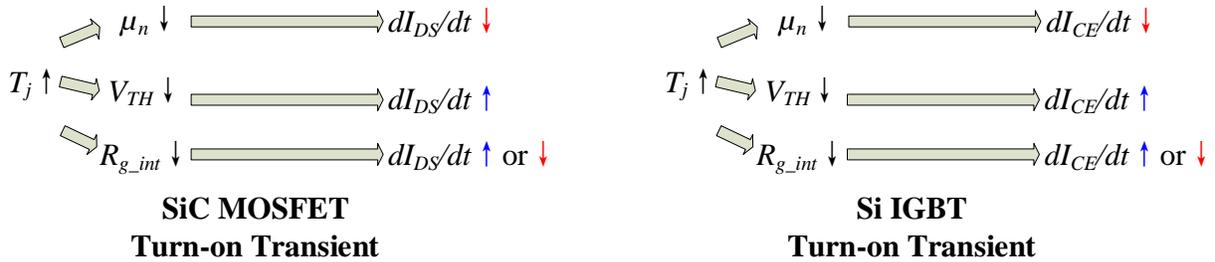


Figure 4.4. Physics of current switching rate temperature dependence

As analyzed above, both the threshold voltage and the effective mobility of the electrons decrease with  $T_j$ . Besides, for both devices,  $R_{g\_int}$  decreases with  $T_j$  based on the measurement results, which will be presented in Part 4.1.4 of this section. The  $dI_{DS}/dt$  during turn-on increases with temperature for 1.2 kV SiC MOSFETs [280][276]. But for 3.3 kV, 800 A Si IGBTs, the turn-on  $dI_{CE}/dt$  decreases with increasing  $T_j$  [368]. According to (Eq.4.6), this is basically because of larger electron mobility in Si IGBTs compared with SiC MOSFETs. As a result, the negatively

temperature-dependent characteristics of the Miller plateau amplitude would contribute towards the decreasing of the Si IGBT current switching rate as the temperature rises.

### 4.1.3. Voltage Switching Rate

The negative temperature dependence has been reported for the turn-off voltage switching rate  $dV_{CE}/dt$  [369] of Si IGBTs and the turn-off  $dV_{DS}/dt$  of SiC MOSFETs [281]. The mathematical description is shown in (Eq.4.7). Here, the SiC MOSFETs have been studied. The Si IGBTs would share this equation. It could be further updated by substituting the turn-off gate current. The resulted equation is shown in (Eq.4.8).

$$\frac{dV_{DS}}{dt} = \frac{C_{iss} \cdot (I_{DS} - I_{channel}) + C_{GD} \cdot I_G}{C_{iss} \cdot C_{DS} + C_{GS} \cdot C_{GD}} \quad (\text{Eq.4.7})$$

$$\left( \frac{dV_{DS}}{dt} \right)_{OFF} = \frac{C_{iss} \cdot (I_{DS} - I_{channel}) + C_{GD} \cdot \left[ (V_{GS(p)} - V_{SS}) / (\sum R_G) \right]}{C_{iss} \cdot C_{DS} + C_{GS} \cdot C_{GD}} \quad (\text{Eq.4.8})$$

To clearly present the impact of the junction temperature, external gate resistance and load current, the corresponding partial derivatives are analyzed in (Eq.4.9), (Eq.4.10), and (Eq.4.11), respectively. The temperature dependence of the voltage switching rate is decided by the two partial derivatives, i.e.  $\partial V_{GS(p)}/\partial T_j$  and  $\partial R_{g\_int}/\partial T_j$ . Since the partial derivative to  $R_{g\_ext}$  is consistently negative, the voltage switching rate reduces with the external gate resistance. Besides, due to positive derivative to  $I_{DS}$  ( $I_{CE}$ ), the voltage switching rate increases with the drain-source / collector-emitter current.

$$\frac{\partial \left[ (dV_{DS}/dt)_{OFF} \right]}{\partial T_j} = \frac{C_{GD}}{C_{iss} \cdot C_{DS} + C_{GS} \cdot C_{GD}} \cdot \left[ \frac{1}{\sum R_G} \cdot \frac{\partial V_{GS(p)}}{\partial T_j} - \frac{V_{GS(p)} - V_{SS}}{(\sum R_G)^2} \cdot \frac{\partial R_{g\_int}}{\partial T_j} \right] \quad (\text{Eq.4.9})$$

$$\frac{\partial \left[ (dV_{DS}/dt)_{OFF} \right]}{\partial R_{g\_ext}} = - \frac{C_{GD} \cdot (V_{GS(p)} - V_{SS})}{C_{iss} \cdot C_{DS} + C_{GS} \cdot C_{GD}} \cdot \frac{1}{(\sum R_G)^2} \quad (\text{Eq.4.10})$$

$$\frac{\partial(dV_{DS}/dt)}{\partial I_{DS}} = \frac{C_{iss}}{C_{iss} \cdot C_{DS} + C_{GS} \cdot C_{GD}} \quad (\text{Eq.4.11})$$

Figure 4.5 presents the summary for the above physical mechanisms of the turn-off voltage switching rate temperature relevance in these two groups of devices. As analyzed in the Part 4.1.1, due to the electron mobility of the Si IGBTs exhibits more negative temperature dependence than that of the SiC MOSFETs, the turn-off voltage switching rate is more positive temperature dependent in the Si IGBTs.

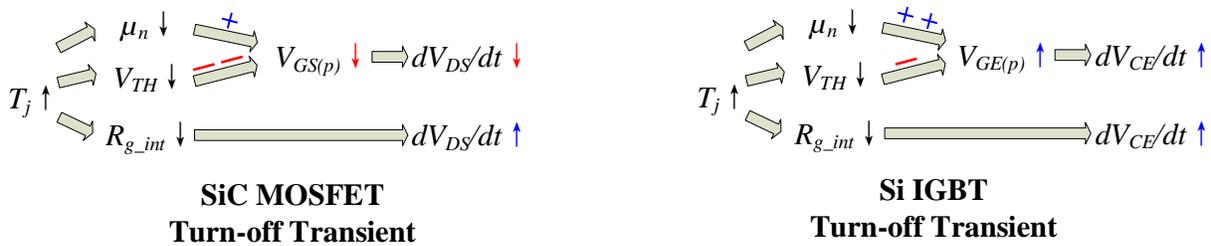


Figure 4.5. Physics of turn-off voltage switching rate temperature dependence

#### 4.1.4. Internal Gate Resistance and Gate Current

The internal gate resistance is composed of two parts, i.e. distributed gate electrode resistance and the distributed channel resistance seen from the gate [370][371]. The gate electrode resistance increases with temperature due to the positive temperature dependence of the gate electrode sheet resistance [372]. But the channel resistance decreases with temperature [370]. Thus, the total internal gate resistance could be either positively or negatively relevant to the temperature, depending on which resistance takes the larger proportion. As the blocking voltage increases, the drift region is thicker and more lightly doped. It has been reported that the thicker drift region would cause the internal gate resistance to increase [373]. The internal gate resistance has been measured with the Venable<sup>®</sup> impedance analyzer with drain and source shorted.

The internal gate resistance, the MOSFET's input capacitance, and the series parasitic inductance are connected in series [371]. The measurement results are illustrated in Figure 4.6. Compared with the low-voltage devices, medium-voltage ones exhibit larger internal gate resistance. This is induced by thicker drift region. The measured 3.3 kV 5 A SiC MOSFET internal gate resistance temperature sensitivity is about  $-1.44 \text{ m}\Omega/\text{C}$ . While the thermal coefficient for the tested 3 kV 12 A Si IGBT is around  $-22.92 \text{ m}\Omega/\text{C}$ , which is approximately 16 times that of SiC MOSFETs. The sum of  $C_{GS}$  and  $C_{GD}$  is about 2 nF for the investigated SiC MOSFET. While the sum of  $C_{GE}$  and  $C_{GC}$  is close to 3 nF for the Si IGBT. The temperature dependence for these medium-voltage devices differs from the existing low-voltage device results. For instance, the internal gate resistance increases with the temperature for 1.2 kV SiC MOSFETs [138]. Its temperature sensitivity is about  $3 \text{ m}\Omega/\text{C}$ . This opposite  $R_{g\_int}$  temperature dependence could be caused by the different doping profiles during the fabrication process [374], which would result in the different internal gate resistance even at the same blocking voltage [137]. Therefore, either the positively temperature-dependent gate electrode resistance or the negatively temperature-dependent channel resistance would take the primary proportion in total internal gate resistance.

The TSEPs that are directly associated with the internal gate resistance are the gate current peak and plateau. They will be analyzed separately in more detail in the following two parts.

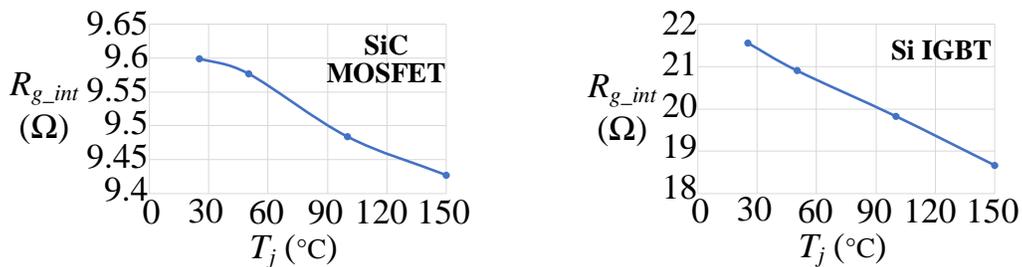


Figure 4.6. Internal gate resistance vs.  $T_j$  for SiC MOSFETs and Si IGBTs

#### 4.1.4.1. Gate Current Peak

It has been reported that the first gate current peak values decrease with the temperature for IGBTs [374] and MOSFETs [375][279][376]. When the voltage of  $C_{GS}$  reaches to the threshold voltage and the device channel starts to flow through current, the gate charge equivalent circuit could be illustrated in Figure 4.7 (a). Assuming the parasitic gate inductance is small and the RLC series circuit is well overdamped with the damping factor  $\zeta$  satisfying (Eq.4.12), it could be further simplified into a first-order RC circuit in Figure 4.7 (b).

$$\zeta = \frac{\sum R_G}{2} \sqrt{(C_{GS} + C_{GD}) / (L_{GS} + L_{SS})} > 1 \quad (\text{Eq.4.12})$$

Based on the simplified circuit, the intrinsic input capacitor voltage is shown in (Eq.4.13).

$$V_{C_{GS}} = \left( V_{GG} - L_{SS} \cdot \frac{dI_{DS}}{dt} \right) \cdot \left( 1 - e^{-t / [(\sum R_G) \cdot C_{iss}]} \right) \quad (\text{Eq.4.13})$$

At the starting point,  $dI_{DS}/dt$  can be regarded as a constant. Therefore, its derivative  $d^2(I_{DS})/dt^2$  could be seen close to zero. Thus, the gate current would be further derived in (Eq.4.14).

$$I_G = C_{iss} \cdot \frac{dV_{C_{GS}}}{dt} = \frac{(V_{GG} - L_{SS} \cdot (dI_{DS}/dt))}{\sum R_G} \cdot e^{-t / [(\sum R_G) \cdot C_{iss}]} \quad (\text{Eq.4.14})$$

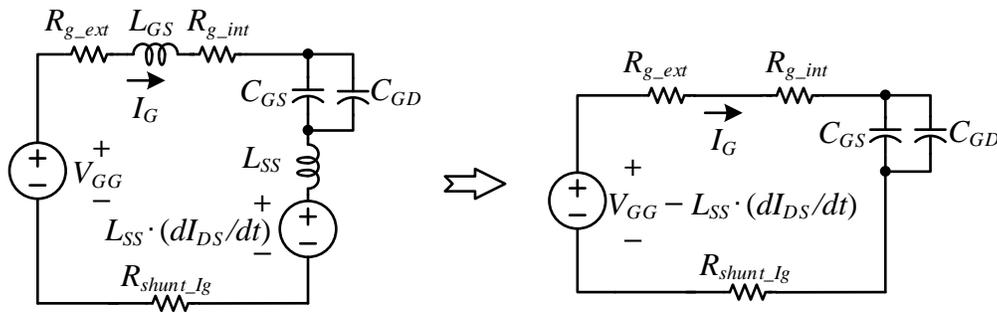


Figure 4.7. Gate charge equivalent circuit and simplified first-order form

Thus, the gate current peak  $I_{G(pk)}$  could be presented in (Eq.4.15). Figure 4.8 further shows the physical relationship between the gate current peak and the junction temperature.

$$I_{G(pk)} = \frac{(V_{GG} - L_{SS} \cdot (dI_{DS}/dt))}{(\sum R_G)} \quad (\text{Eq.4.15})$$



Figure 4.8. Physics of gate current peak temperature dependence

As the  $R_{g\_ext}$  increases, the damping factor becomes larger, which brings in less oscillations. Gate current reaches to its peak at the starting point of the drain-source current, as the current switching rate  $dI_{DS}/dt$  is smallest at this time.

In our test, internal gate resistance decreases with temperature. Turn-on  $dI_{DS}/dt$  increases with temperature. Due to the parasitic inductance impact, the charged voltage on the input capacitance is actually lower. This would cause the gate current peak value to decrease with temperature. When this decreasing extent is higher than the increasing extent caused by the negative temperature coefficient of the internal gate resistance, the gate current peak value would decrease.

But for Si IGBTs, the  $dI_{CE}/dt$  decreases with the temperature based on our previous analysis. Both the drain-source current switching rate and internal gate resistance would have the negative impact on the gate current peak values. Thus,  $I_{g(pk)}$  has a monotonically positive relationship with  $T_j$ .

#### 4.1.4.2. Gate Current Plateau

(Eq.4.16) presents the turn-on gate current plateau. The physical description of this TSEP temperature dependence is shown in Figure 4.9. The turn-on gate current plateau increases with the junction temperature for SiC MOSFETs as a result of the negative temperature coefficient of

both the Miller plateau amplitude and internal gate resistance. But for Si IGBTs, since the Miller plateau amplitude could present positive temperature dependence, the  $I_{G(p)}$  increasing with  $T_j$  would be less obvious.

$$I_{G(p)} = (V_{GG} - V_{GS(p)}) / (\sum R_G) \quad (\text{Eq.4.16})$$

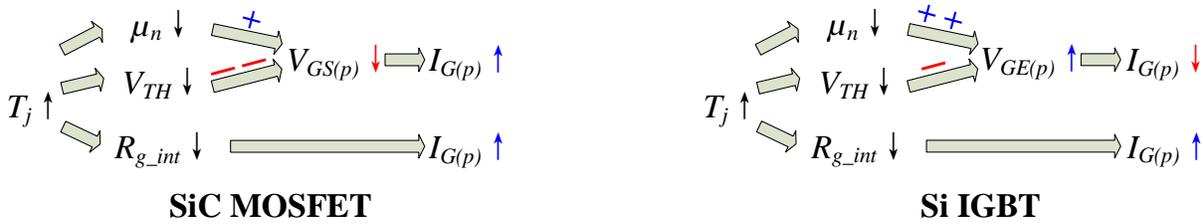


Figure 4.9. Physics of gate current plateau temperature dependence

#### 4.1.5. Turn-off Delay Time

The turn-off delay time is defined as the time interval between the moment when the gate–source voltage falls to 90% of its initial value and the drain–source voltage rises to 10% of the blocking voltage [377][378]. It has been shown to increase with the temperature for SiC MOSFETs [378][299] and Si IGBTs [379][380] with good linearity.

As shown in Figure 4., at time point  $t_{10}$ , the discharging voltage of  $C_{GS}$  is presented in (Eq.4.17). Based on this equation, the corresponding  $t_{10}$  and  $t_{11}$  are further derived in (Eq.4.18) and (Eq.4.19).

$$V_{C_{GS}} = V_{GG} \cdot e^{-t / [(\sum R_G) \cdot C_{iss}]} \quad (\text{Eq.4.17})$$

$$t_{10} = -(\sum R_G) \cdot C_{iss} \cdot \ln(0.9) + t_9 \quad (\text{Eq.4.18})$$

$$t_{11} = -(\sum R_G) \cdot C_{iss} \cdot \ln(V_{GS(p)} / V_{GG}) + t_9 \quad (\text{Eq.4.19})$$

So, the turn-off delay time would be presented in (Eq.4.20).

$$t_{d\_off} \approx t_{11} - t_{10} = (\sum R_G) \cdot C_{iss} \cdot \ln \left( \frac{0.9 \cdot V_{GG}}{V_{GS(p)}} \right) \quad (\text{Eq.4.20})$$

Figure 4.10 shows the physical description of the temperature relevance for the turn-off delay time. The thermal dependence of this TSEP is mainly decided by  $R_{g\_int}$  and  $V_{GS(p)}$  ( $V_{GE(p)}$ ). For the medium-voltage low-current Si and SiC devices, based on our testing results, the internal gate resistance exhibits the negative temperature dependence. For SiC MOSFETs, the Miller plateau amplitude negative thermal coefficient compensates this effect and make the turn-off delay time would present less decrease as temperature goes up. When this compensation is large enough, the  $t_{d\_off}$  would even increase with temperature. For Si IGBTs, since the Miller plateau amplitude has weaker temperature relevance, the internal gate resistance temperature dependence would play a leading role in deciding the thermal dependence of  $t_{d\_off}$ . As a result, the turn-off delay time would exhibit different thermal dependence compared with that of the SiC MOSFETs.

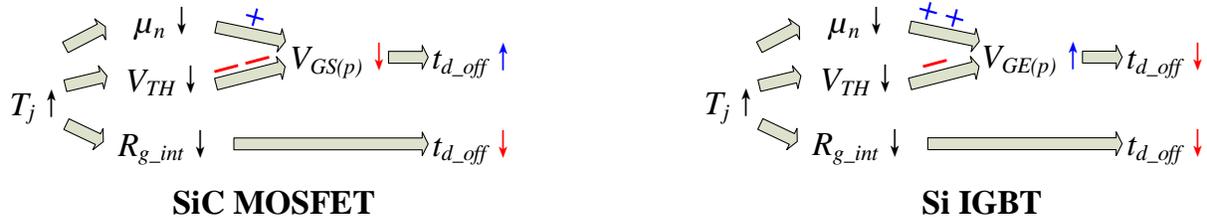


Figure 4.10. Physics of turn-off delay time temperature dependence

#### 4.1.6. Turn-on Delay Time

The turn-on delay time is defined as the time interval between the moment when the gate–source voltage rises to 10% of its peak value and the drain–source voltage drops to 90% of the off-state value [377]. This definition does not consider the parasitic parameters, such as parasitic inductance and recovery current of the freewheeling diode. The turn-on delay time has been reported to increase with  $T_j$  for Si IGBTs with sensitivity about 1.911 ns/°C [351]. This TSEP is

basically generated from the input capacitance charging [350]. At time point  $t_2$ , the charging voltage of  $C_{GS}$  is presented in (Eq.4.21).  $t_2$  can be further derived in (Eq.4.22).

$$V_{C_{GS}} = V_{GG} \cdot \left( 1 - e^{-t/[(\sum R_G) \cdot C_{iss}]} \right) \quad (\text{Eq.4.21})$$

$$t_2 = -(\sum R_G) \cdot C_{iss} \cdot \ln(0.9) + t_1 \quad (\text{Eq.4.22})$$

At time point  $t_4$ , there is drain-source current flowing through the source-to-ground parasitic inductance  $L_{SS}$ . Thus, the  $C_{GS}$  voltage equation is shown in (Eq.4.23). And  $t_4$  is further presented in (Eq.4.24). Finally, the turn-on delay time is described in (Eq.4.25) by subtracting  $t_4$  by  $t_2$ .

$$V_{C_{GS}} = \left( V_{GG} - L_{SS} \cdot \frac{dI_{DS}}{dt} \right) \cdot \left( 1 - e^{-t/[(\sum R_G) \cdot C_{iss}]} \right) \quad (\text{Eq.4.23})$$

$$t_4 = -(\sum R_G) \cdot C_{iss} \cdot \ln \left( 1 - \frac{V_{GS(p)}}{V_{GG} - L_{SS} \cdot (dI_{DS}/dt)} \right) + t_1 \quad (\text{Eq.4.24})$$

$$t_{d\_on} \approx t_4 - t_2 = C_{iss} \cdot \sum R_G \cdot \left[ \ln \left( 0.9 / \left( 1 - \frac{V_{GS(p)}}{V_{GG} - L_{SS} \cdot (dI_{DS}/dt)} \right) \right) \right] \quad (\text{Eq.4.25})$$

Figure 4.11 presents the physical relationship between the turn-on delay time and the junction temperature. Since the Miller plateau amplitude and current switching rate exhibit the opposite thermal dependence on the two devices, the turn-on delay time also presents different temperature coefficients.

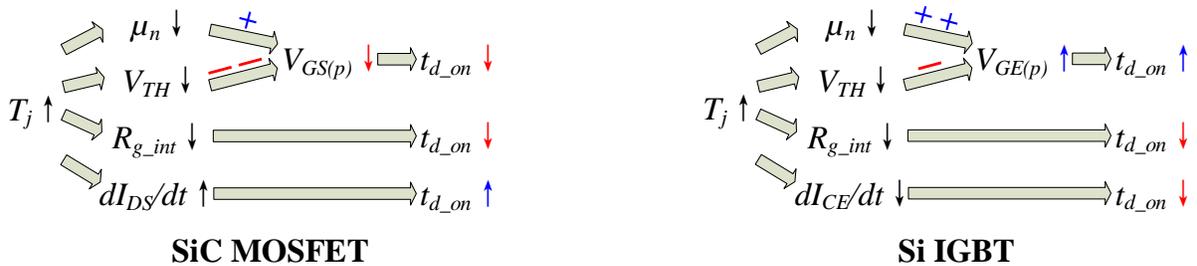


Figure 4.11. Physics of turn-on delay time temperature dependence

## 4.2. Design of the Testing Platform Enabling Thermal Dependence Characterization

The testing schematic is presented in Figure 4.12. The parasitic parameters would potentially interfere with the TSEP evaluation results. The green colored current flow shows  $C_{DC} - L_{DC} - C_j \parallel EPC$  (equivalent paralleled capacitance)  $- L_{DS} - C_{GD} - R_{g\_int} - L_{GS} - R_{g\_ext} - V_{GS} - R_{shunt\_Ig} - R_{shunt\_Ids} - C_{DC}$ . It interferes with the junction temperature estimation accuracy when the gate current and drain-source / collector-emitter current are applied as the TSEPs. The orange colored current flow shows  $V_{GS} - R_{g\_ext} - L_{GS} - R_{g\_int} - C_{GS} - L_{SS} - R_{shunt\_Ig} - V_{GS}$ . It would impact the temperature evaluation accuracy if the gate current is selected. The red colored current flow  $C_{DC} - L_{DC} - C_j \parallel EPC - L_{DS} - C_{DS} - L_{SS} - C_{DC}$  would interfere with the  $T_j$  evaluation when either the gate current or drain-source / collector-emitter current is utilized. More detailed analysis will be conducted along with the testing results as follows.

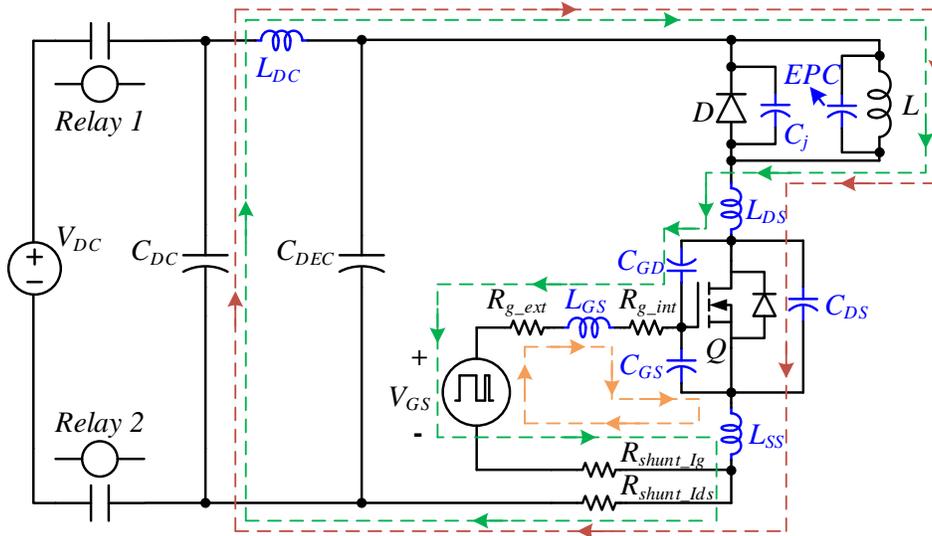


Figure 4.12. The power stage schematic with parasitic parameters included

The assembled prototype and related setup are shown in Figure 4.13. The PCB layout is optimized to reduce the stray inductances so that the corresponding unexpected impact on the characterization accuracy is minimized. To reduce the equivalent paralleled capacitance (EPC) of

the inductor load, two inductors are put in series. The measured frequency characteristics shows that the low-frequency inductance is about 1.5 mH. The  $EPC$  is close to 105.54 pF. The  $V_{DS}$  is measured by Tek P6015A high voltage passive probe.  $V_{GS}$  is detected by a passive probe at a Tek probe tip adapter. The probe wire is minimized to decrease the introduced parasitic inductance. Both the  $I_g$  and  $I_{DS}$  are sensed through the current shunts SSDN-10.

The temperature is got from a multimeter through a thermal couple mounted on the surface of a copper cube, which is contacted to a hot plate underneath it. The devices can be heated to designated temperature by the hot plate. This copper cube is electrically isolated from the device drain-source / collector-emitter by a thermal pad, so that the possible high-voltage creepage could be avoided. In this test, 3.3 kV SiC MOSFETs with 5 A current rating is applied. To make a comparison, a 3 kV Si IGBT with 12 A current rating is also tested.

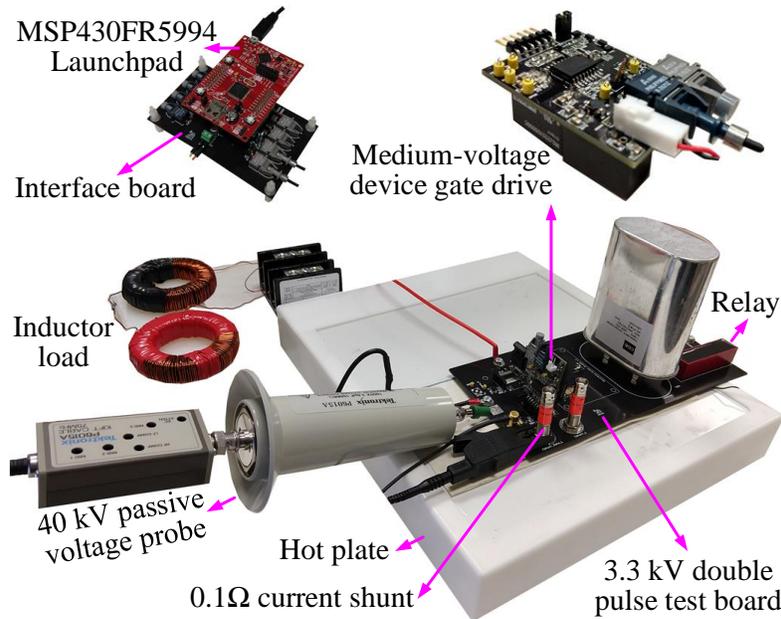


Figure 4.13. The medium-voltage device temperature dependence characterization platform

The utilized high-voltage dc power supply is not galvanically isolated and thus, shares the same ground with the oscilloscope. To cut off the current between the high voltage power supply

and the internal circuit inside the oscilloscope, relays are introduced into the power stage. These relays are normally off. Once the program works, the relays are controlled to be closed to charge the dc capacitor. In this test, the charging time is set as around 2.3 ms. Then the relays are turned off. To make sure the relay is fully open, about 23.6  $\mu$ s delay time has been added before the double pulse is generated.

### 4.3. Test Results and Comparison

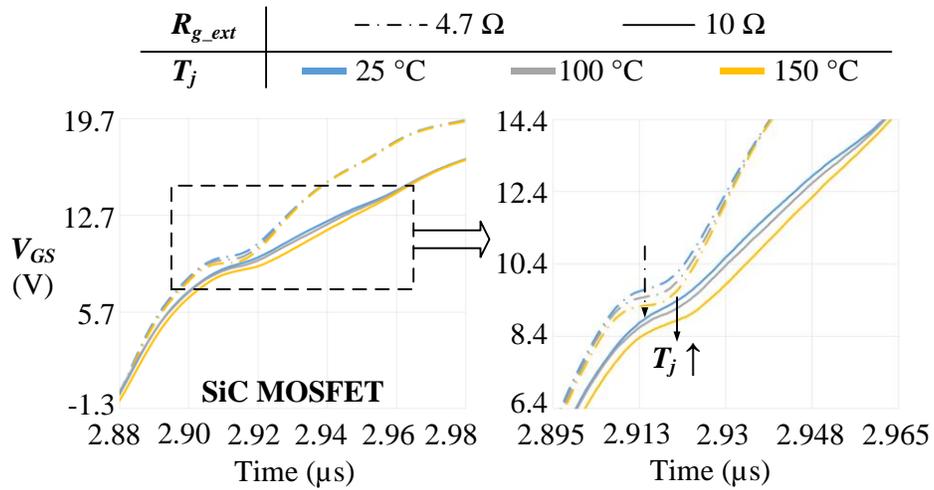
In this section, the testing results are presented. The experimental data is analyzed in combination with theoretical mechanisms. For each TSEP, the comparison between the medium-voltage SiC MOSFETs and Si IGBTs with the identical packaging pattern is conducted. Finally, a summary is given to highlight the better dynamic TSEPs for each device.

#### 4.3.1. Turn-on Miller Plateau Amplitude

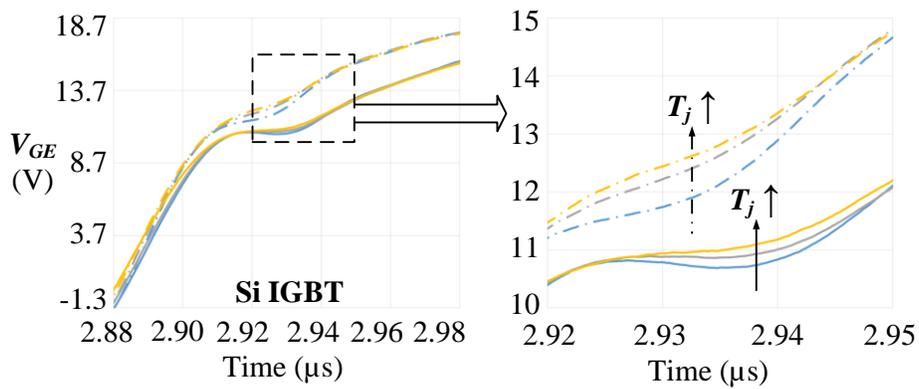
Figure 4.14(a) presents the turn-on  $V_{GS}$  waveforms for the SiC MOSFETs. The Miller plateau amplitude exhibits the negative thermal dependence with the junction temperature. This is consistent with the mechanism analysis in Figure 4.3. It is measured at 3.75 A drain current.

Figure 4.14(b) shows the turn-on  $V_{GE}$  waveform and the thermal dependence for Si IGBTs. As analyzed previously, since the electron mobility is larger in Si materials, the Miller plateau amplitude would exhibit less negative thermal dependence in the Si IGBTs. When the external gate resistance decreases to smaller values such as 4.7  $\Omega$  and 10  $\Omega$ , the Miller plateau amplitude  $V_{GE(p)}$  would even present the positive temperature relevance.

What should be noticed is that the higher resonant collector-emitter current generated in the green loop in Figure 4.12. The current further increases the Miller plateau amplitude, according to (Eq.4.1). This increase would compensate the plateau amplitude decrease due to the negative thermal relevance of the intrinsic parameters, i.e. electron mobility and threshold voltage.



(a)



(b)

Figure 4.14. Turn-on waveforms of (a)  $V_{GS}$  and (b)  $V_{GE}$ 

Figure 4.15 is the Miller plateau amplitude changing trend with  $T_j$ . For SiC MOSFETs, the turn-on Miller plateau amplitude decreases with temperature. This phenomenon is more obvious when either the DC voltage or drain current is higher. But this is not consistent with the medium-voltage low-current Si IGBTs at small gate resistance as analyzed previously.

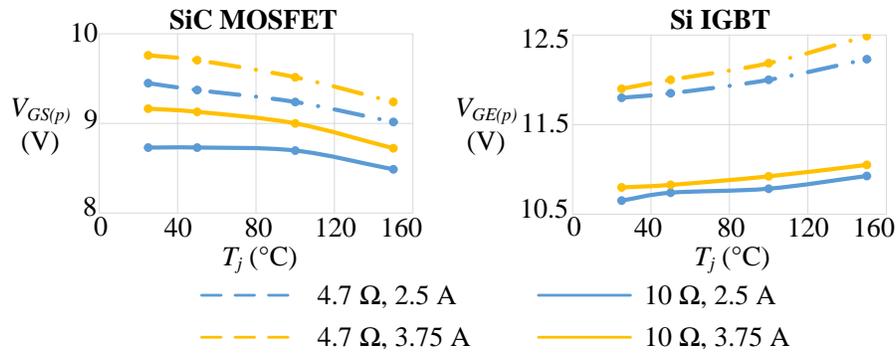


Figure 4.15. Turn-on Miller plateau thermal dependence for SiC and Si devices

Figure 4.16 is the summary of the temperature coefficient of the Miller plateau amplitude. Since the  $V_{TH}$  exhibits stronger temperature dependence compared with the electron mobility, the Miller plateau amplitude of the SiC MOSFETs presents more negative temperature dependence than that of Si IGBTs.

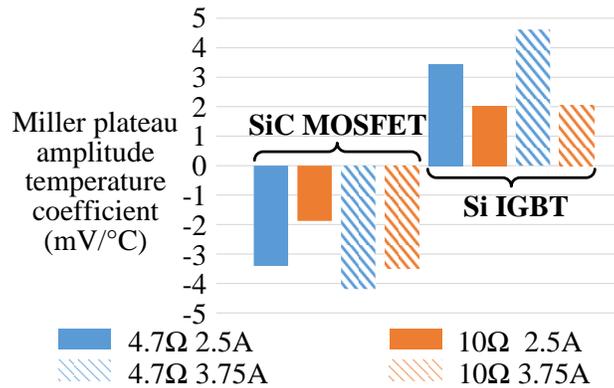


Figure 4.16. Thermal coefficient of Miller plateau amplitude for SiC and Si devices

### 4.3.2. Current Switching Rate

Figure 4.17 (a) and (b) show the turn-on drain-source and collector-emitter current waveforms, respectively. They are both measured at 2000 V dc voltage with 2.5 A load current. As the junction temperature goes up, the turn-on current switching rate of the SiC MOSFET increases. But the opposite trend holds for the Si IGBTs. It can be seen that the drain-source current

of the SiC MOSFET oscillates more obviously because of higher turn-on switching speed compared with that in the Si IGBTs.

Figure 4.18 presents the thermal dependence of the turn-on current switching rate. This TSEP increases with temperature for SiC MOSFETs. But the turn-on  $dI_{CE}/dt$  decreases with temperature for Si IGBTs. Also from Figure 4.18, it can be seen that at the same DC voltage, load current, gate resistance, and temperature, SiC MOSFETs have higher turn-on current switching rate than Si IGBTs. This faster turn-on switching is due to the smaller  $C_{GS}$  in SiC MOSFETs, which needs less time to be fully charged.

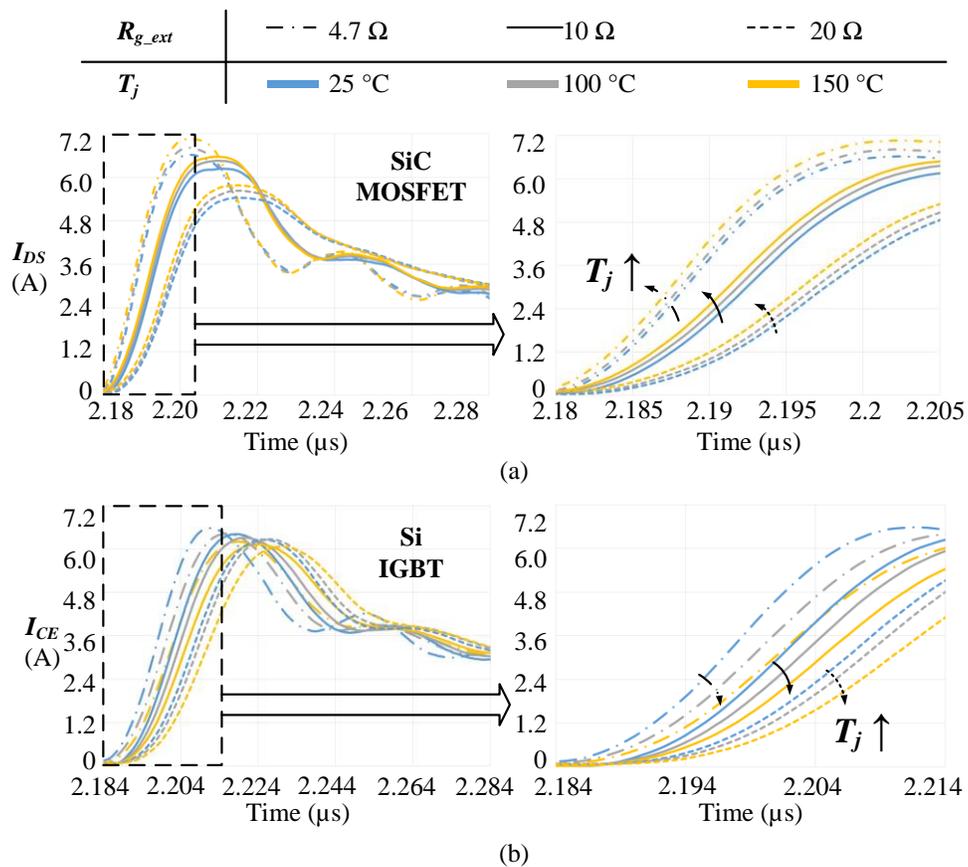


Figure 4.17. Waveforms of the turn-on (a)  $I_{DS}$  and (b)  $I_{CE}$

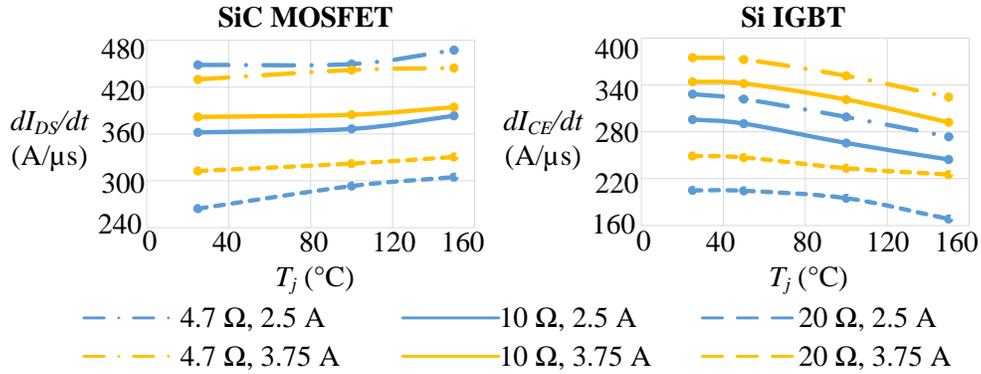


Figure 4.18. Temperature dependent trend of the turn-on  $dI_{DS}/dt$  and  $dI_{CE}/dt$

Figure 4.19 shows the temperature coefficient comparison of the turn-on current switching rate. The medium-voltage low-current Si IGBTs are verified to have higher temperature sensitivity of the turn-on  $dI_{CE}/dt$  compared with SiC MOSFETs.

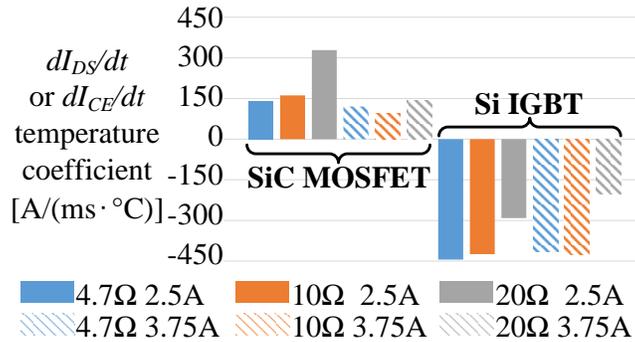


Figure 4.19. Temperature coefficient comparison of turn-on  $dI_{DS}/dt$  and  $dI_{CE}/dt$

As the temperature varies, there is no obvious change in the turn-off current switching rate compared with the turn-on counterpart. This is mainly caused by slower turn-off switching. At 25  $^\circ$ C, 2000 V dc voltage, 3.75 A load current, and 4.7  $\Omega$  external gate resistance, the turn-on transient duration is 37.8% of the turn-off one for SiC MOSFETs, and 24.8% for Si IGBTs.

### 4.3.3. Voltage Switching Rate

Figure 4.20 (a), (b) present the turn-off  $V_{DS}$  and  $V_{CE}$  waveforms. They are captured at 2000 V DC voltage with 3.75 A load current. It can be seen that the turn-off voltage switching rate exhibits a negative temperature dependence for SiC MOSFETs. But for the Si IGBTs, the opposite thermal characteristics exists for this TSEP. From the (Eq.4.8), the turn-off voltage switching rates of both the devices have a positive relevance with the Miller plateau amplitude. Since the Si IGBT Miller plateau amplitude exhibits less negative and even positive thermal dependence, it would contribute towards the turn-off voltage switching rate increasing with the temperature.

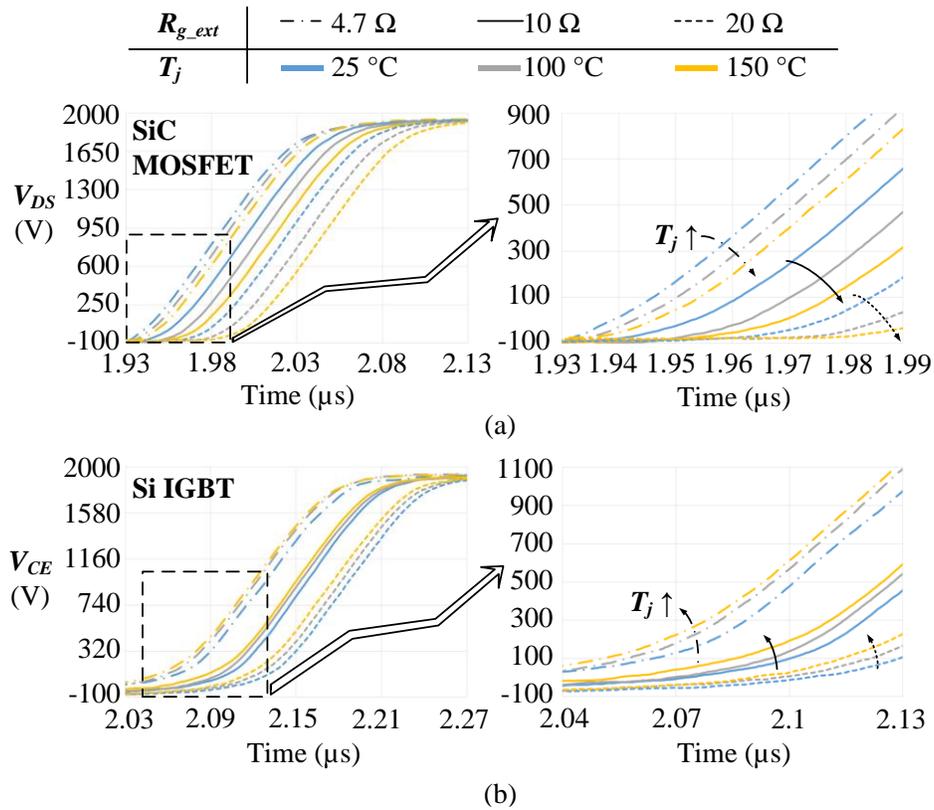


Figure 4.20. Turn-off waveforms of (a)  $V_{DS}$  and (b)  $V_{CE}$

The temperature dependence is shown in Figure 4.21. Both the turn-off  $dV_{DS}/dt$  and  $dV_{CE}/dt$  reduce with temperature. It exhibits more obvious thermal relevance in SiC MOSFETs. Because

of the more negative temperature dependence of the electron mobility in the Si IGBTs than the SiC MOSFETs, the Miller plateau amplitude exhibits more positive thermal relevance for the Si IGBTs. Based on (Eq.4.9), the turn-off voltage switching rate is more positively temperature-dependent in the Si IGBTs. This is consistent with the temperature coefficient given in Figure 4.5, especially at a larger external gate resistance.

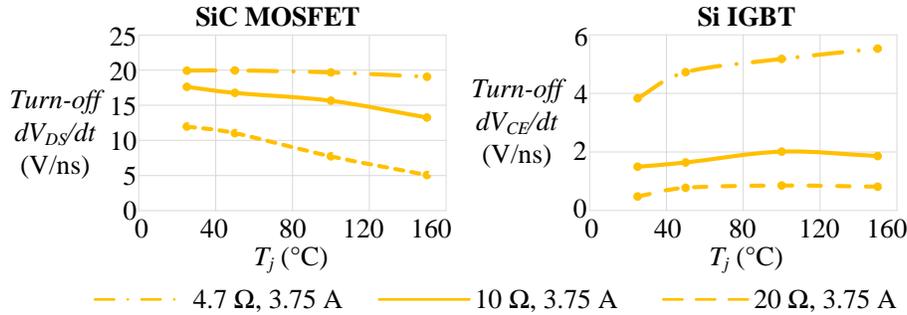


Figure 4.21. Temperature dependent trend of turn-off  $dV_{DS}/dt$  and  $dV_{CE}/dt$

#### 4.3.4. Internal Gate Resistance and Gate Current

Figure 4.22 are the turn-off gate current waveforms at different  $R_{g\_ext}$ . For medium-voltage low-current SiC MOSFETs, this TSEP decreases with the temperature. On the contrary,  $I_{g(pk)\_on}$  exhibits the positive thermal relevance for the Si IGBTs. According to (Eq.4.15), this is fundamentally caused by different thermal characteristics of the current switching rate in these two devices. For both Si IGBTs and SiC MOSFETs, the turn-on gate current experiences more severe oscillations than the turn-off counterpart. This is caused by the faster switching speed during the turn-on transient, which further introduces higher voltage on the parasitic common source inductance. From these overdamped waveforms, the turn-off gate current peak decreases with  $T_j$  for SiC MOSFETs. This is because the voltage on the parasitic common source inductance  $L_{SS}$  increases with the temperature, according to (Eq.4.15).

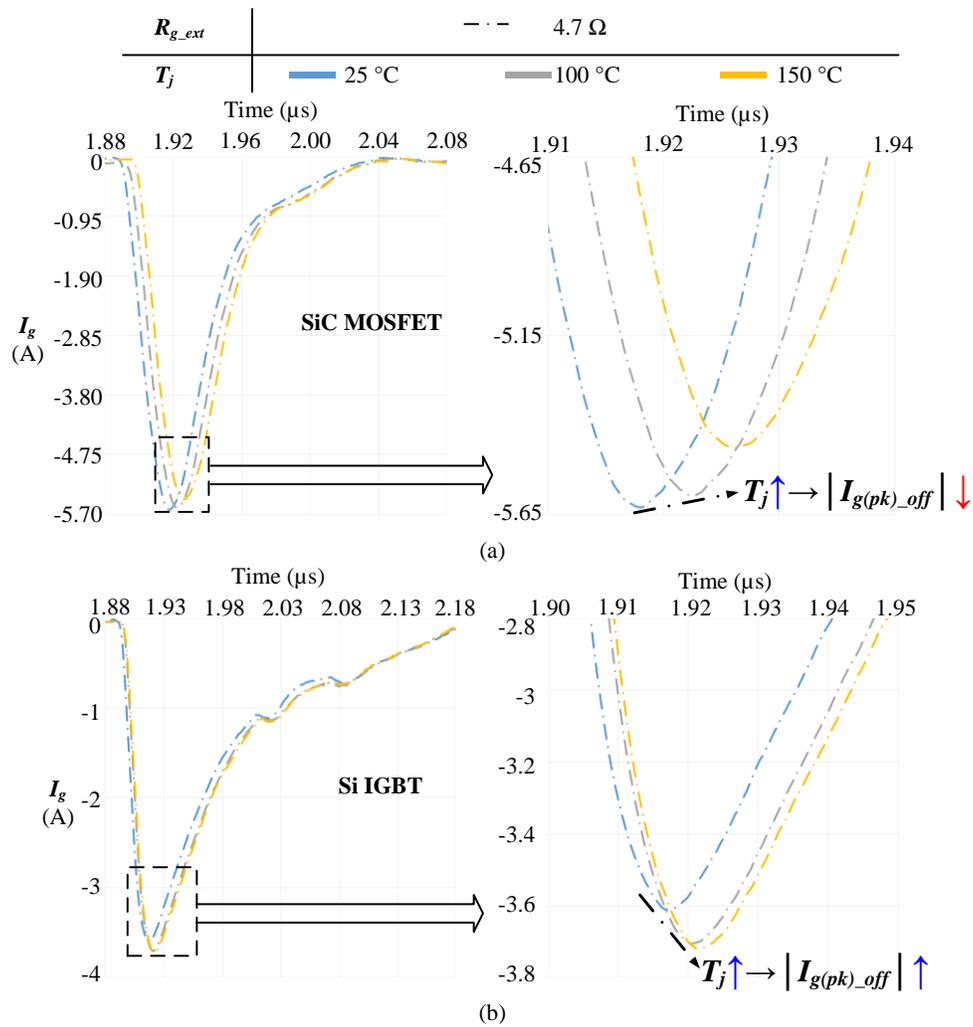


Figure 4.22.  $I_{g(pk)_{off}}$  temperature dependence of (a) SiC MOSFET, (b) Si IGBT

Due to smaller internal gate resistance, both the turn-on and turn-off gate current peaks are higher for SiC MOSFETs. This makes the gate current peak value a relatively better TSEP for SiC MOSFET. For the SiC MOSFET, the turn-off current peak is higher than turn-on current peak. This is because the turn-off speed is about 37.8% slower than the turn-on one. So,  $dI_{DS}/dt$  is much smaller during the turn-off transient. Thus, based on (Eq.4.15), the turn-off peak current is higher.

Figure 4.23 (a) and (b) are the turn-on gate current plateau measured at 2000 V DC voltage with 3.75 A load current. For Si IGBTs, the gate current peak increases with the temperature. This is because both the turn-on current switching rate and internal gate resistance play a promoting

role in the positive thermal relevance of the gate current peak, according to (Eq.4.15). But for SiC MOSFETs, the current switching rate  $dI_{DS}/dt$  and the internal gate resistance exert the opposite influence on the thermal dependence of the gate current peak. As a result, based on (Eq.4.15), the gate current peak is not monotonically associated with the junction temperature for SiC MOSFETs. Its temperature dependence is more obvious for SiC MOSFETs. This is because of the stronger threshold voltage negative thermal dependence. It would make the Miller plateau amplitude negative temperature relevance more obvious, which increases the gate current plateau to a larger extent according to (Eq.4.16). For Si IGBTs, when the external gate resistance is small, such as  $4.7 \Omega$ , the gate current plateau exhibits negative temperature dependence. This is because the Miller plateau amplitude would increase with temperature at small gate resistance. It would further level down  $I_{g(p)}$  according to (Eq.4.16). It is consistent with the Miller plateau thermal shift in Part 4.3.1. Smaller gate resistance helps improve the thermal sensitivity of gate current peak, which is consistent with (Eq.4.15). SiC MOSFETs exhibit larger temperature coefficients for the turn-off gate current peak.

The gate current plateau increases with  $T_j$  for SiC MOSFETs. From (Eq.4.16), the negative thermal dependence of both the  $V_{GS(p)}$  and  $R_{g\_int}$  contributes to this increase. As to Si IGBTs, the thermal relevance of the gate current plateau is either positive or negative, depending on the external gate resistance. As analyzed previously, this TSEP exhibits negative thermal dependence at small gate resistance. As  $T_j$  rises, lower  $V_{GS(p)}$  increases  $I_{g(p)}$  according to (Eq.4.16).

The larger gate resistance is generally instrumental in the temperature sensitivity of the turn-on gate current plateau. SiC MOSFETs exhibit better thermal sensitivity and linearity regarding the gate current plateau.

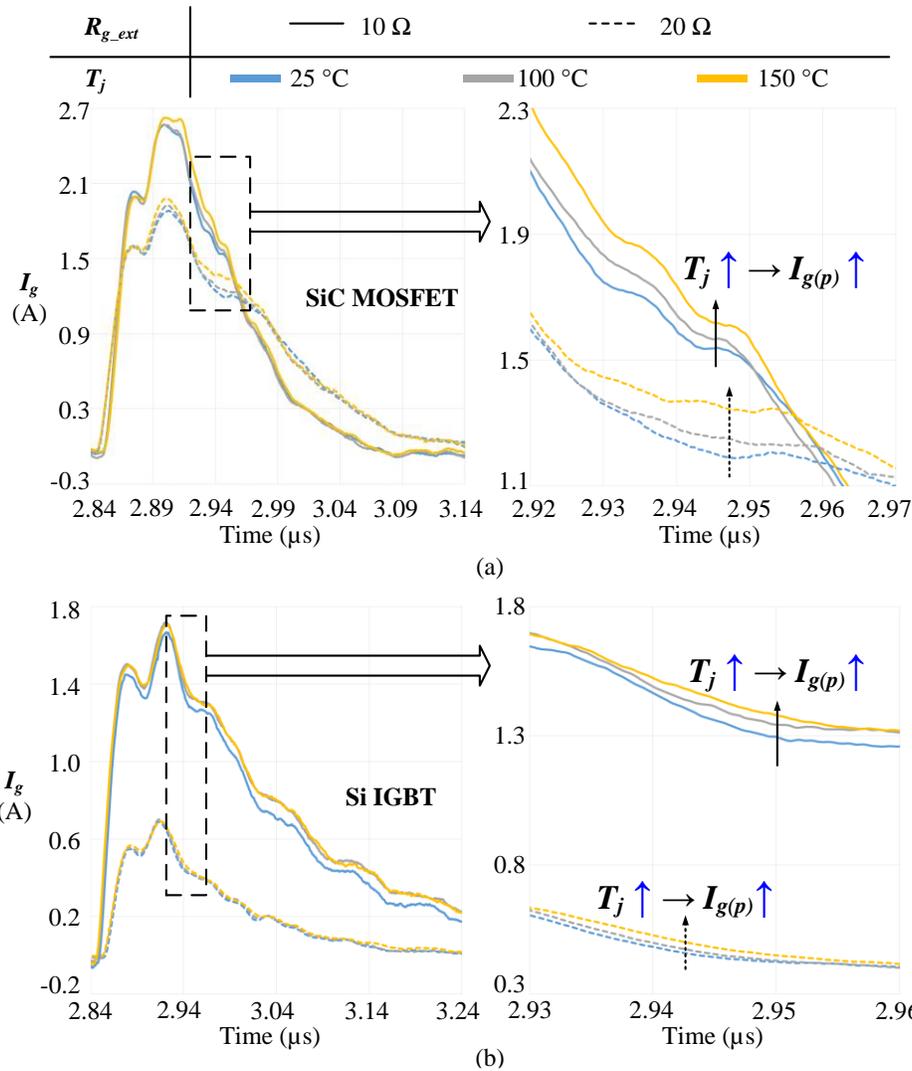


Figure 4.23.  $I_{g(p)}$  temperature dependence of (a) SiC MOSFET, (b) Si IGBT

#### 4.3.5. Turn-off Delay Time and Total Turn-off Time

Figure 4.24 (a) presents the turn-off  $V_{GS}$  and  $V_{DS}$  waveforms for the SiC MOSFET. While Figure 4.24 (b) shows the  $V_{GE}$  and  $V_{CE}$  waveforms for the Si IGBTs. They are both measured at 2000 V dc voltage, 3.75 A drain-source / collector-emitter current, and  $10 \Omega R_{g\_ext}$ . It could be seen that the turn-off delay time presents an obvious increase with the temperature for SiC MOSFETs. Nevertheless, this TSEP exhibits opposite temperature dependence for the tested medium-voltage low-current Si IGBTs. This could be explained in terms of Figure 4.10. According to the turn-off

delay time presented in (Eq.4.20), the fundamental reason is that these two devices have different temperature dependence of the Miller plateau amplitude.

To illustrate the impact of DC voltage and load current on the turn-off delay time, Figure 4.25 (a) and (b) summarize this TSEP for SiC MOSFETs and Si IGBTs, respectively. They are measured at  $10 \Omega R_{g\_ext}$  with different dc voltages and load currents. As can be seen, for SiC MOSFETs, the turn-off delay time increases with the temperature. This is because the Miller plateau and internal gate resistance contradict with each other in determining the thermal dependence of the turn-off delay time. But the turn-off delay time exhibits consistently negative temperature relevance for Si IGBTs. This is because both the Miller plateau amplitude and the internal gate resistance assist in the negative temperature dependence of the turn-off delay time in the Si IGBTs, according to (Eq.4.20). Besides, the Miller plateau increases with the load current, and the turn-off delay time is negatively dependent on the Miller plateau. As a result, the turn-off delay time decreases with the load current.

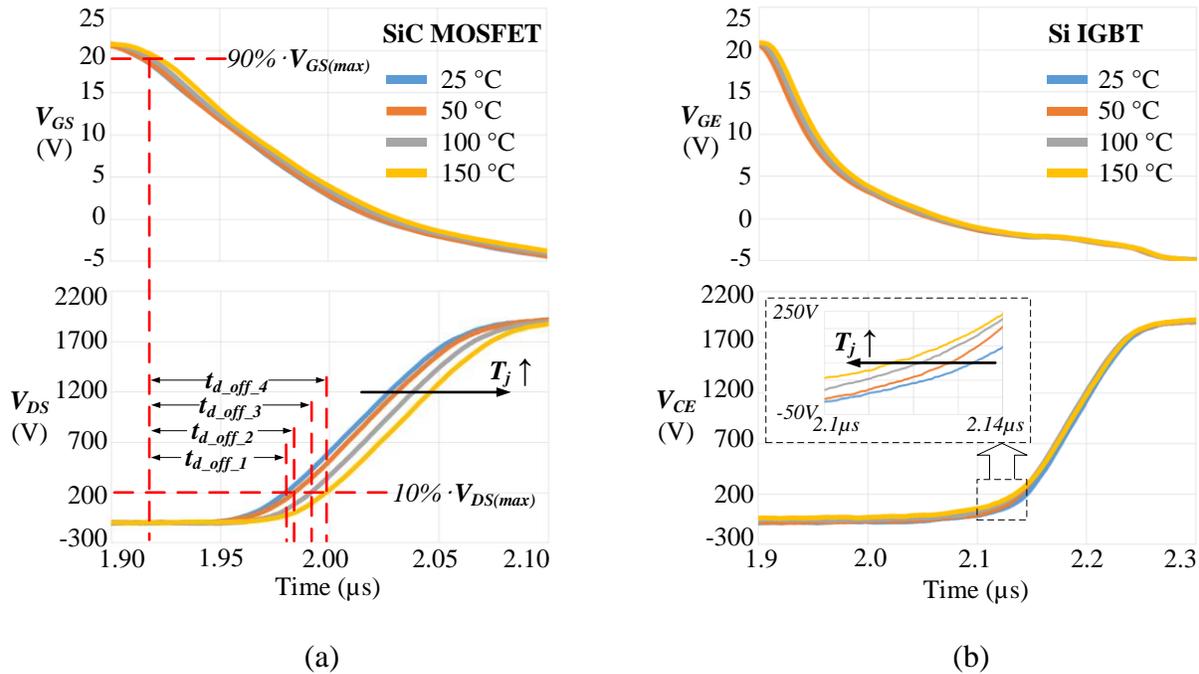


Figure 4.24. Waveforms indicating turn-off delay of a) SiC MOSFET (b) Si IGBT

By comparing Figure 4.25 (a) and (b), it could be concluded that both the DC voltage and load current play a more significant role in interfering the temperature sensitivity of the turn-off delay time for SiC MOSFETs compared with the Si IGBTs. This is caused by faster turn-off transient in the SiC devices. Besides, this TSEP is around three times longer for Si IGBTs, which makes them more detectable. For both of these two devices, this TSEP is more obvious when the dc voltage and load current become larger. But the load current has less obvious impact on the turn-off delay time for the Si IGBTs compared to SiC MOSFETs.

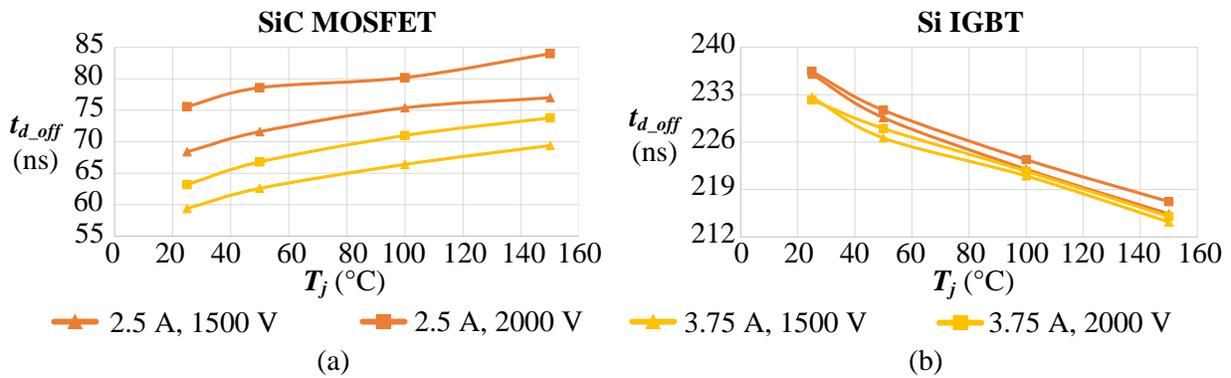


Figure 4.25. SiC MOSFET, Si IGBT turn-off delay time at different  $V_{DC}$ ,  $I_{DS} / I_{CE}$  ( $10 \Omega R_{g\_ext}$ )

Figure 4.26 (a) and (b) compare the  $t_{d\_off}$  in terms of different dc voltage and external gate resistance  $R_{g\_ext}$ , respectively. The average dc voltage sensitivity of the  $t_{d\_off}$  for SiC MOSFETs is about  $20 \mu\text{s}/\text{V}$ , which is approximately three times that of Si IGBTs. For both the devices, the  $t_{d\_off}$  exhibits a nonlinear relationship with the  $R_{g\_ext}$ . In sum, the SiC MOSFETs are more susceptible to the interference from the dc voltage, but less affected by the gate resistance change, compared to Si IGBTs.

Figure 4.27 summarizes the turn-off delay time temperature coefficients for SiC MOSFETs and Si IGBTs. This TSEP presents about three to four times better thermal sensitivity in Si IGBTs

compared with SiC MOSFETs. Larger external gate resistance would contribute towards longer turn-off delay time, which is consistent with (Eq.4.20).

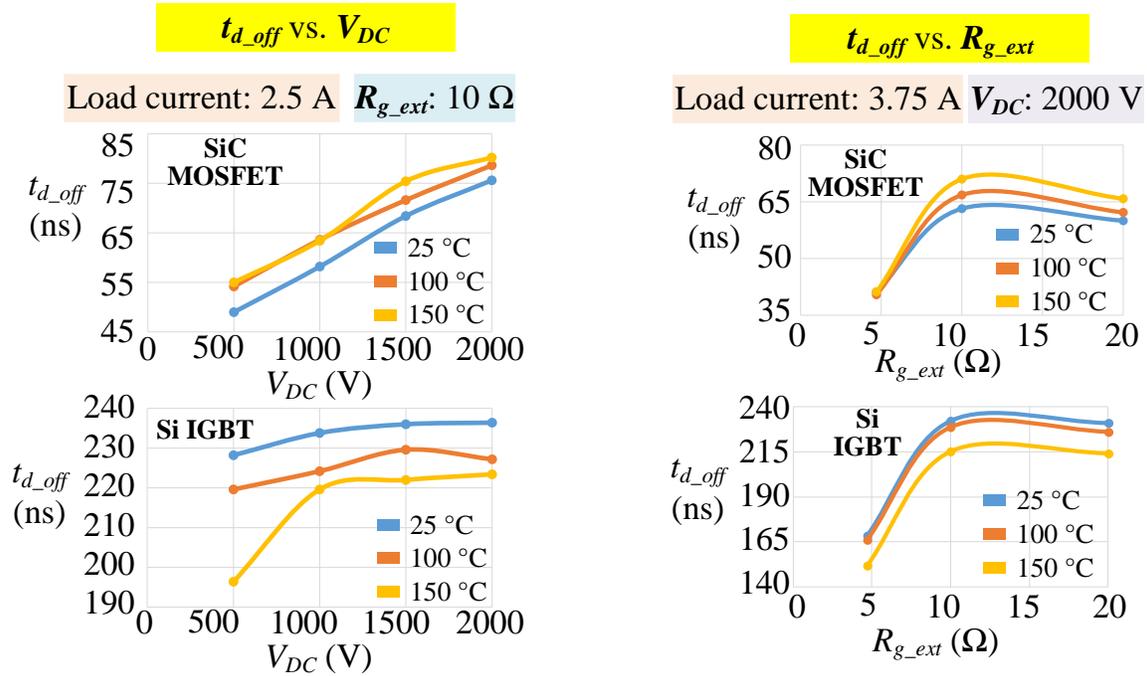


Figure 4.26. (a)  $t_{d\_off}$  vs. dc voltage  $V_{DC}$ , (b)  $t_{d\_off}$  vs. external gate resistance  $R_{g\_ext}$

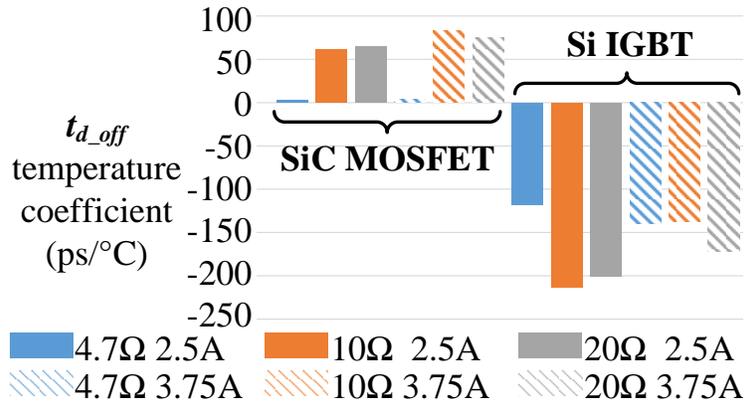


Figure 4.27. Thermal coefficients of  $t_{d\_off}$  for SiC MOSFETs and Si IGBTs

Taking both turn-off delay time and fall time into consideration, the temperature coefficients of the three TSEPs related to the turn-off transient are summarized in Figure 4.28 to examine whether the total turn-off time is a better TSEP regarding thermal sensitivity. For SiC

MOSFETs, the total turn-off time exhibits consistently positive temperature dependence. For Si IGBTs, the turn-off delay time is about twice the fall time but with opposite temperature relevance. So, the total turn-off time follows similar temperature relevance trend as the turn-off delay time. As a result, the total turn-off time presents a negative temperature coefficient for the Si IGBTs.

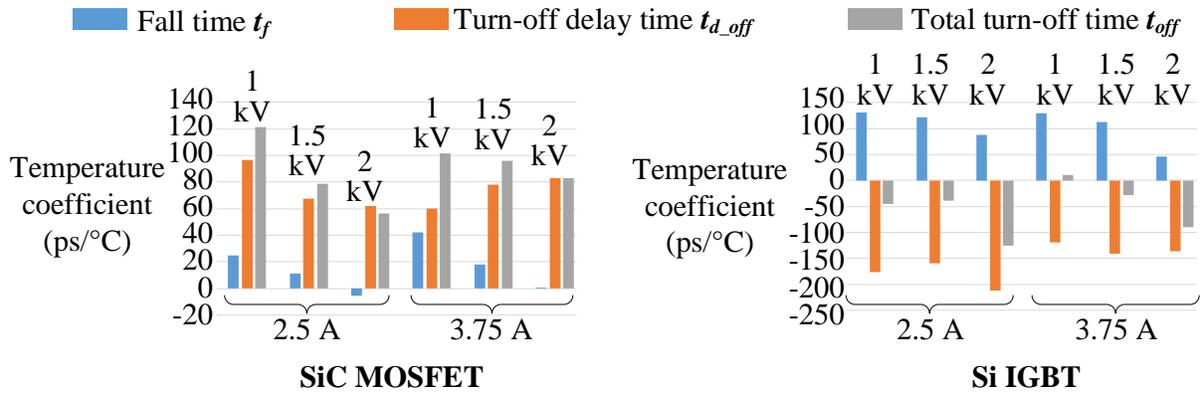


Figure 4.28. Temperature coefficient summary of the three TSEPs in the turn-off transient

#### 4.3.6. Turn-on Delay Time and Total Turn-on Time

Figure 4.29 (a) and (b) summarize the turn-on delay time  $t_{d\_on}$  for SiC MOSFETs and Si IGBTs, respectively. They are measured at  $10 \Omega R_{g\_ext}$  with various dc voltages and load currents. It could be seen that the  $t_{d\_on}$  is less susceptible to the load current change for Si IGBTs compared to SiC MOSFETs. For SiC MOSFETs, the  $t_{d\_on}$  decreases with the temperature. This is because both the Miller plateau amplitude and the internal gate resistance contribute to the negative thermal dependence of the turn-on delay time, according to the (Eq.4.25).

However, different from Si MOSFETs, the  $t_{d\_on}$  consistently increases with the  $T_j$  for Si IGBTs. This would be explained through Figure 4.11. It is basically caused by opposite temperature relevance of the Miller plateau amplitude in these two devices, according to (Eq.4.25). As to Si IGBTs, the positive thermal dependence of the Miller plateau amplitude exists. Besides,

the Miller plateau increases with the load current, and the turn-on delay time is positively dependent on the Miller plateau. As a result, the turn-on delay time increases with the load current.

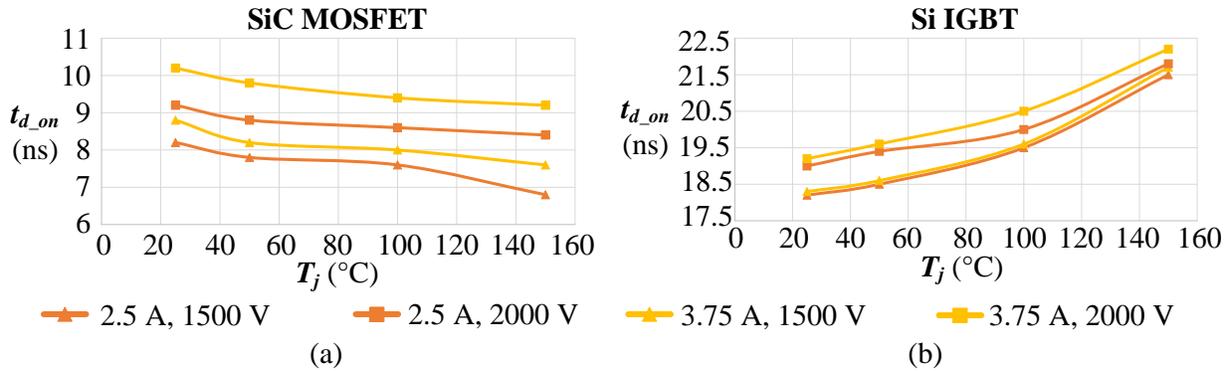


Figure 4.29. SiC MOSFET, Si IGBT turn-on delay time at different  $V_{DC}$  and  $I_{DS} / I_{CE}$

Furthermore, the relationships with the DC voltage and external gate resistance dependence are demonstrated in Figure 4.30 (a) and (b), respectively.

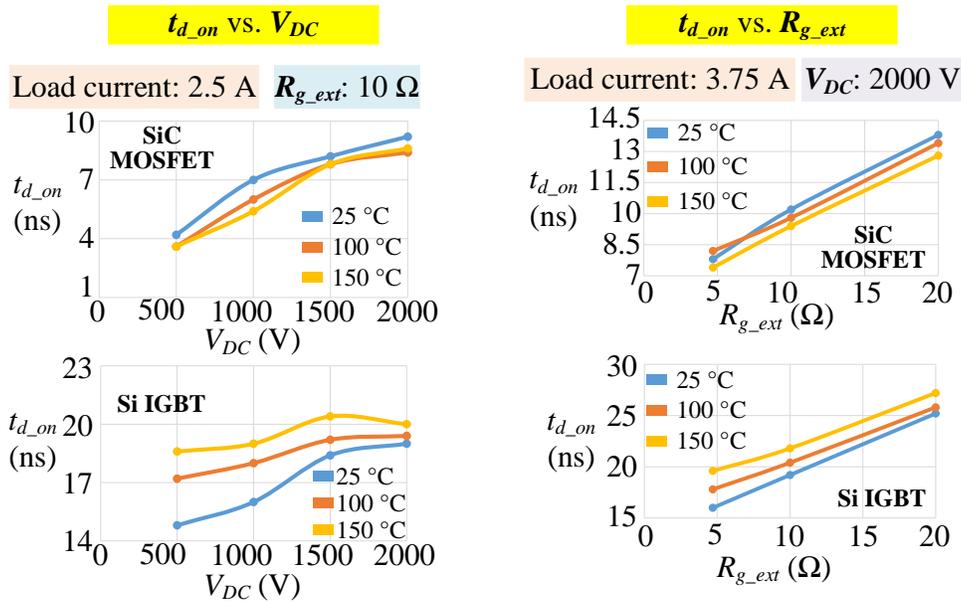


Figure 4.30. (a)  $t_{d\_on}$  vs. DC voltage  $V_{DC}$ , (b)  $t_{d\_on}$  vs. external gate resistance  $R_{g\_ext}$

The average dc voltage sensitivity of the  $t_{d\_on}$  for SiC MOSFETs is about 4 ps/V. While it is close to 3 ps/V for the Si IGBTs. The average external gate resistance sensitivity of the  $t_{d\_on}$  for

SiC MOSFETs is around 0.4 ns/ $\Omega$ . The corresponding one is approximately 0.33 ns/ $\Omega$ . Thus, it can be concluded that the interference from the change of DC voltage and gate resistance exhibits the similar extent for the two devices. Compared with the turn-off delay time, this TSEP is much less susceptible to the impact of either the DC voltage or external gate resistance. It is because the turn-on transient duration is shorter than the turn-off one. The turn-on delay time presents better linear relationship with the external gate resistance compared with turn-off delay time for both the SiC MOSFETs and Si IGBTs.

The temperature coefficients of the turn-on delay time are then summarized in Figure 4.31. For both of these devices, the turn-on delay time is less detectable and has smaller temperature sensitivity compared with the turn-off delay time. Si IGBTs have obviously larger turn-on and turn-off time compared with SiC MOSFETs due to slower switching speed. This is caused by larger intrinsic capacitance values in Si IGBTs. In comparison with SiC MOSFETs, both the turn-off delay and the turn-on delay exhibit better thermal linearity for Si IGBTs.

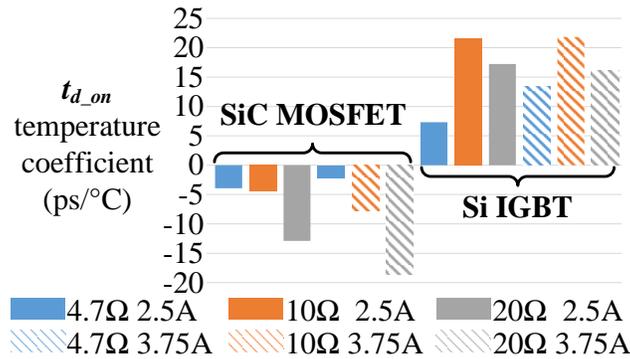


Figure 4.31. Temperature coefficients of the turn-on delay time

Figure 4.32 gives the thermal coefficients of the three TSEPs during the turn-on transient. Different from the total turn-off time, the total turn-on time has a negative temperature coefficient for SiC MOSFETs. Regarding the Si IGBTs, the rise time is around twice the turn-on delay time. So, the temperature coefficients of the total turn-on time are closer to the rise time for Si IGBTs.

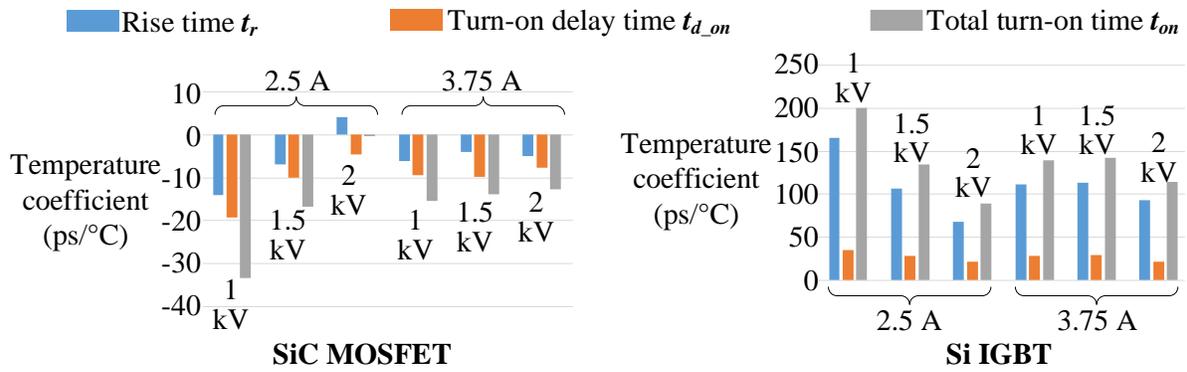


Figure 4.32. Temperature coefficients of the three TSEPs in the turn-on transient

#### 4.4. Summary for This Chapter

Based on the above theoretical analysis and testing results for the six groups of dynamic TSEPs, a summary is presented from the perspectives of the thermal sensitivity and linearity. In terms of the sensitivity, the conclusion would be provided both qualitatively and quantitatively.

On the one hand, the qualitative summary is given below.

1. The electron mobility is much smaller in SiC than in Si semiconductor. As a result, due to stronger temperature dependence of threshold voltage compared with that of the electron mobility, the Miller plateau amplitude of the medium-voltage low-current SiC MOSFETs exhibits more negative temperature dependence than that of Si IGBTs.
2. Because of larger electron mobility in Si IGBTs compared with SiC MOSFETs, as the temperature rises, the negatively temperature-dependent characteristics of the electron mobility would contribute more towards the decreasing of the current switching rate in Si IGBTs than in SiC MOSFETs. Therefore, the turn-on current switching rate exhibits a positive temperature relevance for SiC MOSFETs but a negative one for Si IGBTs. SiC MOSFETs have higher turn-on current switching rate but smaller thermal coefficient.
3. Due to different temperature relevance of the Miller plateau amplitude, the turn-off voltage switching rate exhibits a negative temperature dependence for medium-voltage low-current

SiC MOSFETs, but positive one for Si IGBTs. Smaller active die area contributes to better thermal sensitivity of the turn-off voltage switching rate in SiC MOSFETs.

4. Because the current switching rate exhibits different thermal characteristics on SiC and Si devices, the induced voltage on the common-source parasitic inductance results in different temperature dependence of the gate current peak. The turn-off gate current peak decreases with the temperature for medium-voltage low-current SiC MOSFETs. It presents the positive thermal relevance for the Si IGBTs. Besides, because of smaller internal gate resistance, both the turn-on and turn-off gate current peaks are higher for SiC MOSFETs. This makes the gate current peak a more detectable TSEP for SiC MOSFETs.
5. Due to more negative temperature relevance of Miller plateau amplitude, the positive thermal dependence of the gate current plateau is more obvious for SiC MOSFETs. For Si IGBTs, the thermal dependence of the gate current plateau could be positive or negative, depending on the external gate resistance. Smaller external gate resistance would level up the Miller plateau amplitude and further decrease the gate current plateau. SiC MOSFETs exhibit better thermal sensitivity of this TSEP.
6. Since the Miller plateau and internal gate resistance contradict with each other in determining the thermal dependence of the turn-off delay time, it increases with the temperature for medium-voltage low-current SiC MOSFETs. But both the Miller plateau amplitude and the internal gate resistance assist in the negative temperature dependence of the turn-off delay time in Si IGBTs. This TSEP is more detectable for Si IGBTs. It is more susceptible to the interference from the dc voltage, but less affected by the gate resistance change for SiC MOSFETs, compared to Si IGBTs.

7. The total turn-off time exhibits consistently positive temperature dependence for SiC MOSFETs. It presents a negative temperature coefficient for the Si IGBTs.
8. Both the Miller plateau amplitude and the internal gate resistance contribute towards the negative temperature dependence of the turn-on delay time for SiC MOSFETs. However, it consistently increases with the temperature for Si IGBTs, due to the opposite temperature relevance of the Miller plateau amplitude in these two devices. For both of these devices, the turn-on delay time is less detectable and has smaller temperature sensitivity compared with the turn-off delay time.
9. Different from the total turn-off time, the total turn-on time has a negative temperature coefficient for SiC MOSFETs. For Si IGBTs, the temperature coefficients of the total turn-on time are positive and closely dependent on the rise time.

On the other hand, Table 4.1 provides a quantitative comparison of the largest temperature coefficient at 2000 V DC voltage. The TSEPs that are more sensitive to  $T_j$  are highlighted. Compared with Si IGBTs, the turn-off drain-source voltage switching rate, turn-off gate current peak, turn-on gate current plateau, and turn-on gate-source voltage Miller plateau amplitude present better thermal sensitivity for SiC MOSFETs. Among the three TSEPs related to the gate current, the turn-off gate current peak exhibits the largest temperature coefficient for medium-voltage low-current Si IGBTs. While for the SiC MOSFETs, the turn-on gate current plateau is the most suitable TSEP if only the gate current is measured.

In terms of the linearity, the turn-on gate current plateau exhibits better thermal linearity for the medium-voltage low-current SiC MOSFETs. Comparatively, for the Si IGBTs, the fall time, rise time, turn-off delay time, and turn-on delay time present better temperature linearity.

Besides, for both devices, the turn-on delay time has been verified to present better linear relationship with the external gate resistance compared with turn-off delay time.

Since these dynamic TSEPs do not require the same effort to be detected, an investigation of the implementation complexity has been conducted. Figure 4.33 summarizes the state-of-art measurement approaches for these TSEPs. The detection of the Miller plateau amplitude and the gate current plateau can be realized based on the same theory. One method utilizes both the  $V_{DS}$  and  $V_{GS}$  parameters [48]. When  $V_{GS}$  begins to arrive at the Miller plateau, the  $V_{DS}$  would experience a voltage drop. By identifying this voltage after dropping as the reference, the Miller plateau can be indicated. A sample and hold circuit is normally applied to let the output maintain at the gate voltage Miller plateau by following  $V_{GS}$ , or at the gate current plateau by following the gate resistor

Table 4.1. Temperature Sensitivity Summary of the Investigated TSEPs

Dynamic TSEP names	Dynamic TSEP symbols		Largest temperature coefficient at 2000 V $V_{DC}$		Measured parameters needed
	3.3 kV, 5 A SiC MOSFET	3 kV, 12 A Si IGBT	3.3 kV, 5 A SiC MOSFET	3 kV, 12 A Si IGBT	
Gate-source voltage Miller plateau amplitude	$V_{GS(p)}$	$V_{GE(p)}$	-4.2 mV/°C	4.6 mV/°C	$V_{GS}$ ( $V_{GE}$ )
Turn-on current switching rate	$dI_{DS}/dt$	$dI_{CE}/dt$	328 A/(ms·°C)	-424 A/(ms·°C)	$I_{DS}$ ( $I_{CE}$ )
Turn-off Voltage switching rate	$dV_{DS}/dt$	$dV_{CE}/dt$	-60 V/(μs·°C)	14.4 V/(μs·°C)	$V_{DS}$ ( $V_{CE}$ )
Gate current peak	$I_{g(pk\_off)}$		1.46 mA/°C	-0.79 mA/°C	$I_g$
Gate current plateau	$I_{g(p)}$		1.58 mA/°C	0.47 mA/°C	
Turn-off delay time	$t_{d\_off}$		82.7 ps/°C	-213 ps/°C	$V_{DS}$ and $V_{GS}$ ( $V_{CE}$ and $V_{GE}$ )
Turn-on delay time	$t_{d\_on}$		-18.6 ps/°C	21.8 ps/°C	
Turn-off time	$t_{off}$		83.12 ps/°C	-125.83 ps/°C	
Turn-on time	$t_{on}$		-12.61 ps/°C	114.58 ps/°C	

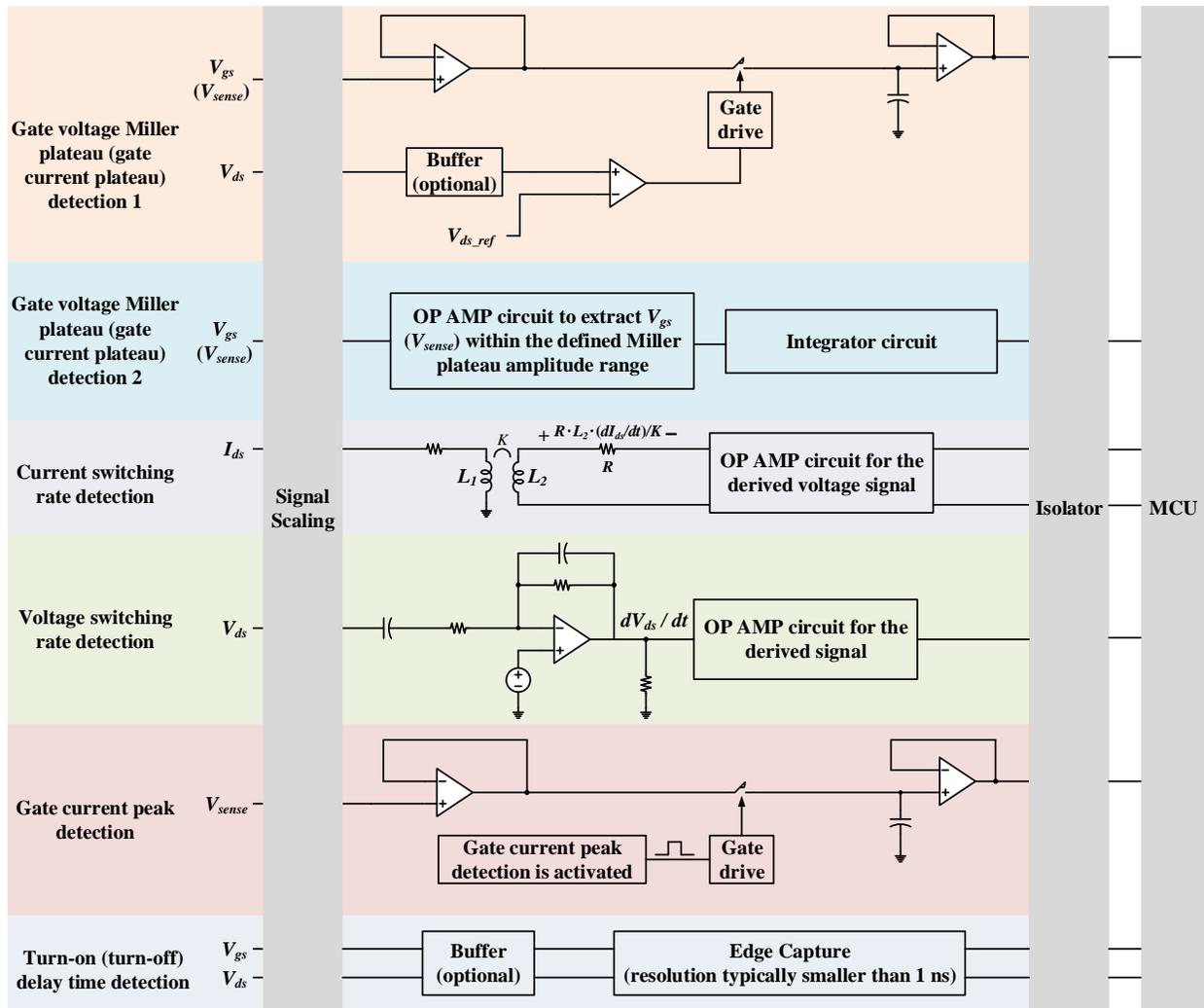


Figure 4.33. Summary of the detection approaches for the investigated dynamic TSEPs

voltage  $V_{sense}$ . Another method is to use the op amp circuit and select the wanted  $V_{GS}$  amplitude range [364]. To get rid of the effect of the high-frequency small noise interference, an integrator can be followed to accumulate the detected signal. The current switching rate is the most challenging TSEP to be detected. It requires a coupled inductor to sense the current switching rate and process the derived voltage signal through op amp circuits [381]. The  $V_{DS}$  switching rate can be measured by a differentiator circuit with stability compensation [382]. The corresponding  $dV_{DS}/dt$  can then be processed with an op amp circuit. The gate current peak detection is based on

a controlled sample and hold circuit [279]. Once the gate current peak detection is activated, the gate current peak would be maintained and recorded into the following stages. As to the turn-on and turn-off delay time, the duration is nano-second level. As a result, the  $V_{DS}$  and  $V_{GS}$  edge capture requires high enough resolution, which is typically smaller than 1 ns [299][294].

In summary, this chapter has explored six groups of the typical dynamic TSEPs for the medium-voltage low-current SiC MOSFETs. Their theoretical temperature dependence has been analyzed. The impact of the parasitic parameters have been considered. A test platform has been designed and dedicated to conduct the temperature dependent characterization. A comparison with the medium-voltage low-current Si IGBTs has been made. Among the investigated TSEPs, the turn-off voltage switching rate  $dV_{DS}/dt$ , the turn-off gate current peak  $I_{g(pk)_{off}}$ , and the turn-on gate current plateau  $I_{g(p)}$  could achieve higher temperature coefficient compared with those of the medium-voltage, low-current Si IGBTs. The turn-on gate current plateau  $I_{g(p)}$  exhibits better thermal linearity for these SiC MOSFETs. While the fall time, rise time, turn-off delay time, and turn-on delay time are better TSEPs for medium-voltage low-current Si IGBTs in terms of the thermal linearity. In terms of the real-time implementation, current switching rate is the most challenging TSEP to be detected due to extra coupled inductor circuit. Besides, high-resolution edge capture MCU is essential in the detection of the turn-on and turn-off delay time due to their nano-second durations. This work would provide helpful directions for the real-time junction temperature detection technique development and health monitoring hardware design for the emerging medium-voltage wide band-gap devices.

## 5. A GENERALIZED TOPOLOGY LEVERAGING WBG DEVICE ADVANTAGES

Compared with the traditional silicon-based devices, the wide band-gap counterparts normally have smaller intrinsic capacitance, lower on-resistance, and operate at higher switching frequency. To fully take advantage of these characteristics of the wide band-gap devices, this chapter proposes a generalized topology called switched tank converter (STC) based on resonant switched-capacitor converter concepts. It has the modular structure with flexible scalability and achievable redundancy. It only utilizes low voltage and low current rating devices to achieve high voltage, high current, and high conversion ratio application. It can achieve soft switching strategies including ZCS [383][384][385][386] and ZVS [387][388] for all the STC switches to minimize the switching losses with the help of the resonant tank design and appropriate control methods. High switching frequency could be adopted to minimize the resonant component size. Besides, the inductances are distributed among resonant tanks, so that each inductance is smaller. The low on-resistance feature of the WBG devices can be leveraged by utilizing this topology. Furthermore, voltage regulation can be achieved with either control or topology adjustment. Finally, since the temperature is evenly distributed within the converter without hot spots, it is desirable for compact thermal design. In the first section, the circuit structure and operation principle will be analyzed.

Since different topologies use different voltage rating devices, it is difficult to compare the semiconductor die area usage among topologies. Relative total semiconductor chip area is introduced in [389], but it does not consider the relationship between total die area and the device power loss. Total switching device power is defined in [390] using the product of switch voltage and current stresses as the evaluation method. But it cannot indicate the optimized die area requirement for different topology designs. Dr. B. Jayant Baliga proposed a device-level index

called figure of merit in [25], but it fails to evaluate the total device power loss among different topologies by using only on-resistance and the total gate charge.

To overcome the above issue of comparing topologies with different device voltage rating, the second section proposes the total semiconductor loss index (TSLI) as the topology evaluation method. It tries to generate the relationship between the converter total semiconductor die area and the total device power loss. Different topologies could achieve similar power loss at their own optimization points with different semiconductor die area. The semiconductor die area has a direct relationship with the manufacturing costs. Thus, a customized die area usage for a converter with specific electrical parameters helps optimize the efficiency with reasonable device manufacturing costs. Therefore, a relatively fair total semiconductor power loss comparison assuming the same die area usage is important. It provides a more comprehensive understanding about which topology can achieve the lower power loss with the same die area usage.

This chapter serves as the fundamental overture for the following three chapters. Chapter 6 through 8 will utilize the generalized circuit structure proposed in the below section to develop WBG based applications. They will also apply the TSLI to evaluate the derived topologies.

### **5.1. Circuit Structure and Operation Principle**

Figure 5.1 shows the proposed generalized  $N$ -cell STC [391]. Each cell can be considered as a four-terminal two-port network with two terminals on the input port and two terminals on the output port. All the cells share the same input and output port voltage. In the generalized  $N$ -cell STC architecture,  $N$  input ports are connected in parallel and  $N$  output ports are connected in series, while the bottom terminal of the output port in the 1<sup>st</sup> cell is connected with the top terminal of the input port, as shown in Figure 5.1. As a result, the output voltage is  $(N+1)$  times  $V_{in}$ . A voltage

transfer ratio of  $1:(N+1)$  can be realized in a  $N$ -cell STC topology. The proposed topology can also provide opposite current flow when the input and output terminals are reversed.

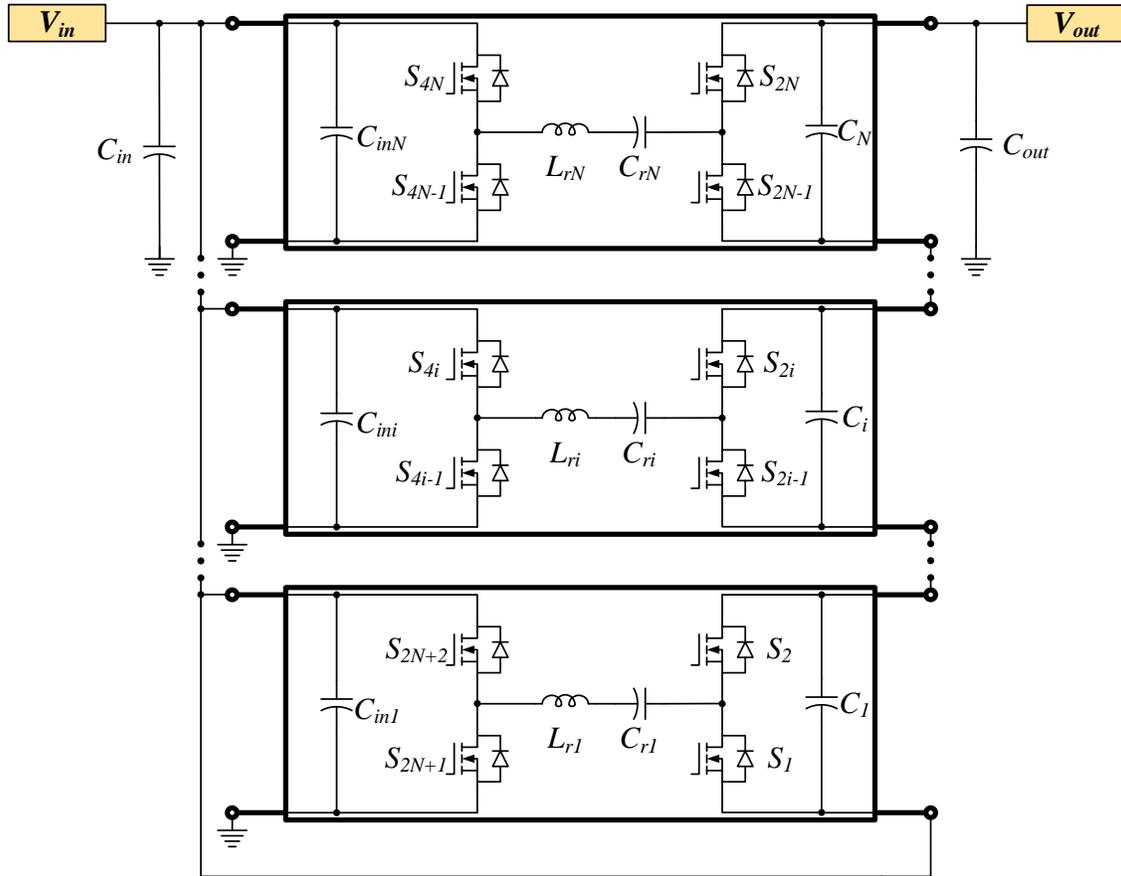


Figure 5.1. Generalized  $N$ -cell STC topology with voltage transfer ratio  $1:(N+1)$

Each cell of the proposed STC is composed of two half-bridges, one resonant tank and two clamping capacitors on both the input and output sides. All the switch voltage stress of the proposed STC is equal to the low side voltage, which makes it more suitable for higher voltage applications. Recently published STCs [383][384][385] have some switches with voltage stress twice of the low side voltage, which are more suitable for the low voltage applications, e.g. the 48-V-to-12-V DC-to-DC converter, where the 25 V and 40 V devices can be utilized. However, for the high voltage applications, the devices with voltage rating twice of the input voltage might not

be available. The proposed STC could utilize all low voltage devices to achieve the high output voltage, e.g. 300-V-to-1200-V DC-to-DC converter utilizing the 650 V GaN HEMTs. The resonant tank of the cell # $i$ 's capacitor  $C_{ri}$  DC bias voltage equals to  $i$  times  $V_{in}$ . The inductor  $L_{ri}$  has pure AC current. Thanks to the clamping of the capacitor  $C_i$  in each cell, the drain-source voltage stress of the switches is clamped to the low side voltage. For the current stress evaluation, from the switch current  $I_S$  in (Eq.5.1), the switch average current  $I_{S(AVG)}$  is shown in (Eq.5.2) [392], which is  $1/\pi$  of the switch peak current  $I_{S(PK)}$ .

$$I_S = \begin{cases} I_{S(PK)} \cdot \sin \omega t & 0 \leq t \leq (T_S / 2) \\ 0 & (T_S / 2) < t \leq T_S \end{cases} \quad (\text{Eq.5.1})$$

$$I_{S(AVG)} = \frac{1}{T_S} \int_0^{T_S/2} I_{S(PK)} \cdot \sin(\omega t) dt = \frac{I_{S(PK)}}{\pi} \quad (\text{Eq.5.2})$$

In this  $N$ -cell generalized STC topology, the average switch current  $I_{S(AVG)}$  is equal to the current on the low-current side. The current stress is  $\pi$  times the current on the low-current side.

In order to validate the proposed topology, a one-cell STC topology is presented in Figure 5.2 (a). This topology has been briefly mentioned in [393], but the soft switching operation principles have not been illustrated in detail. There are two main switching modes of this STC operating at ZCS. When  $S_1$  and  $S_3$  are ON, the switching mode I is presented in Figure 5.2 (b). The resonant capacitor  $C_R$  is charged and resonant inductor  $L_R$  stores energy. When  $S_2$  and  $S_4$  are ON, the resonant capacitor  $C_R$  discharges together with the input voltage source in the switching mode II as presented in Figure 5.2 (c). The resonant inductor  $L_R$  releases energy in this mode.

Figure 5.3 presents the ideal operating waveforms of this topology. In switching mode I,  $C_I$  keeps releasing energy to the load.  $C_{in}$  releases the energy most of the time. In switching mode II,  $C_I$  stores energy most of the time.  $C_{in}$  keeps storing energy. According to the analysis in the

generalized  $N$ -cell STC topology, the voltage transfer ratio is 2 in this one-cell STC circuit. As a result, a voltage doubler is achieved.

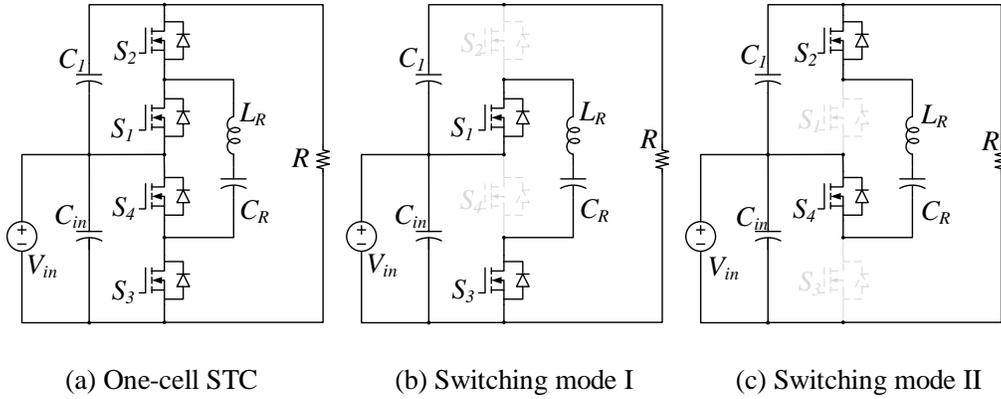


Figure 5.2. One-cell STC and equivalent circuits of the two switching modes

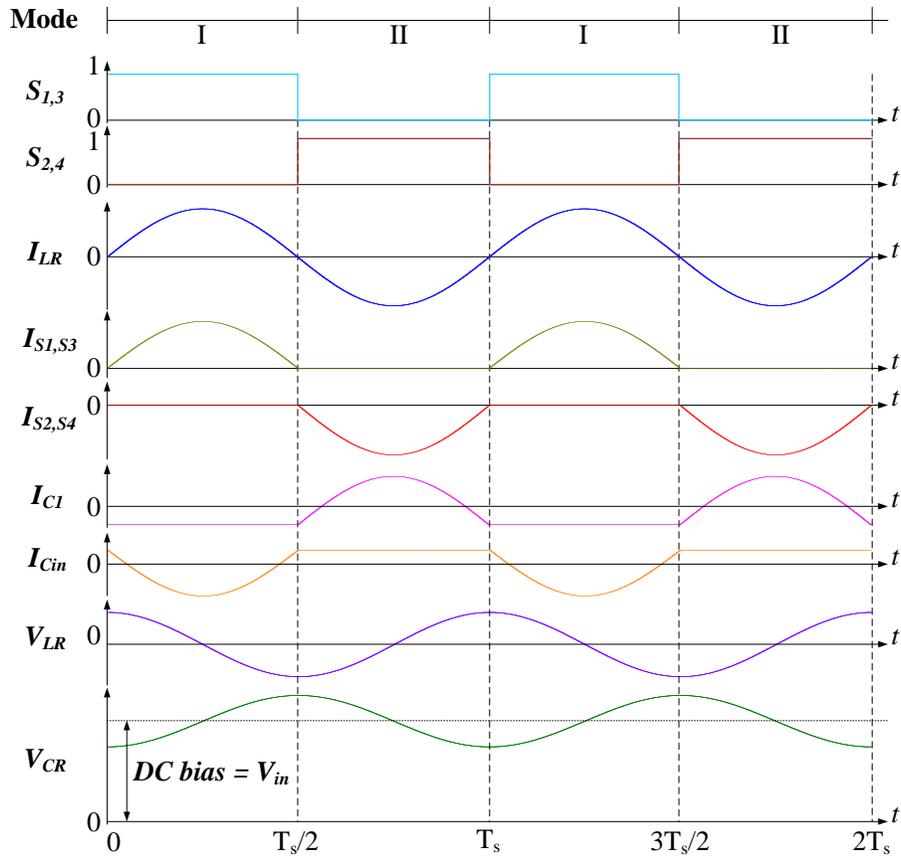


Figure 5.3. Theoretical waveforms of the one-cell switched tank converter

To further illustrate the proposed topology, a 2-cell STC topology is also analyzed. The circuit of 2-cell STC is shown in Figure 5.4. There are two switching modes, which are presented in Figure 5.5.

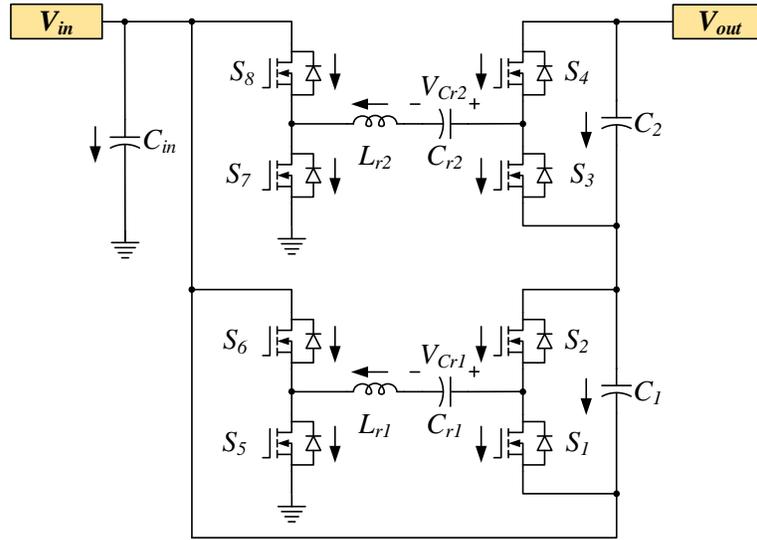


Figure 5.4. The 2-cell STC topology

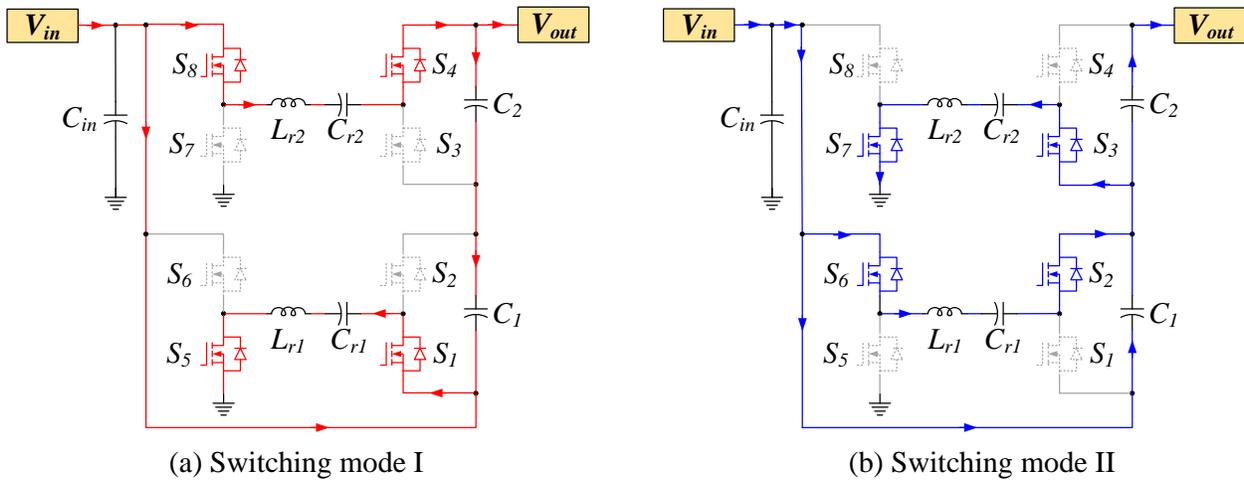


Figure 5.5. Two switching modes for the 2-cell STC

The ideal operation waveforms are shown in Figure 5.6 based on MATHCAD calculation. In switching mode 1, the  $C_{r1}$  is charged,  $C_{r2}$  is discharged and delivers power to output side. Two

clamping capacitors  $C_1$  and  $C_2$  are charged most of time in this mode. In switching mode 2,  $C_{r2}$  is charged,  $C_{r1}$  is discharged. Two clamping capacitors both discharge to the output side.

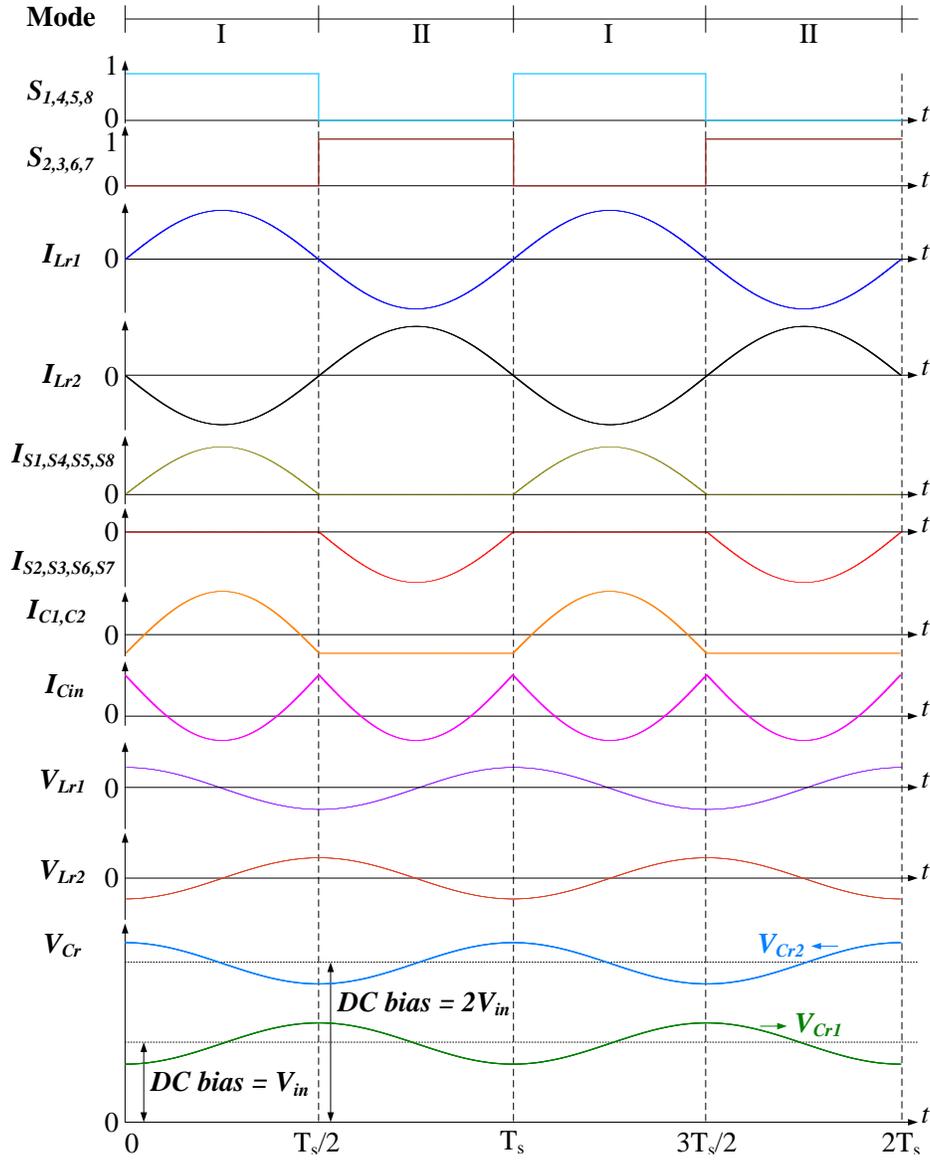


Figure 5.6. Operation waveforms of the 2-cell STC

Compared with conventional STC, the proposed STC shares the following similarities.

- 1) They have the same current stress for all the switches. For the  $N$ -cell STC, the switch RMS current of both two topologies can be expressed in (Eq.5.3).

$$I_{RMS\_S} = \sqrt{\frac{1}{T_s} \int_0^{T_s} (i_S(t))^2 dt} = \frac{\pi}{2} \cdot \frac{P_o}{V_{in} \cdot (N+1)} \quad (\text{Eq.5.3})$$

2) They share the same synchronous rectifier switches. Take the 1:4 converter for example.

From Figure 5.7 (a) and (b), these two circuits have the same switch types for  $S_{5(a)} \sim S_{10(a)}$  in conventional STC and  $S_{7(b)} \sim S_{12(b)}$  in the proposed STC.

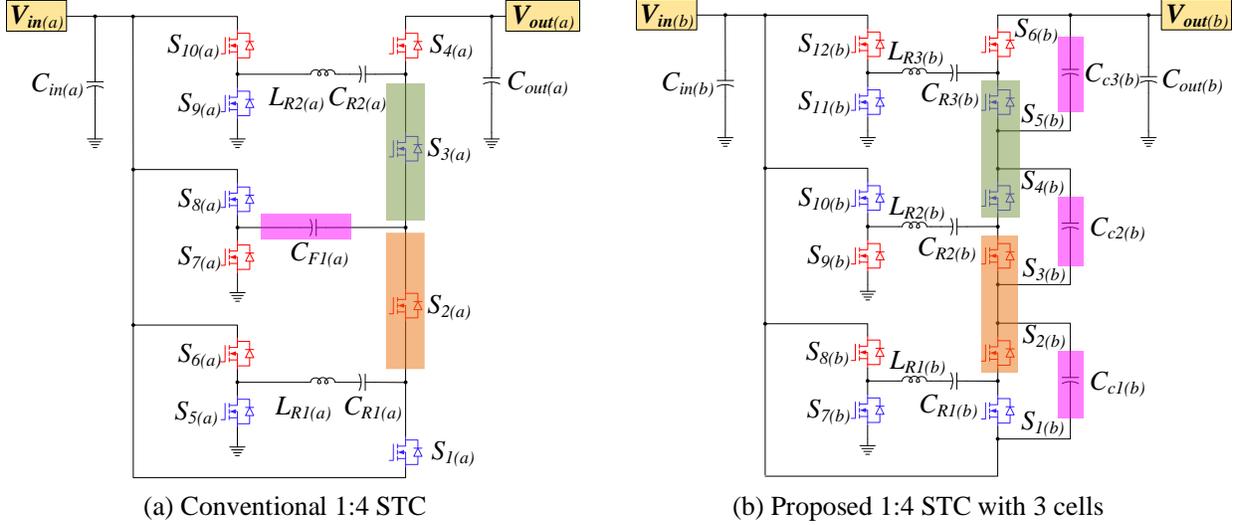


Figure 5.7. Conventional and proposed STC topologies with 1:4 conversion ratio

3) The resonant tank current and voltage are the same for the two topologies. Specifically, for the two circuits,  $L_{R1(a)}$ ,  $C_{R1(a)}$ ,  $L_{R2(a)}$ ,  $C_{R2(a)}$  in the conventional STC have the same voltage and current waveforms with  $L_{R1(b)}$ ,  $C_{R1(b)}$ ,  $L_{R2(b)}$ ,  $C_{R2(b)}$ ,  $L_{R3(b)}$ ,  $C_{R3(b)}$  in the proposed STC.

On the other hand, the proposed circuit has the following characteristics.

1) Only one type of switches is needed for  $S_{1(b)} \sim S_{12(b)}$  in the proposed STC topology with all the switch voltage stress equal to input voltage. But the conventional switched tank converter needs two types of switches. From Figure 5.7,  $S_{1(a)}$ ,  $S_{4(a)}$ ,  $S_{5(a)} \sim S_{10(a)}$  can be selected as one type of switches with the voltage stress equal to input voltage, but  $S_{2(a)}$ ,  $S_{3(a)}$

should be selected as another type of switches with the voltage stress equal to twice the input voltage.

- 2) In the proposed STC, the clamping capacitance is smaller than previous STC's clamping capacitance, which is also called non-resonant capacitance or DC filtering flying capacitance [383]. To make sure all the resonant loops have almost the same resonant frequency, the dc filtering flying capacitance is required to be large enough, e.g. ten times the resonant capacitance [384]. But for the proposed STC, the clamping capacitance can be as small as several hundred nano Farads.
- 3) Both ZCS and ZVS are achievable for the proposed STC. But for the conventional STC, only ZCS can be conducted. For conventional STC, not all the switch  $C_{oss}$  can find nearby loops to recycle their stored energy before being turned on. Thus, there is limitation for this topology to realize ZVS. But in the proposed topology, for all the switches, ZVS can be achieved by adjusting the control PWM and creating the recycling loops for the  $C_{oss}$  to fully release the energy through the inductor in the resonant tank circuit before the switches are turned on. Since the  $C_{oss}$  loss takes about 8% of the total loss in the 450 W prototype [384], it would decrease the total power loss and increase the efficiency by around 0.2% in this specific application if the ZVS is achieved in the proposed topology.

## 5.2. Total Semiconductor Loss Index (TSLI)

Different topologies use devices with various voltage ratings and operate at their own optimized output power. As investigated above, multiple topologies such as boost converter, flying capacitor multilevel converter (FCMC) could achieve relatively high efficiency by selecting specific semiconductor die areas at the same power rating. But different from the traditional boost converter, the FCMC and STC topologies utilize the devices with lower voltage rating. Thus, how

to evaluate these topologies needs to be deliberated. A new evaluation index called total semiconductor loss index (TSLI) is proposed to relate the device power loss with the total die area usage so that minimal device power loss with an optimized die area can be achieved.

The product of on-resistance  $R_{DS\_ON}$  and die area  $A_{die}$ , called specific on-resistance has been regarded as an index to reflect the device technologies [394]–[399]. By taking Cree/Wolfspeed® SiC MOSFET die for example, the  $R_{DS\_ON} \cdot A_{die}$  versus blocking voltage  $V_B$  and the junction temperature  $T_j$  can be analyzed. To evaluate the  $R_{DS\_ON}$  vs.  $T_j$  information, the following assumptions could be made. For Cree 900 V SiC die CPM3-0900-0010A, only  $R_{DS\_ON}$  at 25°C has been given from available resources. For Cree 1200 V SiC die CPM2-1200-0025B and Cree 1700 V SiC die CPM2-1700-0045B, the  $R_{DS\_ON}$  vs.  $T_j$  curves have been provided. Since the  $R_{DS\_ON}$  vs.  $T_j$  curves are close to each other for the 1200 V and 1700 V dies, one  $R_{DS\_ON}$  vs.  $T_j$  curve is utilized for all the Cree SiC dies to simplify this problem. Based on the normalized  $R_{DS\_ON}$  vs.  $T_j$  curve fitting of the 1200 V Cree die, the following (Eq.5.4) is derived.

$$\frac{R_{DS(ON)}(T_j)}{R_{DS(ON)}(25^\circ C)} = -9 \times 10^{-9} \cdot (T_j)^3 + 3 \times 10^{-5} \cdot (T_j)^2 + 0.0022 \cdot (T_j) + 0.9251 \quad (\text{Eq.5.4})$$

By utilizing the above function to consider the junction temperature impact on the on-resistance for Cree SiC dies, the updated specific on-resistance equation is shown in (Eq.5.5).

$$R_{DS(ON)} \cdot A_{die} = \alpha_2(\xi, V_B) \cdot \frac{R_{DS(ON)}(T_j)}{R_{DS(ON)}(25^\circ C)} = 6 \times 10^{-8} \cdot (V_B)^{2.2735} \cdot \frac{R_{DS(ON)}(T_j)}{R_{DS(ON)}(25^\circ C)} \quad (\text{Eq.5.5})$$

Based on this relationship, and considering the on-resistance at 25°C with 18 V  $V_{GS}$  is about 3.1 mΩ, the specific on-resistance vs. breakdown voltage and junction temperature is illustrated in Figure 5.8. This plot has utilized the above on-resistance thermal characteristics from Cree/Wolfspeed® SiC MOSFET die as a reference. It can not only reflect that the specific on-resistance decreases with the voltage rating reduction, but also show the junction temperature's

positive impact on the specific on-resistance. The FCMC and STC topologies utilize the devices with lower voltage rating to achieve smaller specific on-resistance, which indicates lower conduction loss and smaller die area. However, the device number increases with extended modules, which dwarfs these advantages. Therefore, by evaluating the total semiconductor die area usage, the topology-level specific on-resistance can reflect the impact of different chip technologies on the device conduction loss among various topologies.

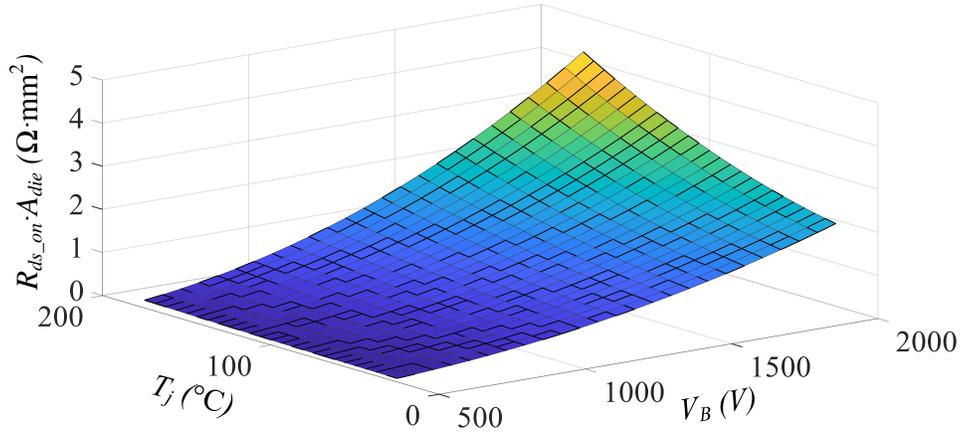


Figure 5.8. Specific on-resistance versus the breakdown voltage and junction temperature

Basically, the relationship between  $R_{DS\_ON} \cdot A_{die}$  and  $V_B$  can be represented by using the on-resistance technology function  $\alpha(\xi, V_B)$  in (Eq.5.6) [394]–[399]. It is derived from the theoretical SiC  $R_{DS\_ON} \cdot A_{die}$  versus  $V_B$  curves and the product information.

$$R_{DS(ON)} \cdot A_{die} = \alpha(\xi, V_B) = \xi \cdot (V_B)^X \quad (\text{Eq.5.6})$$

where,  $\xi$  is the constant dependent on semiconductor manufacturing technologies.  $X$  is an exponent close to 2. The theoretical SiC limit  $\alpha_{SiC}(\xi, V_B)$  is presented in (Eq.5.7).

$$\alpha_{SiC}(\xi, V_B) = 4 \times 10^{-8} \cdot (V_B)^{1.988} \quad (\text{Eq.5.7})$$

The on-resistance technology function is represented as  $\alpha_1(\xi, V_B)$  in (Eq.5.8) for SiC MOSFETs from Rohm and  $\alpha_2(\xi, V_B)$  in (Eq.5.9) for those from Cree, based on the curve fitting results.

$$\alpha_1(\xi, V_B) = 3.984 \times 10^{-7} \cdot (V_B)^2 \quad (\text{Eq.5.8})$$

$$\alpha_2(\xi, V_B) = 6 \times 10^{-8} \cdot (V_B)^{2.2735} \quad (\text{Eq.5.9})$$

With different companies' semiconductor technology, the on-resistance technology function  $\alpha(\xi, V_B)$  varies. Therefore, the device  $R_{DS\_ON}$  could be represented by (Eq.5.10).

$$R_{DS\_ON} = \alpha(\xi, V_B) / A_{die} \quad (\text{Eq.5.10})$$

In this way, the total device conduction loss  $P_{cond}$  and the device die area usage  $A_{die}$  can be correlated by using (Eq.5.11).

$$P_{cond} = (I_{RMS\_S})^2 \cdot R_{DS\_ON} = (I_{RMS\_S})^2 \cdot \frac{\alpha(\xi, V_B)}{A_{die}} \quad (\text{Eq.5.11})$$

where,  $I_{RMS\_S}$  is the switch RMS current. When  $N$  devices are used, the total conduction loss function versus total semiconductor die area usage could be described in (Eq.5.12).

$$P_{cond}(A_{die\_t}) = \sum_{i=1}^N \left( (I_{RMS\_S(i)})^2 \cdot \frac{\alpha_i(\xi_i, V_{B(i)})}{\kappa_i A_{die\_t}} \right) \quad (\text{Eq.5.12})$$

where,  $\kappa_i$  is the die cutting factor ranging from 0 to 1, reflecting different die cutting strategies. The sum of each  $\kappa_i$  equals to 1. For the one-cell STC with four identical switches,  $\kappa_1 = \kappa_2 = \kappa_3 = \kappa_4 = 0.25$ .  $A_{die\_t}$  is total die area of the converter devices. It can be used to compare the total conduction loss versus total die area usage. Since the blocking voltage information is included in this function, it can be also applied to evaluate the topologies with different device voltage stresses. This conduction loss function is normalized in (Eq.5.13).

$$P^*_{cond}(A_{die\_t}) = \frac{1}{P_o} \sum_{i=1}^N \left( (I_{RMS\_S(i)})^2 \cdot \frac{\alpha_i(\xi_i, V_{B(i)})}{\kappa_i A_{die\_t}} \right) \quad (\text{Eq.5.13})$$

Similarly, the normalized gate drive power loss, switching loss can be derived. When the die area is enlarged, the input capacitance increases [400]. Larger gate current is needed to charge the input capacitor. So, the total gate charge induced switching loss increases. The gate drive loss is in (Eq.5.14) [401].

$$P_{Gate} = Q_g \cdot \Delta V_{gs} \cdot f_{sw} \ ; \ \beta = Q_g / A_{die} \quad (\text{Eq.5.14})$$

where,  $Q_g$  is the total gate charge.  $\Delta V_{GS}$  is the difference of the recommended maximum and minimum  $V_{GS}$  ratings.  $f_{sw}$  is switching frequency.  $\beta$  is the device total gate charge per unit die area. The total normalized gate drive loss is in (Eq.5.15).

$$P^*_{Gate}(A_{die\_t}) = \frac{1}{P_o} \sum_{i=1}^N \left( \beta_i \cdot \kappa_i \cdot A_{die\_t} \cdot \Delta V_{gs(i)} \cdot f_{sw(i)} \right) \quad (\text{Eq.5.15})$$

Generalized turn-on and turn-off switching losses are derived in a similar manner in (Eq.5.16), (Eq.5.17), respectively.

$$P_{on} = E_{on} \cdot f_{sw} \ ; \ \delta = E_{on} / A_{die} \quad (\text{Eq.5.16})$$

$$P_{off} = E_{off} \cdot f_{sw} \ ; \ \sigma = E_{off} / A_{die} \quad (\text{Eq.5.17})$$

where,  $P_{on}$ ,  $P_{off}$  are turn-on and turn-off power losses.  $E_{on}$   $E_{off}$  are turn-on and turn-off energy.  $\delta$  and  $\sigma$  are turn-on and turn-off energy per unit die area. The normalized turn-on and turn-off switching losses are in (Eq.5.18) and (Eq.5.19), respectively.

$$P^*_{on}(A_{die\_t}) = \frac{1}{P_o} \sum_{i=1}^N \left( \delta_i \cdot \kappa_i \cdot A_{die\_t} \cdot f_{sw(i)} \right) \quad (\text{Eq.5.18})$$

$$P^*_{off}(A_{die\_t}) = \frac{1}{P_o} \sum_{i=1}^N \left( \sigma_i \cdot \kappa_i \cdot A_{die\_t} \cdot f_{sw(i)} \right) \quad (\text{Eq.5.19})$$

In the ZCS case, the output capacitance  $C_{oss}$  discharge induced turn-on switching loss is considered. The gate-drain capacitance  $C_{GD}$  and drain-source capacitance  $C_{DS}$  increase with the die area [402][403]. Thus,  $C_{oss}$  (i.e.  $C_{GD} + C_{DS}$ ) loss is positively dependent on die area. This turn-on switching loss is in (Eq.5.20) [404]. The corresponding normalized equation is in (Eq.5.21).

$$P_{C_{oss}} = C_{oss} \cdot V_{ds}^2 \cdot f_{sw} \ ; \ \gamma = C_{oss} / A_{die} \quad (\text{Eq.5.20})$$

$$P_{C_{oss}}^* (A_{die\_t}) = \frac{1}{P_o} \sum_{i=1}^N \left( \gamma_i \cdot \kappa_i \cdot A_{die\_t} \cdot V_{ds(i)}^2 \cdot f_{sw(i)} \right) \quad (\text{Eq.5.21})$$

where,  $V_{DS}$  is drain-source voltage.  $\gamma_i$  is the device output capacitance per unit die area, which is dependent on the device semiconductor manufacturing technologies.

The semiconductor device is the major cost contributor of a power converter. Since the semiconductor cost is proportional to total semiconductor die area usage, it is useful to identify the topology that can achieve the minimal power loss with the minimal semiconductor die usage. On the one hand, with the increase of the total device die area, the total device conduction loss reduces. On the other hand, the increased die area leads to larger parasitic capacitance, which causes higher switching loss and gate drive loss. So, the optimized total device die area exists to minimize total converter semiconductor power loss.

Therefore, in this chapter, a novel evaluation index called the total semiconductor loss index (TSLI) will be demonstrated. It is the normalized total semiconductor power loss as a function of total semiconductor die area. With this index, the total device power loss can be evaluated in terms of total die area usage among different topologies and device technologies. TSLI can be derived by summarizing the previous presented normalized power losses in (Eq.5.22).

$$TSLI(A_{die\_t}) = P_{cond}^* (A_{die\_t}) + P_{Gate}^* (A_{die\_t}) + P_{sw}^* (A_{die\_t}) \quad (\text{Eq.5.22})$$

When hard-switching is applied,  $P_{sw}^*$  is the sum of  $P_{on}^*$  and  $P_{off}^*$ . When ZCS is utilized,  $P_{sw}^*$  is equal to  $P_{Coss}^*$ . For a specific topology, when the output power and switching frequency are fixed, theoretically an optimal die area for each switch can be derived to achieve the minimized total device power loss. In other words, when the total device power loss is the same, the one with smaller total die area can achieve lower device manufacturing costs. These two evaluation perspectives based on the above TSLI parameter provide comprehensive understandings to compare different topologies and devices.

### **5.3. Summary for This Chapter**

This chapter serves as a theoretical preparation for the following three ones. It has proposed a generalized STC topology, which can be flexibly designed as DC-to-DC and DC-to-AC topologies, so that they can adapt to multiple different applications. This topology is especially suitable for the emerging WBG devices. With small intrinsic capacitances, higher switching frequency, the WBG devices can fully demonstrate the advantages with proposed topology.

Besides, a novel topology evaluation index has been proposed in this chapter. It provides a new insight into the device power loss by including the chip die area into the consideration. As a result, the device technology is no longer departed from the topological loss analysis. With a specific chip die design for a specific topology, the device power loss can be optimized. This index will be utilized and analyzed in more detail in the following chapters. It will be verified to provide valuable evaluation information for different topologies.

## 6. SIC MOSFET DC-TO-DC CONVERTER WITH 100-KW POWER RATING

High power DC-to-DC converters have been widely applied in multiple transportation electrification areas such as aeronautical power distribution systems [405]–[407], electric ship power networks [408][409], and electric vehicles [410]. In aerospace secondary power distribution networks, the DC-to-DC converters are needed to interface the battery and the DC bus [411]. It provides the desired voltage for different load requirements [405][411]. For the marine vessels, the DC-to-DC converters also play an essential part in the integrated power systems in the propulsion units [412]–[415]. The shipboard DC power systems promote more energy saving compared with the conventional AC systems by adjusting the motors to work at an optimal speed [412]. In hybrid electric vehicle power trains, a bidirectional DC-to-DC converter is normally used to boost the battery voltage to a higher DC bus voltage to drive the high voltage electric motors or generators using a 3-phase voltage source inverter [416]–[418]. Typical voltage requirements of such a DC-to-DC converter are 300 V on the battery side and 650 V on DC bus side [419]. It aims to regulate the bus voltage, protect the battery from over/under voltage, excessive charge/discharge currents [419]–[421]. In a recent report of U.S. Department of Energy [410], by 2025, the electric traction drive system cost is expected to be lower than \$2.7/kW, and the power density is supposed to exceed 100 kW/L based on the 100 kW power level. To achieve this goal, a proper topology with optimized device and passive component design should be deliberated and verified.

Conventional bidirectional boost/buck converter is a basic solution for such applications. A 40 kW bidirectional DC-to-DC converter based on boost topology is designed in [422] with 6 kW/L power density working at 20 kHz switching frequency. However, conventional boost converter suffers from low efficiency and bulky reactive components. To reduce the input and output capacitor size, a 3-phase interleaved boost converter with discrete inductors is assembled

to achieve a power density of 30.8 kW/L and 97.9% peak efficiency [423]. But the total inductor core volume is about 1.3 Liters, which is very bulky. To overcome this issue, constant frequency quasi square wave zero voltage switching (ZVS) 3-phase interleaved boost converter is studied in [424]. But it is inefficient at light load. Variable-frequency boundary mode quasi square wave ZVS control is applied in a 200 kW Si IGBT based prototype [419] to further increase the peak efficiency to 98%, but the power density is only 6 kW/L. Besides, ZVS is realized to improve the efficiency based on a 150 kW, 8.6 L interleaved boost DC-to-DC converter with multiple split DC sources, but the power density is 17.44 kW/L [425]. Another widely investigated topology for this application is flying capacitor multilevel converter (FCMC) [426]–[429]. To increase the voltage conversion flexibility, an inductor is placed on the DC input side [416][430]. Over 97% efficiency at 30 kW continuous operation is claimed in [416] by using FCMC with a power density around 8.612 kW/L. However, it is difficult to realize a compact mechanical layout design considering the separate locations of the DC-side resonant inductor and AC-side resonant capacitor. SiC MOSFET power modules have shown better efficiency and higher temperature capability compared with the Si counterparts [431]–[434]. 1200 V 100 A SiC MOSFET power modules have been applied in a boost based 60 kW DC-to-DC converter, which can achieve 20 kW/L power density [435]. However, hard-switching operation at 75 kHz switching frequency does not fully utilize their advantages, which degrades the overall 98.7% peak efficiency. Recently, resonant multilevel DC-to-DC converters, resonant switched capacitor converters, and switched tank converters are investigated for their modularity, high power density and high efficiency [429][383], [393], [436]–[439]. But the high power applications of these topologies have not been well explored.

This chapter will utilize the STC circuit structure introduced in last chapter for the 100 kW transportation electrification applications. In different electric vehicle applications, various voltage

transfer ratios may be desired, which means different number of cells should be used for the proposed STC topology. For the specific application in this project, i.e. 300 V – 600 V conversion, only one cell of the generalized STC structure is needed. Moreover, if the voltage regulation is expected in some applications, the ZVS control could be used to realize this function [437][440]. Another derivative STC topology could also regulate voltage with minimum efforts. This STC is integrated with a partial-power processed voltage regulator [439]. It could achieve high voltage conversion ratio using multiple STC cells and achieve full voltage regulation without ZVS. This chapter will focus on the one-cell STC for the 300 V – 600 V 100 kW vehicle application.

Compared with the state-of-art high-power DC-to-DC converter research, this chapter endeavors to apply the new topology derived from resonant switched capacitor concept and utilize the new evaluation index to compare potential topology candidates in terms of the device power loss and chip die area. High-power design challenges of both the active switches and passive components are analyzed. The corresponding solutions are provided in detail. A 100 kW hardware prototype using the proposed topology achieving 98.7% efficiency and 42 kW/L power density has been developed and tested. The circuit operation, component design procedure as well as hardware prototype experimental results will be presented in this chapter.

### **6.1. Topology Comparison**

Through investigating SiC MOSFETs with three different voltage ratings from two device companies, the proposed TSLI of the boost converter and the one-cell STC is compared [441].

For boost converter, 1200 V SiC devices are applied, since the device voltage stress is 600 V. Two SiC dies with 1200 V voltage ratings, i.e. Rohm S4103 [442] and Cree CPM2-1200-0025B [443] are selected. The device turn-on and turn-off losses are considered at continuous conduction mode assuming the inductor current ripple is 30% of its average current [444].

For the boost converter with two identical switches, the die cutting factors  $\kappa_1 = \kappa_2 = 0.5$ . According to the last chapter, the normalized conduction loss of the boost converter is presented in (Eq.6.1).

$$P^*_{cond(B)}(A_{die\_t}) = \frac{2}{P_o} \left( I_{RMS\_S(B)} \right)^2 \cdot \frac{R_{ds(on)} \cdot A_{die}}{0.5 \cdot A_{die\_t}} \quad (\text{Eq.6.1})$$

where, the subscript  $B$  represents boost converter.  $I_{RMS\_S(B)}$  is device RMS current, which is 236.58 A in this application.

The normalized gate drive loss function of the boost converter can be described in (Eq.6.2).

$$P^*_{Gate(B)}(A_{die\_t}) = \frac{2}{P_o} \left( \frac{Q_g}{A_{die}} \cdot 0.5 \cdot A_{die\_t} \cdot \Delta V_{gs} \cdot f_{sw} \right) \quad (\text{Eq.6.2})$$

For Rohm's S4103 and Cree's CPM2-1200-0025B,  $\Delta V_{GS}$  is 18 V and 25 V, respectively.  $f_{sw}$  is 100 kHz. The normalized turn-on, turn-off loss functions for boost converter are in (Eq.6.3), (Eq.6.4), respectively.

$$P^*_{on(B)}(A_{die\_t}) = \frac{2}{P_o} \left( \frac{E_{on}}{A_{die}} \cdot 0.5 \cdot A_{die\_t} \cdot f_{sw} \right) \quad (\text{Eq.6.3})$$

$$P^*_{off(B)}(A_{die\_t}) = \frac{2}{P_o} \left( \frac{E_{off}}{A_{die}} \cdot 0.5 \cdot A_{die\_t} \cdot f_{sw} \right) \quad (\text{Eq.6.4})$$

The switching energy versus drain current curves of the two selected SiC bare dies can be found in the datasheets of Rohm 1200 V SCT3022KL and Cree 1200 V C2M0025120D SiC MOSFETs due to the matched on-resistance and current rating between the bare die and the corresponding device.

TSLI of the boost converter is the sum of the above four individual semiconductor loss indexes, as shown in (Eq.6.5).

$$TSLI_B(A_{die\_t}) = P_{cond(B)}^* + P_{Gate(B)}^* + P_{on(B)}^* + P_{off(B)}^* \quad (\text{Eq.6.5})$$

One-cell STC is designed to operate at ZCS mode in this project.  $C_{oss}$  discharge induced turn-on loss is included in the switching loss. In 300 V – 600 V application, 650 V, 900 V and 1200 V devices can be used. For the four identical switches, the die cutting factors  $\kappa_1 = \kappa_2 = \kappa_3 = \kappa_4 = 0.25$ . Similarly, the normalized conduction loss function, gate drive loss function and  $C_{oss}$  loss function of the one-cell STC are in (Eq.6.6), (Eq.6.7), and (Eq.6.8), respectively.

$$P_{cond(STC)}^*(A_{die\_t}) = \frac{4}{P_o} \left( I_{RMS\_S(STC)} \right)^2 \cdot \frac{R_{ds(on)} \cdot A_{die}}{0.25 \cdot A_{die\_t}} \quad (\text{Eq.6.6})$$

$$P_{Gate(STC)}^*(A_{die\_t}) = \frac{4}{P_o} \left( \frac{Q_g}{A_{die}} \cdot 0.25 \cdot A_{die\_t} \cdot \Delta V_{gs} \cdot f_{sw} \right) \quad (\text{Eq.6.7})$$

$$P_{C_{oss}}^*(A_{die\_t}) = \frac{4}{P_o} \left( \frac{C_{oss}}{A_{die}} \cdot 0.25 \cdot A_{die\_t} \cdot V_{ds}^2 \cdot f_{sw} \right) \quad (\text{Eq.6.8})$$

where,  $I_{RMS\_S(STC)}$  is the device RMS value of the one-cell STC, which is 261.8 A at full load. For Rohm's 650 V S4003 and Cree's 900 V CPM3-0900-0010A,  $\Delta V_{GS}$  is 18 V and 19 V, respectively.  $C_{oss}$  is 148 pF and 350 pF for Rohm's S4003 and Cree's CPM3-0900-0010A, respectively.  $V_{DS}$  is the device voltage stress, which is 300 V in this application.

The TSLI for the proposed one-cell STC is presented in (Eq.6.9).

$$TSLI_{STC}(A_{die\_t}) = P_{cond(STC)}^* + P_{Gate(STC)}^* + P_{C_{oss}(STC)}^* \quad (\text{Eq.6.9})$$

The TSLIs of the boost converter and one-cell STC for the selected SiC bare dies with different voltage rating are plotted in Figure 6.1 for a comprehensive comparison. Although various devices could reach the same level of power loss with different total semiconductor die areas, one-cell STC with 900 V Cree SiC bare die utilizes the minimal die area, which indicates lower die manufacturing costs. Compared with boost converter, one-cell STC can achieve lower

total semiconductor loss with the same die area usage. In other words, at the same total device loss, one-cell STC consumes smaller total die area.

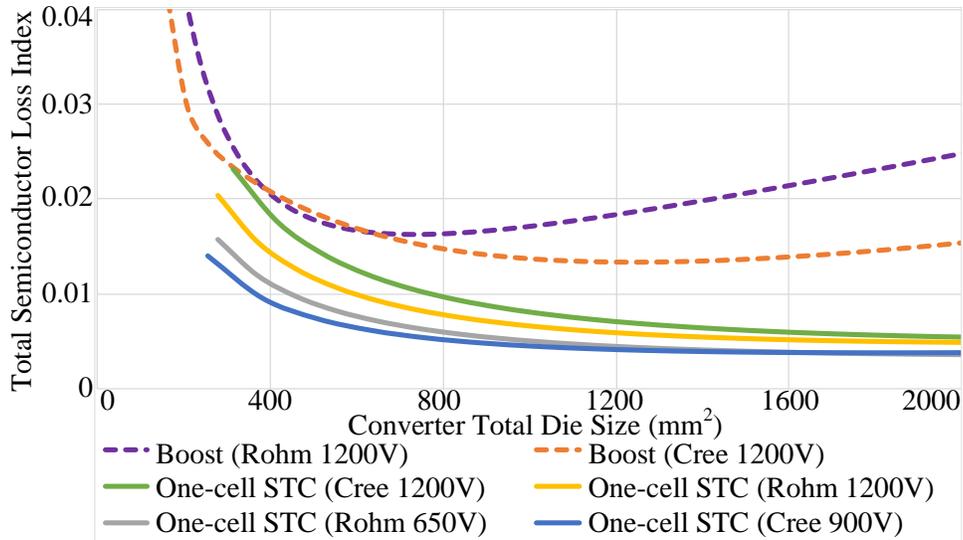


Figure 6.1. Total semiconductor loss index comparison

To illustrate the proposed evaluation index in more detail, a breakdown analysis is further conducted for each individual power loss index in both the boost converter and one-cell STC to compare the impact of individual power loss on the TSLI. An evaluation of TSLI for different output power and switching frequency is conducted as well. With the same input voltage and output power, the TSLI changing trend with the number of the STC cells is also mathematically analyzed. The demonstration is presented in the following.

### 6.1.1. Semiconductor Loss Index Breakdown Analysis

As can be seen from Figure 6.1, the lowest total device power loss can be realized by the Cree 1200 V SiC die (part number: CPM2-1200-0025B) for boost converter, and the Cree 900 V SiC die (part number: CPM3-0900-0010A) for the one-cell STC. Therefore, these two dies have been identified to be used for the following individual power loss index breakdown analysis.

For boost converter, by using Cree 1200 V SiC die, curve fitted  $E_{on}$  vs.  $I_d$  and  $E_{off}$  vs.  $I_d$  are based on the datasheet of 1200 V 90 A C2M0025120D SiC MOSFET with TO-247-3 package, because this product has pretty close current rating with the studied Cree 1200 V die with 98 A current rating. Take  $E_{on}$  for example, curve fitted  $E_{on}$  vs.  $I_d$  can be expressed in (Eq.6.10).

$$E_{on} = p_1 \cdot (I_d)^4 + p_2 \cdot (I_d)^3 + p_3 \cdot (I_d)^2 + p_4 \cdot (I_d) + p_5 \quad (\text{Eq.6.10})$$

where,  $E_{on}$  has the unit of mJ.  $I_d$  has the unit of A.  $p_1 \sim p_5$  are  $-1 \times 10^{-8}$ ,  $2 \times 10^{-6}$ ,  $2 \times 10^{-4}$ , 0.0071, and 0.0361, respectively.

The die area is symbolized as  $A_{die}$ , which is 26.0176 mm<sup>2</sup> for one Cree 1200 V SiC die.  $N_{die}$  signifies the number of the dies in parallel. Thus, the total die area can be presented as  $A_{die\_t} = N_{die} \cdot A_{die}$ . The full-load turn-on current of the load-side switch and voltage source side switch, i.e.  $I_{d1}$  and  $I_{d2}$ , are 383.33 A and 283.33 A, respectively, based on the MATHCAD calculation. With  $N_{die}$  in parallel, the turn-on current flowing through each die is  $I_{d1}/N_{die}$  and  $I_{d2}/N_{die}$ , respectively. Based on the above, the normalized turn-on power loss is shown in (Eq.6.11).

$$P_{on(B)}^*(A_{die\_t}) = \frac{(E_{on(Q_{B1})} + E_{on(Q_{B2})}) \cdot f_{sw} \cdot N_{die}}{P_o} \quad (\text{Eq.6.11})$$

where,  $E_{on(Q_{B1})}$  and  $E_{on(Q_{B2})}$  are the turn-on energy of the two switches in boost converter based on (Eq.6.10) with the drain current replaced by  $I_{d1}/N_{die}$  and  $I_{d2}/N_{die}$ , respectively.

Therefore,  $P_{on}^*$  can be plotted as the function of the total die area usage for the two switches in the boost converter. Similarly,  $E_{off}$  vs.  $I_d$  can be curve fitted and  $P_{off}^*$  is further plotted. The other two power loss indexes, i.e. conduction loss index and gate drive loss index are derived based on (Eq.5.13) and (Eq.5.15).

For one-cell STC, the three power loss indexes, i.e. conduction loss index, gate drive loss index and  $C_{oss}$  loss index are calculated based on (Eq.5.13), (Eq.5.15), and (Eq.5.21), respectively.

Figure 6.2 (a) and (b) present the individual loss index vs. total die area for boost converter and one-cell STC, respectively.

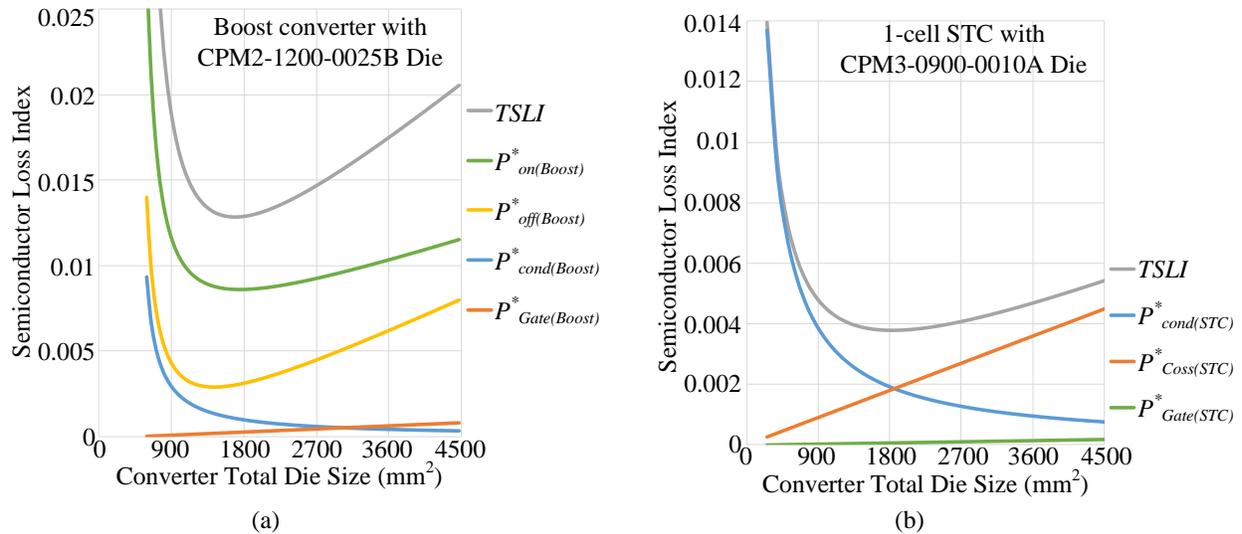


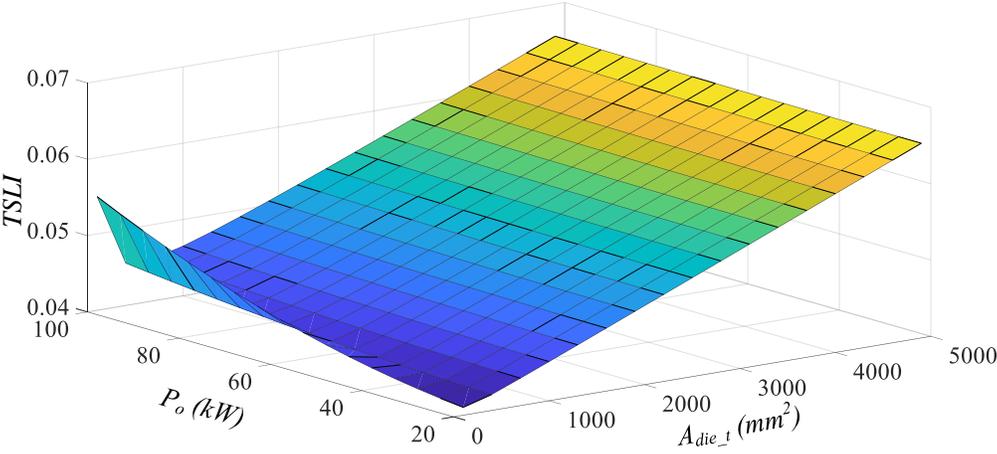
Figure 6.2. Semiconductor loss index breakdown of (a) Boost converter, and (b) One-cell STC.

For the boost converter, the turn-on and turn-off power loss indexes are not a linear function of the total die area, which means that there is a specific die area that could achieve the minimum switching power loss for the boost converter. For both the two topologies, the conduction loss index decreases with the total die area, because with more dies in parallel, the current flowing through each die drops by  $1/N_{die}$ . Both the two gate drive loss indexes increase with the total die area, because there is larger total gate charge with more dies. For the one-cell STC, the  $C_{oss}$  loss index increases with the total die area, because the total  $C_{oss}$  turn-on discharge induced switching loss increases with more dies in parallel.

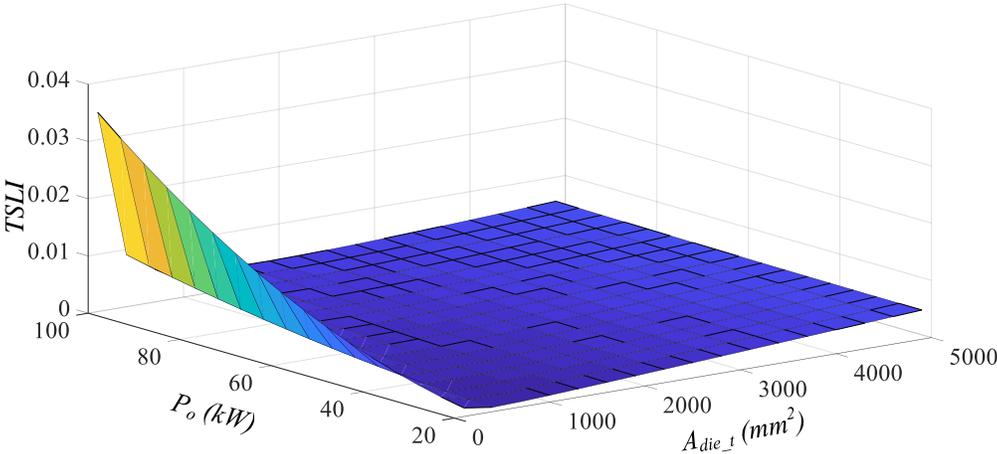
### 6.1.2. TSLI as a Reflection of Different Output Power

Besides, TSLI could also be regarded as the function of the total die area and the output power. Figure 6.3 (a) and (b) show the TSLI versus die area usage and output power for boost converter and one-cell STC, respectively at 100 kHz switching frequency. In this comparison, for

boost converter, assume the inductance is  $15 \mu\text{H}$  to make sure that the inductor current ripple is 30% the average current at 100 kW operation [444].



(a)



(b)

Figure 6.3. TSLI vs. total die area and output power for (a) boost converter and (b) one-cell STC

At a specific total die area, with higher output power rating, the TSLIs of both the boost converter and the one-cell STC experience an increasing trend because the conduction loss increases with output power, but the switching loss is not affected by output power. This increasing extent of TSLI with output power is more obvious when the total die area is small, because the conduction loss takes a larger proportion than total switching loss at the small total die area.

At a specific output power, when more dies are in parallel and the total die area becomes larger, the total conduction losses for both the two converters decrease, but the total switching losses increase. As a result, gradually the increased switching losses offset the decreased conduction losses. Therefore, at each specific output power, there exists a valley bottom point for the TSLI when the total die area changes. It means that an optimized total die area can be achieved to realize minimum total device power loss for this specific output power.

### **6.1.3. TSLI as a Reflection of Switching Frequency**

TSLI can also be illustrated as the function of total die area usage and the switching frequency. Figure 6.4 (a) and (b) show the TSLI vs. die area usage and switching frequency for boost converter and one-cell STC, respectively when the output power is fixed at 100 kW.

At a specific total die area, the TSLIs of both the two converters increase with the switching frequency, because the total switching losses rise due to higher switching frequency, but the conduction losses are not affected. This increasing extent of TSLI with switching frequency is more obvious in the boost converter because the switching loss is higher compared with that in the one-cell STC at ZCS operation. At a specific switching frequency, there also exists a valley bottom for the TSLIs in both the two topologies.

### **6.1.4. TSLI as a Reflection of Different Number of Cells for N-cell STC**

Figure 6.5 shows that the TSLI can also be used to reflect the relationship with total die area usage and the number of cells for the generalized  $N$ -cell STC. This comparison is based on the same output power (100 kW), input voltage (300 V) and switching frequency (100 kHz), utilizing the Cree 900 V SiC die (part number: CPM3-0900-0010A) information.

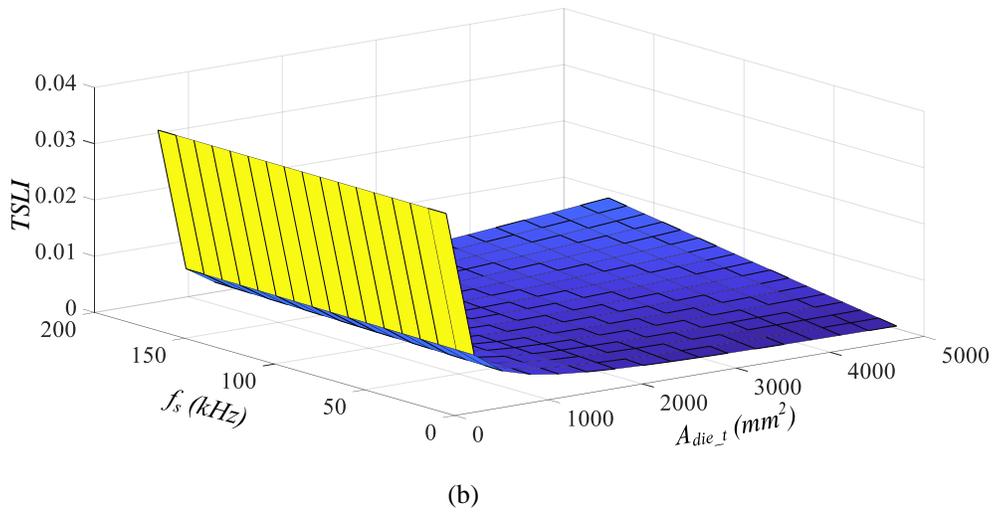
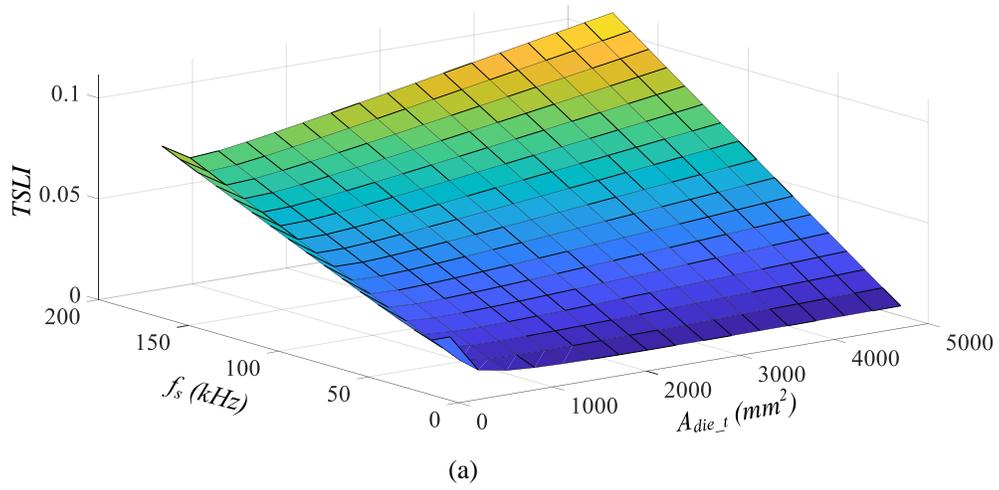


Figure 6.4. TSLI vs. total die area, switching frequency for (a) boost converter, (b) one-cell STC

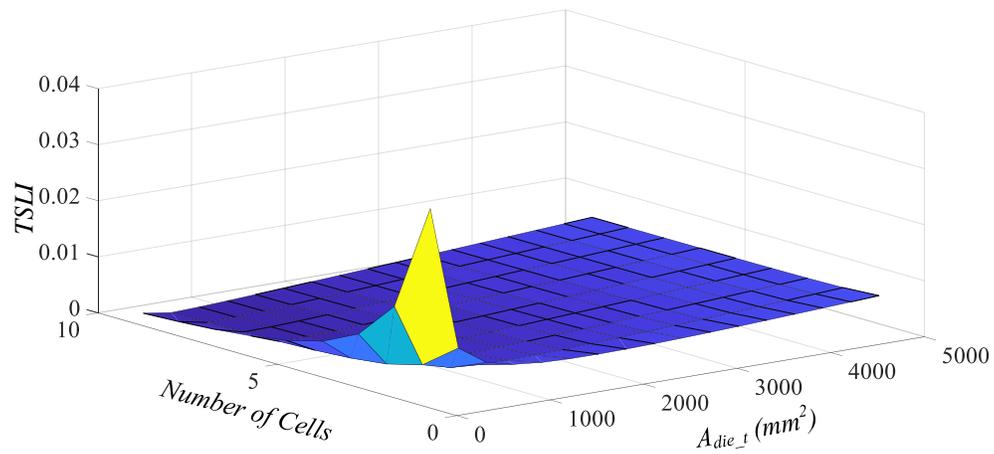


Figure 6.5. TSLI as a function of total die area and number of cells for  $N$ -cell STC

The device RMS current in the  $N$ -cell STC can be presented in (Eq.6.12). At a specific total die area, since the device RMS current decreases with the number of STC cells, the total conduction losses drop with the cell number, as shown in Figure 6.5.

$$I_{RMS\_S} = \sqrt{\frac{1}{T_s} \int_0^{T_s} (i_S(t))^2 dt} = \frac{\pi}{2} \cdot \frac{P_o}{V_{in} \cdot (N+1)} \quad (\text{Eq.6.12})$$

The decreasing extent of TSLI with the number of STC cells becomes less obvious at large total die area, because the conduction losses take a smaller proportion compared with switching losses as the total die area increases. With a given number of STC cells, there also exist a valley bottom as the total die area increases. It tells us that the total power device loss can be minimized at an optimized total die area when the number of STC cells is fixed.

## 6.2. Design of Devices and Passive Components

The detailed component design is presented in this section [445][446][447]. Part 6.2.1 talks about the design of SiC MOSFET power modules. Part 6.2.2 presents the heatsink design process. Part 6.2.3 discusses details regarding the resonant capacitor design. Detailed resonant capacitor design criteria is provided in Part 6.2.3. The high current, high frequency resonant inductor design is also a major challenge to achieve the minimal size and power loss. The optimal considerations of the resonant inductor winding and core designs are analyzed in Part 6.2.4. The DC capacitor design is discussed in detail in Part 6.2.5.

### 6.2.1. Design of Devices

The challenges for the device design in the high-power applications are mainly caused by the high conduction power loss and potentially high die temperature rise. To respond to these challenges, both the optimized device power loss and temperature rise are to be achieved in a wide load range.

Based on the TSLI evaluation in Figure 6.1, 900 V Cree and 650 V Rohm SiC MOSFET achieve lower semiconductor power loss. However, the SiC MOSFET products based on 900 V Cree die and 650 V Rohm die have limited current capability. As a result, multiple paralleled devices are needed, which increases the total device volume, induces current imbalance and leads to parasitic oscillation [448]. So, Rohm and Cree 1200 V SiC MOSFET power modules with higher current capabilities are evaluated. Figure 6.6 shows the total MOSFET power loss of five 1200 V SiC MOSFET power modules at different output power ratings. The switching frequency is 100 kHz, and the maximum output power is 100 kW. Input, output voltages are 300 V and 600 V, respectively. The Rohm 1200 V 600 A SiC module can achieve the lowest total MOSFET power loss at full load.

To optimize the thermal performance of the devices, a temperature rise comparison of different SiC power modules is further conducted. The temperature rise calculation is based on the thermal resistance circuit in Figure 6.7.

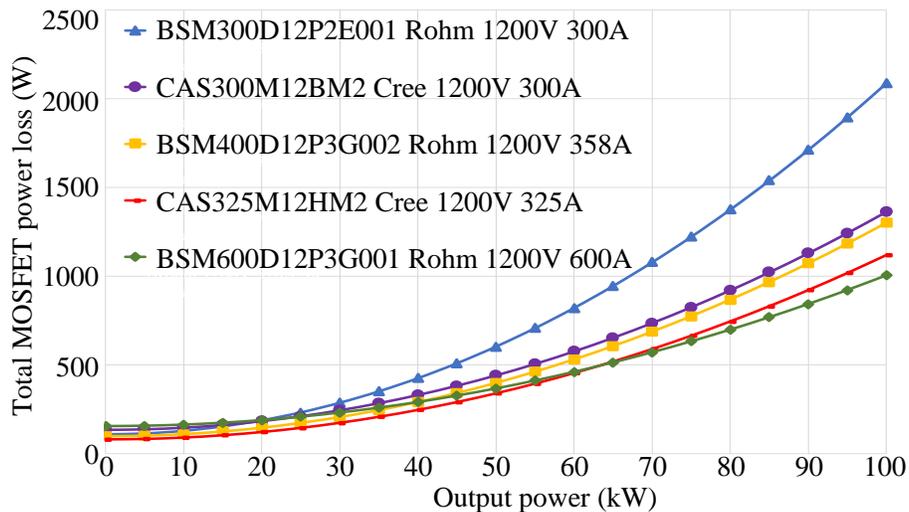


Figure 6.6. Total MOSFET power loss comparison among different MOSFETs

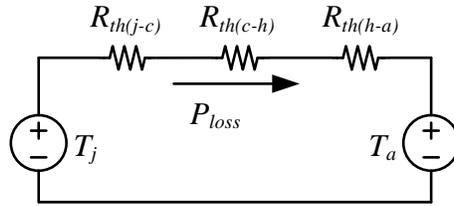


Figure 6.7. Thermal resistance circuit

The temperature rise vs. output power curves for these five SiC MOSFET modules are presented in Figure 6.8. With competitive thermal resistance, the Rohm 1200 V 600 A SiC module realizes lowest temperature rise in a wide output power range. Thus, the thermal performance is relatively optimized.

Although higher frequency helps decrease the magnetic component size, speed up the transient load response, it introduces more AC loss to the high frequency resonant capacitor and AC busbar, increases the core loss of the resonant inductor. Considering this trade-off, the switching frequency is designed at 100 kHz for this project.

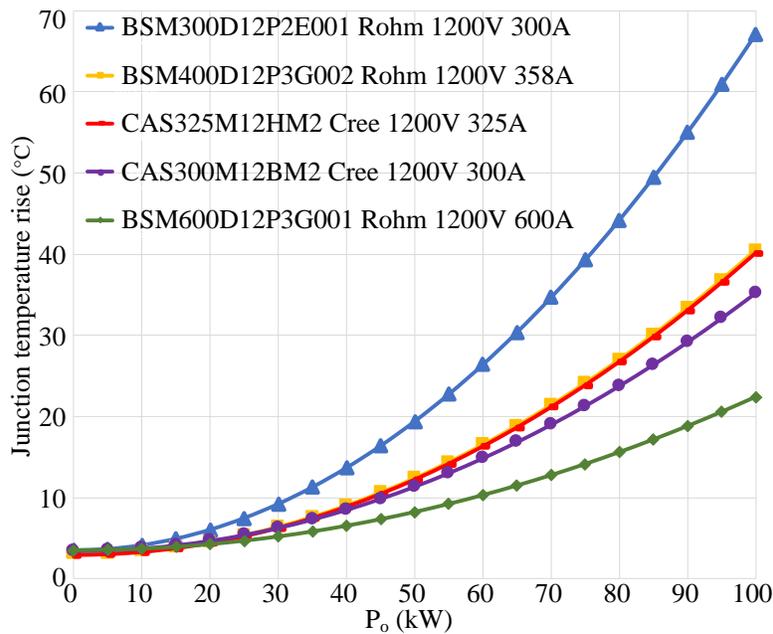


Figure 6.8. Thermal performance comparison among five 1200 V SiC modules

### 6.2.2. Design of Heatsink

Heatsink design is based on the thermal resistance circuit in Figure 6.7. The heatsink thermal resistance can be derived in (Eq.6.13) according to the thermal dissipation and device power loss.

$$R_{th(h-a)} = \frac{T_j - T_a}{P_{loss}} - R_{th(j-c)} - R_{th(c-h)} \quad (\text{Eq.6.13})$$

where,  $R_{th(h-a)}$ ,  $R_{th(j-c)}$  and  $R_{th(c-h)}$  are thermal resistance between heatsink and ambient, junction and case, case and heatsink, respectively.  $R_{th(j-c)}$  and  $R_{th(c-h)}$  are equal to 0.061 °C/W and 0.015 °C/W, respectively [449].  $T_j$  and  $T_a$  are junction and ambient temperature.  $P_{loss}$  is the total power loss of the devices.

The maximum junction temperature for the selected SiC module is 175 °C [449]. The total device power loss at 100 kW is 1004.37 W based on previous calculation. To reflect the real cooling system in hybrid electric vehicles, the ambient temperature  $T_a$  is designed as the water tank outlet temperature 85 °C [450]. Therefore, designed heatsink-ambient thermal resistance should satisfy:  $R_{th(h-a)} \leq 0.0136$  °C/W. An off-the-shelf water cooling heatsink from wakefiled-vette® is selected. With 5.3 L/minute water flowing speed, the thermal resistance is around 0.013 °C/W. With this heatsink, maximum junction temperature is 174.39 °C at 85 °C water cooling temperature.

### 6.2.3. Design of Resonant Capacitor

The major challenges in this high-power resonant capacitor design are high frequency and high RMS current. High frequency helps shrink the passive component size, but brings in non-negligible voltage rating drops in the polypropylene film capacitors. High RMS current levels up the current capability threshold, which narrows the available candidate range. Another challenge is regarding the compact size while satisfying the current capability. When we try to solve these

challenges, the resonant capacitor design is comprehensively conducted based on operating frequency range, resonant capacitance, required resonant inductance, volume, maximum allowed RMS voltage and current capability, as shown below.

To achieve the high-frequency and high RMS current resonant operation, both ceramic and film capacitors could be used. The Class II multi-layer ceramic capacitors (MLCC) have higher power density compared to the film capacitors assuming the same capacitance and current rating. However, considering that the ceramics are weak in tension, a crack can be relatively easily generated when excessive board flex is put on the soldered MLCC [451]. As a result, an electrical conduction between the two electrodes would happen, which could progress to a short circuit. Therefore, MLCCs are not preferred for the automotive, aerospace, and marine power electronic applications due to these reliability concerns. Thus, the polypropylene film capacitors with the excellent current capability are considered for the desired resonant tank design.

Based on a summarization of high power resonant capacitors from different companies [452], the polypropylene film capacitors from Illinois Capacitor<sup>®</sup> provides specifically designed high-current, high-frequency resonant capacitors. Thus, all the conduction cooled high-density resonant capacitors from this company are studied, including LC1 ~ LC6, HC1 ~ HC6 and HC3A, HC3B series. In each category, one type with highest capacitance density, satisfying frequency range, full-load peak voltage and current requirements is selected. Figure 6.9 shows the comparison of the capacitance density per unit volume. From the results in Figure 6.9, LC2 and LC3 series can achieve much higher capacitance density.

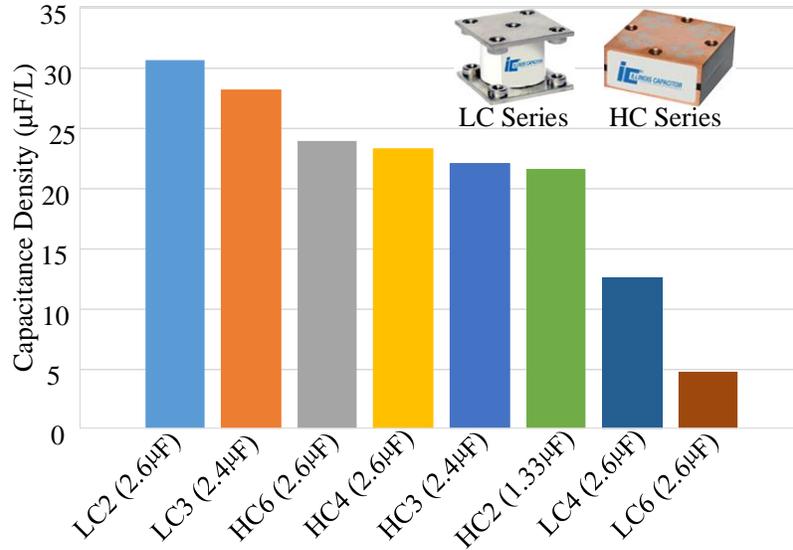


Figure 6.9. Capacitance density per unit volume comparison

Not only should the volume of the resonant capacitors be considered, but also does the whole resonant tank size need to be analyzed. Thus, the smaller inductance is preferred in our design. Figure 6.10 (a) shows the relationship between the required inductance and total resonant capacitance. Considering the practical size as well as the design of core and winding, the maximum inductance has been designed as 500 nH. Correspondingly, the minimum resonant capacitance is 5.066 µF. Besides, considering the power module and heatsink layout, the total capacitor volume is designed below 0.3 L. Figure 6.10 (b) shows the trade-off between the total capacitance and the volume. The remaining candidates in the shaded area are further compared in Table 6.1, from which three 2.4 µF LC2 and three 2.6 µF LC3 are preferable due to smaller required inductance.

However, the polypropylene film capacitor voltage rating drops at higher switching frequency, because of the heat generated by the AC loss at high frequency [453]. Thus, a safe margin needs to be maintained between the full-load peak voltage and the maximum voltage capability after derating at 100 kHz resonant frequency. In Figure 6.11, the voltage derating with the resonant frequency of selected film capacitors are shown. The margin between the full-load

voltage peak and the maximum voltage capability for the LC2 series is about 41 V, while for LC3 series it is around 100 V, which makes LC3 series more suitable for our application.

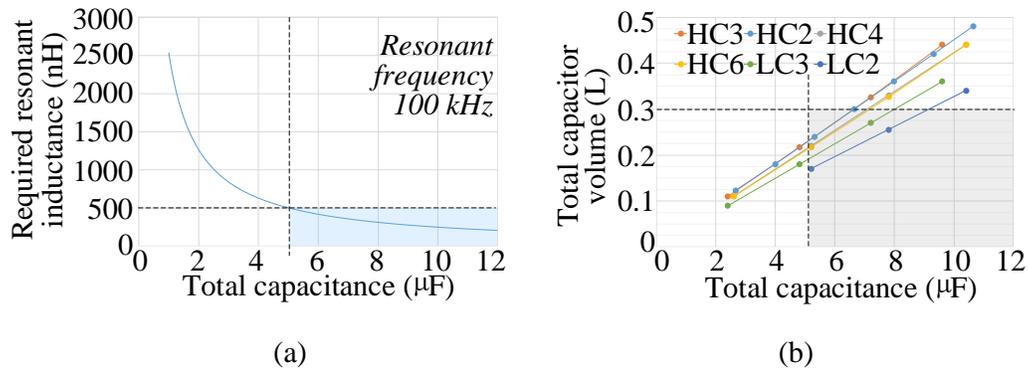


Figure 6.10. Capacitor evaluation based on required inductance and total volume

Table 6.1. Comparison Among Prospective Capacitors

Series	Total capacitance (µF)	Total volume (Liter)	RMS voltage (V)	RMS voltage capability at 100kHz (V)	Required inductance at 100kHz (nH)
HC2	5.32	0.24	319.79	500	476.13
HC4	5.2	0.22	320.69	500	487.12
HC6	5.2	0.22	320.69	600	487.12
LC3	7.2	0.27	310.96	410	351.81
LC2	5.2	0.17	320.69	350	487.12
LC2	7.8	0.26	309.36	350	324.75

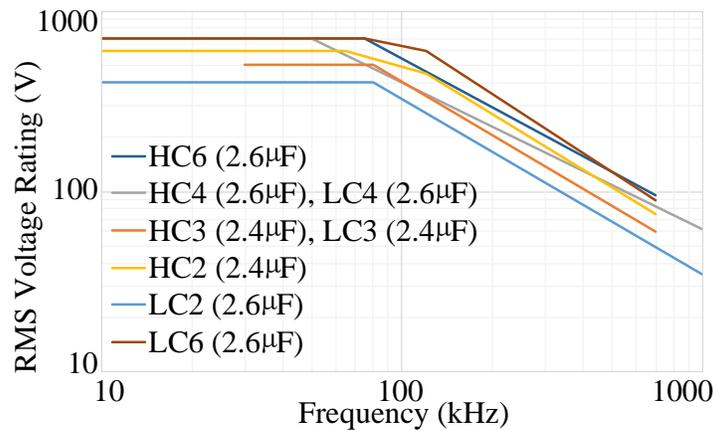


Figure 6.11. Voltage derating curves for HC and LC series capacitors

Finally, to evaluate the thermal performance of the selected resonant capacitors, the thermal impedance and temperature rise are calculated in (Eq.6.14), (Eq.6.15), respectively.

$$R_{TH(Cr)} = \Delta T_{Cr(max)} / \left[ \left( I_{Cr(RMS\_max)} \right)^2 \cdot ESR \right] \quad (\text{Eq.6.14})$$

$$\Delta T_{Cr} = R_{TH(Cr)} \cdot \left( I_{Lr(RMS)} / 3 \right)^2 \cdot ESR \quad (\text{Eq.6.15})$$

Based on (Eq.6.14), the thermal resistance is calculated as  $(40 \text{ }^\circ\text{C}) / [(650 \text{ A})^2 \times 0.2 \text{ m}\Omega] = 0.47 \text{ }^\circ\text{C/W}$ . From calculation results,  $7.8 \text{ }\mu\text{F}$  LC2 and  $7.2 \text{ }\mu\text{F}$  LC3 experience the temperature rise of  $3.01 \text{ }^\circ\text{C}$  and  $1.44 \text{ }^\circ\text{C}$ , respectively at full load and  $100 \text{ kHz}$  resonant frequency. By taking the above comparison and temperature verification into comprehensive consideration, three  $2.4 \text{ }\mu\text{F}$  LC3 capacitors have been finalized. Furthermore, in reference to the Table 6.1, the corresponding required inductance at  $100 \text{ kHz}$  resonant frequency is  $351.81 \text{ nH}$ .

#### 6.2.4. Design of Resonant Inductor

The challenges of the resonant inductor selection in this application are primarily due to high RMS current, high frequency core and winding design. High RMS, high frequency current is responsible for the remarkable AC winding loss due to the skin effect. A multi-layer AC busbar is designed to alleviate this issue. High power and high frequency also lead to significant core loss and corresponding temperature rise. Therefore, a careful core material evaluation and the trade-off between the core thermal performance and core volume are conducted to conquer this problem.

With the above  $7.2 \text{ }\mu\text{F}$  resonant capacitance design, to achieve a  $100 \text{ kHz}$  resonant frequency, the resonant inductance value is required to be  $351.81 \text{ nH}$ . The winding design and core design will be conducted in this section.

##### 6.2.4.1. Winding Design

Figure 6.12 (a) shows two resonant side layout possibilities. The left-hand side presents a layout with only one-turn winding. The inductor is split into two with similar inductance. The

right-hand side layout can achieve more flexible number of turns, but it brings challenge for the winding geometry design. The connecting copper joint between adjacent copper layers introduces more manufacturing difficulties. The copper bar linking with the power module overpasses resonant capacitors, which increases AC copper loss and prolong the prototype height. Thus, one-turn winding design is adopted. The AC inductor could be designed in the similar height with the AC capacitors, power module, heatsink, and the DC side. Therefore, the space can be fully utilized in a compact way.

In Figure 6.12 (b), the 3D model and the assembly of the AC busbar are illustrated in the top and bottom two pictures, respectively. The multi-layer copper foil AC busbar has been designed for this high-current high-frequency winding. By distributing the current through multiple layers, the wide-range temperature arrangement reduces AC loss caused by the AC current skin effect. The Kapton tape with capability is applied to insulate each layer. The skin depth  $\delta$  is calculated based on (Eq.6.16) [454][455].

$$\delta = \sqrt{\rho / (\pi f \mu_{copper})} \quad (\text{Eq.6.16})$$

where,  $f$  is the AC frequency of the current flowing through the copper busbars. The copper resistivity  $\rho$  and permeability  $\mu_{copper}$  are  $1.76 \times 10^{-8} \Omega \cdot \text{m}$ ,  $1.257 \times 10^{-6} \text{ H/m}$ , respectively.

At 100 kHz, the skin depth for copper is calculated as 0.211 mm. So, the copper foil with a thickness no larger than 0.211 mm has been selected. To further design the copper cross-section area and number of layers, the current density should be considered. For the one-turn winding design, current density is recommended as 300 mil<sup>2</sup>/A or 5.167 A/mm<sup>2</sup> to avoid excessive copper loss and temperature rise [456]. Considering that AC RMS current value is 370.24 A and the cross-section area of selected one-layer copper foil is 7.112 mm<sup>2</sup>, the total number of layers is  $(370.24 / 5.167) / (7.112) \approx 10$ . Thus, the 10-layer copper foil has been applied in this AC busbar. The total

cross-section area of AC busbar  $A_{AC\_Busbar}$  is  $71.12 \text{ mm}^2$ . More inductor winding optimization strategies will be addressed in future publications.

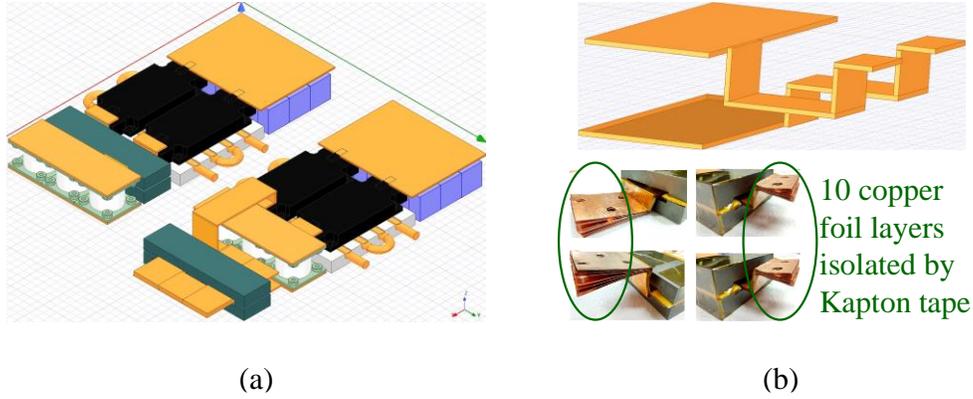


Figure 6.12. (a) One-turn and multiple-turn winding. (b) AC busbar 3D model and assembly

#### 6.2.4.2. Core Design

The core loss induced heat is a significant design constraint in the AC inductor design [457]. Thus, the core loss and temperature rise are compared in the core selection. The trade-off between the core temperature rise and volume is analyzed.

The powder cores and ferrite cores from major magnetic manufacturers are compared. The core loss density equation of Chang Sung Corporation<sup>®</sup> (CSC) cores and Hitachi<sup>®</sup> soft ferrite cores is shown in (Eq.6.17) [458][459].

$$P_{V(core)} = (K_h \cdot f + K_e \cdot f^\lambda) \cdot (B_{PK})^Y \quad (\text{Eq.6.17})$$

where,  $P_{V(core)}$  is the core loss density per volume with the unit of  $\text{kW/m}^3$ .  $f$  is the frequency (kHz) of the current flowing through the inductor.  $K_h$  is the hysteresis loss coefficient.  $K_e$  is the eddy current loss coefficient.  $B_{PK}$  is the peak flux density.  $Y$  is an exponent close to 2.

Core loss density of Hitachi HLM50 amorphous powder core, and the Magnetics<sup>®</sup> powder, ferrite cores is presented in (Eq.6.18) [460]–[462].

$$P_{V(core)} = a \cdot (B_{PK})^b \cdot (f)^c \quad (\text{Eq.6.18})$$

By applying the above two equations, the core loss density comparison is plotted in Figure 6.13 at 100 kHz frequency. Hitachi soft ferrite core ML29D is finalized due to its smaller core loss density in the 0.1 ~ 1 T flux density range.

E-shaped cores are selected in this project because it can achieve simpler assembly and more cost-effective solutions compared with pot cores [463]. Figure 6.14 shows a typical E-core dimension and the magnetic paths. In this design,  $\alpha_2$  is fixed as 152.4 mm due to the length constraints of the heatsink and SiC module.  $\beta_2$  is restricted by the height of the prototype, which is selected as 15 mm. According to the reference design of planar E cores [454][464], the core height  $\beta_2$  is the sum of  $\beta_1$  and  $\alpha_1$ .

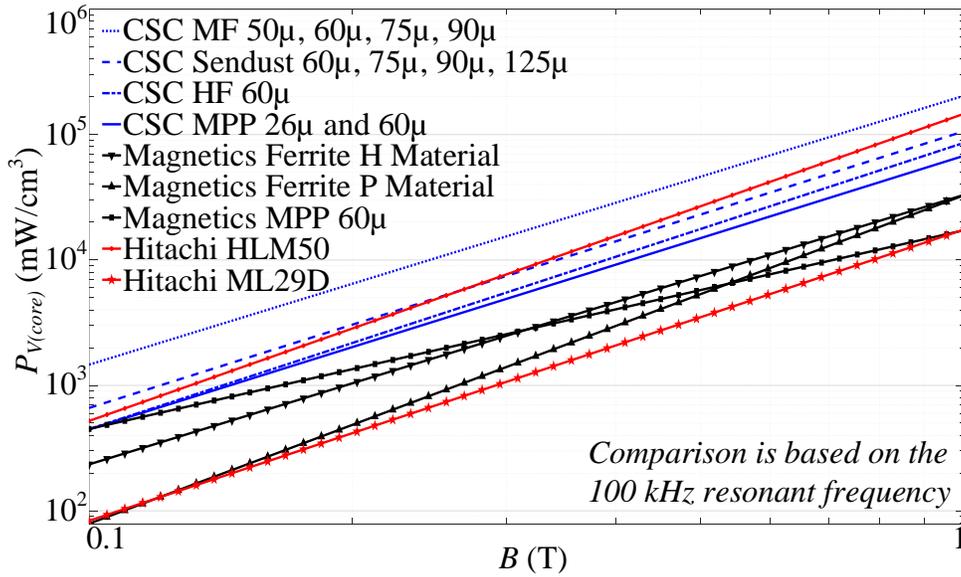


Figure 6.13. Core loss density comparison at 100 kHz frequency

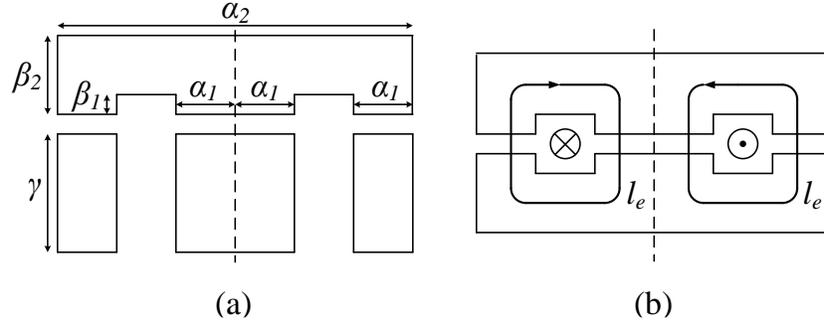


Figure 6.14. (a) E core dimensions. (b) Equivalent magnetic paths

To achieve desired inductance, core cross-section area  $A_e$  and air gap length  $l_g$  need to be designed based on (Eq.6.19) [465].

$$L = (N_{turn}^2 \cdot A_e) / [(l_g / \mu_0) + (l_e / \mu_c)] \quad (\text{Eq.6.19})$$

where,  $N_{turn}$  is number of turns.  $A_e$  is effective core cross-section area.  $\mu_0$  and  $\mu_c$  represent the permeability of the free space and core, respectively.  $l_g$  is the air gap length.  $l_e$  is the equivalent magnetic path length as shown in (Eq.6.20) [466].

$$l_e = 2(\alpha_2/2 - 2\alpha_1 + 2\beta_1 + l_g) + \pi \cdot \alpha_1 \quad (\text{Eq.6.20})$$

A proper core shape needs to satisfy the window utilization requirement due to the winding insulation. The window utilization factor  $K_u$  should be less than 0.65 for low voltage foil inductor design [467], as shown in (Eq.6.21).

$$K_u = A_{AC\_Bus} / A_{window} = 71.12 \text{mm}^2 / A_{window} \leq 65\% \quad (\text{Eq.6.21})$$

Based on the core geometry in Figure 6.14 (a), the window area  $A_{window}$  equals to  $2\beta_1 \cdot (\alpha_2/2 - 2\alpha_1)$ . Thus, a constraint for  $\alpha_1$  is derived:  $\alpha_1 \leq 13.87$  mm. In this project, 13 mm has been applied. The magnetic path length can be further calculated once  $\alpha_1$  is fixed. The calculated  $l_e$  is 149.24 mm from (Eq.6.20) while the air gap length is relatively small to be ignored here.

To further determine the core width  $\gamma$  and corresponding core cross-section area  $A_e$ , a trade-off between core temperature rise and core volume should be made. According to Faraday's law, the flux density swing  $\Delta B$  is derived as shown in (Eq.6.22).

$$\Delta B = \left| \left[ \int_{T_s/4}^{3T_s/4} L di_L(t) \right] / (N_{turn} \cdot A_e) \right| \quad (\text{Eq.6.22})$$

From (Eq.5.2, the peak resonant current  $I_{PK}$  is  $\pi$  times the average output current. Thus,  $\Delta B$  is further derived in (Eq.6.23).

$$\Delta B = (L \cdot 2I_o \cdot \pi) / (N_{turn} \cdot A_e) \quad (\text{Eq.6.23})$$

For the AC flux swing in our case, peak flux density  $B_{PK}$  is half the flux density swing  $\Delta B$  [461], as shown in (Eq.6.24).

$$B_{PK} = \Delta B / 2 = (L \cdot P_o \cdot \pi) / (N_{turn} \cdot A_e \cdot 2V_{in}) \quad (\text{Eq.6.24})$$

The core loss density  $P_{V(core)}$  is further derived in (Eq.6.25) by combining (Eq.6.17) and (Eq.6.24).

$$P_{V(core)} = (K_h \cdot f + K_e \cdot f^\lambda) \cdot \left[ (L \cdot P_o \cdot \pi) / (2N_{turn} \cdot A_e \cdot V_{in}) \right]^X \quad (\text{Eq.6.25})$$

where,  $K_h$  is 0.1035.  $K_e$  is  $7.178 \times 10^{-7}$ .  $\lambda$  is 2.  $X$  is 2.323 [459].  $N_{turn}$  is 1.  $P_o$  is 100 kW.  $V_{in}$  is 300 V.  $f$  is 100 kHz.  $L$  is 351.18 nH, according to the design in Section 6.2.3.

Core loss density is further shown in (Eq.6.26) considering  $A_e = 2\alpha_1 \cdot \gamma$ . The core volume  $V_{core}$  is in (Eq.6.27). Correspondingly, the core power loss can be calculated by  $P_{core} = P_{V(core)} \cdot V_{core}$ .

$$P_{V(core)} = (K_h \cdot f + K_e \cdot f^\lambda) \cdot \left[ (L \cdot P_o \cdot \pi) / (4N_{turn} \cdot \alpha_1 \cdot \gamma \cdot V_{in}) \right]^X \quad (\text{Eq.6.26})$$

$$V_{core} = 4 \cdot \alpha_1 \cdot (\beta_2 - \alpha_1) \cdot \gamma + \alpha_1 \cdot \alpha_2 \cdot \gamma \quad (\text{Eq.6.27})$$

The core temperature rise is estimated by (Eq.6.28) [457].

$$\Delta T_{core} = (P_{core} / A_{surface})^{0.833} \quad (\text{Eq.6.28})$$

where,  $\Delta T_{core}$  is the core temperature rise with the unit  $^{\circ}\text{C}$ .  $P_{core}$  is of the unit mW.  $A_{surface}$  has the unit of  $\text{cm}^2$ .

Based on above analysis, the core temperature rise versus core width is plotted in Figure 6.15. To reflect the optimized design region for the core width, the core volume is also plotted. Two constraints have been considered in the core width design. One is the core temperature rise, which is limited below  $100^{\circ}\text{C}$  in order to guarantee a safe operation region without external cooling for the core. Another is the core volume, which is designed to be smaller than 0.1 Liter, considering the dimensions of the resonant capacitors, heatsink and SiC power modules. Hence, a design range can be obtained based on this quantitative trade-off. Correspondingly, the core width  $\gamma$  range from 32.5 to 48 mm is derived for this application. Thus, the core cross-section area  $A_e$  has the range of  $845 \sim 1248 \text{ mm}^2$ .

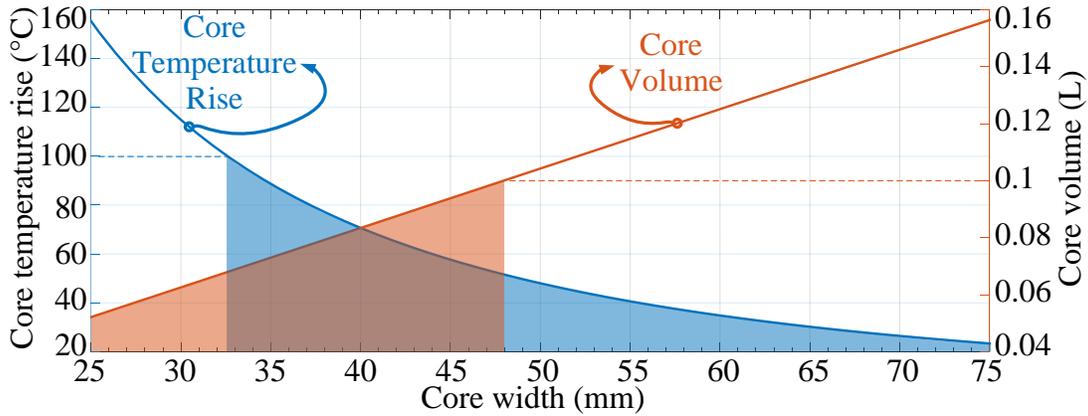


Figure 6.15. Core temperature rise and core volume trade-off

Based on the derived range of the core cross-section area, Figure 6.16 (a) shows the range of the peak flux density, i.e.  $0.1476 \sim 0.218 \text{ T}$  according to (Eq.6.24). Considering  $0.54 \text{ T}$  saturation magnetic flux density  $B_{sat}$  for the ML29D core with  $1000 \text{ A/m}$  magnetic field strength at  $23^{\circ}\text{C}$  [468], the designed flux density range is below half the saturated flux density. Thus, the full utilization and the flux saturation of the core are avoided.

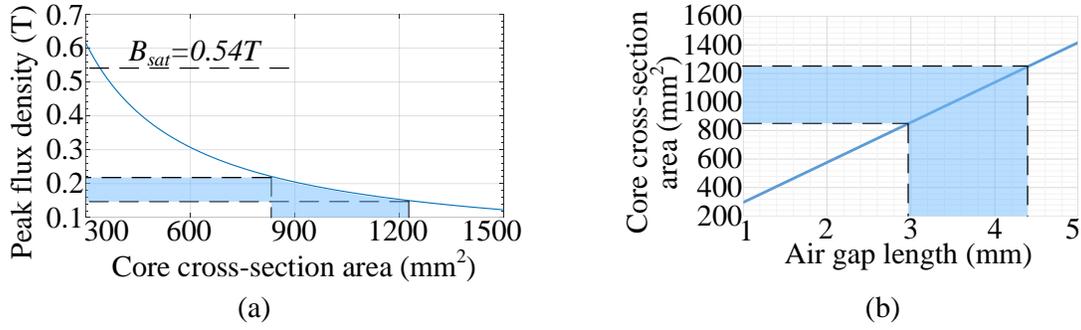


Figure 6.16. The relationship between (a) flux density and core cross-section area. (b) core cross-section area and air gap length

When the inductance and the number of the winding are fixed, based on the inductance calculation in (Eq.6.19), the relationship between  $A_e$  and  $l_g$  is described in (Eq.6.29).

$$A_e = L \cdot (l_g / \mu_0 + l_e / \mu_c) \quad (\text{Eq.6.29})$$

Since the range of the core cross-section area is known, based on the above (Eq.6.29), the relationship between the core cross-section area  $A_e$  and the air gap length  $l_g$  is plotted in Figure 6.16 (b). A design range for the air gap length  $l_g$  can be derived. From the figure,  $l_g$  ranges from 2.967 mm to 4.407 mm.

With the above core temperature rise and volume trade-off considered, in the finalized design, a core width of 40 mm is selected in the preferable region. According to this designed core width, the corresponding core cross-section area is calculated as 1040 mm². The peak flux density and the air gap length are finalized as 0.1771 T and 3.664 mm, respectively. With this designed core shape, according to the curve in Figure 6.15, the core temperature rise is about 70 °C at 100 kW. According to the core loss density  $P_{V(\text{core})}$  and core temperature rise  $\Delta T_{\text{core}}$  equations, there exists a relationship between the core temperature rise and output current  $\Delta T_{\text{core}} \propto (I_o)^{(2.323 \times 0.833)}$ . Hence, at 50 kW, the core temperature rise is 0.2615 times the counterpart at the full load, which

is about 18.3 °C. So, this inductor shape design results in a desired thermal region at 100-kW operation.

### 6.2.5. Design of DC Capacitors

Challenges of DC capacitor design in this application are mainly from the high RMS current. Higher current capability per volume normally accompanies smaller capacitance, which may not meet the minimum voltage ripple needs. Another challenge is to achieve a compact size while satisfying the other requirements. To solve these challenges, three parameters are selected as the design criteria, i.e. the total capacitance, RMS current capability, and capacitor volume. The larger total capacitance, higher RMS current density per unit volume, and smaller total volume are preferred in the evaluation.

Figure 6.17 shows seven major film capacitor manufacturer investigation, considering the RMS current capability requirement indicated in the simulated  $C_l$  and  $C_{in}$  current waveforms in Figure 6.19 (b). In each provider, the series with highest RMS current density per unit volume have been identified. Figure 6.17 (a) shows three prospective candidates, i.e. FFB and FFV3 Series from AVX<sup>®</sup>, FH series from Murata<sup>®</sup>, and B32674D Series from TDK<sup>®</sup>, have higher RMS current density. Figure 6.17 (b) presents that TDK series capacitors achieve smaller capacitance compared with others. Although the total capacitance is smaller compared with the other candidates, it can still satisfy the minimum DC capacitance requirement to realize desirable small voltage ripple. Based on the PLECS simulation, 75  $\mu$ F DC capacitance is enough to achieve a 5% voltage ripple. Therefore, the B32674D3126 from TDK has been selected for its highest RMS current per unit volume and the smallest volume with sufficient capacitance.

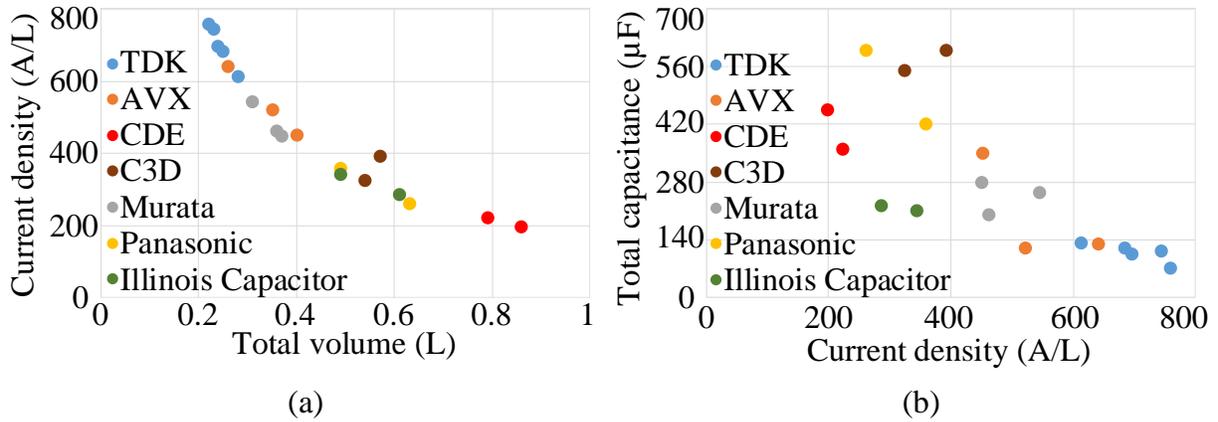


Figure 6.17. Investigation of DC capacitors from major manufacturers

In order to decide a proper number of DC capacitors, the trade-off between the temperature rise and DC capacitor volume is conducted in Figure 6.18. This design selects 9 input and 9 output capacitors considering these two factors as well as the practical mechanical layout, which needs to match the dimensions of the power modules and heatsink. The full-load temperature rise is about 39 °C. Due to the half capacitor RMS current at the half load, the 50 kW temperature rise can be derived as one quarter of the full-load temperature rise, which is around 9.75 °C. The full-load temperature is designed to be 64 °C at 25 °C ambient temperature. This is lower than the rated temperature, which is 85 °C [469].

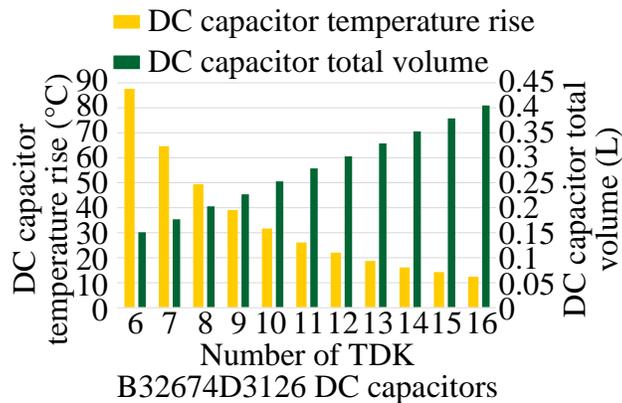


Figure 6.18. Trade-off between temperature rise and total volume for DC capacitors

### 6.3. Simulation and Experiment Results

The 100 kW 300 V - 600 V one-cell STC at ZCS mode has been simulated in PLECS.

Figure 6.19 (a) shows resonant current and  $S_1$ ,  $S_2$ ,  $S_3$ ,  $S_4$  switch current. Figure 6.19 (b) presents resonant capacitor voltage, DC capacitor voltage and current. The simulation results are consistent with the analysis in Section 5.1.

Figure 6.20 shows the developed 100-kW prototype. The control is realized through the TI<sup>®</sup> TMS320F28335 microcontroller and Xilinx<sup>®</sup> FPGA Spartan-6 XC6SLX9 IC. Figure 6.20 also presents the three dimensions of the converter. The length, width and height are 37.8 cm, 15.1 cm, and 4.2 cm, respectively. So, the converter main power processing part volume is about 2.4 Liter. The power density can be further calculated as 41.7 kW/L.

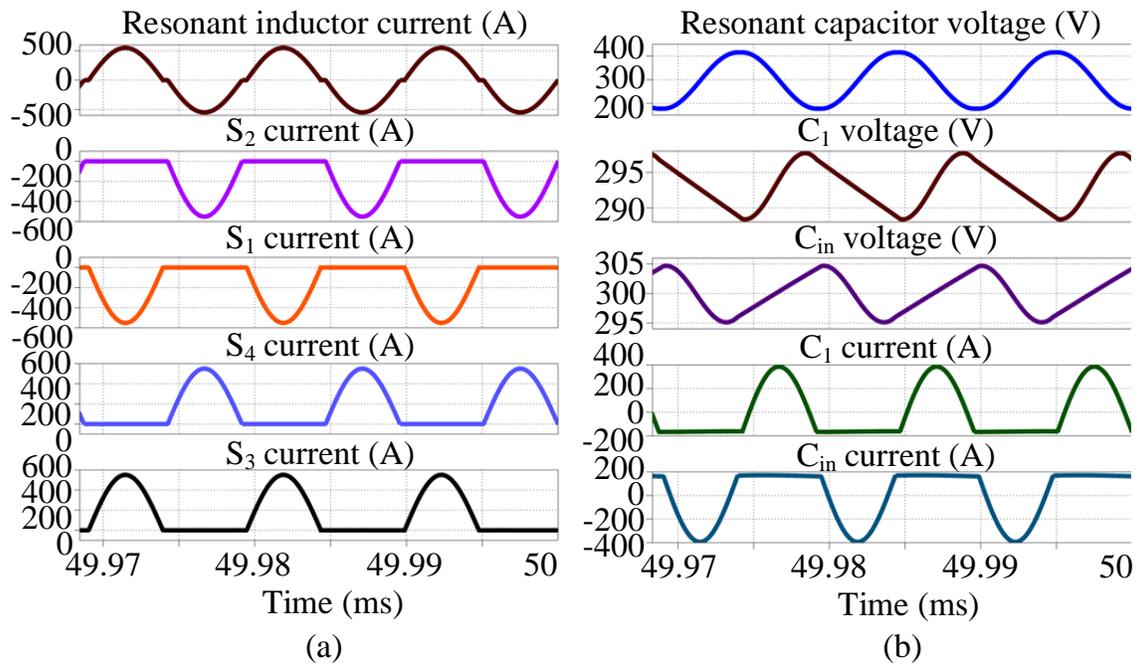


Figure 6.19. Simulation results at 300 V – 600 V with 100-kW output power

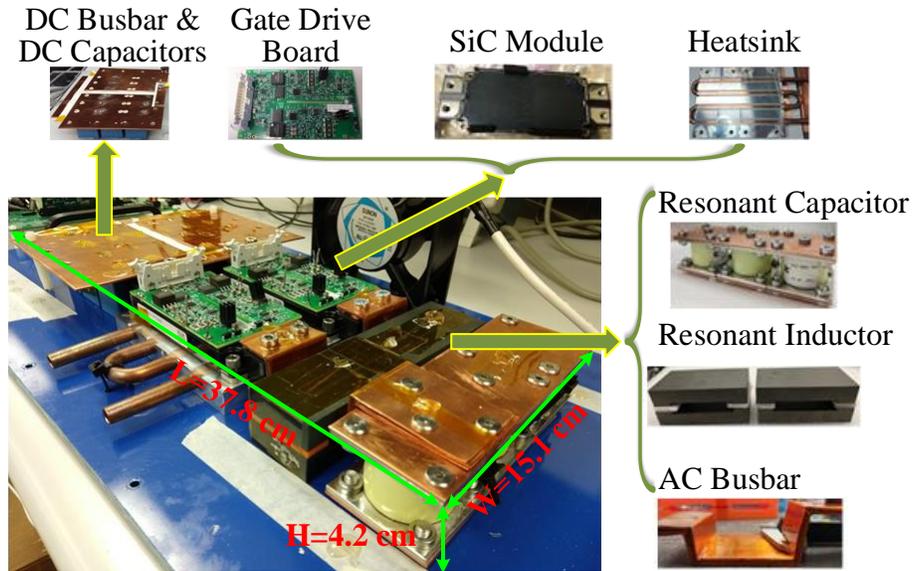


Figure 6.20. The designed and assembled 100 kW one-cell STC

The schematic of the test platform is shown in Figure 6.21. The power is circulated in a 3-phase motor-generator system. The DC power supply is aimed to compensate the power loss, most of which is consumed by the motors and generators. Therefore, the efficiency is much higher and overall thermal performance is better for this test platform compared to the platform with a high-current resistive load.

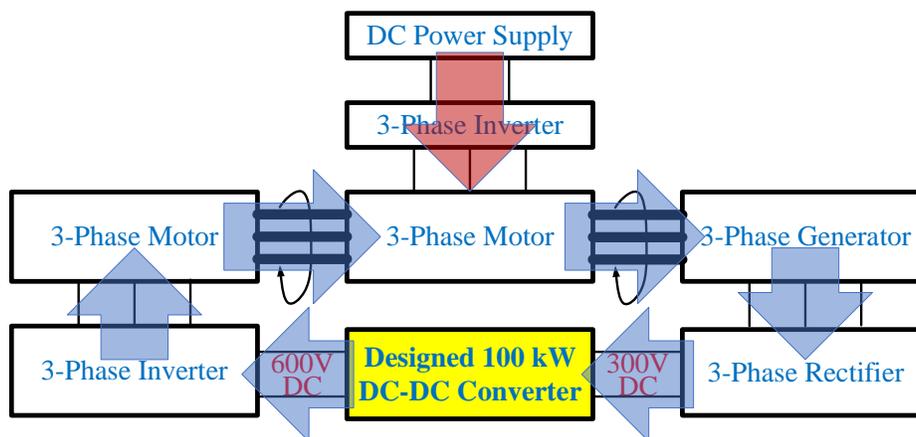


Figure 6.21. The test platform schematic for the assembled 100-kW prototype

In the test, the switching frequency is fine-tuned as 84.9 kHz, which includes the deadtime. Deadtime is set as 300 ns. The actual resonant frequency of the design is higher than the switching frequency. Figure 6.22 shows the testing results at 50 kW with 300.24 V  $V_{in}$ , 598.98 V  $V_o$  and 100 kW with 299.95 V  $V_{in}$ , 584.23 V  $V_o$ . As shown Figure 6.22 (a), the switch drain current decreases to zero before it is turned off so that the ZCS is achieved. The top two waveforms are  $V_{GS}$  of switches  $S_1$ ,  $S_2$  corresponding to Figure 5.2 (a). The middle one is tested resonant current with the RMS value around 383.2 A. Based on Eq.5.2, the corresponding theoretical RMS current value is 370.24 A, which is smaller than the tested value. This is because the current peak rises when the deadtime is included. The bottom trace is  $V_{DS}$  of  $S_2$ . Tested waveforms at 100 kW are in Figure 6.22 (b).

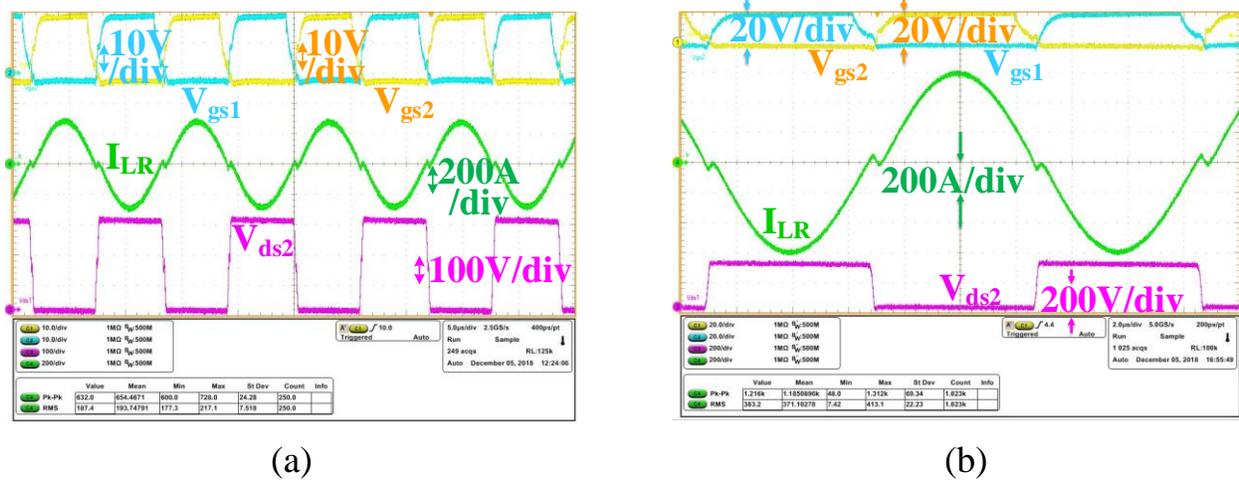
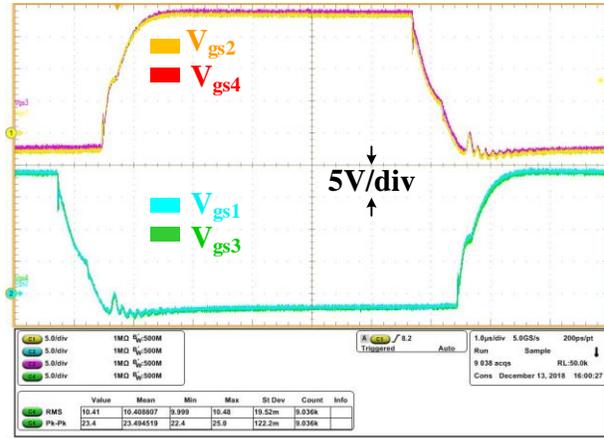
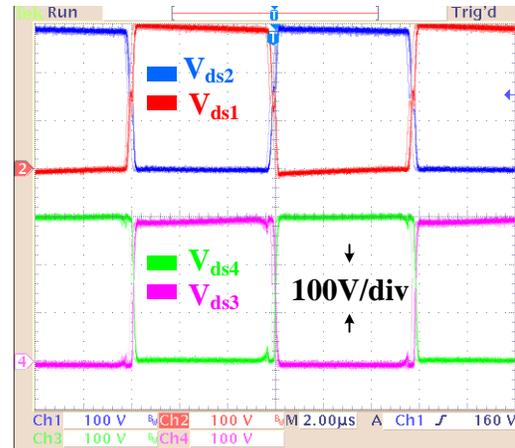


Figure 6.22. 300 V – 600 V test results at (a) 50 kW and (b) 100 kW

The tested gate-source voltage  $V_{GS}$  waveforms of the four SiC MOSFET switches are presented in Figure 6.23 (a). The gate drive output high and low voltages are +18 V and -3 V, respectively. The drain-source voltage  $V_{DS}$  waveforms are measured at about 300 V input and around 600 V output, as shown in Figure 6.23 (b). From the figure, each switch voltage stress is equal to the input voltage.



(a) Gate-source waveforms



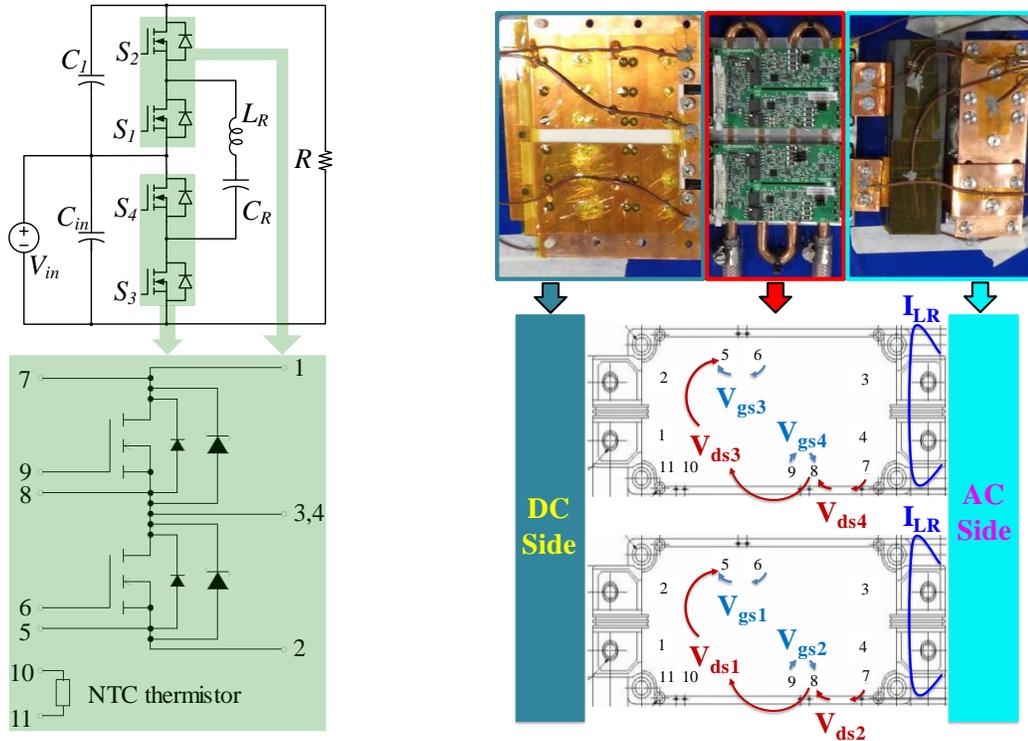
(b) Drain-source waveforms

Figure 6.23. Tested gate-source and drain-source waveforms

In these tested waveforms,  $V_{GS1}$ ,  $V_{GS2}$  corresponds to the gate-source voltages of  $S_1$  and  $S_2$  as shown in the Figure 6.24 (a). Also,  $V_{DS2}$  is the drain-source voltage waveform of  $S_2$ .  $I_{LR}$  is the resonant inductor current waveform. It is measured from the middle point of the half bridge module, as shown in Figure 6.24 (b).

The tested thermal performance at 50 kW continuous operation is shown in Figure 6.25 captured from the thermal camera. The steady-state DC and AC busbar maximum temperature is around 64.4 °C and 81.2 °C, respectively.

Table 6.2 shows the detailed tested thermal performance at 50 kW continuous operation, based on thermal couple measurement. The resonant inductor core temperature rise is 17.5 °C, which matches the theoretical half-load thermal analysis in Part 6.2.4. The two DC capacitors  $C_{in}$  and  $C_l$  show temperature of 37 °C and 24 °C, respectively. Thus, the maximum temperature rise for the DC capacitor is about 12 °C, which matches the 9.75 °C theoretical temperature rise at half load in Part 6.2.5. From the thermal results, high DC and AC busbar power losses are indicated.



(a) Selected SiC module half bridge pin diagram (b) Measured parameters in the tests

Figure 6.24. Selected SiC module half bridge pin diagram and parameter measurement details

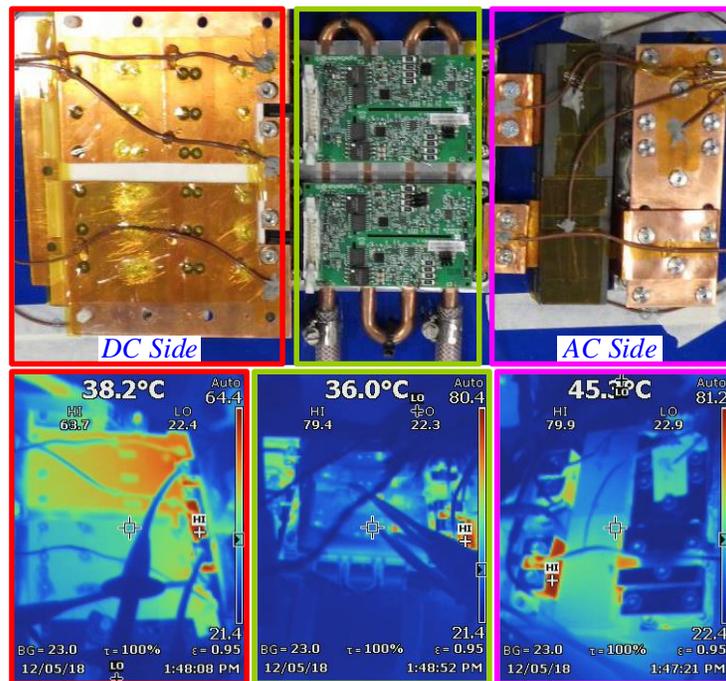


Figure 6.25. Tested thermal performance at 50 kW continuous operation

Table 6.2. Steady-state Temperature at 50 kW Operation

Component	Temperature (°C)	Component	Temperature (°C)
AC busbar	56.5	Heatsink	25
$V_{in}$ DC busbar	59	Inductor core	42.5
$V_o$ DC busbar	46	DC capacitors $C_{in}$	37
GND DC busbar	54	DC capacitors $C_l$	24

The baseplate temperature measured based on the negative temperature coefficient thermistor inside the SiC power module is acquired through the analog-to-digital sampling circuit and DSP code. It can be further utilized to derive the junction temperature  $T_j$  based on the junction-baseplate thermal impedance 61 °C/kW [449]. Considering the self-heating effect caused by the increased junction temperature, the iterations have been conducted based on the  $R_{DS\_ON}$  vs.  $T_j$  relationship until the  $T_j$  arrives to stable.  $T_j$  is calculated based on (Eq.6.30).

$$T_j = T_c + R_{th(j-c)} \cdot \left( (I_{RMS\_S})^2 \cdot R_{DS\_ON}(T_{j(1)}) + P_{Gate} + P_{Coss} \right) \quad (\text{Eq.6.30})$$

where,  $T_{j(1)}$  is the junction temperature in the previous state. The estimated  $T_j$  is used to evaluate the thermal performance of the SiC module.

Figure 6.26 shows the tested baseplate temperature and calculated  $T_j$ . Based on the curve fitted polynomial linear model in MATLAB curve fitting tool, the relationship between junction temperature and output power is presented in (Eq.6.31).

$$T_j = p_1 \cdot (P_o)^3 + p_2 \cdot (P_o)^2 + p_3 \cdot (P_o) + p_4 \quad (\text{Eq.6.31})$$

where,  $p_1, p_2, p_3, p_4$  are  $-4.174 \times 10^{-5}$ ,  $7.416 \times 10^{-3}$ ,  $-0.05791$ , and  $34.44$ , respectively.

Based on (Eq.6.31), the full-load junction temperature could be estimated as 61.07 °C. Compared with the theoretical junction temperature evaluation for the selected SiC module in Figure 6.8, if the ambient temperature is assumed as 25 °C, the tested  $T_j$  at 50 kW continuous operation is about 5 °C higher. This could be explained from three aspects. First, the total practical

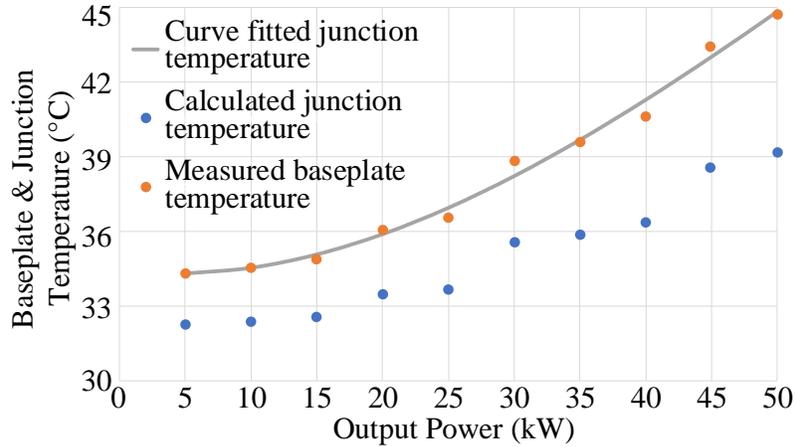
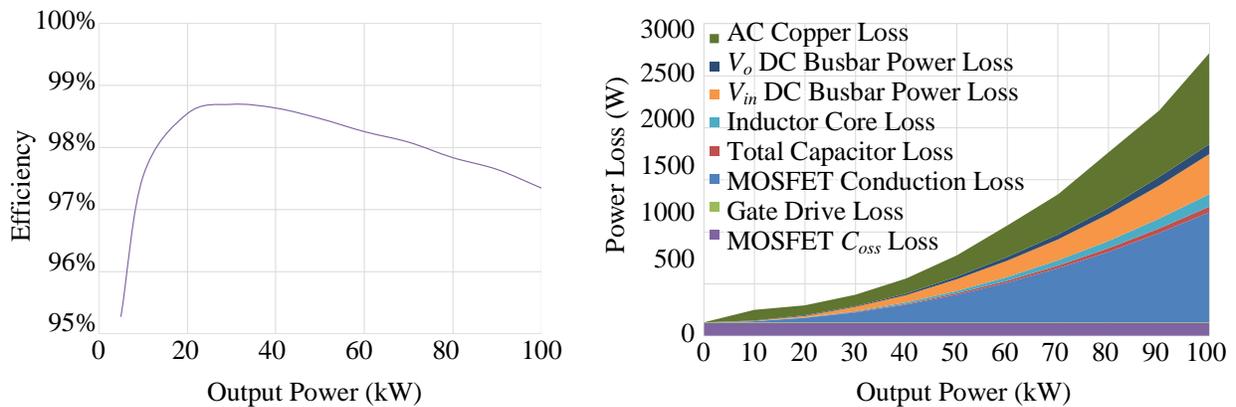


Figure 6.26. The tested baseplate temperature and calculated junction temperature

thermal impedance is larger than estimated. Second, the deadtime induced device RMS current increase was not considered in Figure 6.8. Third, the impact of junction temperature on  $R_{DS\_ON}$  increase was not included.

Figure 6.27 (a) shows tested efficiency based on the measured voltage, current and power data from Yokogawa® WT1800 power analyzer. The tested peak efficiency is about 98.7% at 30 kW. The tested full-load and half-load efficiencies are about 97.35% and 98.47%, respectively.



(a) Tested efficiency versus the output power

(b) Tested power loss breakdown versus output power

Figure 6.27. Tested efficiency and power loss breakdown for the assembled prototype

The power loss breakdown is conducted with different output power in Figure 6.27 (b). The MOSFET conduction loss is a major contribution at full load. Both the on-resistance increase with the junction temperature and the device RMS current increase with the deadtime have been included in the conduction loss estimation. Besides, the  $V_{in}$  DC busbar loss and AC copper loss are also significant in the total power loss. The  $V_{in}$  and  $V_o$  DC busbar power losses are calculated based on the measured voltage drops between two ends on the  $V_{in}$  DC busbar and  $V_o$  DC busbar.

Figure 6.28 presents the changes of DC busbar power loss and AC copper loss with output power. Figure 6.28 (a) shows that at 100 kW output power, the  $V_{in}$  and  $V_o$  DC busbar power losses reach to around 386.9 W, and 94.4 W, respectively. The AC copper loss is estimated based on the difference between the tested total power loss and the power loss estimated from the output and input power difference. Figure 6.28 (b) illustrates the AC copper loss versus the output power, from which the maximum AC copper loss reaches up to about 876.2 W at 100 kW output power.

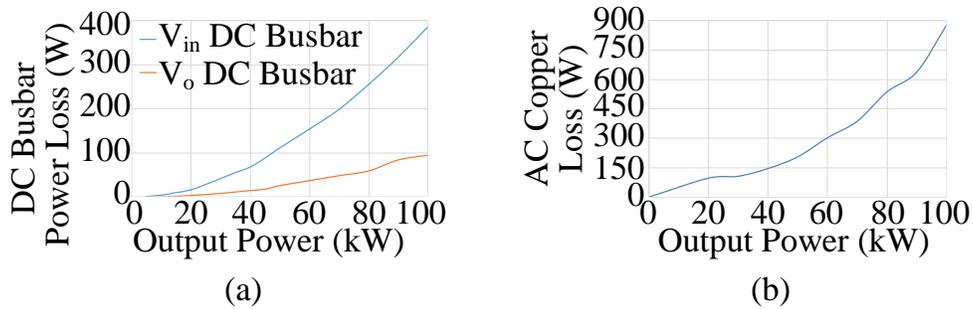


Figure 6.28. (a) DC busbar power loss vs.  $P_o$ . (b) AC copper loss vs.  $P_o$

To verify the theoretical calculated TSLI based on Rohm 1200 V 95 A SiC die (part number: S4103 [442]), a comparison has been conducted in Figure 6.29 between the theoretical and tested TSLIs with changing output power for this application. Considering 576 A current rating (at 60 °C case temperature) of the selected Rohm 1200 V SiC power module, six S4103 bare dies would be needed. Besides, four SiC MOSFETs are utilized in the prototype. Therefore, the total

die area is 24 times the S4103 die area. The difference between the theoretical and tested TSLI is mainly caused by the current measurement noise, which further impacts the total conduction losses. As can be seen from Figure 6.29, the tested TSLI based on the 1200 V 576 A SiC MOSFET module matches well with the theoretical value calculated from the 1200 V 95 A SiC bare die.

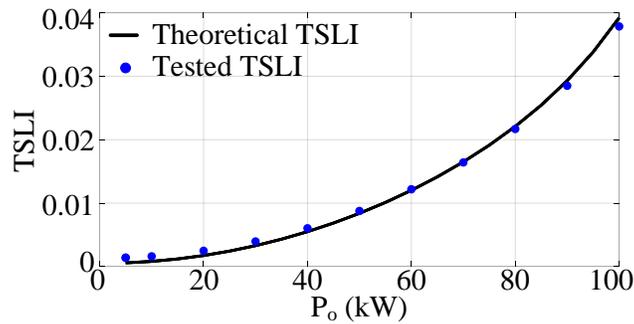


Figure 6.29. Comparison between the theoretical and tested TSLIs

From the current rating and on-resistance information of the available Rohm 1200 V SiC bare dies, the most suitable match for the utilized Rohm 1200 V SiC MOSFET power module is the Rohm 1200 V SiC die (part number: S4103). With this die applied in our one-cell STC topology at ZCS operation for 300 V – 600 V 100 kW application, the calculated TSLI is plotted in Figure 6.30. Our current prototype has utilized about 500 mm<sup>2</sup> total die area, but it is not the optimal solution in terms of the total device power loss.

As shown in Figure 6.30, when the valley bottom appears around 2000 mm<sup>2</sup> total die area, the smallest TSLI is realized. This means the total device power loss is minimized for this specific topology with given switching frequency, input, output voltage, current requirements. If the chip manufacturer works together with the power electronics engineer to figure out a larger SiC bare die area (for example, around 500 mm<sup>2</sup> die area per SiC MOSFET device in this four-switch case) with other parameters almost the same, then the optimized device total power loss can be achieved.

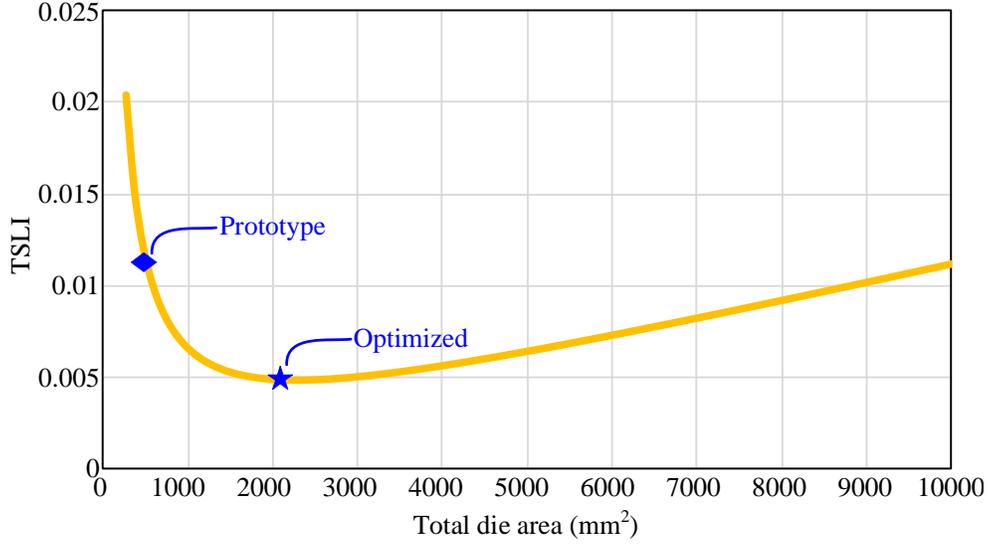


Figure 6.30. TSLI in the designed prototype and optimized solution

#### 6.4. Thermal Performance Comparison Between One-cell and N-cell STC

Thermal design is indeed a critical part in this kind of high-power high-current converters. The smaller thermal resistance could lead to lower junction temperature. The thermal evaluation is conducted on the generalized  $N$ -cell STC for the three main components, i.e. resonant capacitor, resonant inductor core, and power module, as presented in the following.

##### (1) Thermal performance comparison of the resonant capacitors

The thermal impedance and temperature rise of the resonant capacitors have already been calculated in (Eq.6.14) and (Eq.6.15), respectively.

If the  $I_{Lr(RMS)}$  is generalized as the RMS resonant current of the  $N$ -cell STC. With the given input voltage  $V_{in}$  and output power  $P_o$ , it can be presented in (Eq.6.32).

$$I_{Lr(RMS)} = \frac{\pi}{\sqrt{2}} \cdot \frac{P_o}{(N+1) \cdot V_{in}} \quad (\text{Eq.6.32})$$

For a fair comparison, the same three resonant capacitors are assumed in  $N$ -cell STCs, i.e. Illinois Capacitor<sup>®</sup> LC3 AC resonant capacitors. This configuration can satisfy the resonant current requirement for the one-cell STC. Since when  $N \geq 2$ , the resonant RMS value is smaller, this

configuration is also applicable for the generalized  $N$ -cell STCs. Substituting the (Eq.5.4) into (Eq.6.15) can lead to the resonant capacitor temperature rise versus the number of cells at the same input voltage and output power as shown in Figure 6.31. As can be observed, the resonant capacitor temperature rise decreases with the number of the STC cells, because smaller RMS current leads to lower power loss.

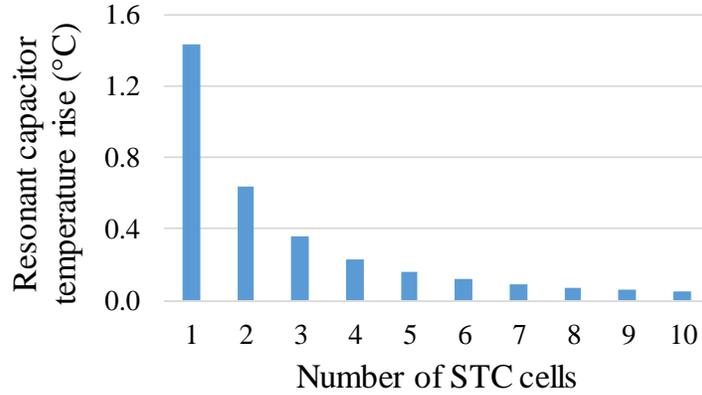


Figure 6.31. Resonant capacitor temperature rise vs. number of STC cells

## (2) Thermal performance comparison of the resonant inductor core

This comparison assumes that  $N$ -cell STCs use the same inductance value, the same Hitachi ML29D cores and share the same E-core dimensions. The core loss volumetric density has been demonstrated in (Eq.6.17). The peak flux density  $B_{PK}$  can be further updated as a function of the number of STC cells, as shown in (Eq.6.33).

$$B_{PK} = \frac{\Delta B}{2} = \frac{1}{2} \left[ \int_{T_s/4}^{3T_s/4} L di_L(t) \right] / A_e = \left( \frac{\pi L}{A_e} \right) \cdot \left( \frac{P_o}{(N+1)V_{in}} \right) \quad (\text{Eq.6.33})$$

By updating the core temperature rise in (Eq.6.28) using the above generalized peak flux density, the core temperature rise versus the number of the STC cells can be plotted in Figure 6.32. The core temperature rise experiences a decreasing trend as the number of the STC cells increases, because of smaller peak flux density and resulted lower core loss density per unit volume.

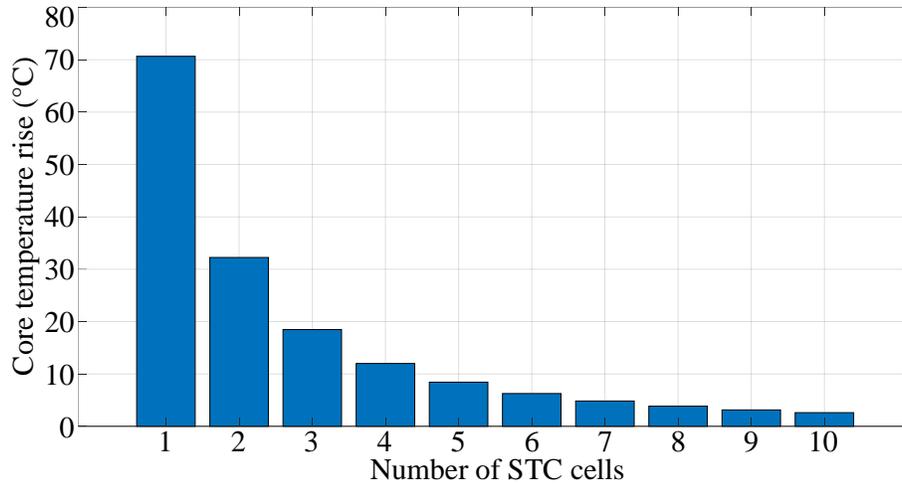


Figure 6.32. Core temperature rise vs. the number of the STC cells

(3) Thermal performance comparison of the power module

The generalized switch RMS current has been shown in (Eq.5.3). By substituting (Eq.5.3) into (Eq.6.30), the relationship between  $T_j$  and the number of cells can be drawn in Figure 6.33. As the number of the STC cells increases, the junction temperature becomes lower, because the RMS current and the conduction loss decrease.

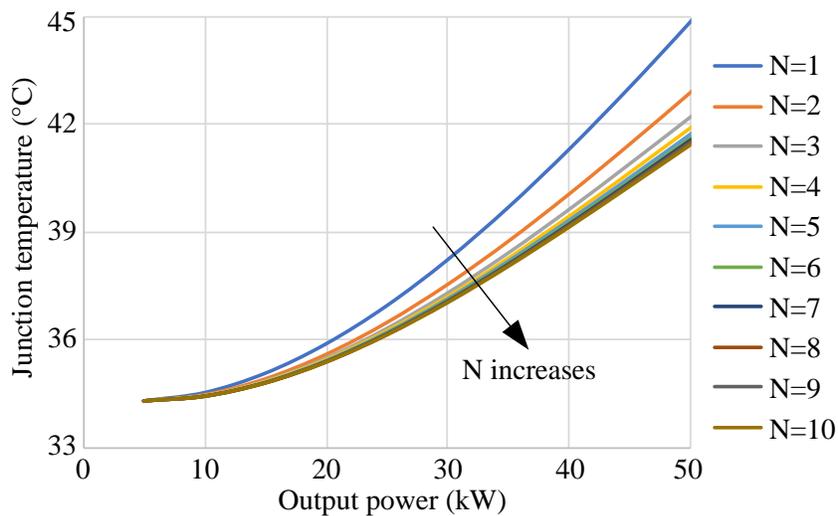


Figure 6.33. The relationship between junction temperature and the number of cells

## 6.5. Summary for This Chapter

This chapter has demonstrated a development of a 100 kW SiC based switched tank converter for the transportation electrification applications. The proposed total semiconductor loss index (TSLI) has been shown as an effective method to evaluate different topologies and device technologies to achieve the lowest device power loss with minimum semiconductor die area. By applying this index, the optimal topology and device technology for the STC could be identified. From the detailed design procedures and passive component optimization, a compact resonant tank with single-turn soft-ferrite-core inductor and three low-volume high-current high-frequency polypropylene film capacitors has been achieved. From the experimental results, the proposed thermal design has shown expected performance at 50 kW continuous operation and 100 kW peak operation. The assembled prototype main power circuit power density is about 42 kW/L. The tested peak efficiency is around 98.7% at 30 kW. The tested 100 kW efficiency is about 97.35%. Future power density and efficiency improvement will include more suitable lower-voltage-rating power device selection, high frequency AC and DC busbar optimization with reduced volume and power loss.

## 7. GAN BASED STC WITH PARTIAL-POWER VOLTAGE REGULATION

Figure 7.1 presents a typical high-power high-voltage power electronic system in an electric vehicle. High-conversion-ratio DC-to-DC converters between the battery and the inverter can increase the dc-link voltage further for the inverter, compared with the conventional DC-to-DC converters. The higher dc-link voltage would help decrease both the input and output current for the inverter at the same operated power. This scenario is especially helpful to decrease the power loss when the high-voltage-rating and low-current-rating devices are available. These compact, high-efficiency, high-conversion-ratio step-up converters have been widely studied these days [410][470].

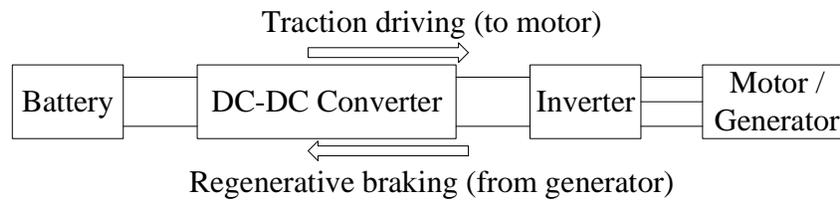


Figure 7.1. A typical high-power high-voltage power electronic system in an electric vehicle

Commonly, a traditional boost [418], [471]–[476], interleaved boost [424], buck-boost [477][478], and isolated dual active bridge [479] converters have been used to step up the voltage from the battery to DC bus for the inverter. However, the traditional boost converter suffers from low efficiency, high switch voltage and current stresses when the converter operates at high conversion ratios. To overcome these problems, the partial-power voltage regulation has been utilized into the regulated DC-to-DC converters. The idea of the partial-power processing is firstly mentioned in PV area. As illustrated in Figure 7.2, this concept allows the in-series PV elements to operate at independent current  $I_{MPP1}$  and  $I_{MPP2}$  by injecting an external controllable current source. Correspondingly, the maximum power point tracking (MPPT) can be achieved for each PV element, which can be either solar module, panel, or array [480].

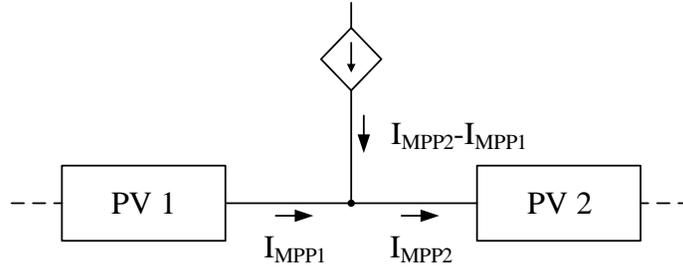


Figure 7.2. Differential power converters modeled as a controlled current source

Applying this partial-power processing concept into the voltage regulation results in a generalized composite structure for regulated DC-to-DC converters, as shown in Figure 7.3. They normally use multiple converter topologies combined in an overall system to form a composite structure, which basically consists of an unregulated stage and a voltage-regulated stage. This is important for motor drive applications because the stable DC-link voltage is critical to the motor control. The system efficiency is high because the unregulated stage processes most of the overall power while the less efficient voltage regulator consumes a small amount of power to keep the output voltage regulated.

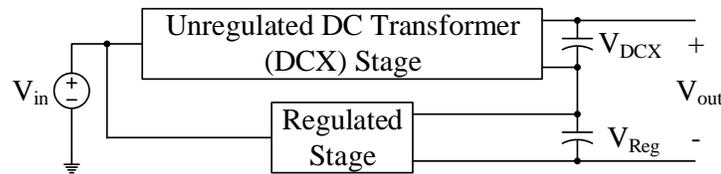


Figure 7.3. Generalized composite structure for regulated DC-to-DC converters

Some of these composite topologies are the isolated composite resonant multilevel converter [481], the sigma converter in Figure 7.4 (a) [482][483], the boost composite converter in Figure 7.4 (b) [484][485], and the quasi-parallel voltage regulator [486]. These new topologies offer higher system efficiencies with lower switch voltage and current stresses than the traditional boost converter. They primarily consist of a full-bridge converter and a buck converter [482][483]

or a boost converter [484][485], which is in series with the output but shares the same input voltage. The full-bridge converter acts as the unregulated stage while the others provide the voltage regulation.

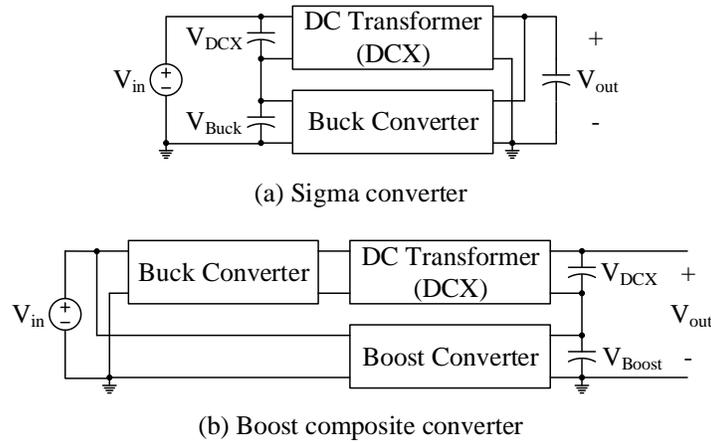


Figure 7.4. Two typical composite structures for regulated DC-to-DC converters

The unregulated stage can be realized by either the isolated or non-isolated forms. In terms of the isolated version, the LLC [482] and dual active bridge (DAB) [487] topologies have been utilized, as presented in Figure 7.5. Although LLC topology can be optimally designed at a certain operating point, due to too wide frequency range, the adjustable input voltage and load ranges are both limited [488]. Besides, the DAB topology has the circulating current issue caused by the transformer leakage inductance [489].

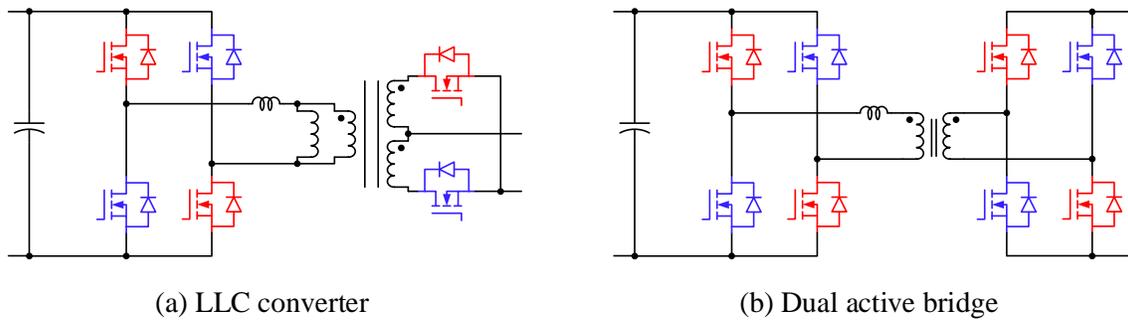


Figure 7.5. Two isolated forms of the unregulated stage

In terms of the non-isolated version, the resonant switched capacitor converters have been well studied these years for high efficiency and high power density [383], [384], [436], [438], [490]–[494]. It can realize wide input voltage and load range. There is no issues related to the transformers, such as the bulky size and large power loss. Based on the demonstrated STC topology [383], a buck-boost converter has been added to realize the partial-power voltage regulation [494]. The proposed step-up converter in this project combines the STC unregulated stage analyzed in Section 5.1 and a buck converter as the voltage-regulated stage. With the proposed converter, the device voltage stress can be decreased to the low-voltage-side voltage, which means the device technology can make it possible to increase the DC-link side voltage to much higher level. So, the 1200 V DC-link voltage is studied in this research. In this chapter, the TSLI will be utilized to compare different topologies.

### **7.1. Operation Principles of Proposed STC with Partial-Power Voltage Regulation**

Figure 7.6 presents a generalized topology of the proposed STC with partial-power voltage regulation (PPVR), which is derived from the one in Figure 5.1. It utilizes a modular, resonant converter to offer low switch voltage and current stress, which makes it possible to optimize the devices and increase the power density. It can also achieve soft switching, which helps improve the efficiency. The unregulated STC is composed of  $N$  basic cells to achieve a  $1:(N+1)$  voltage conversion ratio. In each cell, there are four switches  $S_i$ , one clamping capacitor  $C_{ci}$ , one resonant capacitor  $C_{ri}$  and one resonant inductor  $L_{ri}$ . The drain-source voltage overshoot during switching transient is alleviated by the clamping capacitors  $C_{ci}$ . The voltage regulation is realized by the partial-power voltage regulator, which can be buck, boost or buck-boost converters. The switch voltage stress of both the STC and partial-power voltage regulator is equal to the input voltage.

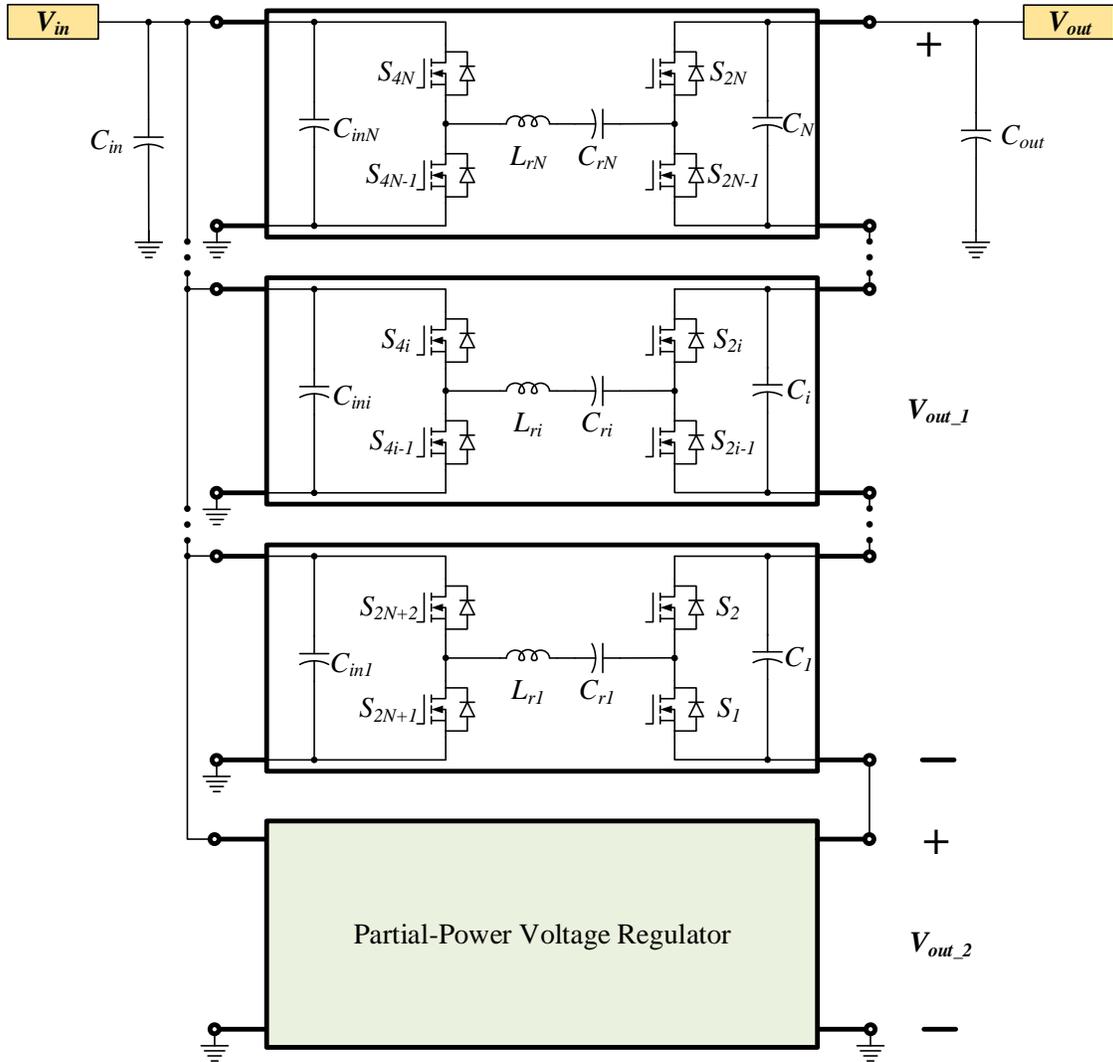


Figure 7.6. Generalized STC integrated with partial-power processed voltage regulator

In this chapter, the proposed converter is designed for an electric vehicle application where the battery voltage ranges from 200 V to 400 V. The output voltage is 1200 V for the DC-link of a 4-kW inverter to drive the electric motors and generators. Due to the wide-range battery voltage, a conversion ratio from 3 to 6 is required. Below, the operation principles of the converter are demonstrated including the STC part and regulated PPVR buck converter part.

### 7.1.1. 1:6 STC as the Unregulated Stage

Figure 7.7 shows a  $1 : (5+D)$  regulated STC. It consists of a  $1 : 6$  unregulated STC and a regulated buck converter with conversion ratio of  $D$ .

The two switching modes of the STC are shown in Figure 7.8. All the switches marked in blue work simultaneously for half the switching cycle, while the other switches marked in red operate complementarily at another half cycle. The DC voltages of  $C_{r1}$ ,  $C_{r2}$ ,  $C_{r3}$ ,  $C_{r4}$  and  $C_{r5}$  are  $V_{in}$ ,  $2V_{in}$ ,  $3V_{in}$ ,  $4V_{in}$ ,  $5V_{in}$ , respectively when they are charged to the steady state, so that the output voltage is  $6V_{in}$ . By controlling the number of active STC modules, the regulated stage can achieve discrete conversion ratios of  $0 \sim 6$ .

In switching mode 1 shown in Figure 7.8 (a), the odd indexed resonant capacitors are charged.  $C_{r1}$  is charged by the input voltage.  $C_{r3}$  is charged by the input voltage and  $C_{r2}$ . And  $C_{r5}$  is charged by the input voltage and  $C_{r4}$ . In the switching mode 2 illustrated in Figure 7.8 (b), the even indexed resonant capacitors are charged.  $C_{r2}$  is charged by the input voltage and  $C_{r1}$ .  $C_{r4}$  is charged by the input voltage and  $C_{r3}$ .  $C_{r5}$  and input voltage together charge the output capacitor. In each mode, the resonant current is sinusoidal and starts from zero, which realizes the turn-on ZCS. Besides, by designing the switching frequency a little lower than the resonant frequency, the sinusoidal current reverses the polarity before the switches are turned off. Furthermore, through selecting a proper deadtime between the two complementary PWM signals, the current flowing through the body diode can be controlled to decrease to zero before the next half cycle starts. Therefore, all the switches can be turned off at ZCS.

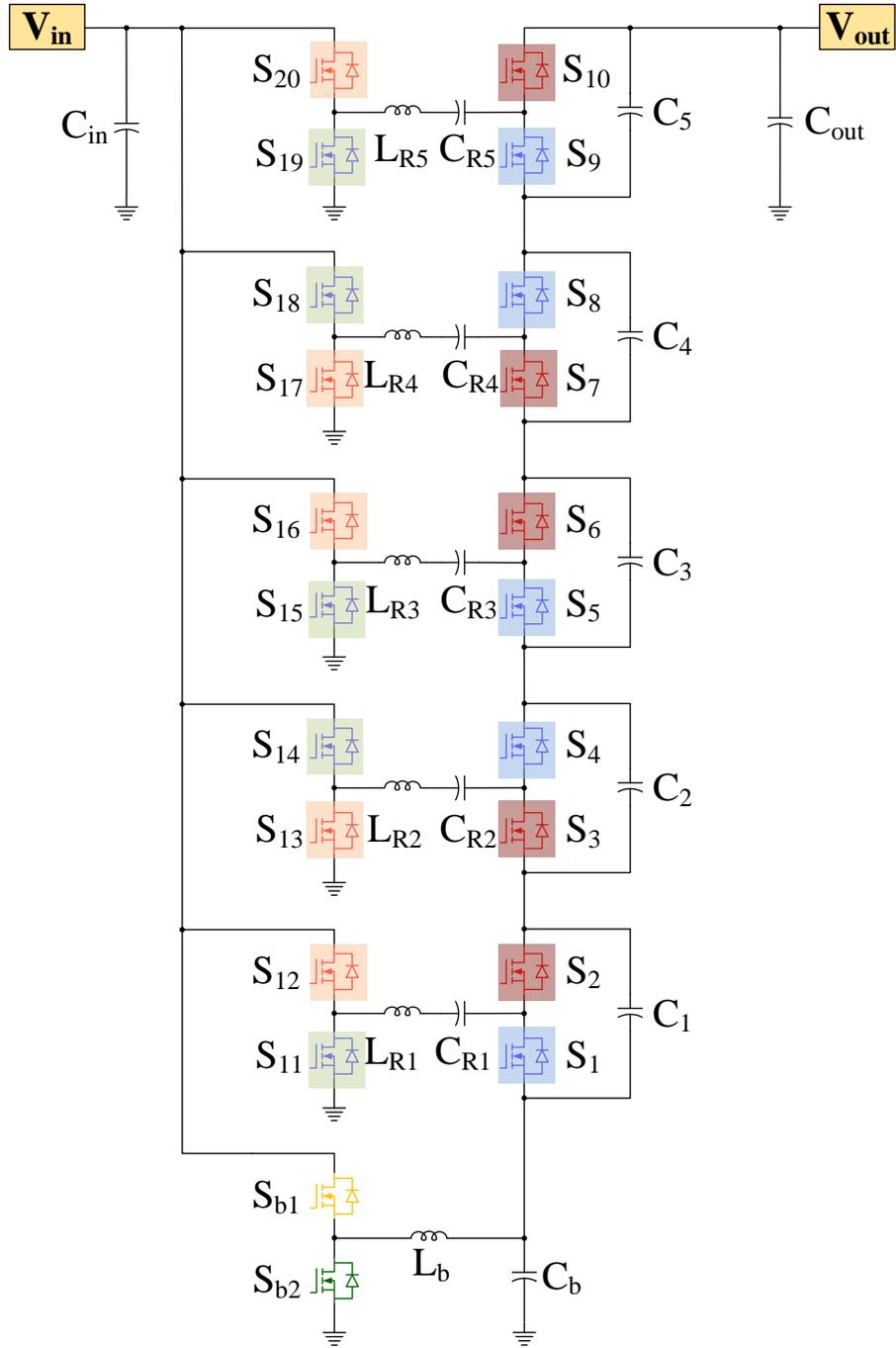


Figure 7.7. STC integrated with a buck converter with  $1 : (5+D)$  conversion ratio

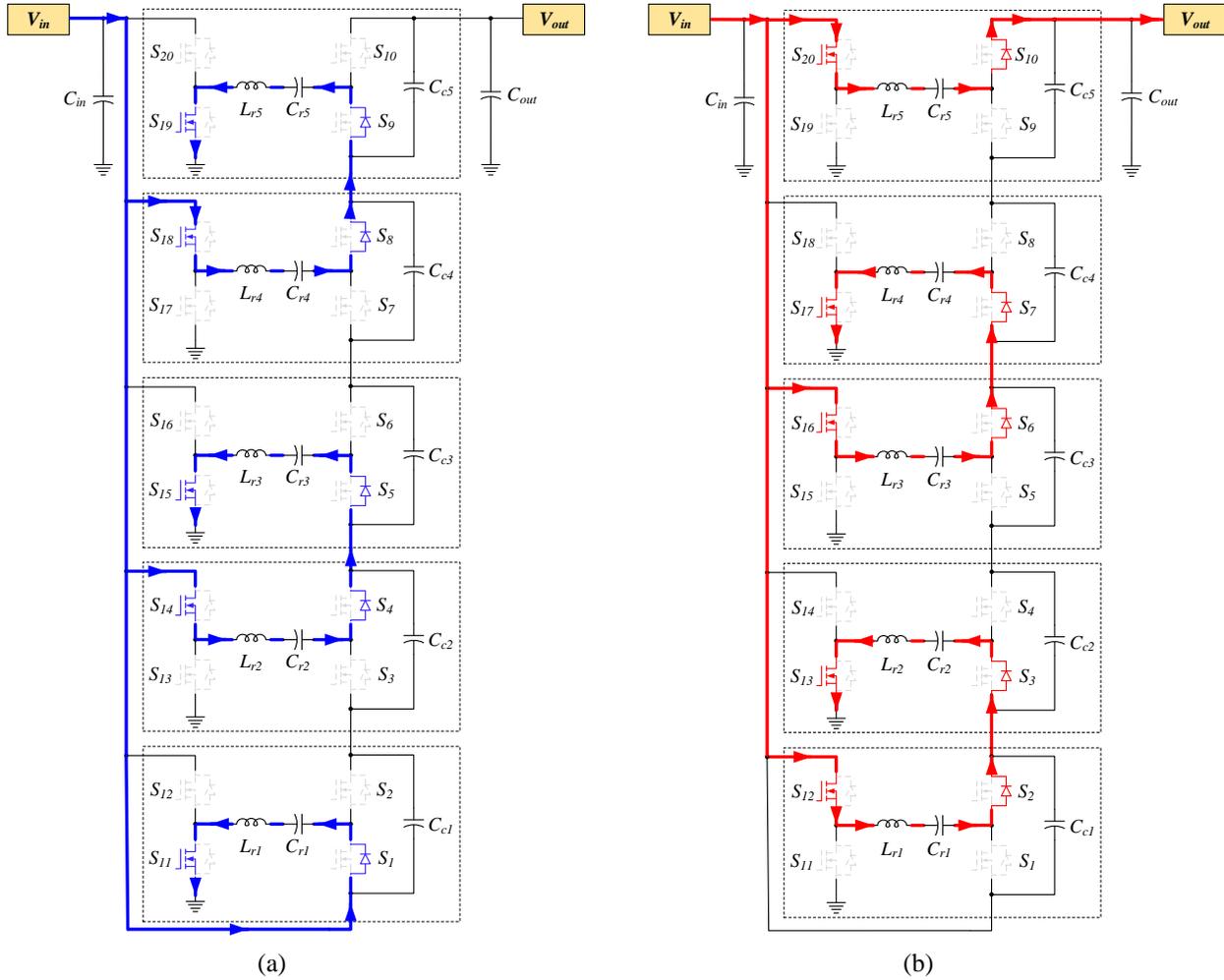


Figure 7.8. Two switching states of the proposed 1 : 6 STC

The five clamping capacitors  $C_{c1}$ ,  $C_{c2}$ ,  $C_{c3}$ ,  $C_{c4}$  and  $C_{c5}$  are used to alleviate the drain-source voltage overshoot of  $S_1$  to  $S_{10}$ . The voltage stress of all the switches is equal to the input voltage. Hence, lower device voltage ratings can be selected, which normally accompany smaller on-resistance and corresponding lower conduction loss.

### 7.1.2. Buck Converter as the Voltage-Regulated Stage

With the addition of the partial-power voltage regulator, this converter can operate at any conversion ratio between 0 and 6. Assuming the total number of active STC modules is  $N$ , the duty cycle of the buck converter is  $D$ , the system conversion ratio can be found in (Eq.7.1).

$$V_o / V_{in} = N + D \quad (\text{Eq.7.1})$$

By adjusting  $N$  and  $D$ , the conversion ratio can be tuned flexibly for various battery voltage ranges. The timing graph of the above circuit is presented in Figure 7.9.  $Main\_R$  and  $Main\_B$  represent the control signals for the STC switches in red and in blue, respectively. While  $Buck\_Y$  and  $Buck\_G$  mean the control signals for the buck converter switches in yellow and in green, respectively. The four STC switch current waveforms are related to the switches in corresponding colors as shown in Figure 7.7.  $I_{S_{b1}}$ ,  $I_{S_{b2}}$ , and  $I_{C_b}$  are the upper, lower switch, and output capacitor current waveforms in the buck converter, respectively.  $DT$  is the deadtime. There are six working modes for this regulated converter.

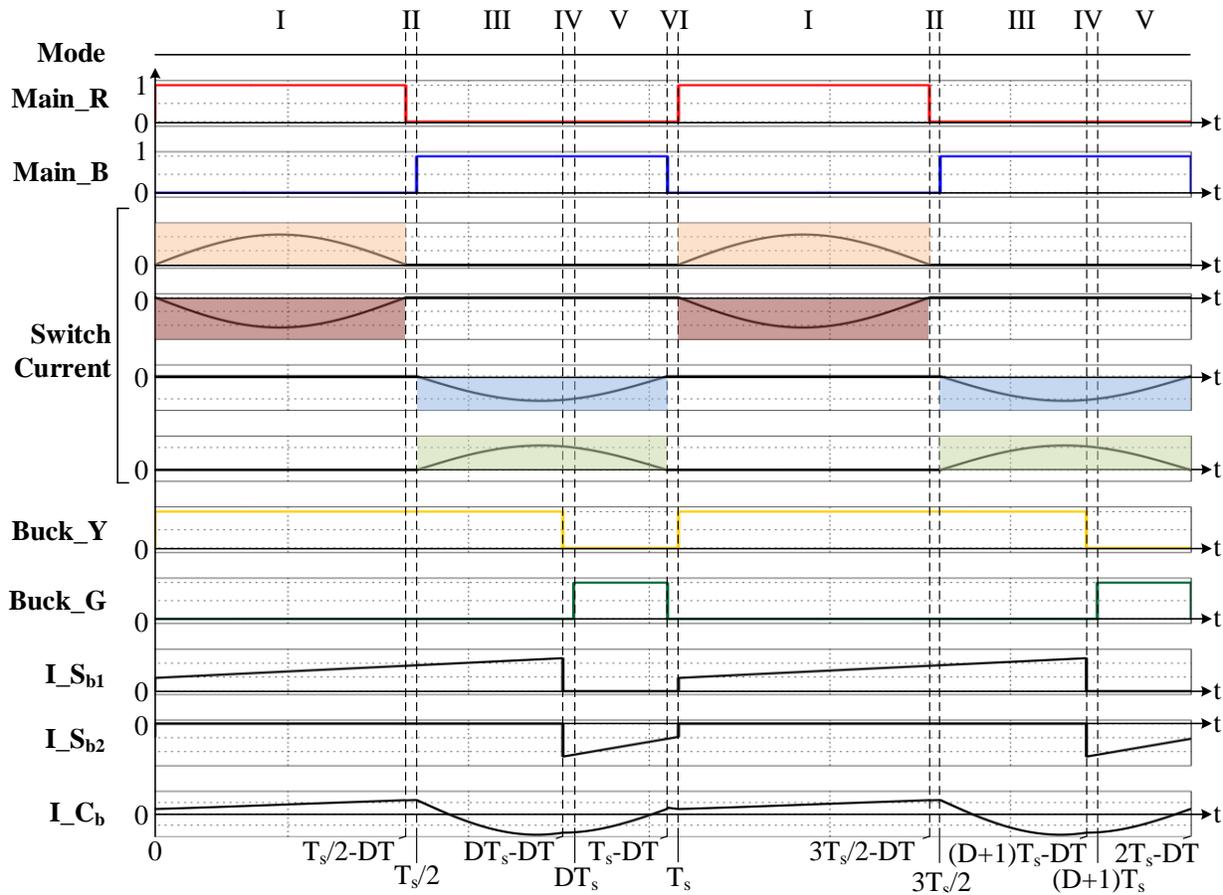


Figure 7.9. Timing graph of the 1 : (5+D) regulated STC

Because the voltage stress on switches of proposed converter is equal to input voltage, the converter can utilize GaN power transistors with 650V voltage rating. With 350V battery voltage and 1200V output voltage, the overall conversion ratio is 3.4286. The unregulated converter stage has 3 active modules and has a conversion ratio of 4. The inactive module works in a bypass mode where the switches closer to the output voltage side are on and the switches closer to the input voltage side are off. The regulated stage works at 0.4286 duty cycle so that the system conversion ratio is dropped down to 3.4286 and thus 1200 V output voltage is achieved. The power processed by the STC and the regulated buck converter are presented in (Eq.7.2) and (Eq.7.3), respectively.

$$P_{STC} = V_{out\_1} \cdot I_{out} \quad (\text{Eq.7.2})$$

$$P_{reg} = V_{out\_2} \cdot I_{out} \quad (\text{Eq.7.3})$$

where,  $P_{STC}$  and  $P_{reg}$  are the power consumed by the STC and regulated buck converter, respectively. The overall efficiency  $\eta_{overall}$  can be further calculated with the (Eq.7.4).

$$\eta_{overall} = \frac{V_{out\_1}}{V_{out}} \cdot \eta_{STC} + \frac{V_{out\_2}}{V_{out}} \cdot \eta_{reg} \quad (\text{Eq.7.4})$$

where,  $\eta_{STC}$  and  $\eta_{reg}$  are the efficiency of the STC and the buck converter, respectively.

## 7.2. Evaluation of the STC with Partial-Power Voltage Regulation

The TSLI defined in Section 5.2 is utilized in the following to evaluate the impact of different device technologies on the voltage-regulated converter topologies. Before the comparison, several assumptions are made. First, the boost or buck converter ZVS turn-on [495][496] and ZCS turn-off [497] are often realized by adding additional components and auxiliary circuits. To avoid to bring in extra unobtainable power loss, the boost converter inductance is designed in hard switching with 30% current ripple [498] considering the tradeoff between the size and the RMS current of the inductor. Second, by adjusting the deadtime and making the switching frequency slightly smaller than the resonant frequency, the ZCS turn-off can

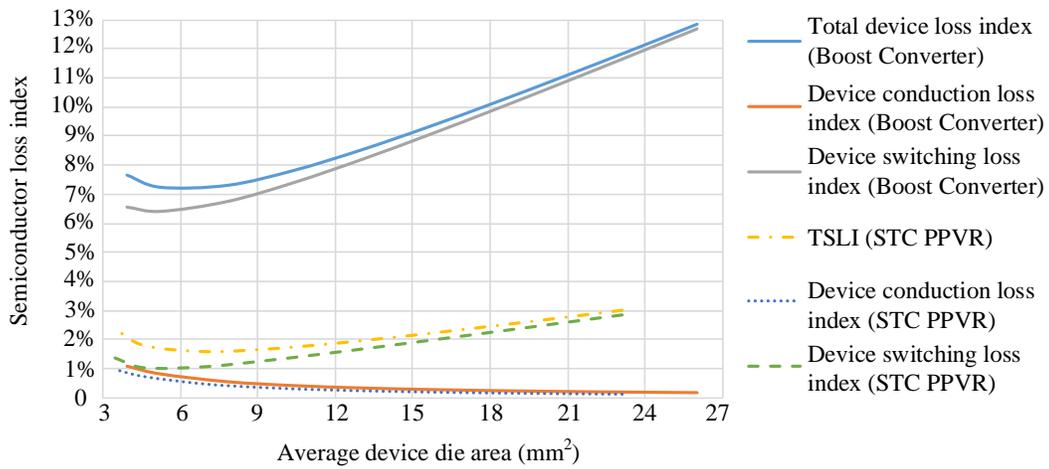
be achieved. Thus, only  $C_{oss}$  induced turn-on loss is considered in the STC switching loss. Third, the 350-V-to-1200-V DC-to-DC step-up converter for electric vehicle application is targeted.

According to the 350 V voltage stress of the switches, Rohm 650 V SiC dies (S4003) are selected for all the switches in proposed converter. Considering the 1200 V switch voltage stress in the boost converter, two in-series Wolfspeed 1200 V SiC dies (CPM2-1200-0025B) are used for each switch in boost converter in this evaluation. Since the switching loss versus drain current is not included in the datasheet of Rohm SiC die S4003 and Wolfspeed SiC die CPM2-1200-0025B, the relationship between the turn-on, turn-off switching energy and drain current for these two dies is derived from the datasheets of Rohm's 650 V SCT3120AL SiC MOSFET and Cree's 1700 V C2M0045170P SiC MOSFET, respectively.

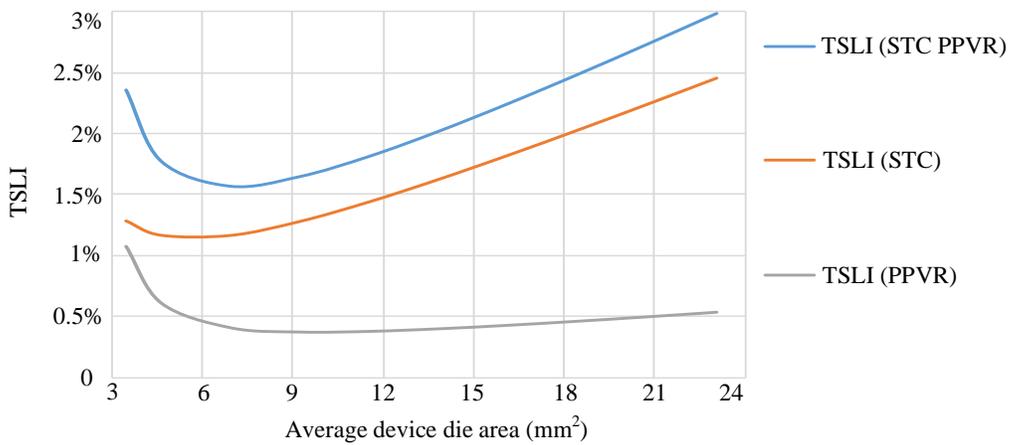
As presented in Figure 7.10 (a), at the same 350 V input, 1200 V output voltage and 4 kW output power, with the same switching frequency 357 kHz, the total device power loss of STC with PPVR is less than 1/3 of boost converter with the same die area. It can achieve more effective die utilization at the same conduction loss. By further breaking down the total device power loss of each converter, it can be found that they share similar conduction loss. It is the switching loss that contributes largely to the total device power loss.

From Figure 7.10 (b), the PPVR power loss becomes less significant as the die area increases. That is because the  $C_{oss}$  discharge induced STC device switching loss becomes more dominant as the die area is enlarged.

The TSLI can also be applied to evaluate the impact of different output power operation, switching frequency, and conversion ratio on the total device power loss to comprehensively compare converter topologies in terms of the optimized device technology.



(a) Device power loss Indices versus die area for boost converter & STC PPVR

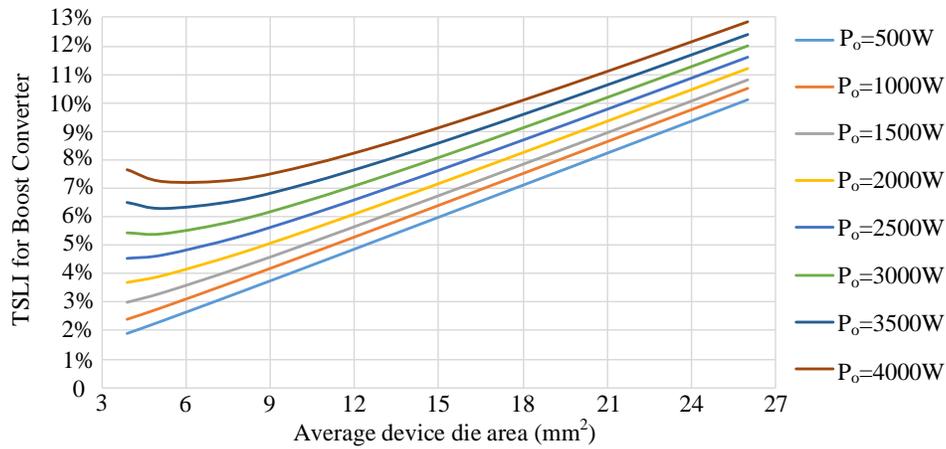


(b) Device power loss Index versus die area of STC PPVR

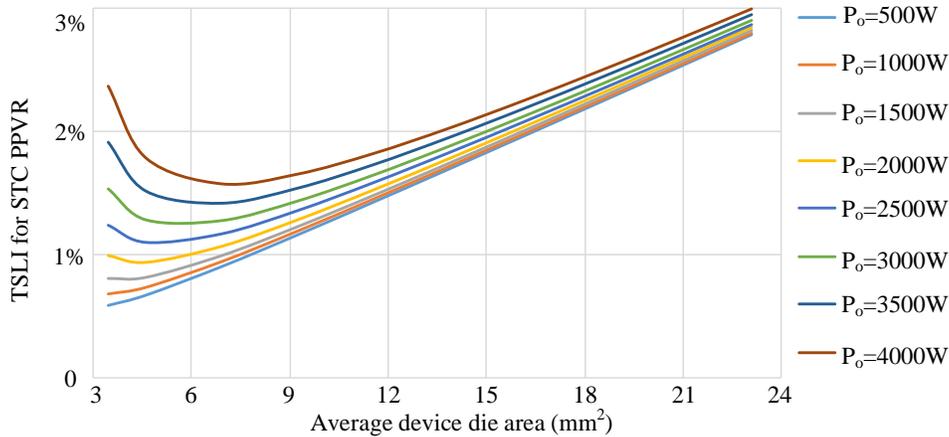
Figure 7.10. TSLI evaluation for the proposed STC with PPVR

To further investigate the relationship of different output power operation and the die area, the TSLI is compared between boost converter and proposed STC with PPVR. This comparison is based on the 4000 W designed output power rating, 350 V input voltage rating, and 1200 V output voltage rating. The comparison results are shown in Figure 7.11 (a) and (b) for the boost converter and STC with PPVR, respectively. As the output power increases, the total semiconductor loss index becomes larger in both the two converters. Compared with boost converter, the proposed one can achieve less total device power loss under both the light-load and heavy-load conditions.

With different switching frequency, the relationship between total device power loss and semiconductor die area is shown in Figure 7.12 for both the boost converter and STC with PPVR. Both the two converters can achieve larger semiconductor power loss as the switching frequency increases. The percentage of the semiconductor power loss among the output power for the boost converter can be decreased to about 2.5% when the switching frequency is reduced to 100 kHz. But for the proposed STC with PPVR, this percentage can be decreased to smaller than 1% at 100 kHz.



(a) TSLI of boost converter with different output power operation



(b) TSLI of STC PPVR with different output power operation

Figure 7.11. TSLI evaluation with different output power operation

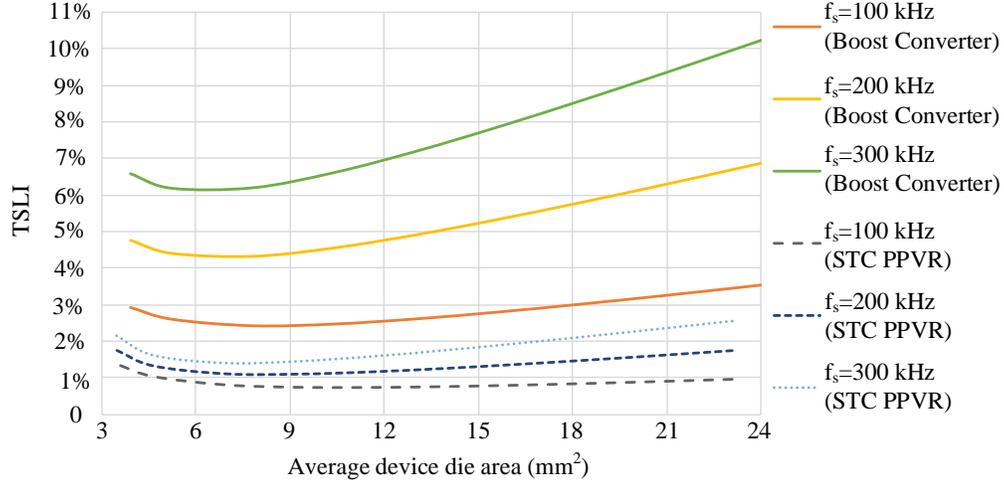


Figure 7.12. TSLI of boost converter and STC with PPVR under different switching frequency

To evaluate the impact of conversion ratio on the total device power loss, the comparison between boost converter and STC with PPVR is made with the 4 kW output power, 1200 V output voltage, 200 V ~ 400 V input voltage range as shown in Figure 7.13. It is based on the same cutting ratio of the corresponding dies. For boost converter, each switch die has 0.3 times the die area of Wolfspeed 1200V SiC dies (CPM2-1200-0025B). For STC with PPVR, each switch die has 0.3 times the die area of the Rohm 650V SiC dies (S4003). As the conversion ratio rises, the device power loss of the boost converter increases linearly. For the STC with PPVR, when the conversion ratio changes, the device power loss fluctuates nonlinearly. This is because the number of the working STC modules changes at different conversion ratio ranges. During conversion ratio range 3~4, 4~5 and 5~6, the number of active STC modules is 3, 4, and 5, respectively. The total device conduction loss of STC is unrelated to the conversion ratio because the STC device RMS current  $i_{STC\_SW\_RMS}$  is only dependent on the output current according to (Eq.7.5).

$$i_{STC\_SW\_RMS} = \sqrt{\frac{1}{T_s} \int_0^{\frac{1}{2}T_s} \left( \frac{P_o}{V_o} \cdot \pi \cdot \sin(2\pi f_s \cdot t) \right)^2 dt} = \frac{\pi}{2} \cdot I_o \quad (\text{Eq.7.5})$$

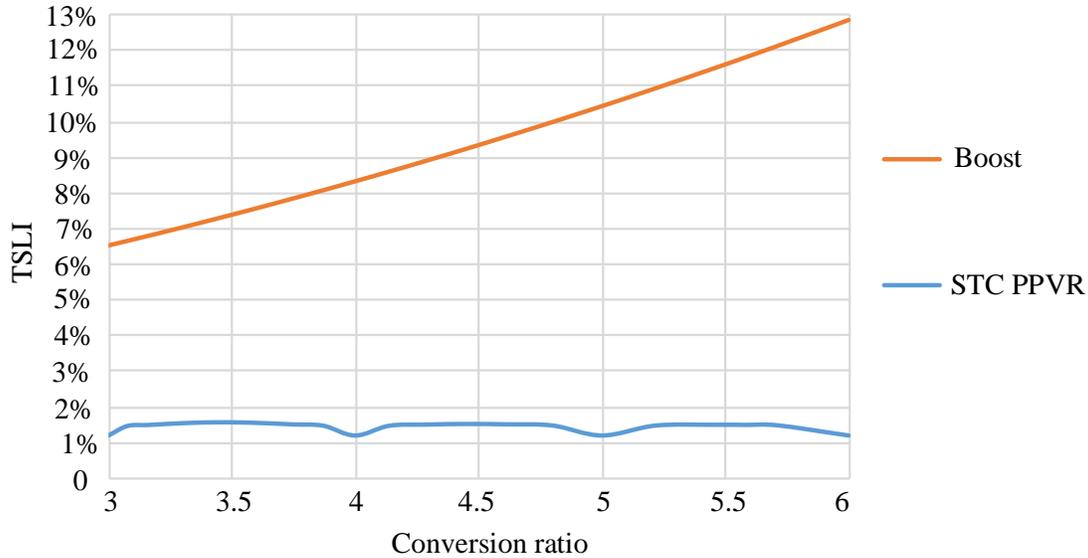


Figure 7.13. TSLI versus total die area with different conversion ratio

Besides, the gate charge induced switching loss and  $C_{oss}$  related turn-on switching loss do not change with the conversion ratio when the die area is fixed. Thus, the STC switching loss is fixed. Therefore the total device power loss of the STC with PPVR is affected only by the buck converter when the conversion ratio changes. Since the buck converter device current RMS changes with the similar trend during each conversion ratio range 3~4, 4~5 and 5~6, the buck converter device conduction loss follows the periodical curve when the conversion range is in each range. As a result, the STC with PPVR device power loss versus conversion ratio appears as can be observed from the blue curve in Figure 7.13.

To evaluate the power processed by buck converter under different conversion ratios from 3 to 6, calculation has been made in MATHCAD and the results are shown in Figure 7.14. In this evaluation, 4 kW output power, 1200 V output voltage, 200 V ~ 400 V input voltage range have been applied. The percentage of the power processed by buck converter reaches to the peak when the duty cycle of the buck converter is close to 0.5. This is because the turn-on and turn-off switching power losses of the buck converter are the highest around 0.5 duty cycle.

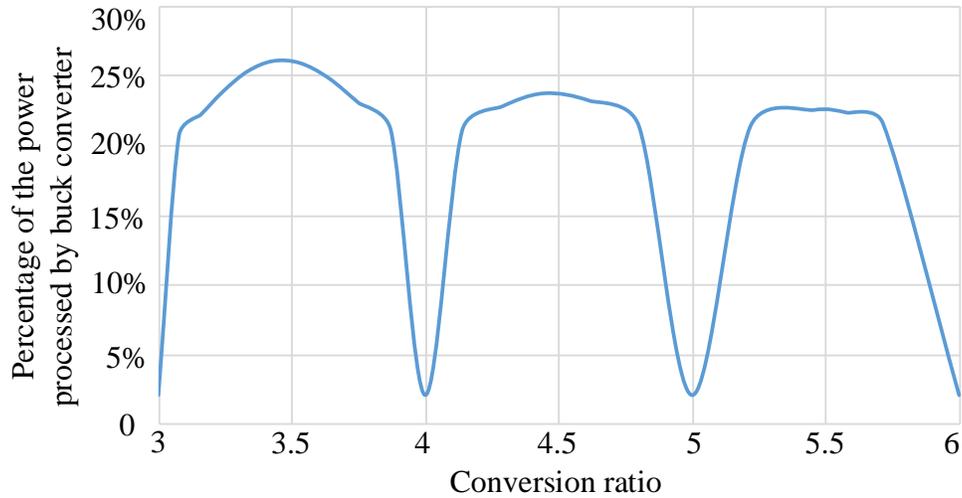


Figure 7.14. Percentage of the power processed by buck converter versus conversion ratio

### 7.3. Power Loss Breakdown and Efficiency Estimation

Based on the designed key components listed in Table 7.1, the device, inductor and capacitor RMS currents are calculated. The power loss breakdown analysis and efficiency estimation are further conducted.

In Figure 7.15, the STC switch conduction loss, gate drive loss and  $C_{oss}$  induced turn-on switching loss are calculated. The resonant inductor loss, the resonant capacitor ESR loss are included. Besides, the buck converter switch conduction loss, turn-on and turn-off switching loss and gate drive loss are calculated. Since the typical switching loss versus drain current is not included in the GS66508B datasheet, the relationship between turn-on, turn-off switching energy and drain current is derived from the datasheet of Rohm's 650V 21A SiC MOSFET SCT3120AL. The AC winding loss and core losses of both the STC resonant inductor and buck converter inductor are analyzed through Coilcraft core and winding loss calculation tool. From Figure 7.15, the  $C_{oss}$  loss contributes the largest portion of the total power loss.

Table 7.1. Key Components of Designed 4-kW 1200-V Output Converter

Name	Part Number / Company	Parameters
Resonant inductor	XAL1060-152MEB /Coilcraft	1.5 $\mu\text{H}$ , $I_{sat}$ 36 A
Resonant capacitor	CGA9Q1C0G3A333J280KC /TDK	C0G / 33 nF*4
Clamping capacitor	C5750X6S2W225K250KA /TDK	X6S / 2.2 $\mu\text{F}$ *6
Buck output capacitor		
Buck converter inductor	XAL6060-223MEB /Coilcraft	22 $\mu\text{H}$ *2
Output capacitor	B58031U9254M062 /TDK	250 nF*38
STC switches	GS66508B /Gan Systems	$V_{DS(max)}$ 650 V
Buck switches		$I_{DS(max)}$ 30 A
Gate driver IC of GS66508B	SI8271GB-IS /Silicon Labs	Peak output current 4 A

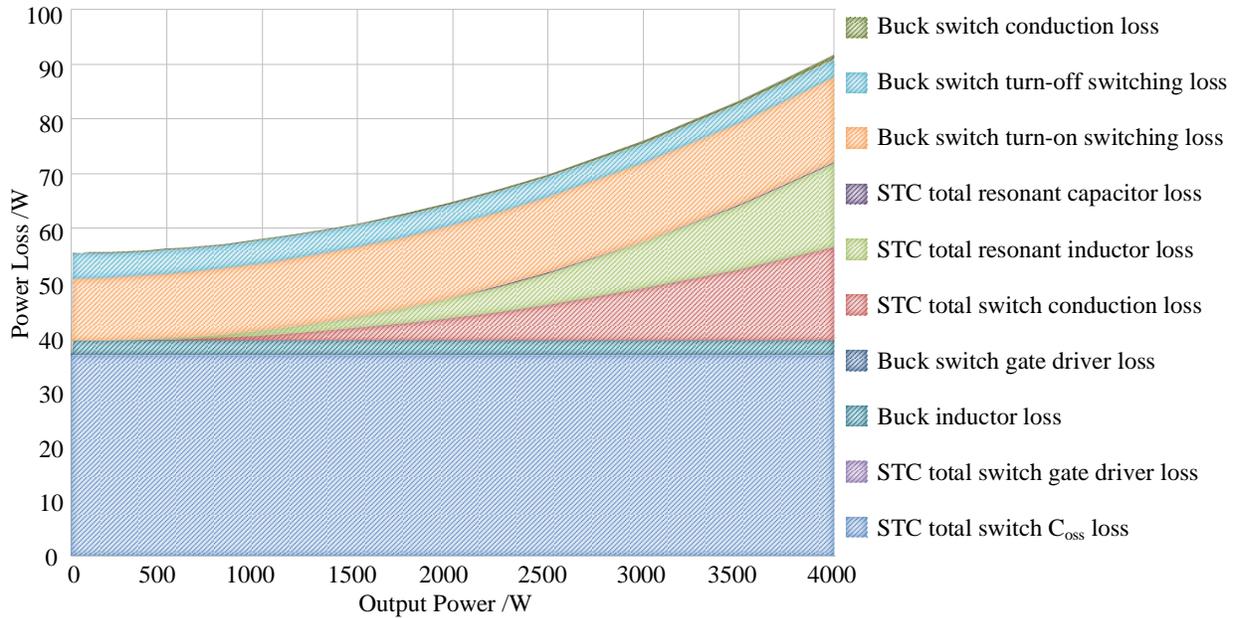


Figure 7.15. Power loss breakdown of the STC with PPVR

In addition, the power loss is classified into STC and PPVR buck converter in Figure 7.16.

The buck converter power loss is smaller than one third of the power loss of the STC at full load.

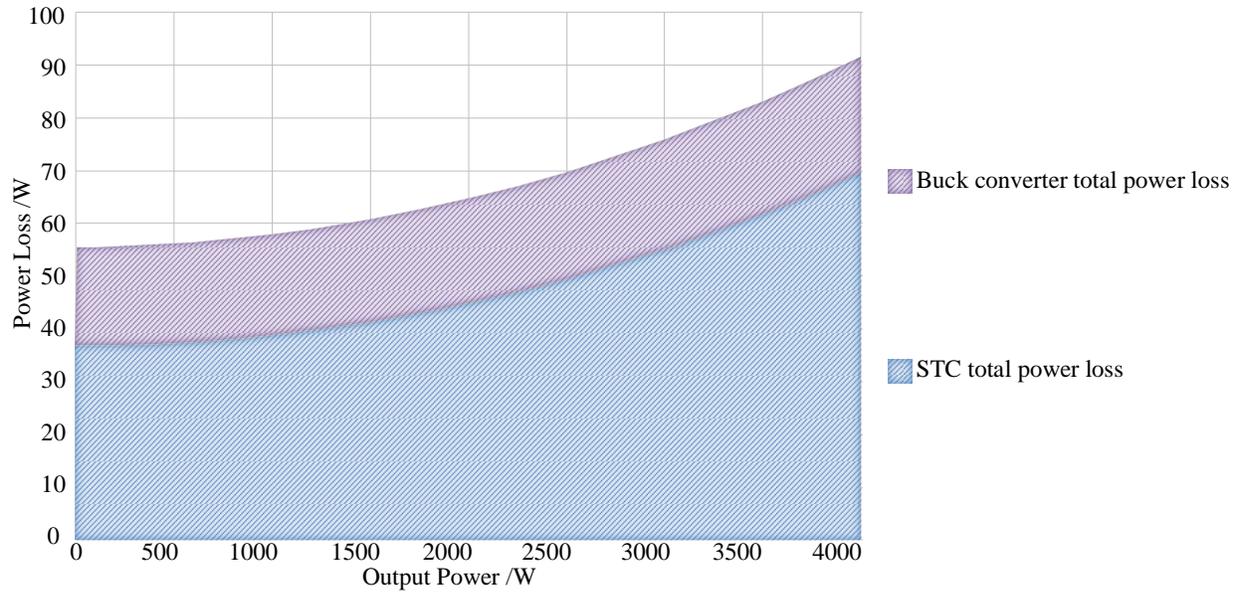


Figure 7.16. Power loss comparison of the STC and the partial-power voltage regulator

Finally, based on the power loss analysis, the overall efficiency is estimated in Figure 7.17.

The peak efficiency is around 97.71% at full load.

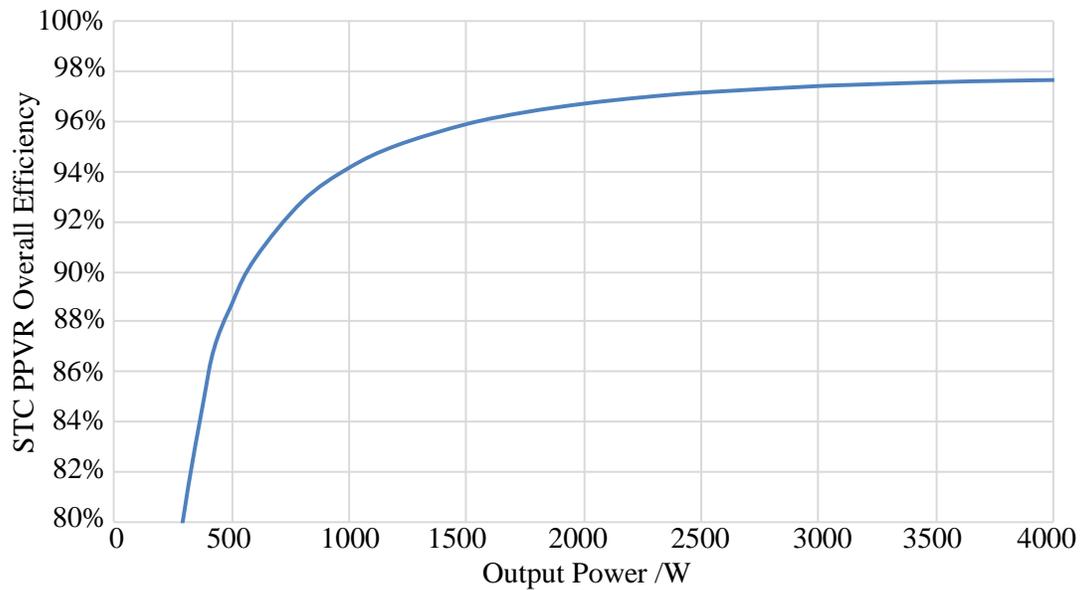


Figure 7.17. Efficiency estimation of STC with PPVR

#### 7.4. Simulation Results

To verify the function of the designed 350-V-to-1200-V 4-kW STC with PPVR, the simulation is carried out in PLECS. A boost converter with the same input, output voltage and output power is also simulated for comparison.

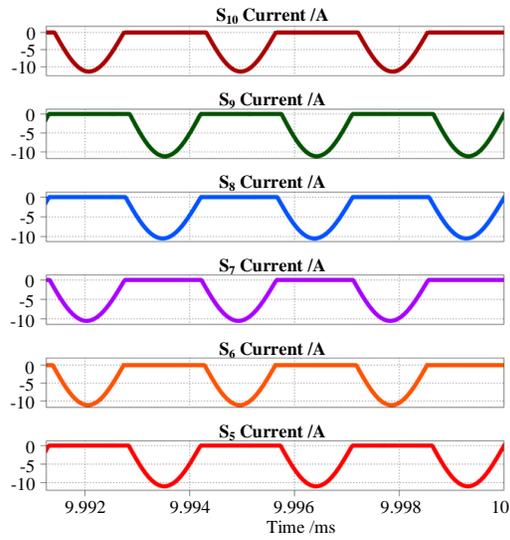
To achieve 1200-V output voltage from 350-V input voltage, the boost converter duty cycle is set as 0.70833. In the proposed STC with PPVR, the duty cycle of buck converter is 0.4286. Three STC cells are considered to generate 1:4 conversion ratio in the unregulated stage. The inductor in the buck converter is 44  $\mu\text{H}$  to make it work in continuous conduction mode.

In Figure 7.7,  $S_1\sim S_4$  are always ON.  $S_{11}\sim S_{14}$  are always OFF. Based on the resonant inductance 1.5  $\mu\text{H}$  and resonant capacitance 132 nF, the resonant frequency  $f_r$  can be calculated according to (Eq.7.6).

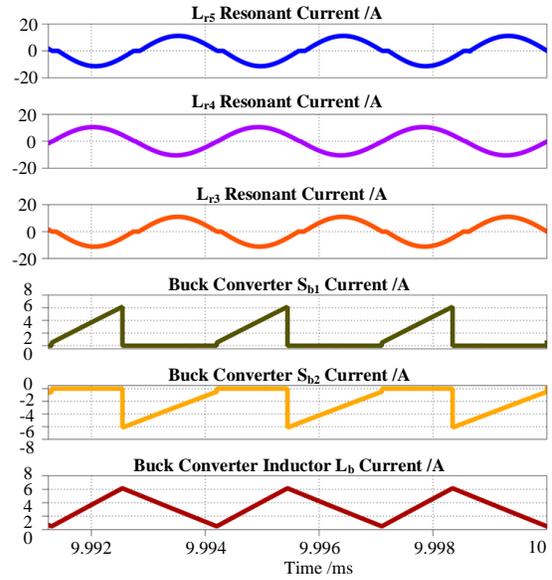
$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{1.5\mu\text{H} \times 132\text{nF}}} = 357.674\text{kHz} \quad (\text{Eq.7.6})$$

The switching frequency is fine-tuned as 353.77 kHz, which is slightly smaller than the resonant frequency.

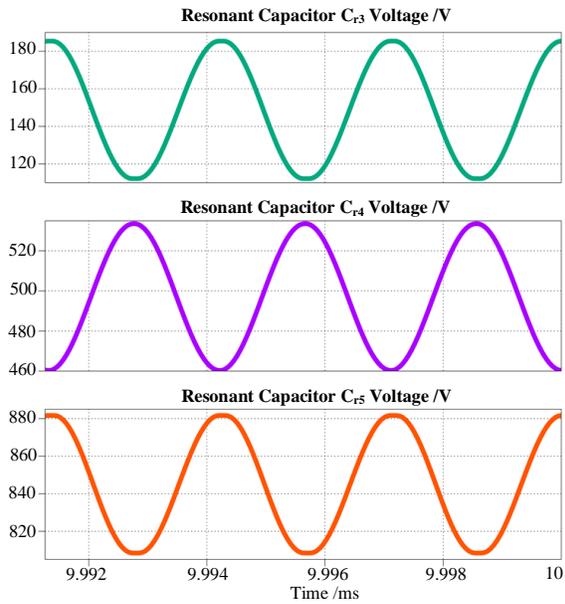
Figure 7.18 (a) shows the simulated current waveforms of the switches in the STC cells. Figure 7.18 (b) shows the resonant current waveforms, the buck converter switch current and inductor current waveforms. Figure 7.18 (c) shows the resonant capacitor output voltage waveforms. Figure 7.18 (d) shows the input voltage, STC output voltage, buck converter output voltage and the whole converter output voltage waveforms.



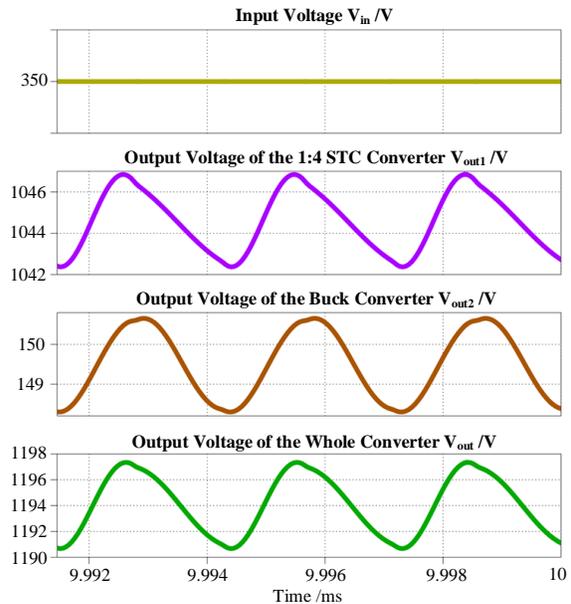
(a) STC switch current



(b) Resonant current, buck converter switch current and inductor current



(c) Resonant capacitor voltage



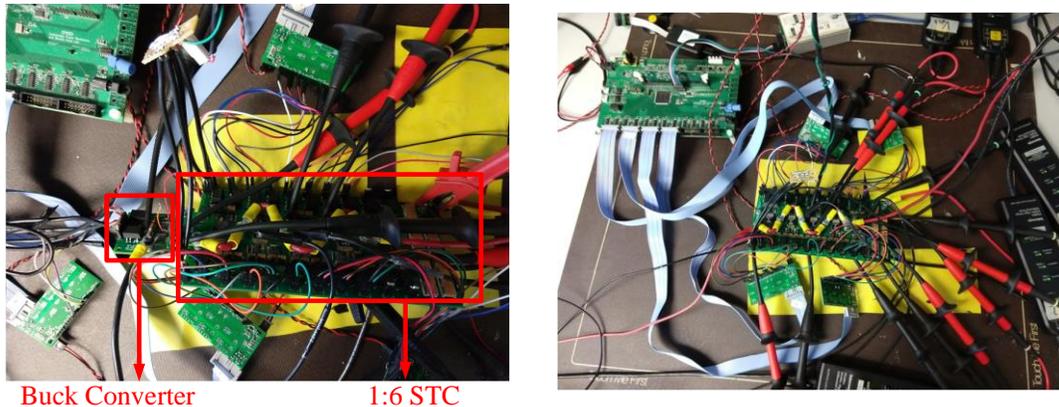
(d) Input, output voltage, buck converter output voltage waveforms

Figure 7.18. Simulation results of 350-V-to-1200-V 4-kW STC with PPVR

## 7.5. Prototype, Test Platform, and Experiment Results

Figure 7.19 presents the tested 1 : 6 STC and the PPVR buck converter. The control boards are included in the Figure 7.19 (b). The overall test platform is shown in Figure 7.20. It is mainly

composed of the tested regulated DC-to-DC converter, control boards, main power supply, auxiliary power supplies, and the wire-wound resistor loads. Although many TE<sup>®</sup> TE2500B470RJ resistors have been shown in the platform, only three of them have been used to be connected in series. By doing this, the total resistance is three times 470  $\Omega$ , which is 1410  $\Omega$ . The maximum power they can sustain is three times 2.5 kW, which is 7.5 kW.



Buck Converter

1:6 STC

(a) Tested STC with buck converter

(b) Tested regulated converter and control boards

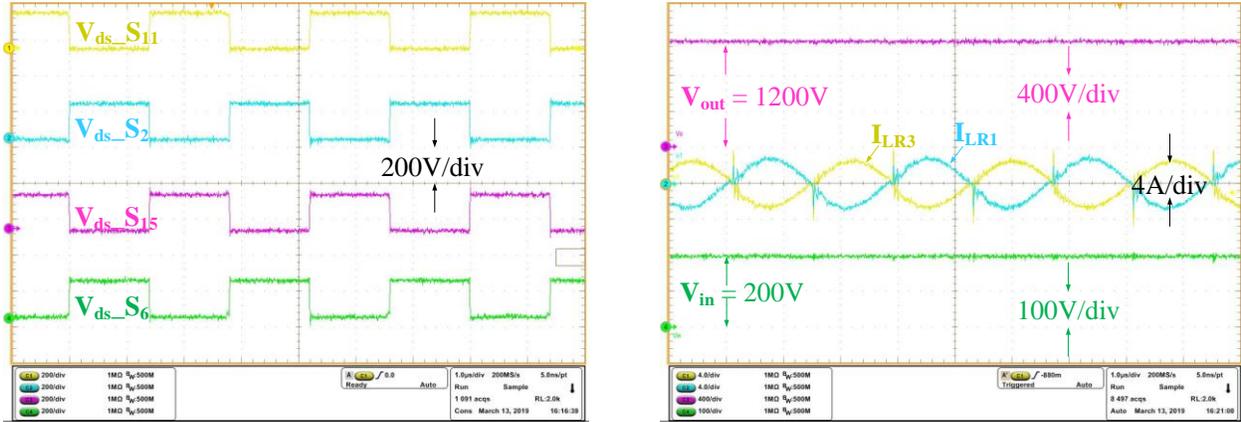
Figure 7.19. Tested prototype and control boards



Figure 7.20. The 200 V – 1200 V 1 kW overall test platform

The testing results of 200-V-to-1200-V 1-kW STC are illustrated in Figure 7.21. The testing circuit is based on Figure 7.7, where the buck converter is bypassed. According to Figure 7.21 (a), the device drain-source voltage clamping has been verified from the four presented  $V_{DS}$  waveforms. From input and output voltage waveforms in Figure 7.21 (b), voltage conversion ratio

is verified. The resonant current in the two modules  $I_{LR1}$  and  $I_{LR3}$  are verified to match the corresponding simulation results.



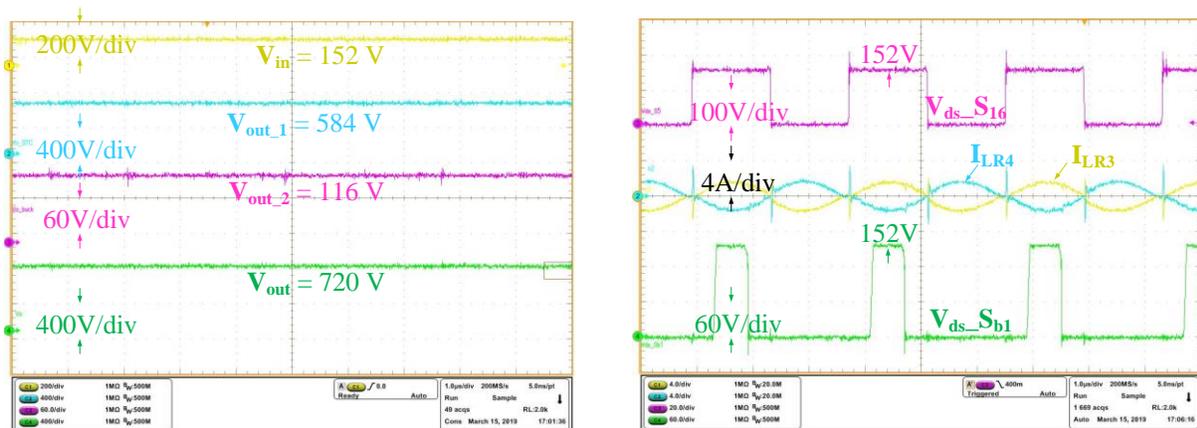
(a) Drain-source voltages of STC switches

(b) Input, output voltage, and resonant current

Figure 7.21. The testing waveforms of 200-V-to-1200-V 1-kW STC

The combination tests including both the STC and buck converter are conducted with 150-V input, 720-V output, and 368-W operated power.

Figure 7.22 shows the testing results. The testing circuit is also associated to Figure 7.7, where the most top STC cell is bypassed. Through this 1 : 4.8 testing, the voltage regulation function has been verified.



(a) Input and output voltages

(b) Switch  $V_{ds}$  of STC and buck converter, resonant current

Figure 7.22. The testing waveforms of 1:4.8 368-W STC with PPVR

## 7.6. Summary for This Chapter

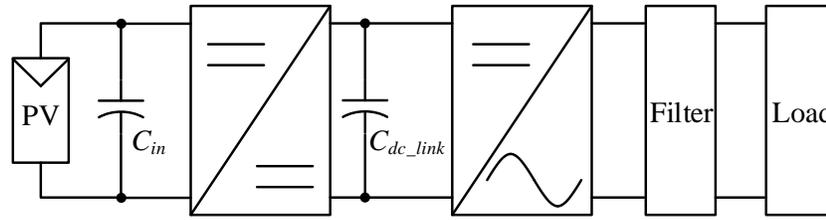
In summary, this chapter has combined the generalized STC topology with a buck converter for the PPVR for the step-up DC-to-DC converters with continuously adjustable conversion ratio. The TSLI has been utilized to evaluate the relationship between device power loss and total die area. With this index, the impact of different operated output power, switching frequency, and conversion ratio on the total device power loss has been analyzed. The proposed regulated converter achieves better die size utilization compared with boost converter under the same device power loss. In other words, the proposed one realizes smaller device power loss compared with boost converter when the semiconductor die area is the same. The modularized design and soft-switching operation make it possible to achieve high power density and high efficiency, so that the advantages of the WBG devices can be fully leveraged. Analysis has shown the overall full-load efficiency of designed 4-kW converter is 97.71%. A 4-kW prototype integrating a 1:6 STC and a buck converter stage has been built to justify the theoretical analysis. Both the simulation and test results have verified the validity of the proposed topology.

## **8. GAN BASED MULTILEVEL BOOST INVERTERS DERIVED FROM STC**

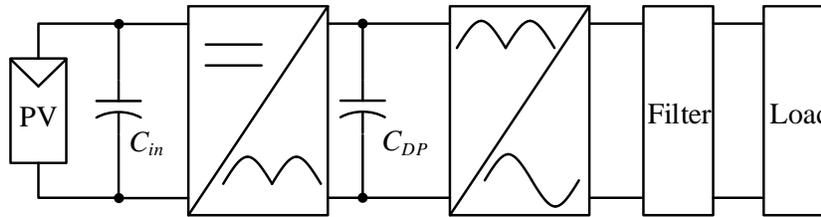
Based on the proposed generalized STC structure with PPVR in Figure 7.6 from last chapter, the DC-to-AC inverters can be further derived to leverage the benefits of the WBG devices. This chapter will propose two corresponding inverter topologies with high conversion ratio. They are especially suitable for the Photovoltaic (PV) inverter applications. First, the research background and challenges will be introduced. After that, the principles and control approaches for the proposed inverter topologies will be analyzed in detail. The simulation and testing results based on GaN devices will be followed to verify the design. Finally, a summary will be presented for this chapter.

### **8.1. Research Background of Applying the STC-Derived Topologies into PV Inverters**

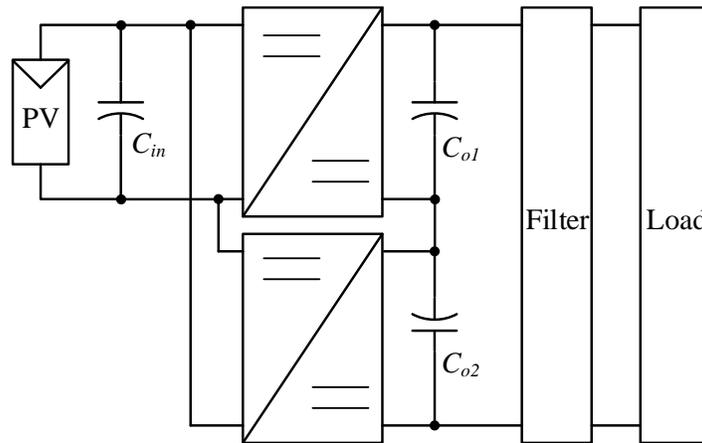
In low-power low-voltage grid-connected applications, since no mandatory isolation is required in most countries [499], transformerless PV inverters are preferred due to higher efficiency, lower cost and smaller volume [499]–[501] compared with isolated topologies. Figure 8.1 shows three types of step-up transformerless PV inverter topologies. However, in this type of structures, when the PV panel frame grounding is necessary, inherent parasitic capacitance exists between the PV panels and ground [502]. Due to the inverter high-frequency switching, the common-mode potential difference is formed on this parasitic capacitance [503][504]. As a result, the capacitive leakage ground current is injected into the circuit and causes electromagnetic interference, unexpected power loss and output power quality deterioration [505]. To solve this challenge, dc-link capacitor midpoint can be connected to the neutral point of load [506]. Another common alternative is to disconnect the PV panel and the load by using bidirectional switches on the inverter dc side [507] or ac side [504][508].



(a) Single-phase two-stage PV inverter



(b) Single-phase pseudo-DC-link PV inverter



(c) Single-phase single-stage PV inverter (Differential mode as an example)

Figure 8.1. Three types of step-up transformerless PV inverter topologies

Another challenge in single-phase transformerless PV inverters is to find a high-efficiency, compact-size topology with high voltage conversion ratio and easily-realizable control. Multilevel inverters are prospective candidates due to lower output voltage and input current distortion [509][510], smaller volume [510] and more balanced voltage sharing among active switches [510][511] compared with two-level inverters.

These days, switched capacitor multilevel converters and inverters have been well researched due to the modular structure, possible ZCS [512][513] and ZVS [437] soft switching, high voltage conversion ratio [514], high power density [515]–[517] and high efficiency [492]. A modular DC-to-DC switched capacitor boost converter cascaded with a full-bridge inverter is proposed in [518]. But big electrolyte capacitors, MOSFETs, diodes and output filtering inductor worsen both the overall efficiency and power density. A flying-capacitor-clamped five-level inverter is analyzed in [519]. However, the flying capacitor and output filtering inductor are bulky. The capacitor voltage balancing method increases the control complexity. Basically, these topologies tend to use large AC-side inductors to make the staircase waveform closer to sinusoidal. The semiconductor chip die sizes are also relatively big. Therefore, both the power density and chip die utilization are not optimized.

More challenges exist for the single-phase PV inverters such as the widely studied power decoupling methods [331], [332], [520]–[524] and the reliability related lifetime prediction [339]. But they will not be addressed here. In this project, two new resonant multilevel modular boost inverters based on a resonant switched capacitor topology are proposed. Different from unipolar SPWM in [525], a constant duty cycle control in the switched capacitor converter switches is applied without using extreme values of duty cycle. The voltage stress of all the switches in the resonant switched capacitor cells of the proposed inverter is equal to the input voltage. With a small clamp capacitor, the transient voltage spike of wing-side switches is alleviated. Compared with other switched capacitor inverters [518][519], zero level is not necessary in this topology because of the voltage regulation of the partial-power processing circuit. Small inductance in the partial-power processing circuit makes it unnecessary to use a bulky filtering inductive component on the AC output side. This is an impressive improvement when compared with other multilevel

boost inverter topologies where large inductors are always essential, such as the multilevel dc-link inverter [510], the flying capacitor inverter [519], the switched capacitor inverter [525], and the differential-mode switched capacitor boost inverter [526]. By taking advantage of the resonance among the resonant inductors and resonant capacitors, soft switching can be realized and thus the switching loss is decreased, which could increase overall efficiency. This resonant multilevel modular boost inverter is especially useful in non-isolated applications with low input voltage, high input current and high voltage conversion ratio. Further through the common-mode voltage and ground leakage current analysis, it is a promising candidate for the single-phase transformerless PV inverter applications.

Based on the proposed STC with partial-power processing, the operation principle of the topology cascading a resonant switched capacitor multilevel modular boost converter with a full-bridge inverter will be analyzed in Part 8.2. The common-mode voltage and ground leakage current analysis will be demonstrated. Based on the same resonant switched capacitor cells, another derived topology including dual differential-mode boost converters will also be discussed in Part 8.3. The PLECS simulation and testing results will be given to verify the validity of these two topologies in Part 8.4. Besides, the comparison of total normalized conduction power stress, total normalized switch stress ratio and relative total semiconductor chip area will be made. The test prototype, overall platform and some preliminary test results will be shown as well. Finally, the conclusion and future work will be described in Part 8.5.

## **8.2. Working Principle of the Resonant Multilevel Modular Boost Inverter with an Unfolder**

Figure 8. presents a generalized resonant multilevel modular boost inverter with an unfold, which is based on the resonant switched capacitor cell with voltage clamping, as

highlighted in the green shaded box. In each resonant switched capacitor cell, there are four same switching devices ( $Q_{bi}$ ,  $Q_{bi}'$  – bridge-side switches,  $Q_{wi}$ ,  $Q_{wi}'$  – wing-side switches), one clamp capacitor ( $C_{ci}$ ), one resonant capacitor ( $C_{ri}$ ) and one resonant inductor ( $L_{ri}$ ). To realize the voltage regulation without full power processing, a buck converter is placed between the first cell and the input voltage source, as shown in the light blue shaded box.  $Q_B$ ,  $Q_B'$  are the buck converter switches.  $L_B$ ,  $C_B$  are buck converter inductor and output capacitor, respectively. By processing partial-power, it decreases the volume of both the device wafer and heatsink. The inductor size in this topology can be decreased obviously compared with the AC-side inductors in other multilevel boost inverters. All the switches  $Q_{bi}$ ,  $Q_{bi}'$ ,  $Q_{wi}$ ,  $Q_{wi}'$  in the resonant switched capacitor cells work at the switching frequency slightly smaller than the resonant frequency so that the ZCS can be achieved. The drain-source voltage clamping of these switches is realized by the decoupling capacitor  $C_{dec}$ . The duty cycles of these switches are equal to 0.5. The four switches  $S_1 \sim S_4$  in the full-bridge inverter operates at 60 Hz line frequency.

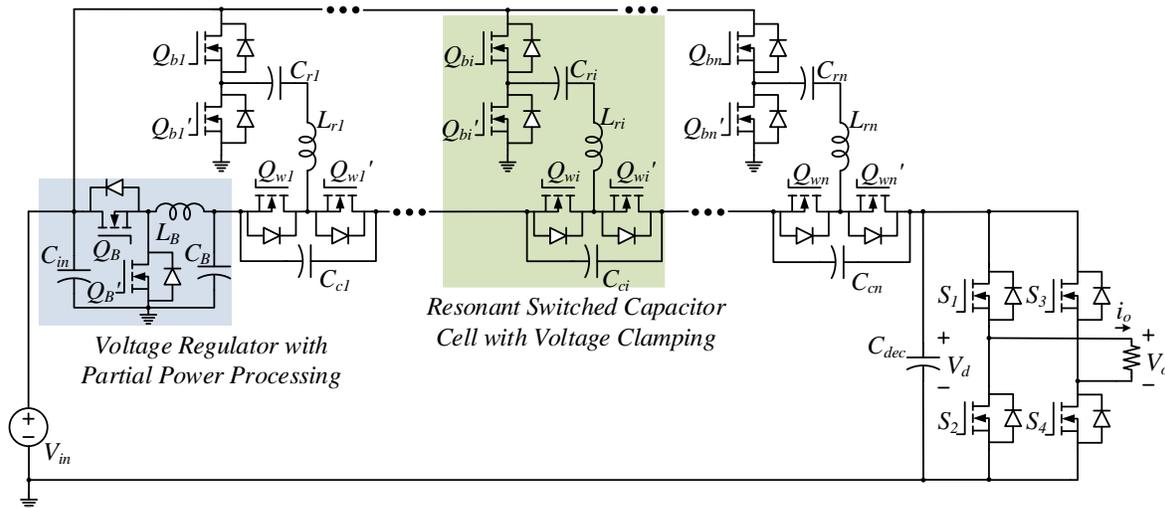


Figure 8.2. Proposed resonant multilevel modular boost inverter with a full-bridge inverter

Although the neutral point of the inverter output is floating to the DC-side ground, the changing frequency of its potential to the DC ground is the line frequency rather than the high

switching frequency. Therefore, the ground leakage current is relatively small with this configuration, which decreases the common-mode EMI effect.

To explain operation principles of the proposed resonant multilevel modular boost inverters, three switched capacitor cells are used. The control logic is presented in Figure 8.3.

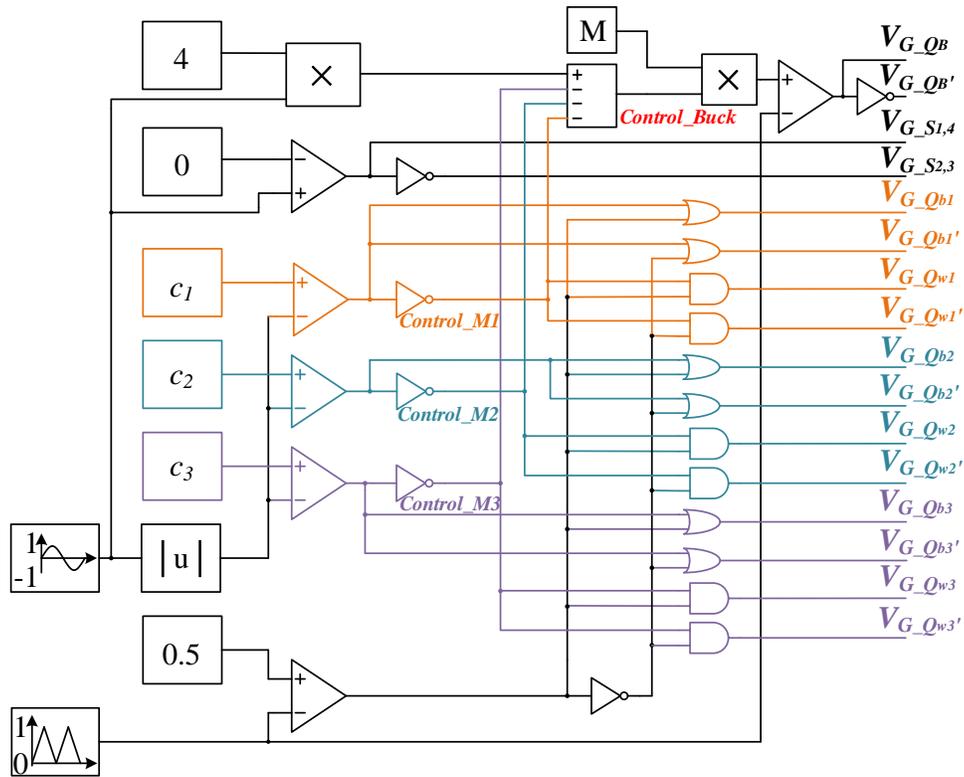


Figure 8.3. Control logic of the resonant 8-level modular boost inverter with an unfold

The key control signals are further illustrated in Figure 8.4. The switches  $Q_B$ ,  $Q_B'$  in the buck converter voltage regulator are controlled with the modulation waveforms shown as *Control\_Buck*. There are 4 steps in the DC staircase waveform. The Fourier series of an  $n$ -step staircase waveform [527] is given in (Eq.8.1).

$$V(\omega t) = \frac{4V_{in}}{\pi} \sum_{k=1,3,5,\dots} \left\{ \left[ \cos(k\theta_1) + \cos(k\theta_2) + \dots + \cos(k\theta_n) \right] \cdot \frac{\sin(k\omega t)}{k} \right\} \quad (\text{Eq.8.1})$$

where,  $n$  is the number of steps, i.e. 4 in this case. This equation has been applied to select the proper commuting angles  $\theta_1$ ,  $\theta_2$ , and  $\theta_3$  so that the specific harmonics can be eliminated.

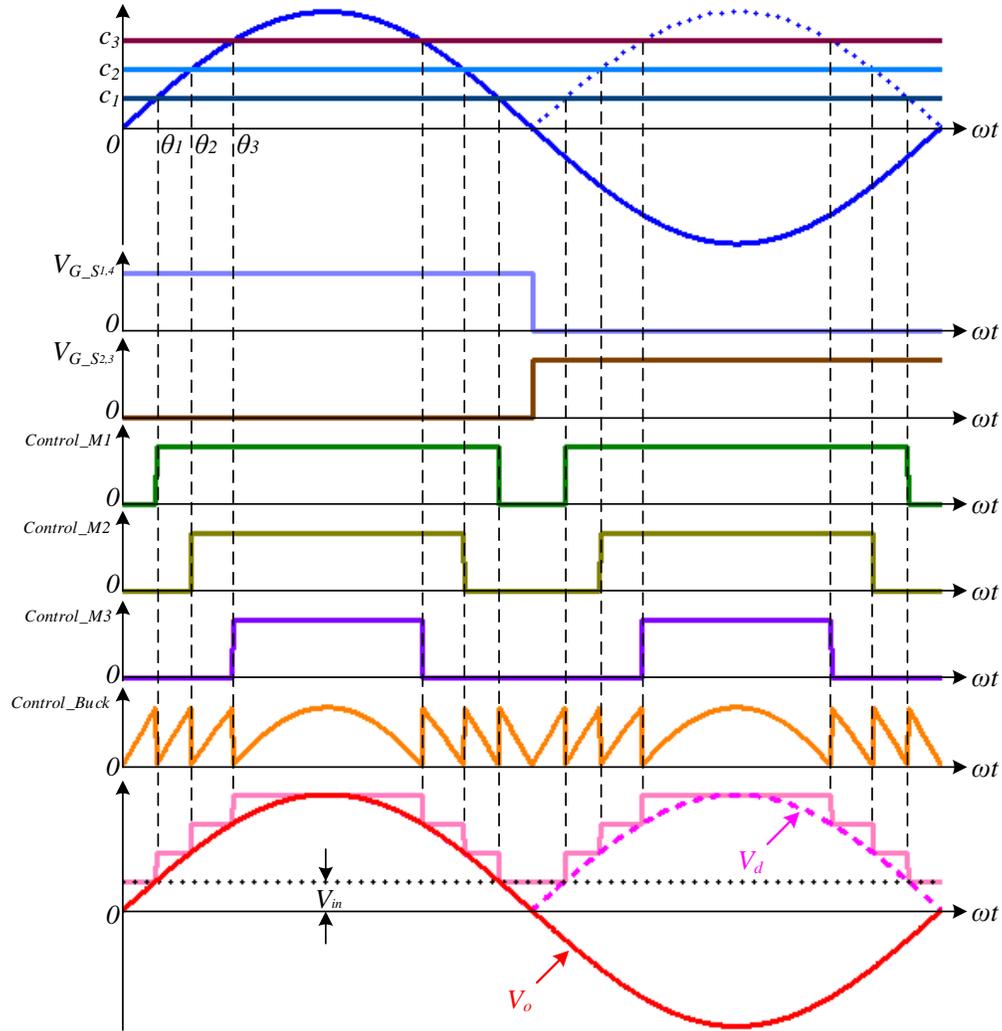


Figure 8.4. Control waveforms of the resonant 8-level modular boost inverter with an unfolded

### 8.3. Working Principle of the Differential-Mode Resonant Multilevel Modular Boost Inverter

The differential-mode resonant multilevel modular boost inverter also based on the resonant switched capacitor cell is shown in Figure 8.5. One significant difficulty in the differential-mode inverters is how to avoid the output capacitors of the two DC-to-DC converters



voltage peak value is 384 V. To make this inverter adaptable to the 240 V RMS AC output voltage requirement, the modulation index  $M$  is calculated in (Eq.8.2).

$$M = \sqrt{2} \times \frac{240}{384} = 0.88388 \quad (\text{Eq.8.2})$$

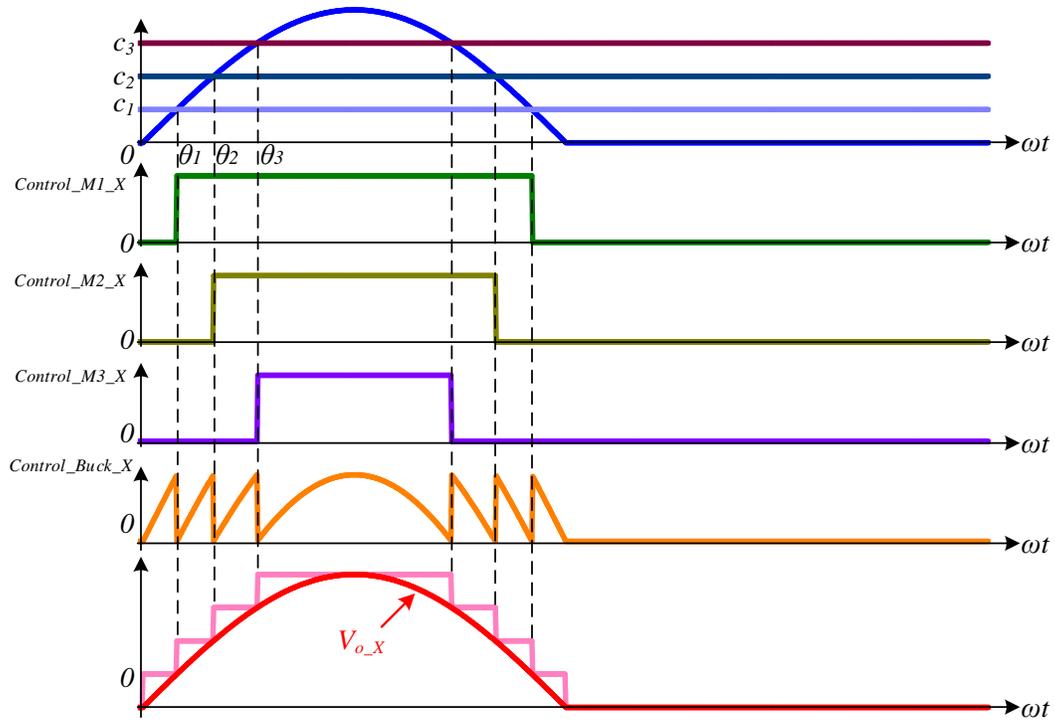
#### 8.4.1. Simulation and Analysis

The simulation is conducted in PLECS. Input voltage is 48 V. Resistive load has 17.56  $\Omega$  resistance. The buck converter inductance is 5  $\mu\text{H}$ .

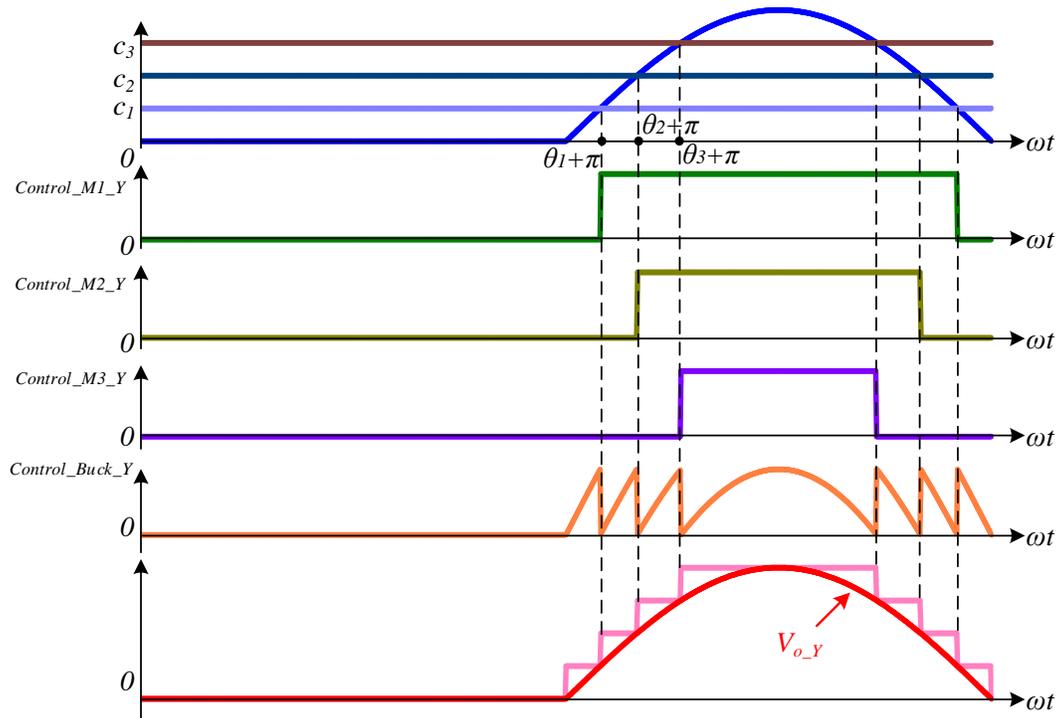
For the 4-kW resonant 16-level modular boost inverter with a full-bridge unfolded, the corresponding simulation results are shown in Figure 8.7.

The top five waveforms in Figure 8.7 are the buck converter control reference signal  $V_{ref}$ , the buck converter output voltage  $V_{o\_buck}$ , the decoupling capacitor voltage before the unfolded  $V_d$ , the input voltage  $V_{in}$ , the AC voltage after the unfolded  $V_o$ , and the current of the unfolded switches  $I_{S1} \sim I_{S4}$ , respectively. The bottom two waveforms show the current of switches in the resonant cells  $I_{sw}$  and the current of the buck converter switches  $I_{QB}, I_{QB}'$  at the 8X-level output voltage plateau.

For the differential-mode switched capacitor inverter, the simulation results are shown in Figure 8.8. The top six waveforms are buck converter control reference signals  $V_{ref1}, V_{ref2}$ , buck converter output voltages  $V_{o\_buck1}, V_{o\_buck2}$ , two converter output voltages  $V_{o\_X}, V_{o\_Y}$ , inverter input voltage  $V_{in}$ , and output voltage  $V_o$ , respectively. The bottom two waveforms are the current of switches in the resonant cells  $I_{sw\_X}$  and current of buck converter switches  $I_{QB\_X}, I_{QB\_X}'$  at the 8X-level output voltage plateau. These current waveforms are from Converter X. The corresponding Converter Y current waveforms have the same shapes but with half the line period delay.



(a) Control waveforms for Converter X of the differential-mode inverter



(b) Control waveforms for Converter Y of the differential-mode inverter

Figure 8.6. Control waveforms of the differential-mode resonant 8-level modular boost inverter

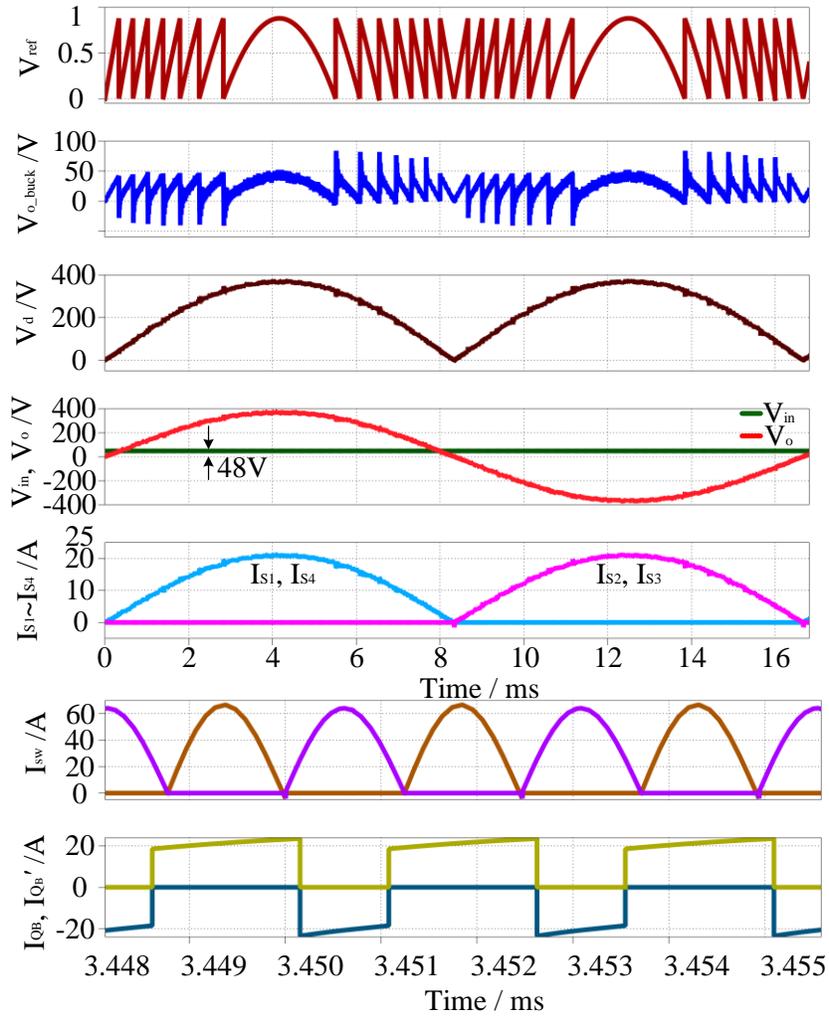


Figure 8.7. Simulation results of the resonant 16-level modular boost inverter with an unfolded

### 8.4.2. Actual Simulation, Prototype and Test Results

To experimentally verify the proposed resonant multilevel modular boost inverter with an unfolded, two switched capacitor modules and one full-bridge inverter are applied. The preliminary testing results without the partial-power voltage regulator will be presented in the following. To be consistent with the testing waveforms, the simulation of a resonant 6-level modular boost inverter with a full-bridge unfolded is carried out to see whether the theoretical analysis and tested

waveforms match or not. The schematic corresponding to both this actual simulation and the following tests is shown in Figure 8.9.

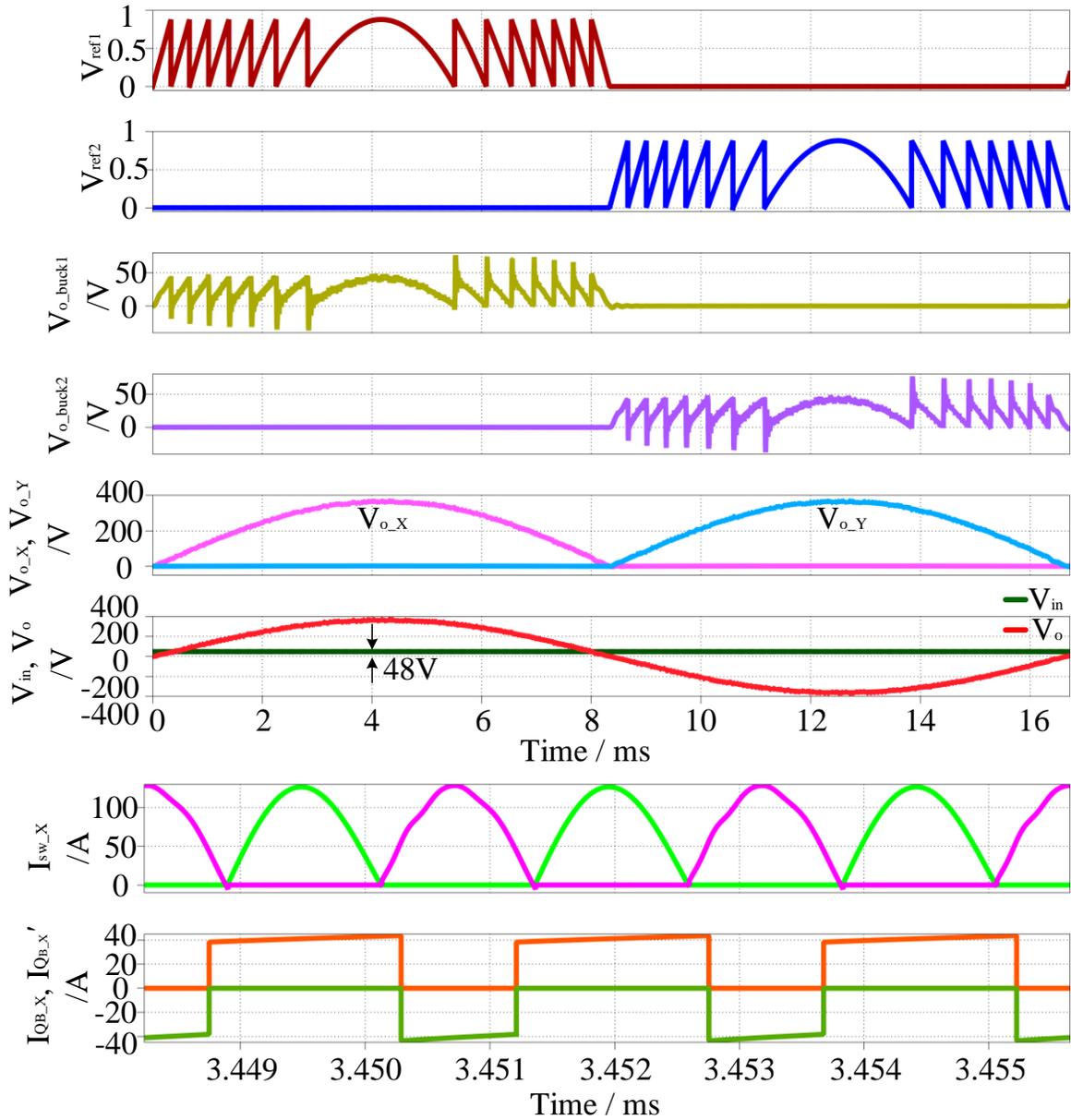


Figure 8.8. Simulation results of the resonant 16-level differential-mode boost inverter

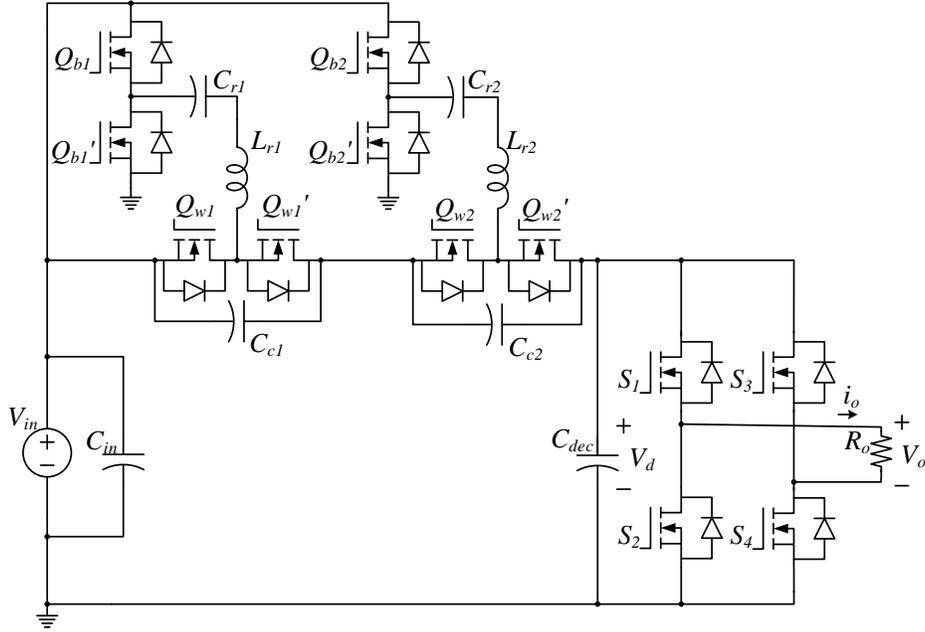
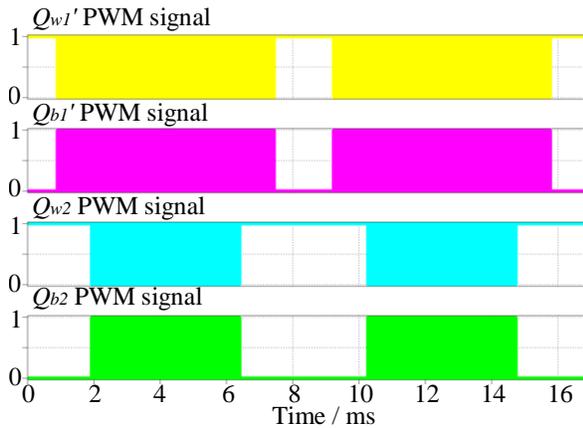
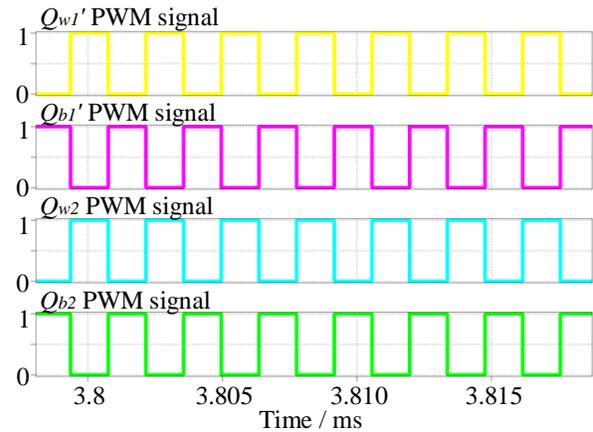


Figure 8.9. The tested 6-level boost inverter prototype schematic

Simulation with 35-V input voltage has been conducted in PLECS. Figure 8.10 (a) presents the control signals of STC switches. The top two show the complementary PWM signal waveforms of  $Q_{w1}'$  and  $Q_{b1}'$  in the switched capacitor cell close to the dc power source side. The bottom two waveforms are corresponding to  $Q_{w2}$  and  $Q_{b2}$  in the switched capacitor cell close to the load side. The enlarged control signals are further illustrated in Figure 8.10 (b).



(a) PWM signals of the switches in STC cells



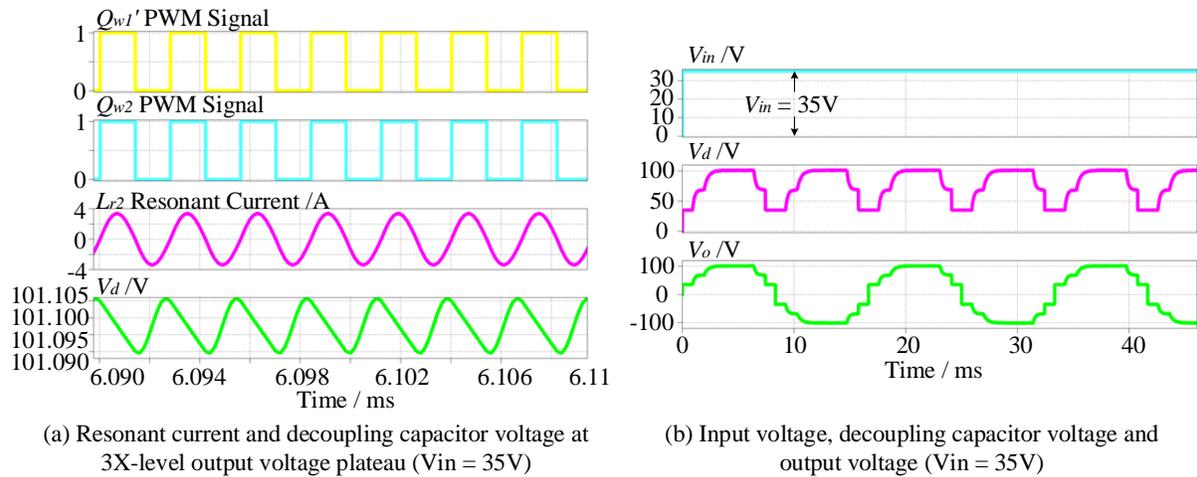
(b) Enlarged PWM signals of the switches in STC cells

Figure 8.10. Control signal waveforms in the simulation

Besides, the resonant current and decoupling capacitor voltage are observed together with two PWM signals in Figure 8.11 (a). These waveforms are corresponding to the 3X-level output voltage plateau. To conveniently analyze the voltage conversion ratio, the input voltage, the decoupling capacitor voltage, and the output voltage are placed in one scope as Figure 8.11 (b) shows. Figure 8.11 (c) further captures three PWM signals from two switched capacitor cells, the full-bridge unfolded, and the output voltage. From the timing relationship, the proposed control method is verified and can be further adopted in the following experiments.

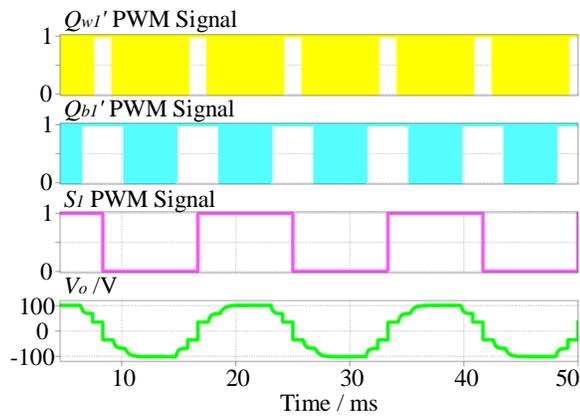
The overall test platform is presented in Figure 8.12, where ①, ②, ③, ④ refer to oscilloscopes, 5 V power supply, main power supply, and computer, respectively.

The bird's-eye view of the test platform is shown in Figure 8.13, where ⑤ is DSP and FPGA control board, ⑥ are opto-receiver interface control boards, ⑦ is the designed resonant multilevel modular boost converter, ⑧ is the full-bridge unfolded, ⑨ is the bleeder resistor (Micron<sup>®</sup> 35.3 k $\Omega$ , 20 W), ⑩ is the 94  $\Omega$  resistive load. The PWM signals are generated by the control board including TI<sup>®</sup> DSP 28335 IC and Xilinx<sup>®</sup> FPGA Spartan-6 XC6SLX9 IC. Five small opto-receiver interface boards are applied to be connected with four resonant switched capacitor cells and a full-bridge unfolded to generate complementary PWM signals for each of them. The switching frequency is set to be close to the resonant frequency. Here, 357.1 kHz switching frequency has been used. The deadtime is 60.003 ns for the five groups of PWM signals. In the main power circuit, a 35.3 k $\Omega$ , 20 W bleeder resistor is paralleled to the decoupling capacitor so that the stored capacitive energy is safely released when all the unfolded switches are OFF. In the measurement, all the voltages are captured by active differential probes. The resonant current is measured by PEM Rogowski current waveform transducer CWTUM/03/B with the sensitivity 100 mV/A and the peak current 60 A.



(a) Resonant current and decoupling capacitor voltage at 3X-level output voltage plateau ( $V_{in} = 35V$ )

(b) Input voltage, decoupling capacitor voltage and output voltage ( $V_{in} = 35V$ )



(c) Output voltage of the unfold ( $V_{in} = 35V$ )

Figure 8.11. Current and voltage waveforms in the simulation with 35-V input voltage

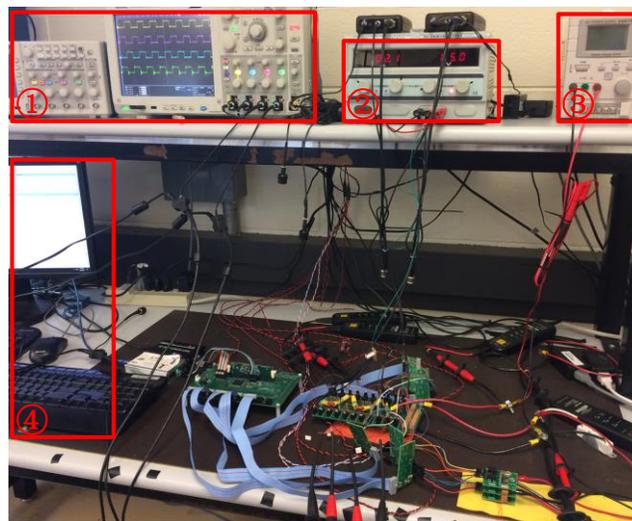


Figure 8.12. Overall perspective of the test platform

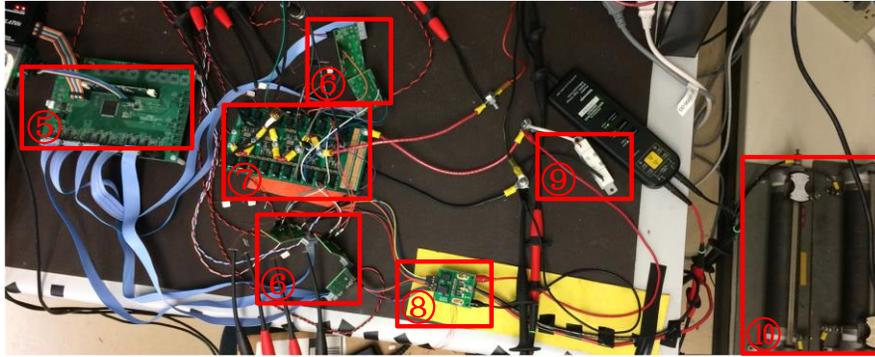


Figure 8.13. Bird's-eye view of the test platform

Figure 8.14 (a) and (b) present the gate drive's gate resistor voltage waveforms, which are consistent with the simulated control strategies shown in Figure 8.10. Silicon Labs SI8271GB-IS isolated gate driver IC is selected. As can be seen from the figures, the gate drive output voltage amplitude is around 9 V. Figure 8.15 (a) gives the resonant current waveform in the switched capacitor cell close to load side. These waveforms are captured at the 3X-level output voltage plateau, which is around 105 V. The resonant current amplitude is about 6 A, which matches the simulation result in Figure 8.11 (a). Three tested voltage waveforms i.e. the input voltage, the decoupling capacitor voltage and output AC voltage are captured in Figure 8.15 (b). Furthermore,

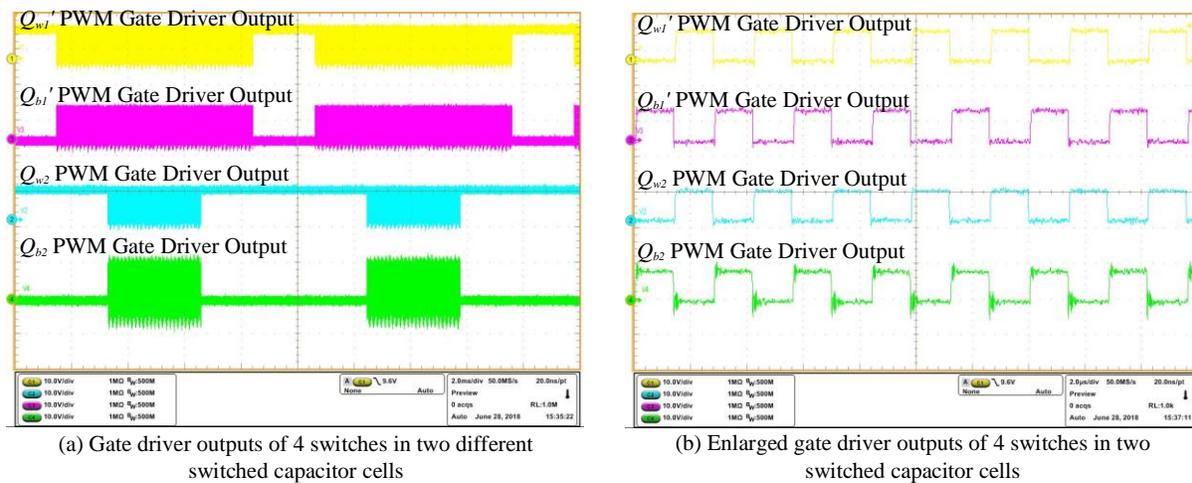
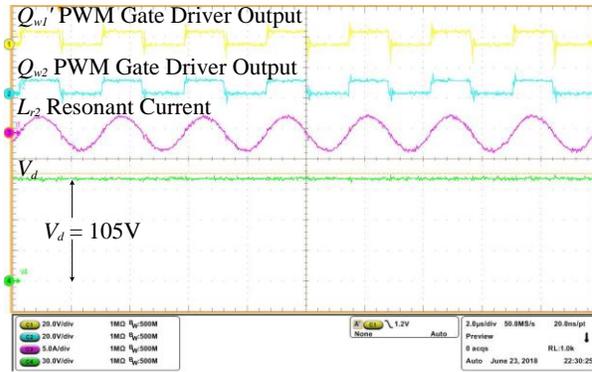
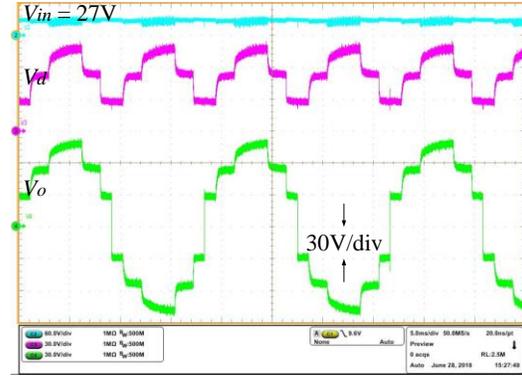


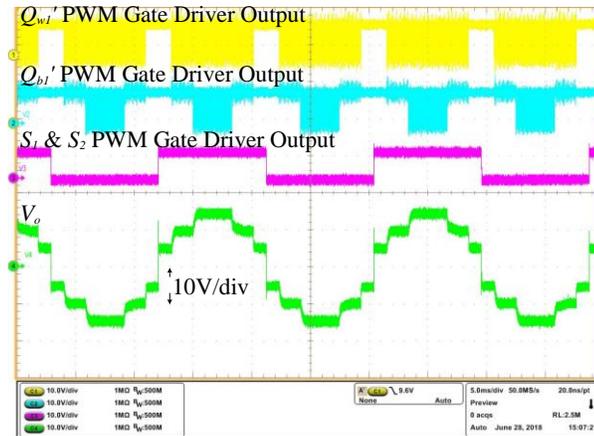
Figure 8.14. Tested control signals of the STC switches



(a) Tested resonant current and decoupling capacitor voltage in relation to two PWM signals at 3X-level output voltage plateau ( $V_{in} = 35V$ )



(b) Tested input voltage, decoupling capacitor voltage and output voltage ( $V_{in} = 27V$ )



(c) Tested output voltage in relation to PWM signals of two switched capacitor cells and the full-bridge unfolded ( $V_{in} = 5V$ )

Figure 8.15. Tested current and voltage results

in Figure 8.15 (c), the timing relationship between output voltage and three gate drive PWM outputs verifies the simulation results in Figure 8.11 (c).

### 8.5. Summary for This Chapter

This chapter has proposed two non-isolated resonant multilevel modular boost inverter topologies based on resonant switched capacitor cells and a partial-power processed buck converter. The operation principles and control strategies of the resonant multilevel modular boost inverters operating with an unfolded and in differential mode have both been illustrated, respectively. PLECS simulation results show the validity of the boost DC-to-AC function in both

the two topologies. They are especially suitable for the single-phase non-isolated photovoltaic applications with low input voltage, high input current, high voltage transfer ratio and small ground leakage current. From the simulation results, a significant decrease of the inductance in the buck converter voltage regulator has been verified compared with the normally used large AC-side filtering inductance. Test results show the validity of the boost inverter function when relatively simple control strategies are implemented.

## 9. CONCLUSION AND RECOMMENDATION

This dissertation has been focused on the wide band-gap semiconductor devices and has tried to get a fundamental understanding in terms of their reliability and well-suited topologies. Two major parts have been integrated in this research. The reliability study serves as a device-level theoretical preparation for the topology investigation. The suitable topologies can be designed to adaptable to the individual WBG device characteristics. Also, the topological analysis and specific application consideration in turn demonstrate the advantages of the WBG devices.

From the perspective of the device reliability, the lifetime modeling and condition monitoring strategies have been studied and verified through tests. First, since the lifetime research in the WBG devices is a relatively new direction, a comprehensive literature review has been conducted regarding both their lifetime prediction and extension. By online updating the ALT-based static lifetime model, the overall system lifetime estimation accuracy is improved. Second, the gate oxide degradation has been investigated based on its failure mechanisms of the WBG devices. Three health indicators have been tested and analyzed through ALT and verification tests. The threshold voltage has been concluded as the most obvious indicator for the SiC MOSFET gate oxide degradation, when either the  $V_{GS}$  stress or temperature stress is placed. As to the integration into the gate drives, the Miller plateau amplitude has been presented as a better realizable health indicator. Third, the junction temperature condition monitoring has been conducted for the medium voltage SiC MOSFETs. The turn-off voltage switching rate  $dV_{DS}/dt$ , the turn-off gate current peak  $I_{g(pk\_off)}$ , and the turn-on gate current plateau  $I_{g(p)}$  have been verified through tests to be able to achieve higher temperature coefficient in the medium-voltage, low-current SiC MOSFETs compared with those of the Si IGBTs. The turn-on gate current plateau  $I_{g(p)}$  has exhibited better thermal linearity for the SiC MOSFETs. The reason has been analyzed from the

physical mechanism perspective. Also, an evaluation of the condition monitoring circuits has been made for those investigated TSEPs.

From the perspective of the well-suited topology investigation, a generalized STC circuit has been proposed to be adaptable to the characteristics of the WBG devices. To evaluate the topologies by combining the chip die area design and the device power loss optimization, a novel index called TSLI has been introduced. Based on this topology and its derivatives, three applications have been considered and designed. First, a 100-kW DC-to-DC converter has been developed in detail to enable the compact and high-efficiency operation with desirable thermal performance. Thanks to the WBG device advantages that are leveraged in this topology, the assembled prototype main power circuit power density has been demonstrated as around 42 kW/L. Furthermore, The tested peak efficiency has been verified to be 98.7% at 30 kW. The tested 100 kW efficiency can achieve 97.35%. Second, by adding a partial-power-voltage-regulated buck converter into the original topology, a continuously-adjustable conversion ratio has been achieved in the electric vehicle DC-to-DC step-up power stage applications. The testing results have validated the 1 : 6 conversion ratio and voltage regulation function. Third, the derived DC-to-AC inverter circuit has been further explored based on the basic voltage-regulated STC cells. Compared with other multilevel inverters, this one enables much simpler control approaches when the boost DC-to-AC is realized. In both the second and third applications, the GaN based semiconductor devices have been applied. The high power density and high efficiency have been verified through the theoretical analysis and the results obtained from the designed test platform.

In conclusion, the emerging applications of the WBG semiconductor devices have brought in desirable advantages as well as design challenges. This research has explored the reliability analysis and has proposed the topologies that can be well suited to them. More opportunities can

be taken regarding the following aspects. The WBG system-level lifetime modeling methods can be developed in more detail with the combination of the emerging artificial intelligence algorithms. The health condition monitoring circuits can be further integrated into the smart gate drive, on either the circuit-board level or the chip level, so that the degradation and junction temperature can be monitored in real time when the system is in operation. Besides, further topological innovation can be conducted as the WBG devices are more and more widely studied. With the WBG device voltage and current ratings increased, the package-level and chip-level reliability performance improved, there would be extensively opened space for the well-suited topology investigation.

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