HIGH POWER DENSITY AND HIGH EFFICIENCY DC-DC CONVERTERS BASED ON WIDE BANDGAP SEMICONDUCTORS

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Title

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The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

DOCTOR OF PHILOSOPHY

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ABSTRACT

As the rapid development of semiconductor technologies, more and more power electronic devices are used in our daily life. The power converters are widely used in many emerging areas, such as renewable energy and clean electricity area, information technology (IT) area and transportation area. Due to the high power usage in all these areas, make the power converter highly efficient is becoming more important than ever. Also, high-density power converters are highly desired in more and more applications. Soft-switching technology is one of the key points that help us to achieve the goals. In this research work, a series of soft-switching power converters are presented and analyzed.

First, a modular multilevel converter (MMC) with zero-current switching capability is proposed. By using different control method, the converter can achieve different voltage conversion ratios. Another attractive feature of the proposed MMC is that it can fully utilize the parasitic inductance existed in the converter system.

Second, high power-density switched-capacitor converters start appearing in many emerging applications. On the one hand, the research proposed a multilevel switched-capacitor converter that is capable of zero-voltage switching (ZVS) and voltage regulation. On the other hand, a switched-tank converter with zero-current switching (ZCS) has been studied. Furthermore, adaptive control method has been proposed to solve the issues that are led by component tolerance during the mass production procedure. Besides, a comparison study of the two operation modes is performed. Also, a composite multilevel converter based on switched-capacitor concept has been developed for telecommunication application.

Finally, a 100kW switched-tank converter has been developed to validate that the high power- density and high-efficiency can be achieved by using the switched-capacitor concept.

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LIST OF ABBREVIATIONS

DC.....direct current.

AC.....alternating current.

PE.....power electronics.

PV .....photovoltaic.

EV .....electric vehicle.

SiC.....silicon carbide.

GaN.....gallium nitride.

PWM.....pulse width modulation.

PCB.....printed circuit board.

DSP .....digital signal processing.

MMSCC.....multilevel modular switched-capacitor.

ZCS .....zero current switching.

ZVS.....zero voltage switching.

kHz.....kilo hertz.

nH.....nano Henry.

uF .....micro Farad.

1. INTRODUCTION OF THIS RESEARCH WORK

As the rapid development wide bandgap semiconductor technology, the silicon carbide device and GaN device start to show their advantages because their high voltage blocking capability and fast switching capability. They have been widely used in a variety of applications. And their reliability has been intensively studied over the past years [1]–[16]. And they enable significant new capabilities on power electronics circuits, such as high power density and high-efficiency.

For the high step-up ratio DC-DC converters, the traditional multilevel have issues such as high switching loss and need complex control algorism to balance the voltage of each module. Therefore, a modular multilevel DC-DC converter is proposed in the chapter 1 to solve the all these issues.

For the datacenter bus converter, the commercial intermediate bus converter has bulky magnetic components, which sacrifices the efficiency and density of the converter. However, the isolation stage in the data center is not necessary. So, develop a magneticless dc-dc converter for the data center application would be meaningful, which is the work shown in cahpter 3. Based on chapter 3, the effects of the component tolerance have been studied in chapter 4. This is because all the parameters of the key components during the converter mass production will not be exactly the same. A new circuit configuration and control strategy is proposed to ensure the reliable operation of the switched-tank converter. Sine the switched-tank converter is optimized for zero-current switching, a switched-capacitor resonant converter that is capable of both zero-current switching and zero-voltage switching is studied. Chapter 5 provides detailed analysis and design procedures of the converter with zero-voltage switching operation. In chapter 6, the two operation modes, zero-current switching mode and zero-voltage switching mode is compared. Furthermore,

a design methodology is provided to show how to properly design the converter to leverage the advantages of the zero-voltage switching mode.

For the telecommunication application, an isolation stage in a bus converter is required in order to protect the server components from power spike that propagate from the front-end AC/DC converter, also voltage regulation is required on the converter. In order to achieve high efficiency and voltage regulation at the same time, the proper use of partial power processing concept becomes one of the key design points. Chapter 7 shows that the traditional converter architecture cannot fully utilize the advantage of the partial power processing concept. So, a new converter architecture has been proposed.

In chapter 8, the study shows that the switched-capacitor concept can be also used in high power applications, such as electrical vehicle. Because the one-phase converter has issues such as bulky input and output capacitors, a three-phase interleaved converter is proposed. Both zero-current switching operation mode and zero-voltage switching operation mode are studied. A very high-density and high-efficiency converter is proposed in this work.

2. A ZERO-CURRENT-SWITCHING HIGH CONVERSION RATIO MODULAR MULTILEVEL DC-DC CONVERTER

2.1. Introduction

With the development of MVDC technology, lots of the existing dc-dc power conversion system are built with ac power conversion technologies due to the easy voltage step-up and step-down feature of transform. However, MMC concept provides opportunities for dc-dc converter to be applied in MVDC system, such as electric ship power system and urban power distribution system. Therefore, modular multilevel dc-dc converter is becoming more and more popular in recent years.

In order to achieve high efficiency and high power density, many multilevel dc-dc converters without any magnetic components are proposed [17]–[20]. Besides, the utilizing of silicon carbide (SiC), gallium nitride (GaN) devices and smal passive components can also reduce the converter size as well as increasing its efficiency [21]–[23]. Although there are some advantages of these traditional multilevel dc-dc converters, their efficiency will drop significantly as their step-up ratio increases. This means their maximum conversion ratio is limited by the high power loss. Hence, they are not suitable for high voltage conversion ratio applications. On the other hand, multilevel modular capacitor clamped dc-dc converters (MMCCC) are proposed for high voltage conversion ratio purpose [24]–[29]. However, some of the MMCCC will face voltage balance problem because of its structure [17]. As a result, complex modeling and control will be introduced.

Other two emerging dc-dc power conversion technologies that can provide high voltage conversion ratio are switched-capacitor [30]–[34] and modular multilevel dual-active-bridge (MMDAB) [35], [36]. Among the switched-capacitor technologies, some of them utilizes stray

inductance to achieve ZCS operation. In this way, high voltage spike and high current spike on switching devices of conventional switched-capacitor circuit can be overcome. As a result, small size, low ESR ceramic or film capacitor can be used. This brings the benefits of high reliability, high power density and high efficiency. Different from switched-capacitor circuit, high frequency transformers are used in the MMDAB circuit, which will provide galvanic isolation between the primary side and secondary side.

Besides switched-capacitor and MMDAB topologies mentioned above, dc-dc power conversion using modular multilevel dc-dc converter are the most emerging technologies in medium and high voltage applications. For step-down purpose, a transformerless step-down dc-dc MMC is proposed [37]. This method uses capacitor to share a high voltage, then a low dc voltage can be obtained. For step-up purpose, some MMCs use capacitor clamped mechanism to generate a high voltage output [38]. In another case, two traditional MMC branches are used to generate two low dc voltage with inversed ac component. The two ac components will cancel out each other and leave the dc component only [39]. In some of the dc-dc converters, transformers are used to attain dc-dc conversion [40], [41]. However, in order to achieve high-efficiency, high power density and lightweight dc-dc converter, passive components such as bulky capacitors, transformers and inductors need to be avoided.

This work presents a novel method to generate high DC voltage by using low DC voltage source with the proposed MMC topology. The proposed converter has the following advantages:

1) Highly modular. This feature makes the converter can be easily modified by just adding or removing a submodule. The cost and difficulty of replacing a submodule can become low. With redundant submodules, the fault tolerance is becoming very high.

2) High conversion ratio. By using multiple submodule, a very high conversion ratio can be achieved. The more submodule one converter has, the higher conversion ratio it can be achieved.

3) Variable conversion ratio. With the same hardware configuration, not only maximum conversion ratio but also lower one can be achieved by changing the control method.

4) Phase-shift control. The converter uses Phase-shifted Pulse-Width Modulation (PWM) control, which is easy to be implemented.

5) Zero current switching (ZCS). Resonant makes it possible to let the converter work under ZCS mode.

6) Smaller passive components. Because only small inductance is needed, wire inductance can be utilized instead of using larger sized inductor. Unlike [38], [39], an additional inductor is required in the converter.

2.2. System Configuration of The Proposed Multilevel DC-DC Converter and Operation Principle

In this section, system architecture of the proposed converter and circuit structure of different submodules are given in the first part. Then the operation principle and control method will be demonstrated. At last, a set of in-depth analysis will be performed to show how to make this converter work under ZCS mode.

2.2.1. System Level Topology and Submodule

The system configuration of proposed converter is shown in Figure 2.1, which consists N series-connected low voltage submodules. Each of the submodules holds a low dc voltage to support the high dc voltage on the output side. The proposed series resonant version converter in

which the resonance is between the wire stray inductance and the capacitor distributed in each submodule is shown in the following analysis.

Figure 2.2 shows the circuit configuration of a full-bridge submodule used to build the converter. Similarly, Figure 2.3 shows the configuration of half-bridge submodule. In both full-bridge and half-bridge submodules, when devices Sp turn on, the $V_{sb\_i} = V_{ci} + V_{Lw}$. On the other hand, ESR is considered to estimate the overall efficiency of the system. According to Figure 2.3, if half-bridge submodules are used to build the converter, the capacitor is bypassed when one submodule is deactivated. However, the wire stray inductance still remains in the resonant loop. As a result, a different resonant frequency needs to be calculated in order to maintain ZCS operation. By using either of the submodules, ESL of the wires will be utilized, thus no inductors are needed in the converter.

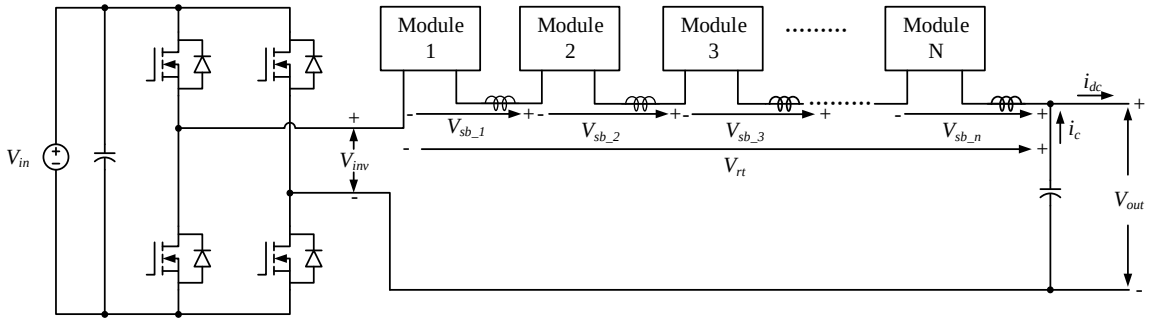

Figure 2.1. System level configuration of the proposed converter

2.2.2. Phase-shifted PWM Control of the Proposed Converter

The proposed converter with 6 half-bridge submodules is shown in Figure 2.4. Similarly, Figure 2.5 shows a 6 full-bridge submodule version of the proposed converter. In order to achieve high conversion ratio, only one submodule will be deactivated at a time, which means no more than one capacitor will be bypassed during the whole operation cycle. Figure 2.6 shows the phase-

shifted PWM signal used for the open loop control of the proposed converter. The PWM signals from submodule 1 to submodule 6 have been shifted by 0◦, 60◦, 120◦, 180◦, 240◦ and 300◦ respectively.

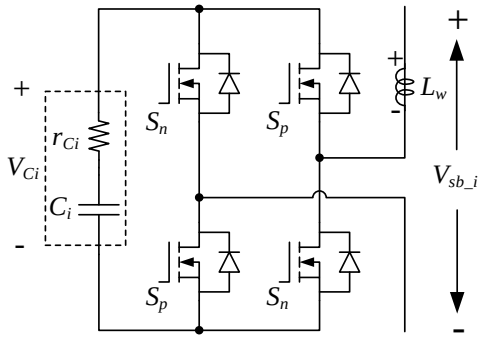

Figure 2.2. Circuit structure of full-bridge submodule

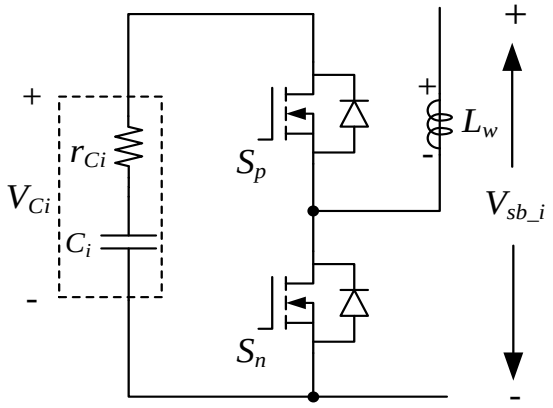

Figure 2.3. Circuit structure of half-bridge submodule

2.2.3. General Analysis and ZCS Resonant Operation

In this part, in order to demonstrate general operation principle, the proposed converter with 6 half-bridge submodules is used as an example. Figure 2.4 shows the example converter to be analyzed

The analysis of the modular multilevel DC-DC boost converter is based on the following assumptions:

1) The switching devices used in the converter are ideal.

2) The parameters of all components in each submodule are identical, which include C_i, r_{Ci}, L_w and parameters of switches.

3) No dead time is applied to the operation of this converter.

4) Voltage variation across the capacitors is neglected, which means $V_{Ci} = \overline{V_C}$.

When the converter is working under steady state, switching frequencies of all the submodule switches are the same. Average voltage stress of the i^{th} capacitor is $\overline{V_{Ci}}$ and voltage across submodules are V_{sb_i}. Also, i_{Qnt} and i_{bus} are used to denote the current flow through the n^{th} switch and DC bus respectively. It can be seen from Figure 2.4 and Figure 2.5, i_{out} is the output current of the inverter. Thus, the voltage across the resonant tank is $V_{rt} = \sum_{i=1}^{6} V_{sb\_i}$. The output voltage can be derived as $V_{out} = V_{inv} + \sum_{i=1}^{6} V_{sb\_i}$.

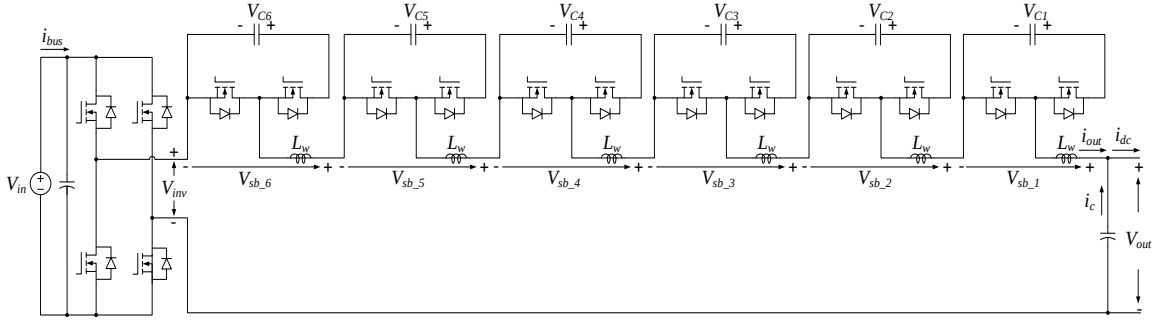

Figure 2.4. The proposed converter with six half-bridge submodules

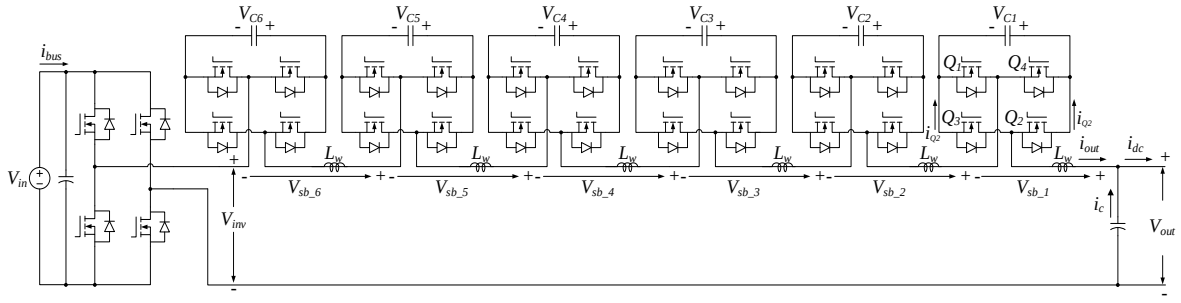

Figure 2.5. The proposed converter with six full-bridge submodules

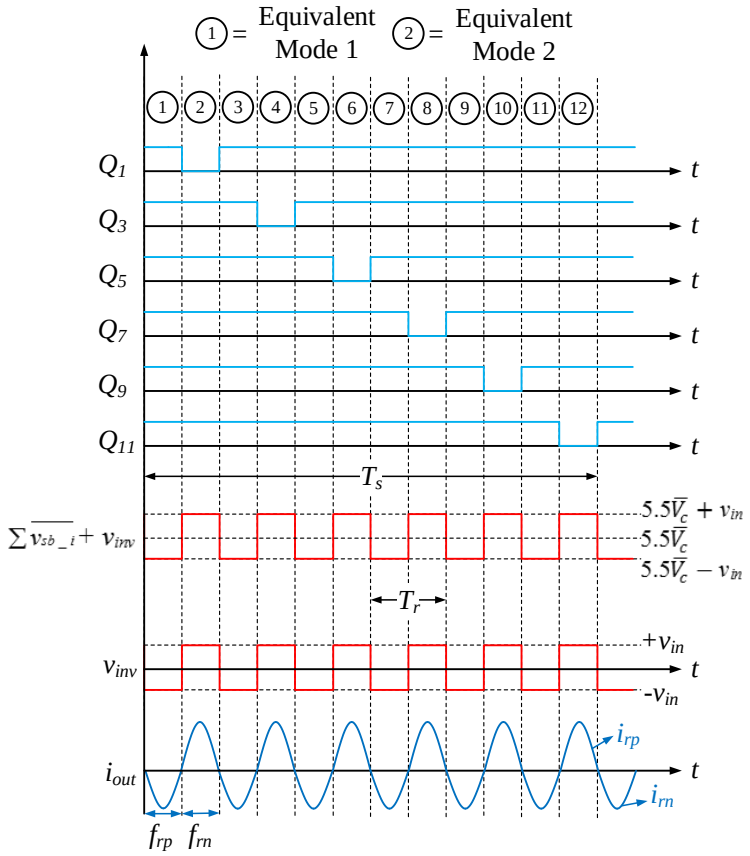

Figure 2.6. Phase-shifted PWM and voltage waveform for proposed converter with 6 half-bridge submodules

According to the assumptions above, average voltage across all the capacitors are assumed to be the same. Then the average voltage across each submodule should be 0 or $\overline{V_C}$. Referring to Figure 2.4, Figure 2.5 and Figure 2.6, there are 12 operating status in total during cycle T_s. However, every submodule has the same operation patterns, thus analysis for one submodule is enough to show how the converter works, which contains 2 operation modes, denoted as equivalent mode 1 and equivalent mode 2.

From Figure 2.7 and Figure 2.8, when the converter works in mode 1, all the upper devices in submodules are turned on. In this mode, one can get $V_{sb\_i} = V_{Ci} + V_{Lw}$ $(i = 1 \dots 6)$. Then the voltage across the resonant tank $V_{rt} = 6\overline{V_C} + 6V_{Lw}$. In general case with N submodules, the voltage relationship between V_{in} and V_{out} can be written as $V_{out} = V_{rt} - V_{in} = N * \overline{V_C} + N * V_{Lw} - V_{in}$.

When the converter works in mode 2, switch Q_1 kick out and Q_2 kick in, then the submodule containing capacitor C1 is deactivated. This means in mode 2, $\overline{V_{sb\_i}} = \overline{V_{Ci}} + \overline{V_{Lw}} = \overline{V_C}$ $(i = 1 \dots 5)$, while $\overline{V_{sb\_6}} = 0$. Then $V_{rt} = 5\overline{V_C}$. In general case with N submodules, the voltage relationship between V_{in} and V_{out} can be written as $V_{out} = V_{rt} + V_{in} = (N - 1)\overline{V_C} + V_{in} + V_{Lw}$. From previous analysis, because average voltage across an inductor operating in periodic steady state is zero, so the average output voltage can be derived as

$$\overline{V_{out}} = \frac{(2N-1) * \overline{V_C}}{2} \qquad \text{(Eq. 2.1)}$$

From Eq. 2.1, the average voltage generated on the output side is $5.5\overline{V_C}$ when $N = 6$, which means the dc offset generated by the resonant tank is $5.5\overline{V_C}$. Figure 2.6 shows the voltage relationship between $(V_{inv} + \sum V_{sb\_i})$, V_{inv} and $\overline{V_C}$. By repeating equivalent mode 1 and equivalent mode 2 for six submodules, there is always a resonance between the wire stray inductance and the capacitor distributed in each submodule, which makes it possible that the converter works under ZCS mode.

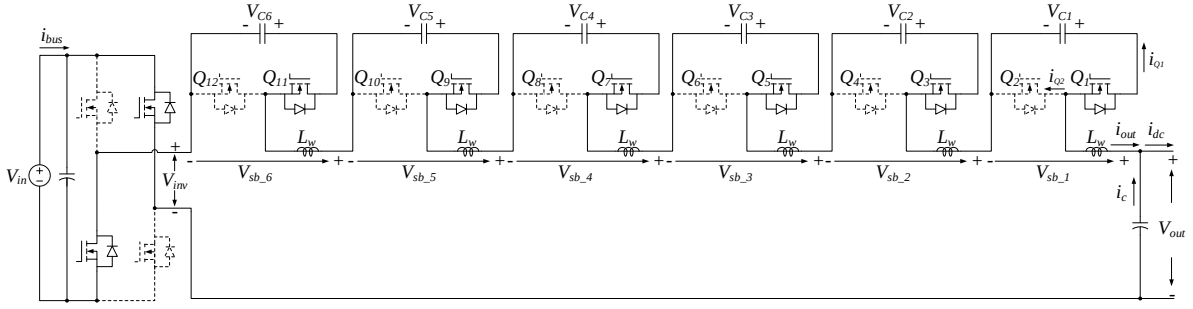

Figure 2.7. Equivalent mode 1

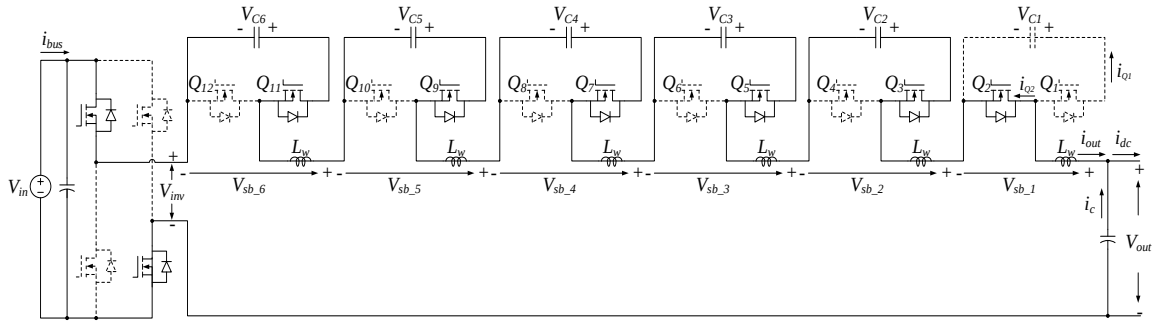

Figure 2.8. Equivalent mode 2

When the converter works in mode 2, switch Q_1 kick out and Q_2 kick in, then the submodule containing capacitor C1 is deactivated. This means in mode 2, $\overline{V_{sb\_1}} = \overline{V_{C1}} + \overline{V_{Lw}} = \overline{V_C}$ $(i = 1 \dots 5)$, while $\overline{V_{sb\_6}} = 0$. Then $V_{rt} = 5\overline{V_C}$. In general case with N submodules, the voltage relationship between V_{in} and V_{out} can be written as $V_{out} = V_{rt} + V_{in} = (N - 1)\overline{V_C} + V_{in} + V_{Lw}$. From previous analysis, because average voltage across an inductor operating in periodic steady state is zero, so the average output voltage can be derived as

$$\overline{V_{out}} = \frac{(2N-1) * \overline{V_C}}{2} \qquad \text{(Eq. 2.2)}$$

From Eq. 2.2, the average voltage generated on the output side is $5.5\overline{V_C}$ when $N = 6$, which means the dc offset generated by the resonant tank is $5.5\overline{V_C}$. Figure 2.6 shows the voltage relationship between $(V_{inv} + \sum V_{sb\_i})$, V_{inv} and $\overline{V_C}$. By repeating equivalent mode 1 and equivalent mode 2 for six submodules, there is always a resonance between the wire stray inductance and the capacitor distributed in each submodule, which makes it possible that the converter works under ZCS mode.

2.3. Features of The Proposed Converter

This section provide analysis for both full-bridge and half-bridge based converters in the aspects of transfer function, resonant frequency as well as duty cycle of the submodules and V_{inv}. Then a brief comparison between these two types of converter is performed.

2.3.1. Analysis of the Converter Based on Half Bridge Submodule

2.3.1.1. Transfer Function

Referring to voltage relationship between V_{in} and V_{out} in equivalent mode 1 and equivalent mode 2. The voltage stress on the capacitors is $\overline{V_C} = 2V_{in}$. And the transfer function can also be derived as

$$\frac{V_{out}}{V_{in}} = 2N - 1 \qquad \text{(Eq. 2.3)}$$

2.3.1.2. Resonant Frequency

If half-bridge submodules are to be adopted to build the converter, then the resonant frequencies of the positive part of i_{out} and negative part of i_{out} can be derived. According to Figure 2.7 and Figure 2.8, the inductance of the loop is always the same, while number of capacitors in the resonant loop keeps changing. And the resonant frequency for both parts are derived as

$$f_{rp} = \frac{1}{2\pi * \sqrt{L_w * C}} \qquad \text{(Eq. 2.4)}$$

$$f_{rn} = \frac{1}{2\pi * \sqrt{N * L_w * \frac{C}{N-1}}} \qquad \text{(Eq. 2.5)}$$

According to Eq.2.4 and Eq.2.5, two resonant frequencies exist if half-bridge submodules are employed. Here, f_{rp} and f_{rn} represent the resonant frequencies of i_{rp} *and* i_{rn} shown in Figure 2.6, respectively. This is obviously different from full-bridge version converter.

2.3.1.3. Duty Cycle

Regardless of the soft-switching feature and two different resonant frequency of the converter, a duty cycle of 0.5 for V_{inv} is considered for the preliminary analysis. The duty cycle of switch S_p in the submodules can be written as Eq.2.6, and there is a phase-shift angle of 360˚/N between every two submodules.

$$D = \frac{2N-1}{2N} \quad \text{(Eq. 2.6)}$$

In order to achieve ZCS resonant operation for all the submodules, the duty cycle of the full-bridge used to generate V_{inv} needs to be tuned according to the two different resonant frequencies derived in Eq.2.5 and Eq.2.6. It can be derived as

$$D_r = 1 - \frac{f_{rp}}{f_{rp} + f_{rn}} \quad \text{(Eq. 2.7)}$$

Also, due to different resonant frequency f_{rp} and f_{rn}, the duty cycle of switching device S_p in submodules needs to be recalculated

$$D_{sb} = D - \frac{0.5 - D_r}{N} \quad \text{(Eq. 2.8)}$$

Plug Eq.2.6 and Eq.2.7 into Eq.2.8, D_{sb} can be derived

$$D_{sb} = \frac{(f_{rp} + f_{rn}) * N - f_{rp}}{(f_{rp} + f_{rn}) * N} \quad \text{(Eq. 2.9)}$$

2.3.1.4. Variable Conversion Ratio

Also, the conversion ratio could be adjusted by changing the duty cycle of phase-shifted PWM signal used to control the submodules. One assume that there are *P*+1 submodules been activated during equivalent mode 1. And in equivalent mode 2, one of the *P*+1 submodules has been kicked out, which means *P* submodules are in the loop during equivalent mode 2. Hence, by replacing *N* with *P*+1 among the numerators in Eq.2.6, one can derive the new transfer function

$$\frac{V_{out}}{V_{in}} = 2P + 1 \qquad \text{(Eq. 2.10)}$$

Similarly, in order to calculate the new duty cycle of the PWM signals sent to submodules, one can replace N with P+1 among the numerators in Eq.2.9. The new duty cycle value can be found with Eq. 2.11

$$D_{sb} = \frac{(f_{rp} + f_{rn}) * P + f_{rn}}{(f_{rp} + f_{rn}) * N} \qquad \text{(Eq. 2.11)}$$

2.3.2. Analysis of the Converter Based on Full Bridge Submodule

2.3.2.1. Transfer Function

By using the same method used to get the transfer function of the half-bridge version converter, average voltage on the capacitor is obtained, which is $\overline{V_C} = V_{in}$. And the transfer function of the full bridge version converter with maximum step-up ratio can be derived as Eq.2.12

$$\frac{V_{out}}{V_{in}} = N - 1 \qquad \text{(Eq. 2.12)}$$

2.3.2.2. Resonant Frequency

Since *N* submodules are used to build the MMC, and every one of them has the same parameters, then the resonant frequency for positive part of i_{out} and negative part of i_{out} can be written as Eq.2.13.

$$f_{rp} = f_{rn} = \frac{1}{2\pi * \sqrt{L_w * N * \frac{C}{N}}} \qquad \text{(Eq. 2.13)}$$

Once Eq.2.13 has been derived, the resonant frequency and switching frequency can be easily derived as Eq.2.14.

$$f_r = N * f_s = 2 * \frac{f_{rp} * f_{rn}}{f_{rp} + f_{rn}} \qquad \text{(Eq. 2.14)}$$

2.3.2.3. Duty Cycle

With the phase-shift angle of $360^{\circ}/N$, the duty cycle of switch S_p in submodules can be found.

$$D_{sb} = \frac{2N-1}{2N} \quad \text{(Eq. 2.15)}$$

Different from the proposed converter using half-bridge submodules, the submodule capacitor and stray inductance are always in the resonant loop, so only one resonant frequency exists. Hence, duty cycle of the full-bridge used to generate V_{inv} is 0.5.

2.3.2.4. Variable Conversion Ratio

Same as the half-bridge version converter, the conversion ratio could be changed by adjusting the duty ratio of each pair of switches in every submodule. The transfer function of the converter under this operation mode is

$$\frac{V_{out}}{V_{in}} = 2P + 1 - N \quad \text{(Eq. 2.16)}$$

In Eq.2.16, parameter P means during equivalent mode 1, there are $P+1$ submodules that have been connected in positive way. And after that, 1 of the $P+1$ submodules will change from positive connection to negative connection during equivalent mode 2. Correspondingly, in equivalent mode 2, P submodules are connected in positive and $N-P$ are connected in negative. Thus the duty ratio of switching device S_p in submodules can be derived

$$D_{sb} = \frac{2P+1}{2N} \quad \text{(Eq. 2.17)}$$

Duty cycle of the submodules needs to be changed in order to change the conversion ratio. However, the change of duty ratio will not affect resonant frequency of the converter. So, the duty cycle of V_{inv} is still 0.5.

2.3.3. Submodule Voltage Balancing and Device Current Stress Balancing

One of the big advantages is the proposed converter possesses automatic voltage balancing capability among the submodules. This feature brings benefits of less voltage and current sensors, simpler hardware design and lower cost. It also makes the converter more reliable. For converter with half-bridge submodules, according to Figure 2.7 and Figure 2.8, the capacitor in activated submodule is always connected in series with the other submodule capacitors. And all the capacitors are trend to share the high voltage across them, with identical voltage on each capacitor. As a result, all the submodule capacitor voltage will be balanced automatically.

Figure 2.9 and Figure 2.10 shows the comparison base on converter using six half-bridge submodules. According to previous analysis, when the conversion ratio is high, duty cycle of the switch S_p in submodules becomes high. Which means S_p in each submodule has longer conduction time than S_n. As a result, the RMS values of the current flow through S_p and S_n are very different, as shown in Figure 2.9. This will lead to different life time of switching devices and some potential issues. Therefore, more balanced current flow through switches is desired under some circumstances. By applying $P = 3$ to Eq. 2.11, D_{sb} will decrease. Thus a relatively more balanced conduction time of S_p and S_n in each submodule has been achieved. This means the RMS values of the current flow through S_p and S_n become more balanced, as shown in Figure 2.10. However, the conversion ratio of this converter will be traded off. According to previous analysis, half-bridge cell is more suitable to work under current balancing mode. Because changing of duty cycle has less effect on the conversion ratio of the converter.

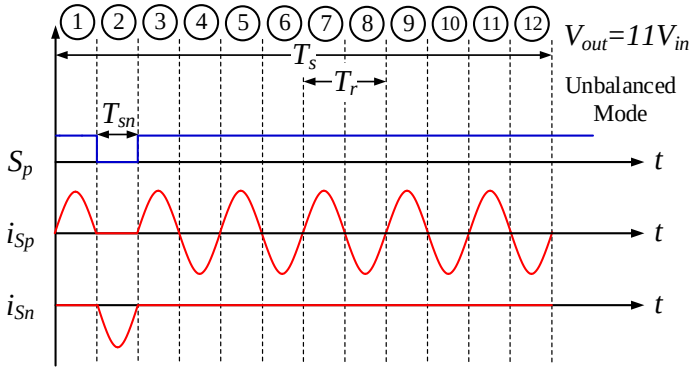

Figure 2.9. S_p conduction time and switch current when P=1

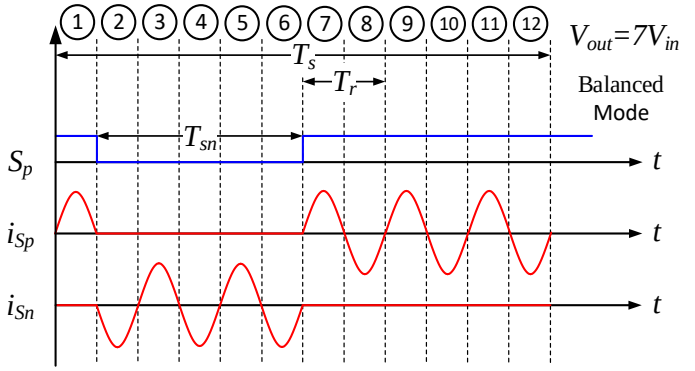

Figure 2.10. S_p conduction time and switch current when P=3

2.3.4. Comparison of the Proposed Converter Using Two Different Submodules

In summary, Table 2.1 shows a brief comparison between the proposed MMC using two different submodules. With the same submodule number, half-bridge version MMC uses less switching device and provide higher step-up ratio at the same time. However, the average device voltage stress on devices in half-bridge submodule is four times of that in full-bridge submodule. Table 2.2 shows the capacitor status under different operation states. For the full-bridge version MMC, all the submodule capacitors are always active, while means they are charging or discharging all the time. While the submodule capacitors in half-bridge version MMC have one inactive state.

Table 2.1. Comparison of the Proposed Converter Using Two Types of Submodules

Description	Value	
Submodule Type	Full- Bridge	Half-Bridge
Submodule Number	N	N
Device Number	4N+4	2N+4
Max Conversion Ratio	N-1	2N-1
Submodule Average Voltage	Vin	2Vin
Device Voltage Stress	Vin /2	2Vin

Table 2.2. Capacitor Status under different Operating States at Maximum Conversion Ratio

	Half-Bridge Submodule	Full-Bridge Submodule
State	Capacitor Status	
1	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑
2	C1→, C2↓, C3↓, C4↓, C5↓, C6↓	C1↑↑, C2↓, C3↓, C4↓, C5↓, C6↓
3	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑
4	C1↓, C2→, C3↓, C4↓, C5↓, C6↓	C1↓, C2↑↑, C3↓, C4↓, C5↓, C6↓
5	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑
6	C1↓, C2↓, C3→, C4↓, C5↓, C6↓	C1↓, C2↓, C3↑↑, C4↓, C5↓, C6↓
7	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑
8	C1↓, C2↓, C3↓, C4→, C5↓, C6↓	C1↓, C2↓, C3↓, C4↑↑, C5↓, C6↓
9	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑
10	C1↓, C2↓, C3↓, C4↓, C5→, C6↓	C1↓, C2↓, C3↓, C4↓, C5↑↑, C6↓
11	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑	C1↑, C2↑, C3↑, C4↑, C5↑, C6↑
12	C1↓, C2↓, C3↓, C4↓, C5↓, C6→	C1↓, C2↓, C3↓, C4↓, C5↓, C6↑↑

↑↑ = Capacitor fast charging, ↑ = Capacitor charging, ↓ = Capacitor discharging, → = Capacitor inactive

2.4. Efficiency of The Converter

As one of the major concern regarding modular multilevel converter is its efficiency. Because multiple switching devices are connected in series when the converter is operating, this section will focus on estimating the switch conduction loss, capacitor loss, cooper loss and gate drive loss of the proposed converter. An application example of the proposed MMC with 6 half-bridge submodule to be analyzed in this part uses mosfet module CAS300M17BM2 from Cree as

main switching device. In this estimation, two mosfet modules are connected in parallel in each submodule to increase the current capability. The parameters of the device are listed in Table 2.3. The system information can be found in Table 2.4

Table 2.3. Key Parameters of IGBT Used in Efficiency Analysis

Parameter	Symbol	Value
Drain-source voltage	V_{DS}	1700 V
Continuous drain current	I_D	225 A
Gate-source voltage	V_{GS}	20 V
Total gate charge	Q_g	1076 nC
On State Resistance	$R_{DS(on)}$	8 mΩ

Table 2.4. Parameters of the Analyzed System

Parameter	Value
Half-bridge submodule number	6
Input / output voltage	600 V / 6.6 kV
Maximum output Power	200 kW
Submodule switching frequency	7.161 kHz
Resonant frequency	42.965 kHz

Assume i_{sw_rms} represents the rms value of current flow through one switching device. Let $R_{DS(on)}$ represents the on-state resistance of each Mosfet module, and P_{loss_semi} represents the power dissipation due to power device conduction. Thus, the device conduction loss of one Mosfet module can be estimated using

$$P_{loss_{semi}} = i_{sw\_rms}^2 * R_{DS(on)} \quad \text{(Eq. 2.18)}$$

Power loss due to gate drive is also considered, denoted as P_{loss_gate}. It can be derived using the following equation:

$$P_{loss\_gate} = V_{gs} Q_g f_s \quad \text{(Eq. 2.19)}$$

In Eq. 2.19, V_{gs} is the gate-source voltage of the power device, Q_g is total gate charge and f_s means switching frequency of the power device.

At last, ESR of the capacitors introduced power loss to the converter, too. Assume capacitor ESR is R_{C_esr}, RMS value of the current flow through capacitor is I_{C_rms}, and capacitor conduction loss is P_{loss_cap}. Thus, power loss due to each capacitor conduction can be estimated:

$$P_{loss\_cap} = R_{C\_esr} * I_{C\_rms}^2 \quad \text{(Eq. 2.20)}$$

With Eq.2.18, Eq. 2.19 and Eq. 2.20, the total power loss can be estimated by adding power device conduction, capacitor conduction and gate drive loss together.

$$P_{loss_{total}} = \sum P_{loss_{semi}} + \sum P_{loss\_gate} + \sum P_{loss\_cap} \quad \text{(Eq. 2.21)}$$

Figure 2.11 shows the relationship between efficiency and output power of the proposed converter with 6 half-bridge submodules. Figure 2.12 shows when the converter work at light load condition, gate drive and auxiliary power will be the primary source of power loss. As the converter delivers more power, device conduction loss will take more and more percentage among the total power loss. The peak efficiency of the converter is approximately 98.8%.

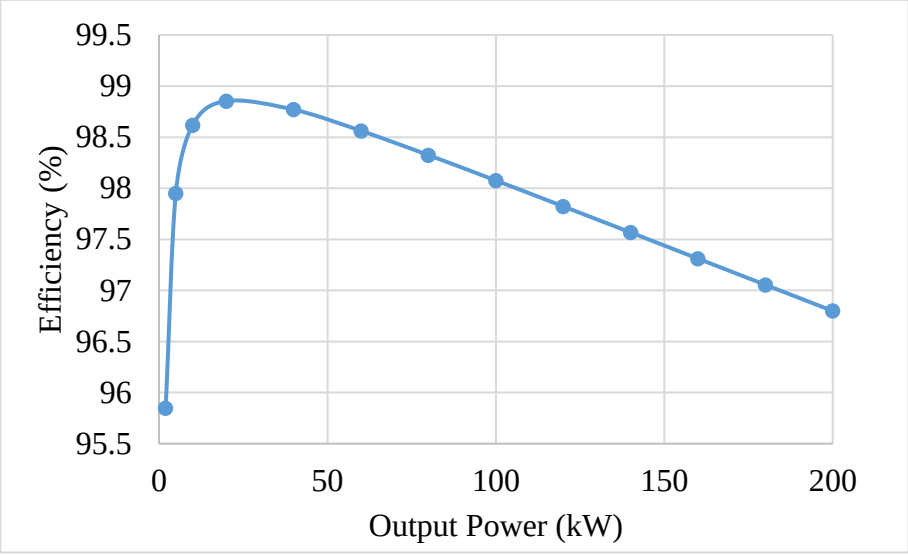

Figure 2.11. Efficiency of the converter

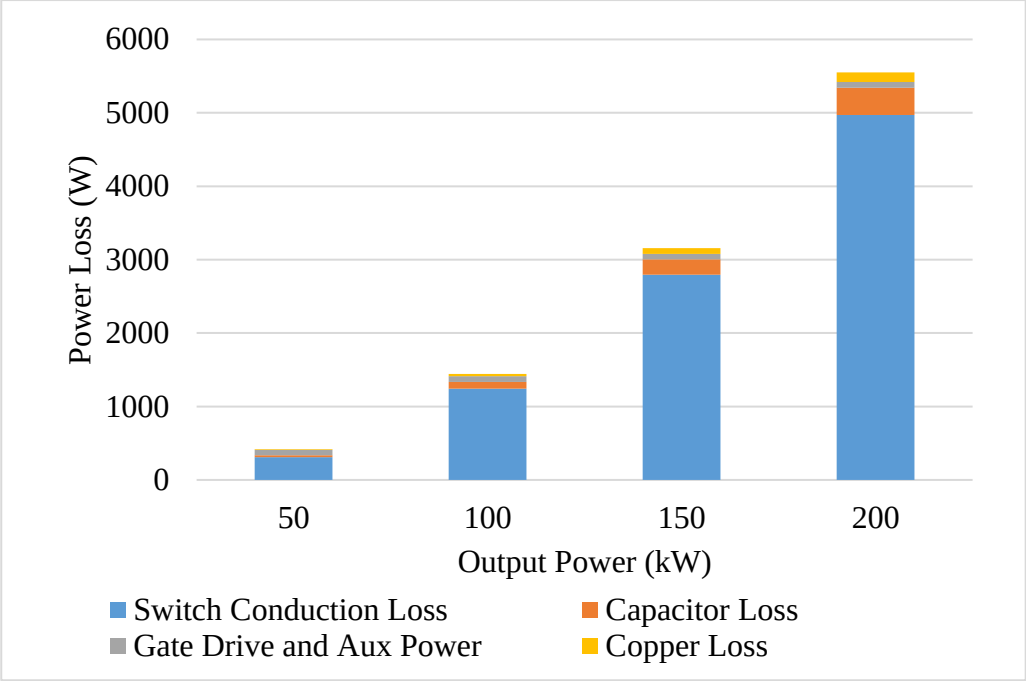

Figure 2.12. Power loss

2.5. Simulation Results

Simulation has been performed to verify the theory of the proposed full-bridge version MMC and the half-bridge version MMC. Referring to previous analysis, Table 2.1 shows a comparison between converters built by this two types of submodules. And all key data used to simulate the proposed converter with half-bridge submodule and full-bridge submodule is given in Table 2.5.

Figure 2.13 and Figure 2.14 shows the simulation result of the proposed converter with 6 submodules. The power rating of converter using half-bridge and full-bridge submodules are 66kW and 30Kw, respectively. In the simulation, a resistive load is used. This result indicate that the converter is working under ZCS mode with open loop phase-shift PWM control.

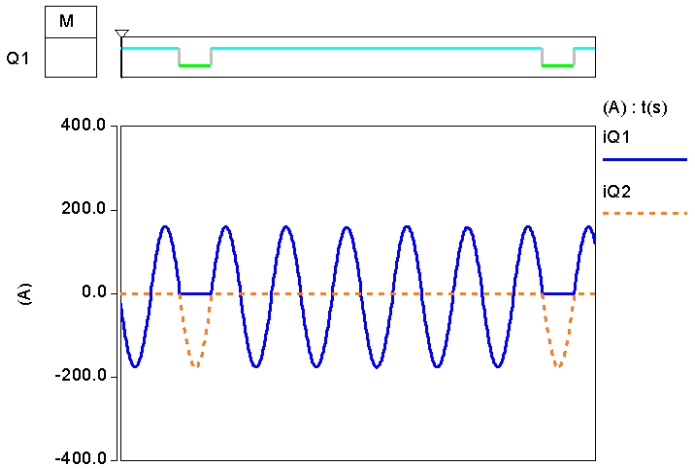

Figure 2.13. ZCS operation of with half-bridge version MMC

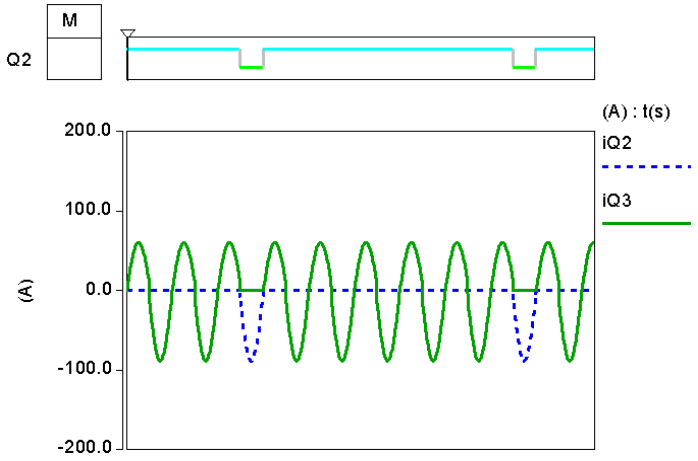

Figure 2.14. ZCS operation of with full-bridge version MMC

Figure 2.15 and Figure 2.16 shows the resonant current flow through the loop and the voltage used to maintain the resonance, which are i_{out} and V_{inv}, respectively. Also Figure 2.15 and Figure 2.16 shows that amplitude of DC bus current, which is i_{bus}, during the first half resonant cycle and the second half cycle is different.

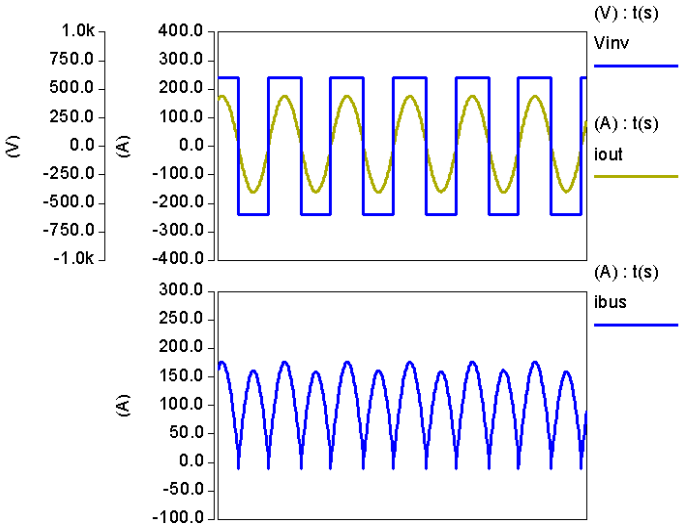

Figure 2.15. Waveforms of half-bridge version MMC

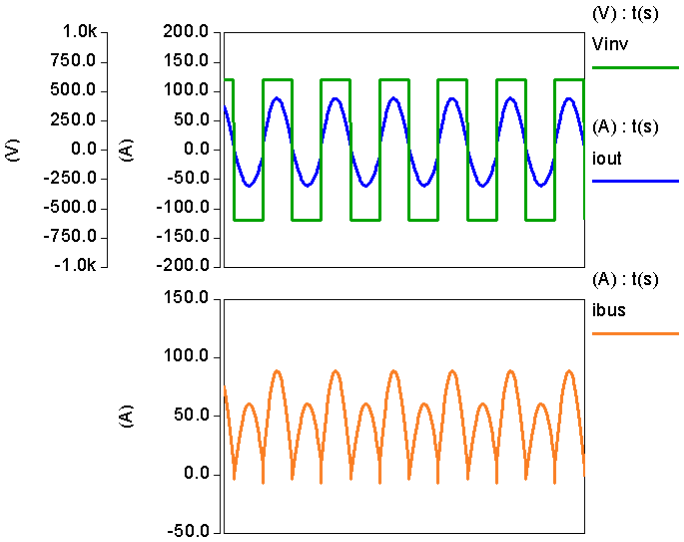

Figure 2.16. Waveforms of full-bridge version MMC

According to Figure 2.17, the proposed converter with half-bridge submodules generates a 6.6kV dc voltage on the output side, average voltage of the submodule capacitors is 1.2kV. Figure 2.19 shows that all submodule capacitor voltages are balanced. Figure 2.18 shows the converter with full-bridge submodules has boosted the voltage from 600V to 3kV as expected, with little voltage drop. And the average voltage of the capacitors in submodules is around 600V, matches the theoretical analysis. Detailed waveforms can be found in Figure 2.20.

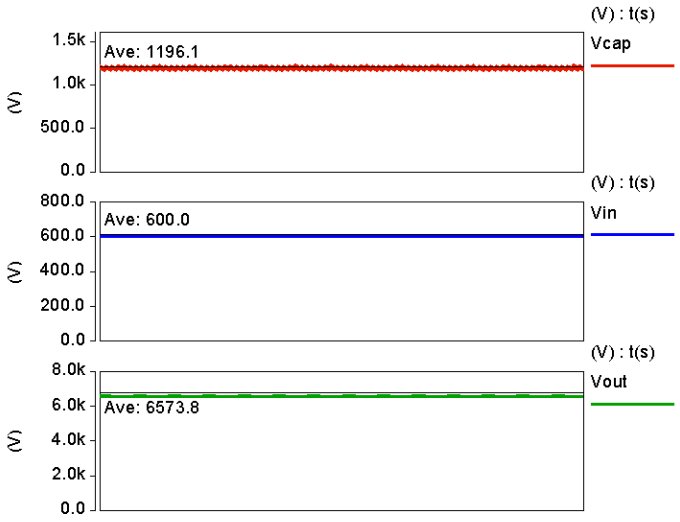

Figure 2.17. Voltage waveform of the half-bridge version MMC

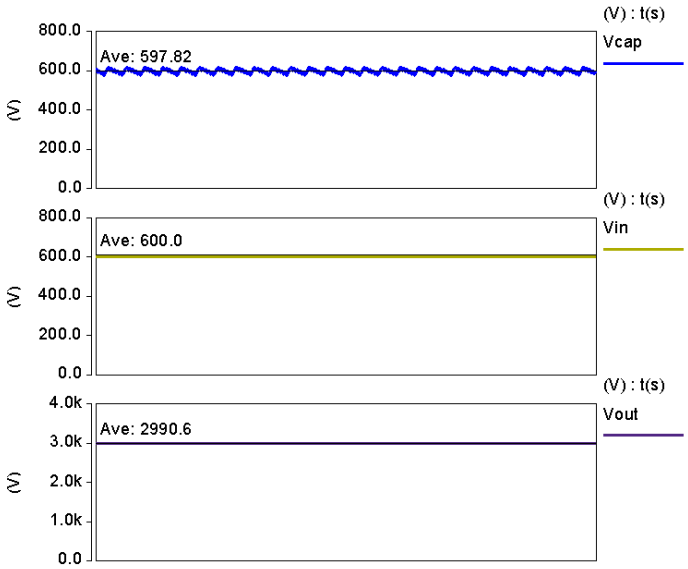

Figure 2.18. Voltage waveform of the full-bridge version MMC

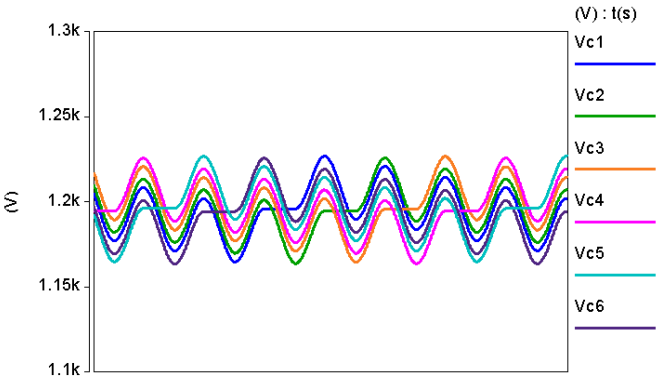

Figure 2.19. Submodule capacitor voltages of half-bridge version MMC

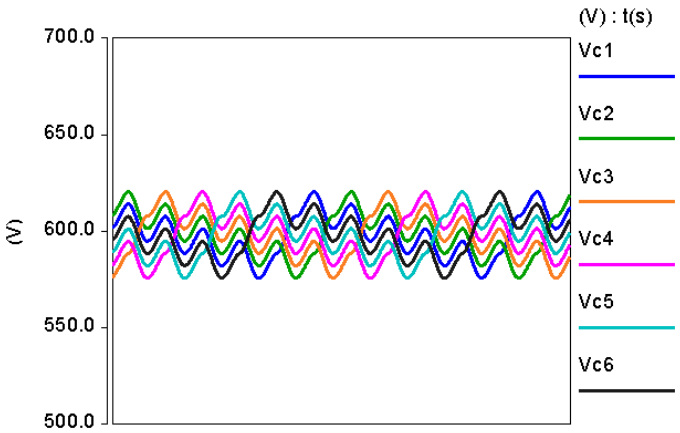

Figure 2.20. Submodule capacitor voltages of full- bridge version MMC

Simulation is also performed to verify the function of converter with 6 half-bridge submodule when it's working under lower step-up ratio mode, as shown in Figure 2.21. The output voltage drops from 6.6kV to 4.2kV, which means the conversion ratio drops from 11 to 7. However, the average voltage across submodule capacitors is still 1.2kV. This also indicates that the change of submodule duty cycle will not have an effect on the capacitor average voltage.

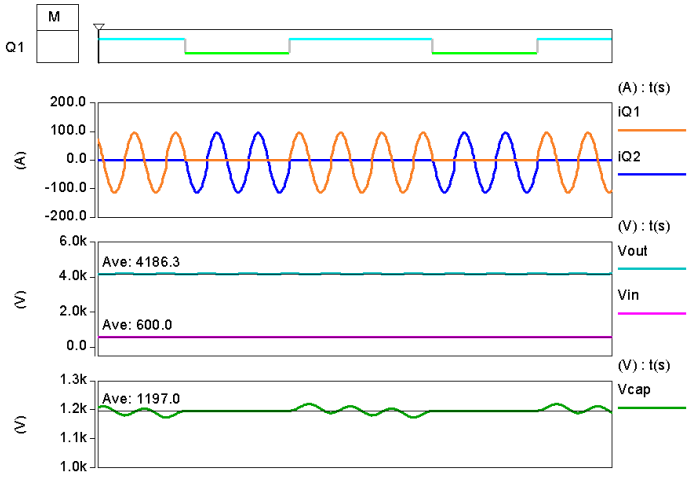

Figure 2.21. Voltage and current waveform when converter with half-bridge submodules working under lower conversion ratio status

2.6. Experimental Results

A scaled down lab prototype with four half-bridge submodule has been built to verify the proposed concept, as shown in Figure 2.22 and Figure 2.23. The submodules use 7.9uF ceramic

capacitors as main capacitors. The stray inductance distributed on wires is 292nH . EPC2023 is selected as switching device to build all the modules, it's detailed parameters is shown in Table 2.7. Because it is difficult to measure the stray inductance very percisely, rough extimation of L_w only allows the converter working under hard switching mode. By measuring the two different resonant frequencies, f_{rp} and f_{rn} under hard-switching mode, a more exact value of wire stray inductance can be obtaioned. Thus the duty cycles of V_{inv} and submodules can be tuned to assist the converter operates under ZCS mode. Figure 2.25 to Figure 2.32 show the experimental waveforms with open loop phase-shifted control. If and only if the switches in submodules operate at resonant frequency, the ZCS operation can be achieved. Due to the package of the switching device, i_d of the mosfets cannot be obtaioned. However, one can still verify the zero current switching according to gate signal and resonant current, shown in Figure 2.25 and Figure 2.29. Figure 2.33 shows the zoomed in waveform. The deadtime of the gate signal is 200ns, shown in Figure 2.34. The capacitor voltage waveforms can be seen from Figure 2.26 and Figure 2.30. The average voltage on the capacitors are 10V and 20V when input voltage is 5V and 10V, respectively. It can be seen that when the output power increases, the voltage ripple on the submodule will increase as well. So, capacitor with a relatively high capacitance is desired in the design, which will help minimize the voltage ripple on it.

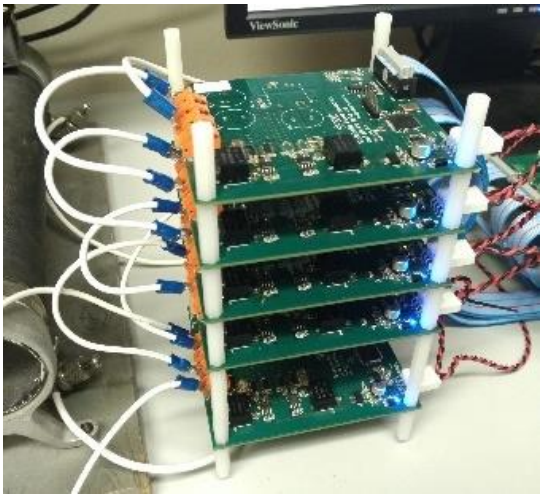

Figure 2.22. Scaled down 200W lab

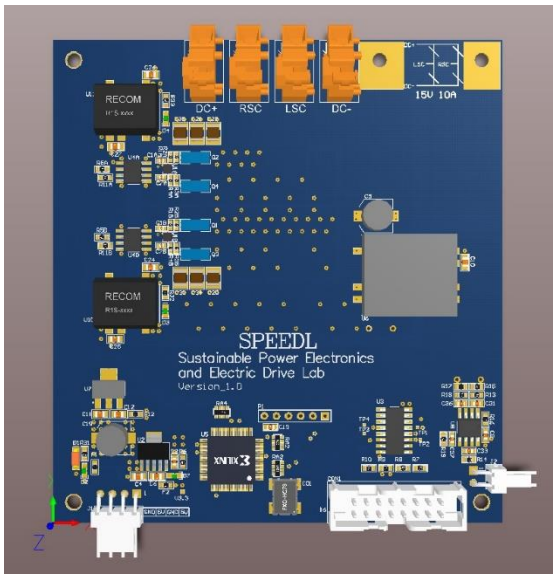

Figure 2.23. 3D view of each submodule

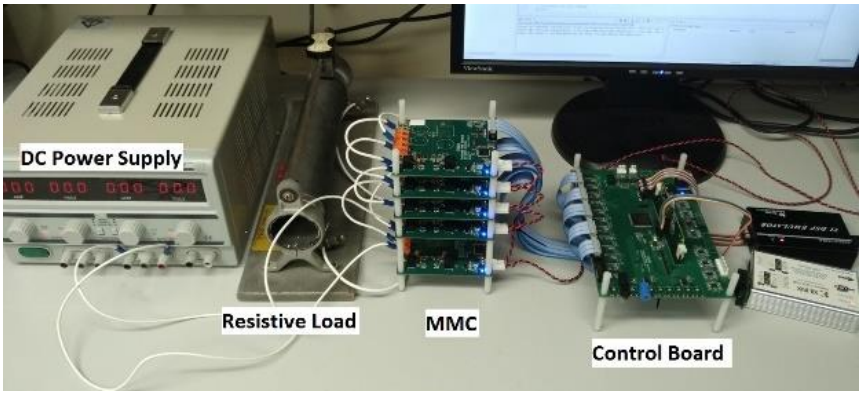

Figure 2.24. Overview of the test bench

Table 2.5. Key Data Used to Simulate the proposed Converter

Parameter	Symbol	Value	
Submodule Type	N	Full-Bridge	Half-Bridge
Submodule number	M	6	6
Max Conversion Raito	V_{in}	5	11
Input voltage	V_{out}	600 V	600 V
Output voltage	P	3 kV	6.6 kV
Power rating of the converter	f_r	30 kW	66 kW
Resonant frequency	f_s	58.12 kHz	43.97 kHz
Submodule Switching frequency	C_i	9.69 kHz	7.16 kHz
Capacitor used in each submodule	L_w	30 uF	30 uF
Inductance distributed on wires	D_{sb}	0.25 uH	0.25 uH
Duty cycle of S_p (submodule)	R_{load}	0.917	0.913

Table 2.6. Parameters of The Experimental System

Description	Symbol	Value
Input voltage	V_{in}	10 V
Maximum power of the converter	P	200 W
Resonant frequency	f_r	86.69 kHz
Submodule Switching frequency	f_s	43.34 kHz
Capacitor used in each submodule	C	7.9 uF
Inductance distributed on wires	L_{wire}	292 nH
Duty cycle of S_p (submodule)	D_{sb}	0.707
Resistive Load	R_{load}	35 Ω
Output Capacitor	C_{out}	20 uF

Table 2.7. Device Paramerters of The Experimental System

Description	Symbol	Value
Max drain-source voltage	V_{DS}	30 V
Gate-source voltage	V_{GS}	5 V
Continuous drain current	I_D	60 A
On state resistance	r_{dson}	1.3 mΩ
Total gate charge	Q_g	20 nC

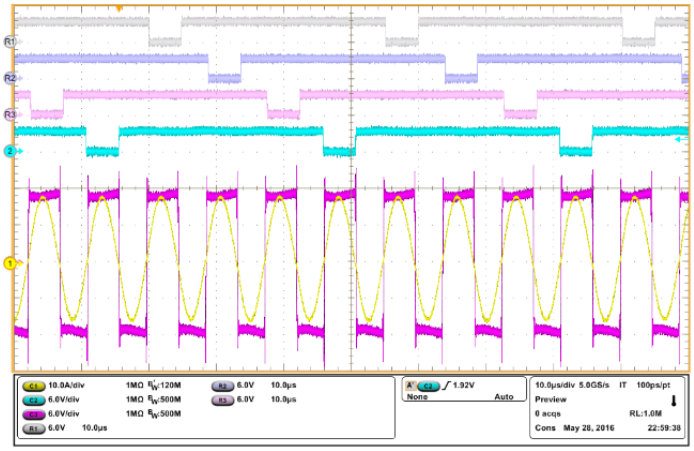

Figure 2.25. Gate Signal, resonant current and Vinv

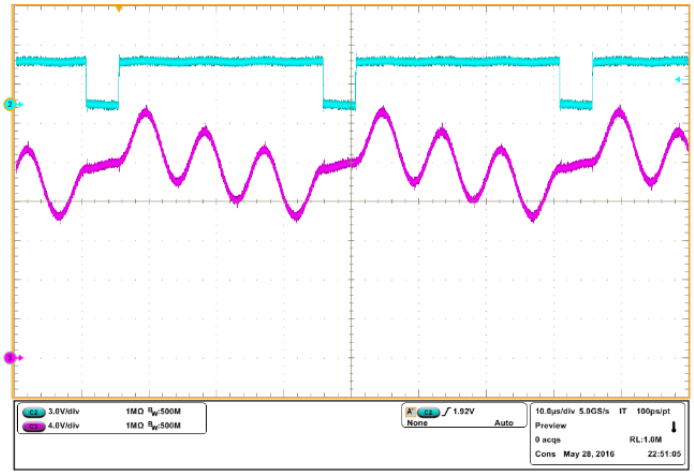

Figure 2.26. Capacitor voltage of one submodule

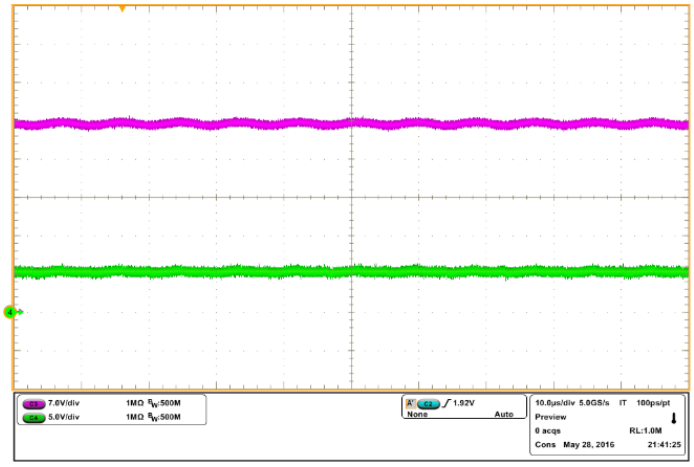

Figure 2.27. Input and output voltage

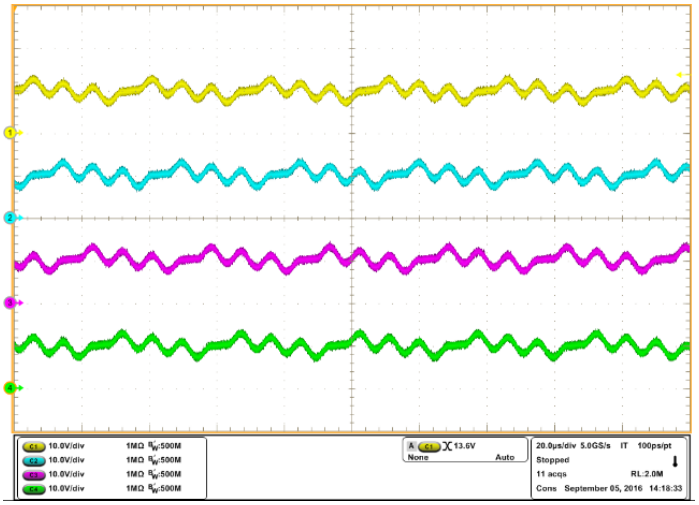

Figure 2.28. All submodule capacitor voltages

With four half-bridge submodules, the converter possesses 7-time voltage step-up capability in theory. Figure 2.27 and Figure 2.31 show the experimental results of input and output voltage. When input voltage changes from 5V to 10V, output voltage changes from 35V to 69.5V, which can verify the proposed MMC concept. At last, Figure 2.28 and Figure 2.32 show the voltage of all the submodule capacitors are autimatically balanced, with a little difference. Because the capacitances in submodules are slightly different. Hence, in order to reduce the voltage difference on submodules, a fine tuned resonant tank is desired.

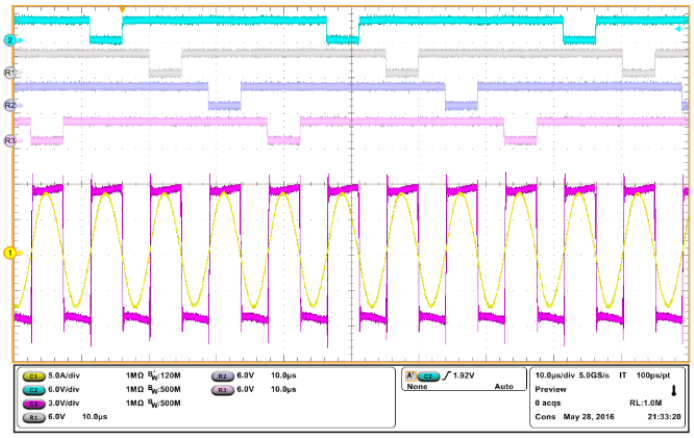

Figure 2.29. Gate Signal, resonant current and V_{inv}

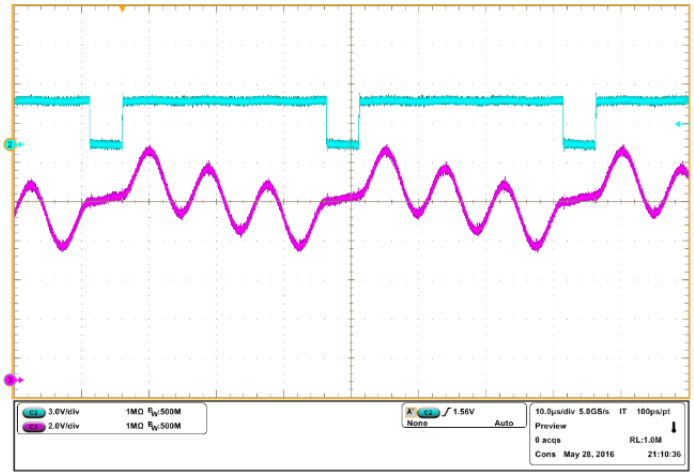

Figure 2.30. Capacitor voltage of one submodule

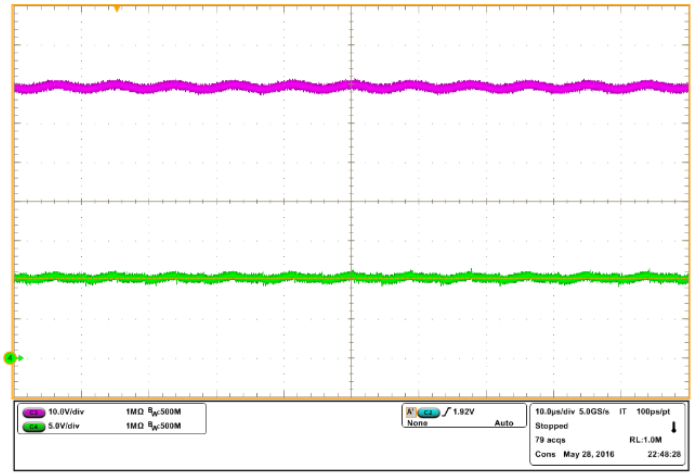

Figure 2.31. Input and output voltage

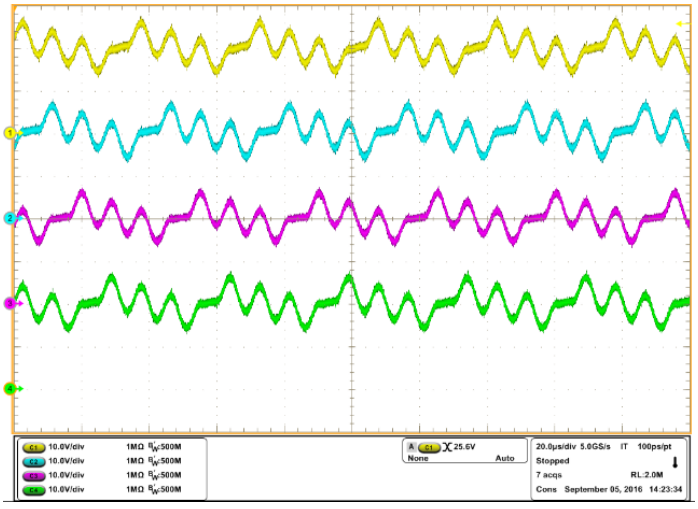

Figure 2.32. All submodule capacitor voltages

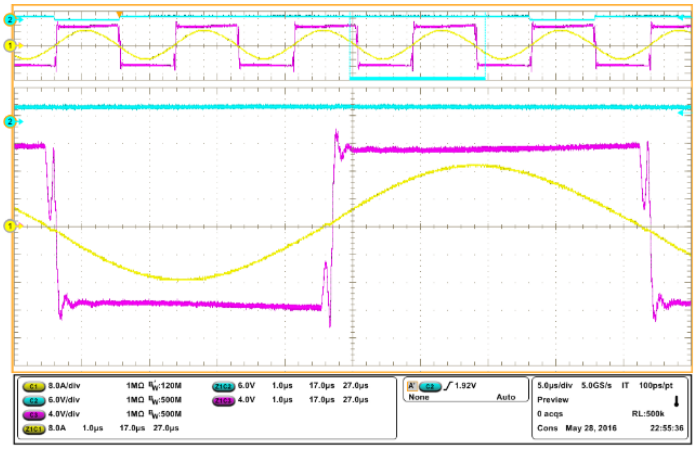

Figure 2.33. ZCS operation of submodules

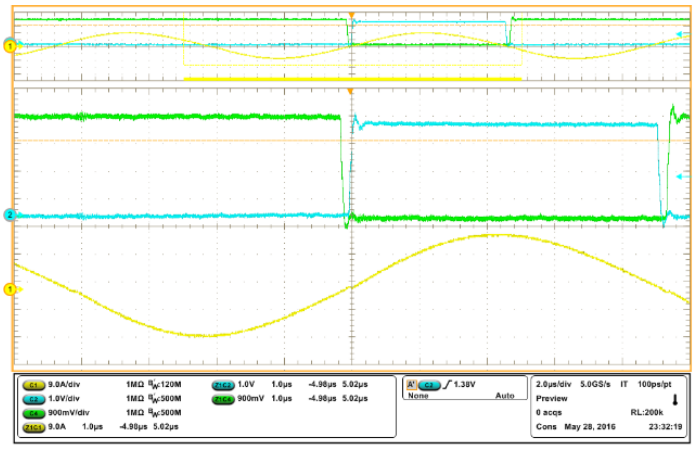

Figure 2.34. Resonant current waveform during deadtime

2.7. Conclusion

Since more and more people are becoming interested in high conversion ratio dc-dc modular multilevel converters, this work presents a new transformerless dc-dc MMC. The proposed converter utilizes the stray inductance distributed in the physical layout of the system, which makes the proposed converter inductorless. This brings the benefits of low cost, high efficiency, high power density and high reliability. Also, the modular structure of each submodule made this converter very easy to be maintained. Furthermore, the faulty submodule can be bypassed, using redundant submodule in the system, which allows the converter have high fault tolerant capability. If the proposed converter is built with half-bridge submodule, two resonant

frequencies are existed. On the other hand, only one resonant frequency is existed in the converter with full-bridge submodule. Resonant operation makes the converter can easily work under ZCS mode. Compare to some other dc-dc MMC converters, the proposed one can change its conversion ratio by modifying the duty cycle of the switches instead of modifying the hardware.

3. A 98.55% EFFICIENCY SWITCHED-TANK CONVERTER FOR DATA CENTER APPLICATION

3.1. Introduction

With the development of big data, internet of things, cloud computing and mobile internet, a growing number of data centers have been built all over the world. All the data centers consume a considerable amount of power. In 2014 alone, around 70kWh energy was consumed by data centers in the U.S [42]. Currently, DC distribution system is widely used to replace traditional AC system in data center due to its high-efficiency feature [43]. Researchers and industry leaders such as Google and Facebook are seeking new approaches to run their data centers more efficiently based on DC distribution systems. In terms of the architecture level power delivery solution, on one hand, 48V DC power delivery architecture has been proposed to replace the traditional 12V DC system used in data centers. It's worth mentioning that use 54V as nominal voltage in 48V architecture is becoming more and more popular in today's computing industry [44][45]. On the other hand, DC bus with higher voltage (such as 380V) has been proposed and claimed more energy efficient than the 48V DC bus [46][47]. However, rebuilding a system means a lot of investment in research and power delivery system construction. As a result, 48V power architecture is still widely used in data centers for now. In [48], differential power processing concept has been proposed by connecting the CPU loads in series to achieve high efficiency. However, the CPU loads in this series connected structure can't share the same ground, which generates other difficulties for peripheral circuits design. At the same time, many efforts have also been devoted to improving the efficiency and power density of dc-dc converters. For the 48V bus power delivery system in the data center, there exists single-stage and two-stage approaches. On one hand, single-stage approach converts 48V DC bus voltage to low voltage and feeds to CPU

directly [49]. To achieve such a high voltage conversion ratio, the single-stage method normally requires a highly efficient and high conversion ratio planar transformer in the topology. On the other hand, the two-stage approach converts 48V to an intermediate voltage (e.g. 9V, 12V) first, then the second stage generates low voltage such as 1.2V and 1.8V for the CPU [50]. This solution uses a non-regulated IBC as the first stage and a regulated point-of-load (POL) converter as the second stage. One of the popular POL converters is highly efficient multiphase buck converter [51]. This two-stage approach is also known as the intermediate-bus architecture (IBA). The advantage of IBA is that an optimal voltage can be generated on the intermediate DC bus to achieve high system efficiency. Therefore, a high efficiency and high power density IBC becomes the key of the IBA.

Isolated IBCs are used in both telecommunication and data center applications. In telecommunication systems, isolated IBC is needed to prevent components on the server to be damaged from power spike that propagates from the front-end AC/DC converter. Since there is no power spike in modern data centers, isolation is only found as an over-provisioned safety requirement for IBCs. This means the isolation in IBCs is not mandatory [52]. Note that this doesn't mean isolation is not required throughout the data center. More importantly, the isolation circuitry limits the power density and efficiency of IBCs. For instance, the power loss of transformer may take 31% of the total power converter power loss in an IBC [53]. Even with a special transformer design, transformer loss still accounts for 22% of the total power loss under full load condition [54]. And the transformer occupies about 37% of the converter size. In [55], the transformer takes about 45% of the converter size. As a result, non-isolated IBC becomes more attractive in the data center. In the two-stage architecture, voltage regulation is normally achieved by the second stage voltage regulators. So the voltage regulation of IBC is not mandatory, which

means the IBC can be fully regulated or unregulated. Thus, the design targets of IBC will focus on converting 40V~60V to an intermediate voltage [44] and achieving high efficiency.

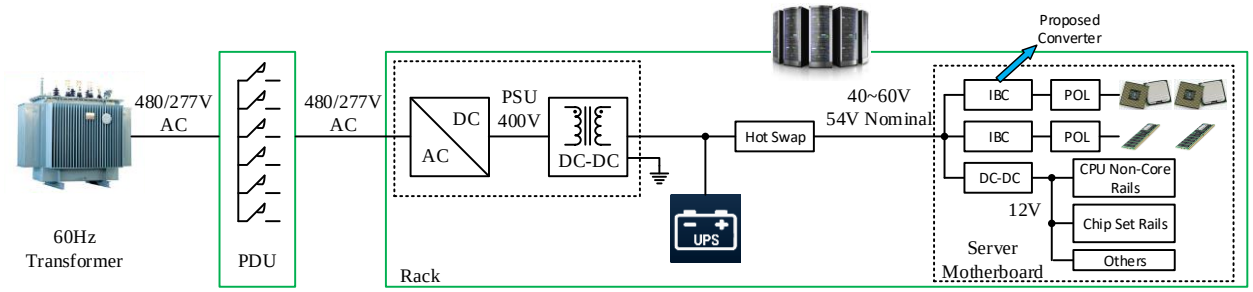

Figure 3.1. A typical 48V data center power architecture

Since isolation is not needed for IBC, the non-isolated switched-capacitor converters could be used as candidates. Because switched-capacitor circuits use capacitors to transfer energy and consequently achieve better stability and higher power density, extensive research has been conducted in the switched-capacitor area since the 1970s [56]–[70]. In order to ensure high-efficiency operation of the switched-capacitor converters in high power application, capacitor banks with high capacitance have to be used in the converters. For example, in [71][72], ten 3300µF and ten 2200µF electrolytic capacitors are used to build the 1kW 4-level flying capacitor dc-dc converter. And the volume of capacitors alone takes over $30in^3$. In order to achieve high voltage conversion ratio and reduce the switch power loss in the traditional flying capacitor dc-dc converter, a multilevel modular capacitor clamped dc-dc converter has been proposed [73][74]. However, the 120W 6-level converter with 75V input still needs five large-sized 1000µF/100V electrolytic capacitors to achieve high-efficiency operation. Thus, achieving high efficiency and reducing capacitor size at the same time becomes a challenge for switched-capacitor converters in high power applications. In [75], a split-phase control technique has been proposed to eliminate the current transient during the phase switching instances, which helps traditional Dickson converter to achieve soft-charging operation. In [76], by adding a dc inductor to existing switched-

capacitor topologies, either resonant or soft-charging operation of the existing topologies could be achieved. Consequently, high density and high efficiency of the converters could be achieved. But the capacitors need to be carefully selected to meet the requirement on capacitors' capacitance, which is vital to achieving soft-charging. And this is a challenge for mass production. In [77]–[80], a zero current switching multilevel modular switched-capacitor dc-dc converter has been proposed and optimized. By utilizing the stray inductance existed in the physical circuit, all the switches in this converter could achieve ZCS. This converter keeps the high voltage conversion ratio and high-efficiency features while reducing the capacitor size by around 20 to 50 times compared with the non-resonant converters shown in [73][74]. These switched-capacitor converters that have LC resonant tanks are now normally named resonant switched-capacitor converters or hybrid switched-capacitor converters. Because the resonant switched-capacitor converters utilize LC resonant tanks to eliminate the current transients [81]–[84], high efficiency and density can be achieved. As a result, resonant switched-capacitor technology tends to be implemented in a wide range of applications [85]. In [86]–[88], resonant switched-capacitor technology has been implemented in chip-level power delivery application. In [89], resonant switched-capacitor converters are used in PV application, which achieves 99% peak efficiency. In [90], voltage balancing circuit based on this technology has been developed for inverters. Intensive research work regarding the performance of the switched-capacitor circuits is also conducted in the past years [91]. In [92], a comparative study regarding resonant switched-capacitor converters has been performed. In [93], a new analysis technique for the complex switched-capacitor converters is proposed. In [94], a dynamic model that shows switched-capacitor circuits' dynamic response to the input voltage and output current changes is proposed.

A lot of switched-capacitor converters have fixed or adjustable voltage conversion ratio by nature [95]–[98]. This means they cannot continuously regulate the output voltage. One issue of the switched-capacitor circuits is that it is very challenging for them to achieve fine voltage regulation without significantly sacrificing efficiency [99]. In [100], lossless regulation methods for resonant switched-capacitor converters are proposed. In [101]–[103], a phase shift control method has been proposed to enable fine voltage regulation capability of the multilevel modular switched-capacitor dc-dc converters. This method achieves fine voltage regulation without scarifying power loss.

Although the previously mentioned zero current switching concept enables possibility for very high power density and high-efficiency design of the multilevel modular switched-capacitor dc-dc converter, some other issues still need to be solved in order to meet the requirement of commercial mass production. For example, during the commercial mass production, the tolerances of components (i.e. capacitors, gate resistors, resonant inductors, etc.) in the converter have to be considered. Figure 3.2 shows the previously proposed zero current switching multilevel modular switched-capacitor dc-dc converter [103]. When this converter faces serious component tolerance issue, its ZCS operation could be lost. Then voltage overshoot across the wing side devices will be observed if they are not properly clamped. Note that all switching devices in this topology that are floating in reference to ground are named wing side devices, while the other devices are called rectifier side devices.

This work proposes a switched-tank converter (STC) that is derived from the existing resonant switched-capacitor converter. This switched-tank converter concept is also proposed by Google in 2017 [104][105]. The STC solves the voltage overshoot issue on wing side devices led by components tolerance and non-ideal resonant operation in tradition circuit, which is one of the

barriers of productizing the resonant switched-capacitor converters. Besides, the STC keeps all the good features of previously proposed zero current switching multilevel modular switched-capacitor dc-dc converters in [77]–[80][103] and solves the voltage overshoot issue without penalties on converter size and efficiency. It has the following main features compared with previous work:

- Small size and high efficiency. The proposed converter relies less on inductive components than the zero current switching multilevel modular dc-dc converter that is shown in Figure 3.2 and leverages the advantages of low voltage rating MOSFETs. Compared with the traditional design [30], low voltage rating eGaNFETs and high-frequency resonant operation allow us to reduce all the passive components' size as well as achieve high efficiency.
- A new wing side device voltage clamping strategy. One drawback of the single wing zero current switching multilevel modular switched-capacitor dc-dc converter is that additional voltage clamping circuit is needed for wing side devices when the resonant tank has tolerance issue. The additional voltage clamping strategy may increase size, cost and complexity of the converter. The proposed STC possesses inherent voltage clamping mechanism for wing side devices, which makes it more favorable for practical industry application.
- The proposed converter is highly scalable. By adding more stages or interleaving more phases, the converter can achieve higher voltage conversion ratio or higher power output.

By using the provided design methodology in this work, semiconductor loss could be minimized. Furthermore, a design procedure for planar inductor using smallest off-the-shelf planar core is provided to demonstrate a way to reduce copper loss. Experimental results show that the designed 6x STC with nominal 54V input and 9V/450W output. Its peak efficiency is 98.55%.

With the help of low-profile planar inductor design, the prototype achieves 750W/in^3 power density at 450W.

This work is organized as follows: section II demonstrates the derivation of the proposed circuit and its operating principle. This section also provides guidance on properly selecting inductors and capacitors. Section III presents the issues caused by tolerances of resonant components and the solution to prevent the issues. Section IV shows a detailed methodology for switching device selection, planner inductor design and comprehensive power loss breakdown and estimation. Section V presents simulation and experimental results. At last, section VI concludes the proposed design.

3.2. System Structure and Theoretical Analysis

Figure 3.1 shows one of the existing data center power delivery solutions. We can tell that two-stage architecture has been used for the motherboard level power delivery in this system. The main target of this work is to propose a high efficiency and high power density intermediate bus converter for the two-stage solution. The proposed IBC will generate an intermediate bus voltage from the 54V nominal dc bus. Then the intermediate bus voltage will be converted to different low voltages to meet the load requirement. Note that the value of intermediate bus voltage depends on system requirement, so how to select optimal intermediate bus voltage is not within the scope of this study. Because voltage regulation function will be implemented in the second stage, voltage regulation function is not implemented in the proposed converter. In this section, the proposed switched-tank converter circuit will be derived based on the traditional switched-capacitor converter to achieve higher efficiency and density. Then operating principle of the proposed converter will be introduced. At last, detailed circuit analysis supports the better selection of passive components.

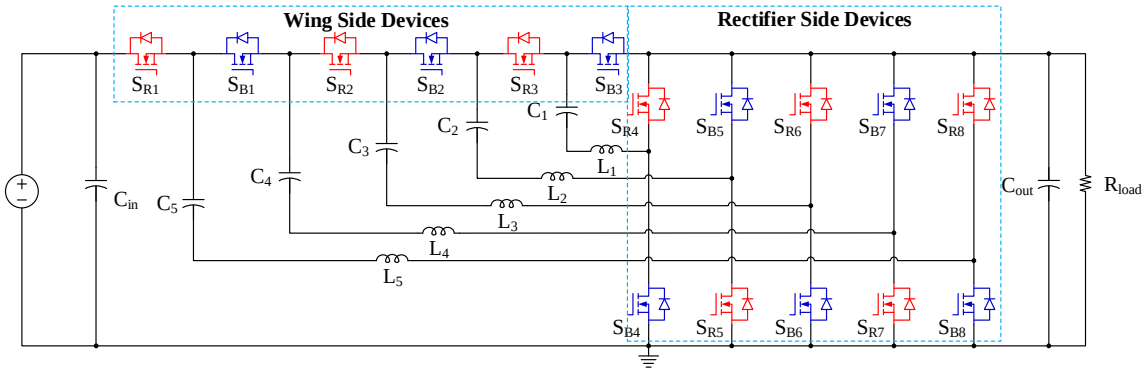

Figure 3.2. Structure of the resonant switched-capacitor converter proposed in previous work [103]

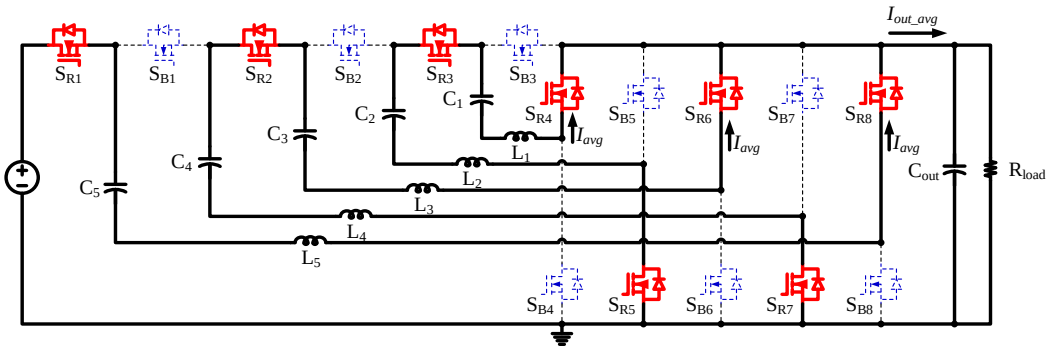

Figure 3.3. Equivalent circuit during state 1

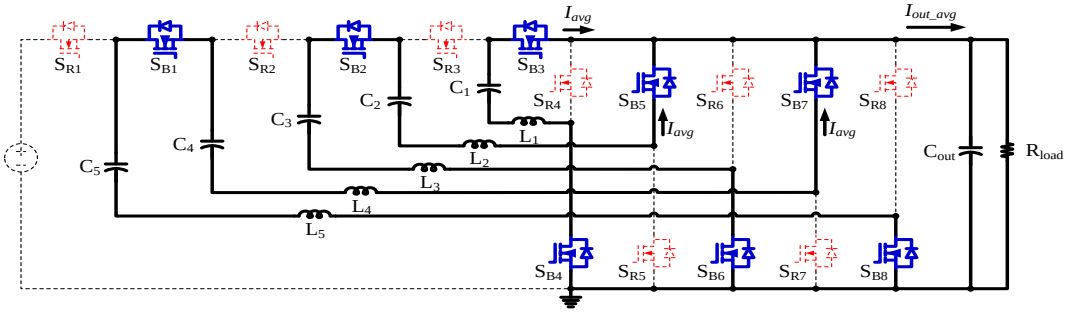

Figure 3.4. Equivalent circuit during state 2

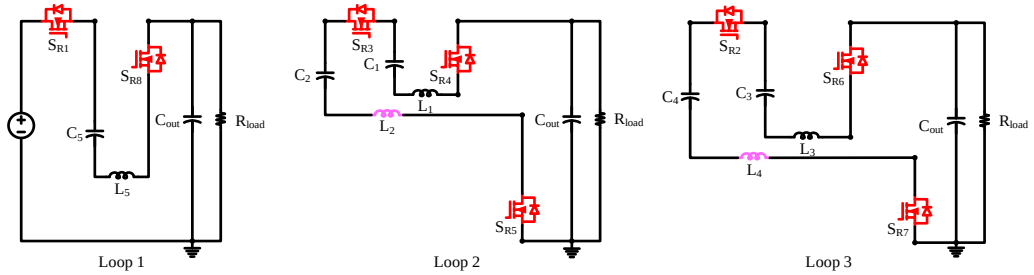

Figure 3.5. Separated equivalent circuits during state 1

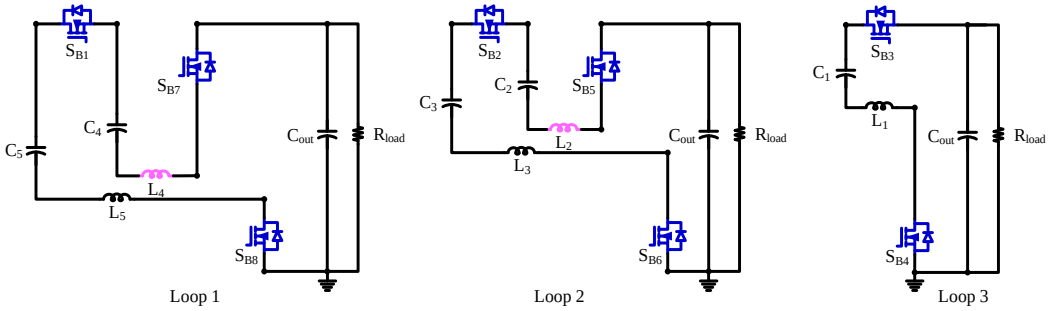

Figure 3.6. Separated equivalent circuits during state 2

3.2.1. Circuit Derivation of the Proposed Converter

As shown in Figure 3.2, a six times conversion ratio (6X) zero current switching multilevel modular switched-capacitor converter has been proposed in previous work [103]. When the MOSFETs' switching frequency equals to the resonant frequency of LC tank, ZCS operation can be achieved. Half-bridges are used as basic modules in this circuit. All the half-bridge modules can be divided into two groups, which are wing side group and rectifier side group. For all the devices in wing side group, they are floating in reference to ground. In general case, a converter with *N* times conversion ratio will needs *N* switching devices on the wing side and 2*N-2* switching devices on the rectifier side. The circuit derivation will be performed based on ZCS operation of the traditional resonant switched-capacitor converter. The goals of this derivation are to keep ZCS operation feature, minimize inductor number and develop inherent voltage clamping mechanism. Inherent voltage clamping mechanism allows us to remove the additional clamping circuit and increase converter density.

Power loss on magnetic components is usually one of the major contributors to total power loss and they occupy a large area on the PCB. The first goal of circuit derivation will focus on removing the unnecessary inductors in the circuit. To begin with, we analyze the two equivalent circuits of the traditional converter, as shown in Figure 3.3 and Figure 3.4. Based on this analysis, we further break the two equivalent circuits down to multiple individual loops, as shown in Figure

3.5 and Figure 3.6. According to the circuits shown in Figure 3.5 and Figure 3.6, the inductors L_2 and L_4 can be removed without jeopardizing ZCS operation of the converter. Figure 3.8 shows the derived circuit with only three inductors based on Figure 3.7.

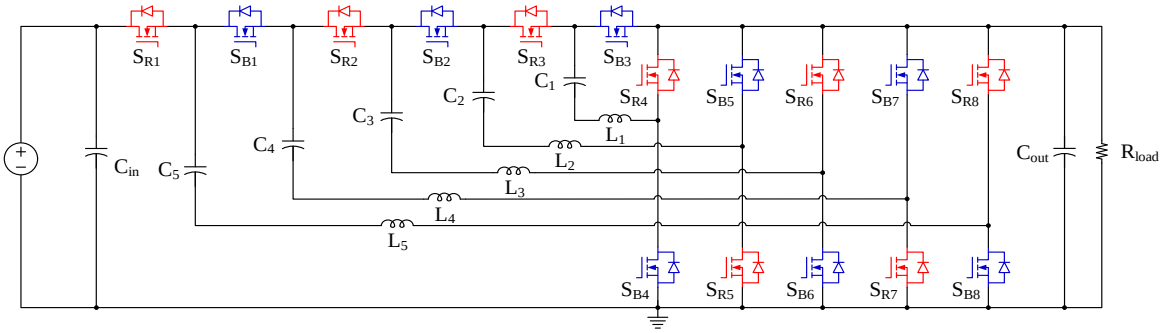

Figure 3.7. Previously proposed converter [103]

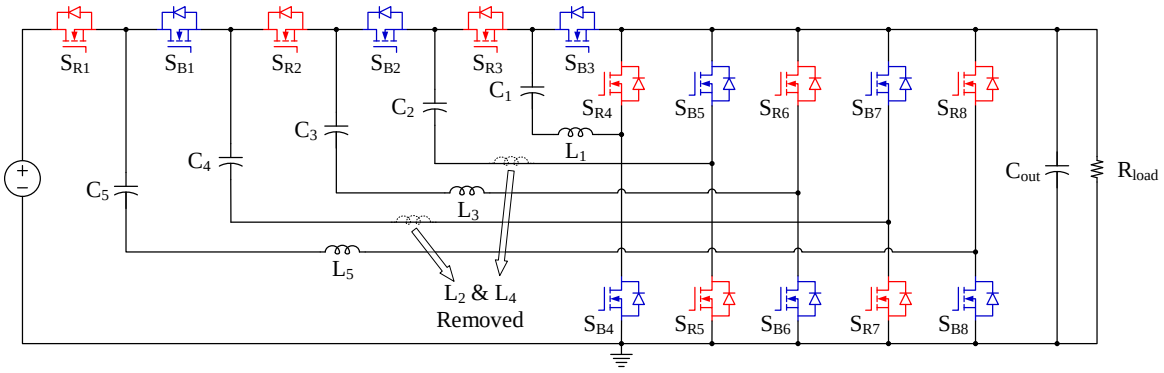

Figure 3.8. Derived circuit with three inductors (C_2=C_4>>C_1=C_3=C_5=C_r)

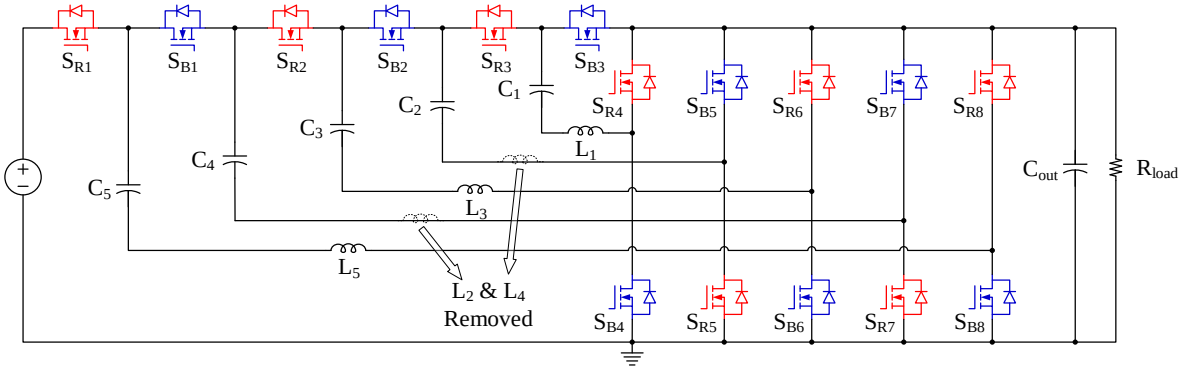

Figure 3.9. Final derived switched-tank converter (C_2=C_4>>C_1=C_3=C_5)

However, simply removing L_2 and L_4 will reduce the resonant inductance L_r by 50%. As a result, the converter's operating frequency will increase by a factor of around 1.4 according to

Eq.3.1. Increased operating frequency will lead to the increase of frequency-related loss, such as gate drive loss and MOSFET C_{oss} loss. In Eq.3.1, ω_d represents damped resonant angular frequency, ω_0 represents resonant angular frequency, and ζ means the damping factor of LC resonant network in the analyzed circuit.

$$\omega_d = \omega_0 * \sqrt{1-\zeta^2} = \sqrt{\frac{1}{L_r C_r} - \frac{R^2}{4}} \quad \text{(Eq. 3.1)}$$

Further circuit derivation targets on eliminating the previously mentioned effects brought by removing L_2 and L_4. And there are two options. First, we can double the capacitance of all capacitor banks shown in Figure 3.8. However, doubling the capacitance means doubling the size of resonant capacitors. And this option does not show a benefit in reducing the converter size. More importantly, inherent voltage clamping mechanism is not enabled by using this method. The circuit still needs additional voltage clamping circuit for wing side devices. Second, class 2 ceramic capacitors can be used in capacitor banks C_2 and C_4 instead of using class 1 capacitors after removing L_2 and L_4. Because class 2 ceramic capacitors offer much higher volumetric efficiency than class 1 ceramic capacitors, the capacitance of C_2 and C_4 can be increased by more than twenty times without sacrificing converter size. With this method, C_2 and C_4 will work as non-resonant capacitors. And the effect of removing L_2 and L_4 can be minimized. The new resonant frequency after the derivation can be calculated using Eq.3.2. Here, C_r means the capacitance of each resonant capacitor bank, L_r means the inductance of the resonant inductor, and C_{nr} means the capacitance of each non-resonant capacitor bank. Comparing with the first option, the voltage ripples across C_2 and C_4 are significantly reduced. As a result, this method adds inherent voltage clamping feature to the circuit shown in Figure 3.7.

$$\omega_0 = \frac{1}{\sqrt{L_r \frac{C_r * C_{nr}}{C_r + C_{nr}}}} \qquad \text{(Eq. 3.2)}$$

Although the non-resonant capacitor banks C_2 and C_4 add inherent voltage clamping feature to the circuit shown in Figure 3.8, long clamping loops in actual PCB design will still lead to some level of voltage overshoot on the wing side devices when the converter loses ZCS operation. This prevents us from using low voltage rating devices on the wing side and applying the proposed circuit to practical industry application.

In order to completely solve the voltage clamping problem, a further circuit derivation has been performed. The final derived circuit is shown in Figure 3.9. Because the clamping loops are significantly reduced in this circuit, low voltage rating devices can be used in the circuit. What's more, the additional clamping circuit is totally removed from the proposed STC. Therefore, density and efficiency will be increased. Figure 3.10 and Figure 3.11 are the two equivalent circuits of the proposed STC. When MOSFETs' turn-on time equals to half resonant period, ZCS operation on all MOSFETs can be achieved.

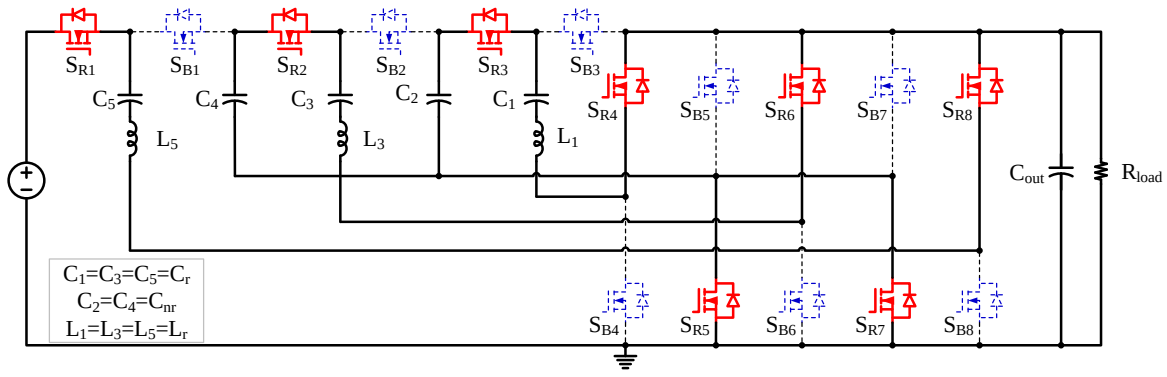

Figure 3.10. Equivalent circuit during state 1

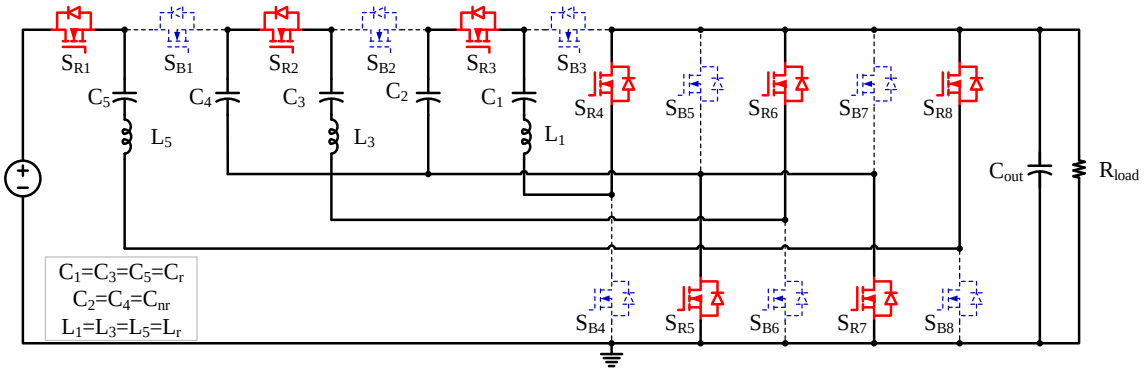

Figure 3.11. Equivalent circuit during state 2

In summary, the number of inductors has been reduced through the circuit derivation. Furthermore, class 1 ceramic capacitors are used in the resonant capacitor banks since they provide superior stability and low loss in the resonant circuit. And class 2 ceramic capacitors are used in the non-resonant capacitor banks because they have high volumetric efficiency. In terms of voltage clamping of wing side MOSFETs, the final derived switched-tank converter has minimized voltage clamping loops and does not require additional clamping circuit. Thus, the goal of circuit derivation has been achieved.

3.2.2. Resonant Tank Design Considerations

In order to achieve high power density and good efficiency, proper selection of resonant inductor and capacitor is very critical. In terms of inductor design, we need to estimate the inductor peak current to avoid core saturation. On the other hand, the main consideration for capacitor banks design lays on their voltage ripple and current capability. Besides, a requirement on the capacitance of C_r will be evaluated in this section.

Here, we assume the inductor current has a maximum value I_{max} (when attenuation factor α equals to zero). Then the inductor current can be represented using Eq.3.3. Thus we can easily get the relationship between inductor average current, output power and output voltage, as shown in Eq.3.4.

$$I_L(t) = I_{max} * e^{-\alpha t} * sin(\omega_d t) \quad \text{(Eq. 3.3)}$$

$$I_{L\_avg} = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} I_{max} * e^{-\alpha t} * sin(\omega_d t)\, dt = \frac{P_o}{3V_{o\_avg}} \quad \text{(Eq. 3.4)}$$

By reforming Eq.3.4, I_{max} can be represented as an equation of switching frequency f_s, output power P_o, output voltage V_{o_avg}, attenuation factor α and damped natural frequency ω_d. The equation is derived as Eq.3.5. Then we plug Eq.3.5 into Eq.3.3, the instantaneous inductor current can be calculated, as shown in Eq.3.6.

$$I_{max} = \frac{T_s * P_o}{2V_{o\_avg} * \int_0^{\frac{T_s}{2}} e^{-\alpha t} * sin(\omega_d t)\, dt} \quad \text{(Eq. 3.5)}$$

$$I_L(t) = \frac{T_s * P_o * e^{-\alpha t} * sin(\omega_d t)}{2V_{o\_avg} * \int_0^{\frac{T_s}{2}} e^{-\alpha t} * sin(\omega_d t)\, dt} \quad \text{(Eq. 3.6)}$$

With the information of inductor instantaneous current, by performing derivation on Eq.3.6 and letting the equation equals to zero, the time t_{peak} that inductor current reaches its peak value can be obtained. In other words, by means of Eq.3.7, the value of t in Eq.3.6 can be calculated when the inductor current reaches the maximum, denoted as t_{peak}. With the previous analysis, the inductor peak current can be calculated with the use of t_{peak}, as shown in Eq.3.8.

$$\frac{d}{dt} I_L(t) = 0 \quad \text{(Eq. 3.7)}$$

$$I_{L\_peak} = I_{max} * e^{-\alpha t_{peak}} * sin(\omega_d t_{peak}) \quad \text{(Eq. 3.8)}$$

Since inductor current information has been obtained. By integrating the current over half switching period, voltage ripple on the capacitor banks can be calculated. The equation is shown in Eq.3.9.

$$\Delta V = \frac{\Delta Q}{C} = \frac{1}{C}\int_0^{\frac{T_s}{2}} \frac{T_s * P_o * e^{-\alpha t} * sin(\omega_d t)}{2V_{o\_avg} * \int_0^{\frac{T_s}{2}} e^{-\alpha t} * sin(\omega_d t)\, dt} dt \quad \text{(Eq. 3.9)}$$

So far, the voltage ripple information on both non-resonant capacitor banks and resonant capacitor banks has been calculated. However, in order to get more detailed voltage information such as instantaneous voltage waveform and DC voltage bias on capacitor banks, analysis on equivalent circuits during different operating modes would be necessary. For the proposed switched-tank converter, all the resonant loops can be simplified into two types of equivalent circuits, as shown in Figure 3.13 and Figure 3.12. Figure 3.12 shows the equivalent circuit when non-resonant capacitor bank is not the in the loop. Figure 3.13 shows the loop with both resonant capacitor bank and non-resonant capacitor bank. Here, R_{loop1} and R_{loop2} represent the total resistance of different switching loop, which includes MOSFET turn ON resistance, inductor dc resistance and capacitor equivalent series resistance (ESR). For the circuit shown in Figure 3.12, two differential equations in Eq.3.10 will be used to get capacitor voltage waveform. Eq.3.11 shows the solved capacitor voltage information. Similarly, by solving differential equations shown in Eq.3.12, resonant capacitor voltage waveform can be calculated as Eq.3.13. Also, the voltage waveform of the non-resonant capacitor can be easily calculated. In order to verify the correctness of the equations, simulated waveforms are used to compare with equation calculated waveforms, as shown in Figure 3.14.

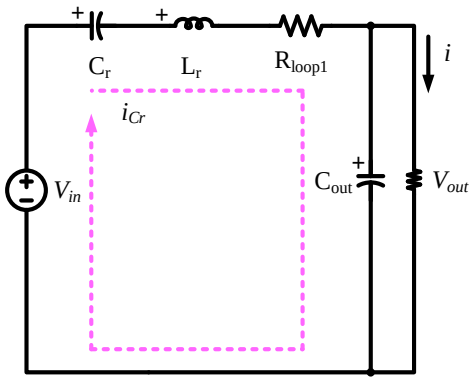

Figure 3.12. Circuit without non-resonant capacitor in the loop

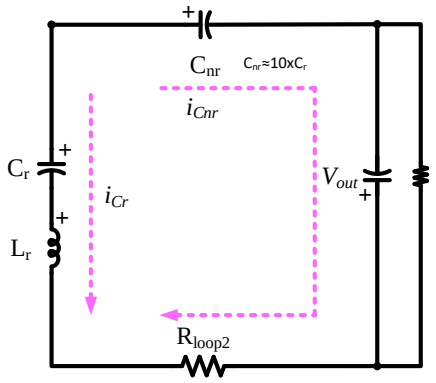

Figure 3.13. Circuit with non-resonant capacitor in the loop

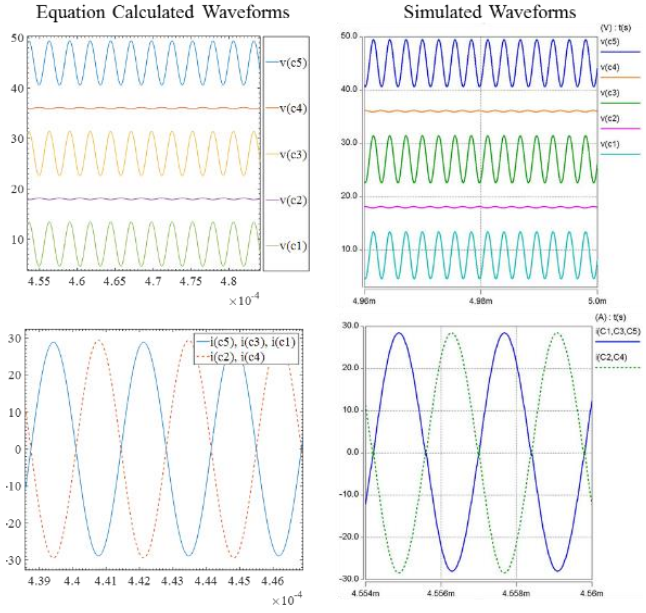

Figure 3.14. Compare calculated and simulated waveforms to validate the derived equations (6x STC, 54V input, 450W output)

Besides the previous analysis on inductor peak current and capacitor voltage ripple, the following analysis also provides guidelines on how to design the resonant tanks. Since the resonant capacitance and inductance values dominant the resonant operation of the proposed STC, it is very necessary to make sure the resonant tanks are properly designed. According to Eq.3.14, the capacitor banks' capacitance values and their voltage ripples are related to switching frequency and power rating of the converter. Here, ΔV is peak-to-peak voltage ripple on capacitor and f_s is switching frequency. This means capacitor voltage ripple will be affected by inductance value in the circuit. Because resonant capacitors have much lower capacitance than that of the non-resonant capacitors, resonant capacitors will have much larger voltage ripples than non-resonant capacitors. Make sure the maximum voltage on resonant capacitors is within their safe operating range becomes the key point to ensure normal operation of the proposed STC. Assume $\Delta V = 2V_o$, by plugging previously derived switching frequency f_s into Eq.3.14, the minimum resonant capacitance, which means C_1, C_3 and C_5 in the 6x STC, can be calculated using Eq.3.15.

$$\frac{1}{2} C * \Delta V^2 * f_s > \frac{1}{6} P_{out} \quad \text{(Eq. 3.10)}$$

$$C_{r\_min} = \frac{L_r \sqrt{C_{nr}(4L_r\pi^2 P_o^2 + 36 C_{nr} V_o^4 - C_{nr}\pi^2 P_o^2 R^2)}}{12 L_r V_o^2 - 3 C_{nr} V_o^2 R^2} - \frac{6 C_{nr} L_r V_o^2}{12 L_r V_o^2 - 3 C_{nr} V_o^2 R^2} \quad \text{(Eq. 3.11)}$$

3.3. Influence from Tolerances of Resonant Components

The proposed converter processes zero-current switching capability. In ideal case, all the resonant capacitors and inductors are identical. When the converter operates under steady state, all the resonant loops have almost the same resonant frequency if the capacitance of non-resonant capacitors is large enough. For example, C_{nr} >10*C_r. However, even with high capacitance non-resonant capacitors, in practice, we still need to consider the problem caused by tolerances of resonant inductors and capacitors. In general, tolerance of inductors is ±10% [106]. And tolerance

of capacitors can range from ±1% to ±20% [107]. With strict sorting procedure and improved manufacturing processes, their tolerances can be well controlled and tightened. If we assume the tolerance of the resonant components has been controlled very well, then -5% to +5% capacitance and inductance variance would be reasonable to be considered in the design. Note that the analytical methodology in this section is also valid when the resonant components have other tolerance values.

$$\begin{cases} v_{Cr}(t) + R_{loop1}C_r\dfrac{dv_{Cr}(t)}{dt} + L_rC_r\dfrac{dv_{Cr}(t)^2}{dt^2} = V_{in} - V_{out} \\ i_{Lr}(t) = i_{Cr}(t) = C_r\dfrac{dv_{Cr}(t)}{dt} \end{cases} \quad \text{(Eq. 3.12)}$$

$$v_{Cr}(t) = [V_{Cr}(0) - (V_{in} - V_{out})] * e^{-\frac{R_{loop1}}{2L_r}t} * cos(\omega_d t) + (V_{in} - V_{out}) \quad \text{(Eq. 3.13)}$$

$$\begin{cases} v_{Cr}(t) + L_rC_r\dfrac{dv_{Cr}(t)^2}{dt^2} - v_{Cnr}(t) + V_{out} = R_{loop2} * C_{nr}\dfrac{dv_{Cnr}(t)}{dt} \\ i_{Cnr}(t) = -i_{Cr}(t) = C_{nr}\dfrac{dv_{Cnr}(t)}{dt} = -C_r\dfrac{dv_{Cr}(t)}{dt} \\ i_{Lr}(t) = i_{Cr}(t) = C_r\dfrac{dv_{Cr}(t)}{dt} \end{cases} \quad \text{(Eq. 3.14)}$$

$$\begin{aligned} v_{Cr}(t) = &\left[\frac{C_{nr} * [v_{Cr}(0) - v_{Cnr}(0) + V_o]}{C_{nr} + C_r}\right] * e^{-\frac{R_{loop2}}{2L_r}t} * cos(\omega_d t) \\ &+ \left[\frac{C_{nr}}{C_{nr} + C_r}(v_{Cnr}(t_0) - V_o) + \frac{C_r}{C_{nr} + C_r}v_{Cr}(t_0)\right] \end{aligned} \quad \text{(Eq. 3.15)}$$

When the damped resonant angular frequencies of different resonant loops are mismatched, inductor current cannot be reset back to zero without proper deadtime. Then the circuit will operate at a new steady state that has considerable circulating power. And the circulating power will pull down the efficiency of the proposed circuit. That is to say, deadtime should be long enough to make sure the inductor current can be reset back to zero before the start of next operating state. Although resonant components L_1, L_3, L_5, C_1, C_3 and C_5 have different component tolerances, one

example would be enough to demonstrate how to properly select the deadtime and achieve ZCS operation. Here, we assume -5%, 0% and -5% tolerance on L_1, L_3 and L_5, respectively. Also, for C_1, C_3 and C_5, the tolerances are -5%, 0% and -5%, respectively. Therefore, resonant branch 1 and 3 have higher resonant frequency than branch 2, as shown in Figure 3.15. In this example, the resonant branch with lowest resonant frequency is selected as a reference for control. In other words, all the S_{Rx} MOSFETs are turned off when all inductor current reach or cross zero points. Details will be included in the following analysis. As shown in Figure 3.15 to Figure 3.18, there are four commutation states during half switching cycle.

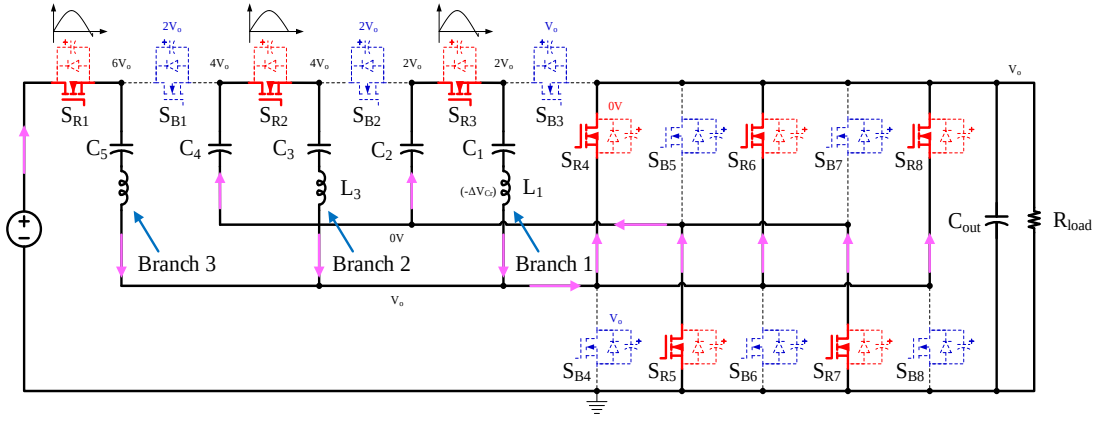

Figure 3.15. State A

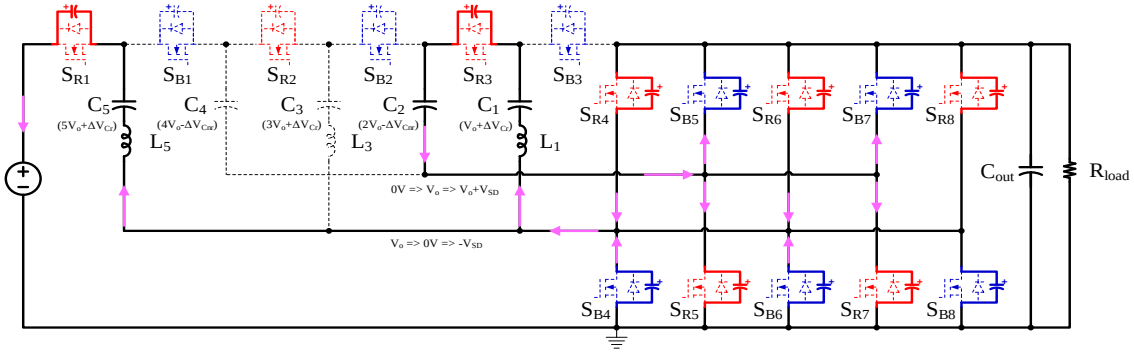

Figure 3.16. State B

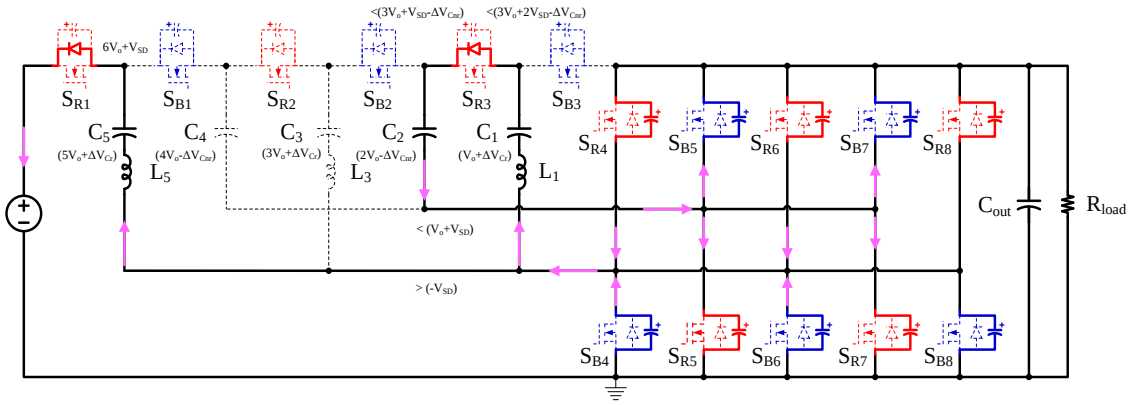

Figure 3.17. State C

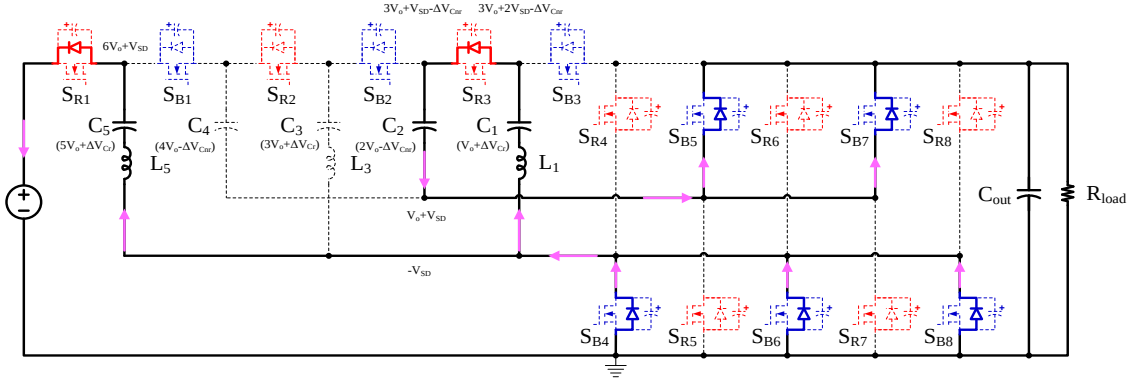

Figure 3.18. State D

State A: Converter operates under steady state. All red devices are conducting. The resonant capacitors and inductors in the circuit start to store energy while the non-resonant capacitors start to release energy.

State B: All the S_{Rx} MOSFETs are turned off during this state. Because resonant branch 1 and 3 have higher resonant frequency than the other branches, when the current in branch 2 reaches zero, the current in branch 1 and 3 have already crossed the zero point. Then the inductor current in branch 1 and 3 starts to charge output capacitor voltage of S_{R1} and S_{R3} to negative and output capacitor voltage of $S_{R4\text{-}8}$ to $V_o + V_{SD}$. Here, V_o represents output voltage of the proposed converter and V_{SD} means the voltage drop of MOSFET's body diode when the diode is conducting. At the same time, output capacitors of $SB_{4\text{-}8}$ start to discharge.

State C: Body diode of MOSFETs S_{R1} and S_{R3} are turned on. During this state, body diodes of rectifier side devices will not conduct. When V_{ds} of MOSFET S_{B4} drops below $V_o - \Delta V_{Cr}$, the current flow through L_1 and L_5 will start resetting back to zero.

State D: The process of charging/discharging the output capacitors of the rectifier MOSFETs is completed. During this state, the current flow through inductor L_1 and L_5 will be reset back to zero at the fastest speed.

In order to achieve good performance, it is necessary to reset all inductor current back to zero during the deadtime. Assume the current value that needs to be reset is I_{rec} and L_r represents the resonant inductance. ΔC_r and ΔC_{nr} represent voltage ripple on resonant capacitors and non-resonant capacitors, respectively. In Eq.3.16, k is the factor that gives the calculated deadtime a margin to make sure it fits different operating condition. In general, k ranges from 1 to 2 and 2 is preferred. As a result, a minimum deadtime t_{dead_min} can be estimated.

$$t_{dead\_min} = \frac{k * I_{rec} * L_r}{2V_o + 3V_{sd} - \frac{1}{2}\Delta C_{nr} - \frac{1}{2}\Delta C_r} \quad \text{(Eq. 3.16)}$$

3.4. Power Loss Analysis and Design Methodology

3.4.1. Switching Device and Gate Voltage Selection

When the proposed STC has maximum 60V input, voltage stress on the switching devices are also maximum. In the 6x STC, voltage stress on S_{B1}, S_{R2}, S_{B2} and S_{R3} is 20V, while the stress on other switching devices is 10V. As a result, there are multiple 25V/30V switching devices that can be used to build the converter. In terms of GaN devices, only EPC has low voltage rating MOSFET available, which is 30V device. On the other hand, Infineon optimos5 provides both 25V and 30V Si MOSFET. In addition, the performance of switching devices with higher voltage rating (i.e. 60V) has been evaluated to show that 25V/30V devices are the best choice for the proposed

converter. In order to have a fair comparison, here we assume all the switching devices in the converter are the same part number. As known to all, when higher gate drive voltage has been provided to the gate, the MOSFET's on-state resistance is lower, which will bring the benefit of lower semiconductor conduction loss. However, high gate voltage will lead to high gate drive loss. Therefore, an evaluation on proper gate drive voltage selection is necessary in order to achieve the best performance. For EPC GaN, 5V gate drive voltage is the only choice. On the other hand, Infineon Si accepts very wide range gate voltage, which is 0 to 16V. Here, two typical values 5V and 10V are considered. This analysis includes five silicon MOSFETs and one eGaNFET that have either low $R_{ds(on)}$ or Q_g among 25V and 30V devices. Besides, two 60V devices are included in this analysis. Their key parameters used in the analysis can be found in Table 3.1. Since there are 16 switching devices in the converter, their footprint occupation information is also provided, as shown in Table 3.2. If eGaNFETs are used to build a 6x STC, they only take 16.5% and 10.4% footprint on an 8th brick board and a quarter brick board, respectively. It is worth mentioning that because the CPUs spending most of their time in 20–50% CPU utilization range [108], 20% to 50% load is determined to be the most common operating range of the proposed 6x STC, the design will be based on this condition.

Table 3.1. Parameters of Switching Devices Used in Analysis

Part#	Vgs (V)	Q_g (nC)	R_{ds_on} (mΩ)	fs (kHz)	C_{oss}@9V (nF)	C_{oss}@18V (nF)
BSC0501NSI (30V 100A)	5	12.5	1.82	387	0.88	0.5
	10	24	1.5	387	0.88	0.5
BSC0500NSI (30V 100A)	5	20	1.3	387	1.5	0.79
	10	39	1.1	387	1.5	0.79
BSZ0500NSI (30V 40A)	5	20	1.4	387	1.5	0.79
	10	39	1.2	387	1.5	0.79
BSZ013NE2LS5I (25V 40A)	5	18	1.25	387	1.7	1.05
	10	37	1.1	387	1.7	1.05
BSZ017NE2LS5I (25V 40A)	5	11.5	1.78	387	0.95	0.62
	10	22	1.45	387	0.95	0.62
EPC2023 (30V 90A)	5	19	1.15	387	1.91	1.55
CSD18532Q5B (60V 172A)	5	23	3.3	387	1.1	0.65
	10	42	2.5	387	1.1	0.65
IPT007N06N (60V 300A)	5	120	0.85	387	9	6
	10	216	0.66	387	9	6

Table 3.2. Switching Device Footprint Comparison

Part#	Length (mm / inch)		Width (mm / inch)		Footprint of 16 Devices (mm^2 / $inch^2$)	
BSC0501NSI	6.15	0.242	5.32	0.209	523.49	0.81
BSC0500NSI						
BSZ0500NSI						
BSZ013NE2LS5I	3.3	0.13	3.3	0.13	174.24	0.27
BSZ017NE2LS5I						
EPC2023	6.05	0.238	2.3	0.091	222.64	0.346

The power loss on the semiconductor includes three parts. First, gate drive loss. When the gate drive voltage is V_{gs}, total gate charge is Q_g and devices turn-on and off at frequency f_s, the gate drive loss can be calculated using Eq.3.17. Second, semiconductor output capacitor loss. When the MOSFETs turn off, their output capacitors with capacitance C_{oss} will be charged to V_{ds},

and the energy in output capacitors will be dissipated through the devices themselves when the MOSFETs turn on. This part of power loss can be estimated using Eq.3.18. Third, semiconductor conduction loss. The drain-to-source on state resistance of one MOSFET is $R_{ds(on)}$. When the rms value of current flow through it, power loss can be calculated using Eq.3.19. Finally, by adding gate drive loss, output capacitor loss and conduction loss together, the total power dissipation on the semiconductor can be estimated, as shown in Eq.3.20.

According to Figure 3.19, when the converter operates below 450W, total semiconductor loss is less when 5V gate drive voltage has been used instead of 10V. When the converter operates between 450W and 600W, 10V would be a better choice because 10V gate voltage brings the benefit of less conduction loss. In this specific design, because the desired typical operating point is around 20% to 50% of the full load, so the high-efficiency operation needs to be achieved in this region. As a result, 5V has been selected to drive all the MOSFETs. Note that the assumption of this analysis is based on 25°C. According to Figure 3.20, the performance of high voltage rating devices is not as good as 25V/30V devices due to their high $R_{ds(on)}$ or C_{oss} values.

$$P_{gate} = V_{gs} Q_g f_s \quad \text{(Eq. 3.17)}$$

$$P_{coss} = C_{oss} V_{ds}^2 f_s \quad \text{(Eq. 3.18)}$$

$$P_{cond} = i_{rms}^2 * R_{ds(on)} \quad \text{(Eq. 3.19)}$$

$$P_{semi} = P_{gate} + P_{coss} + P_{cond} \quad \text{(Eq. 3.20)}$$

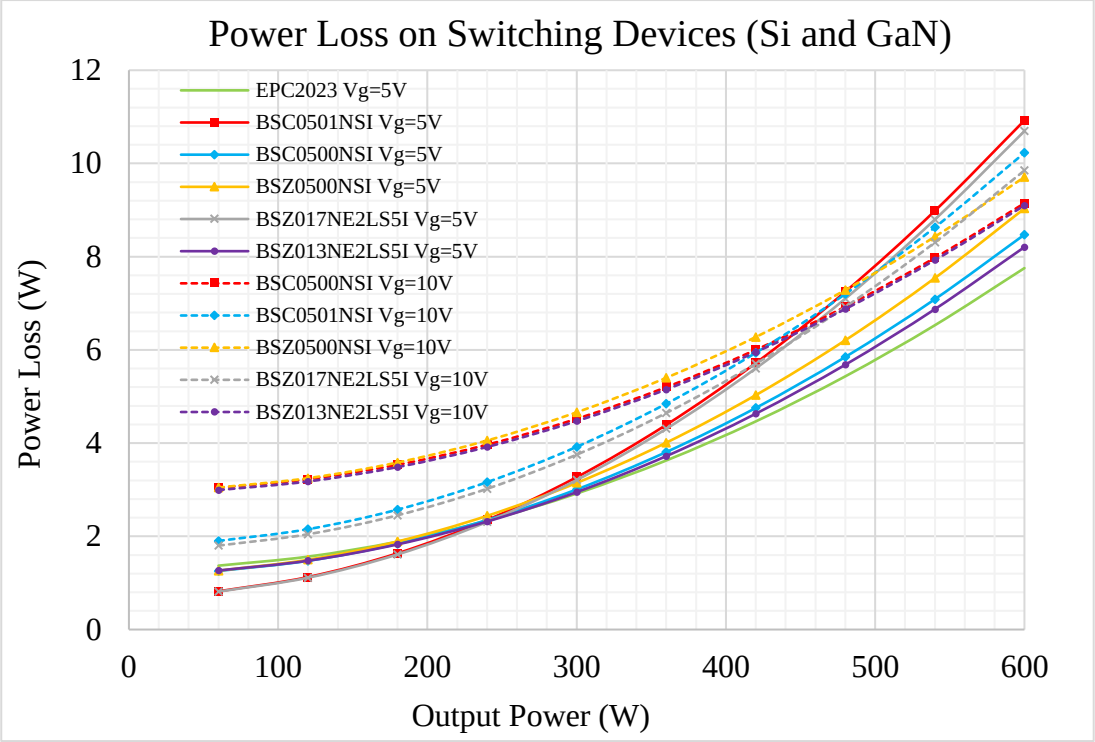

Figure 3.19. Total power loss on switching devices in 6x STC

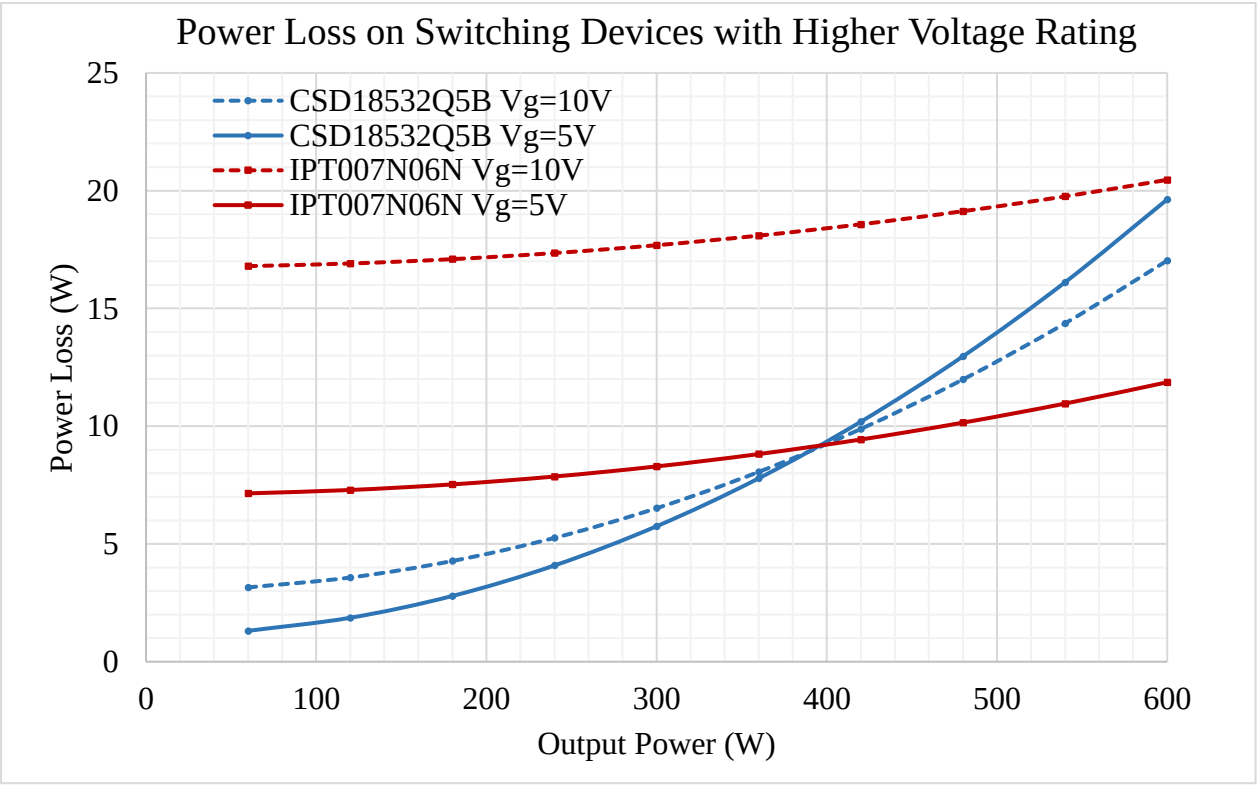

Figure 3.20. Higher voltage rating devices compromise performance of the proposed 6x STC

3.4.2. Semiconductor Power Loss Breakdown and Comparison

Since 5V has been chosen as the gate voltage for both eGaNFETs and Silicon MOSFETs, all the comparison and analysis will be performed based on this assumption. The power on MOSFETs can be divided into MOSFET conduction loss, MOSFET output capacitor loss and gate drive loss. According to Table 3.3, two different output capacitance values will be considered in the power loss breakdown and comparison part. This is because there are two different voltage stress among all the switching devices in the proposed 6x STC. When the input voltage is 54V, the two different voltage stress values are 9V and 18V. Here, we assume that converters built with different MOSFETs have the same operating condition when they deliver the same power to the output. In Figure 3.19, when the designed converter delivers less than 200W power, converter built with BSZ017NE2LS5I has less power loss than that built with other MOSFETs. However, as the power output of the STC goes high, it is very obvious that the conduction loss becomes significant. On the other hand, EPC2023 and BSZ013NE2LS5I enable the lowest semiconductor loss and their analyzed losses are comparable to each other. Nevertheless, Figure 3.19 is not detailed enough for us to know what makes the power loss different between Si-based and GaN-based converters. So further power loss breakdown and comparison has been performed. From Table 3.3 we can tell that EPC2023 and BSZ013NE2LS5I have similar Q_g value, so the power loss difference on gate dive is very minimum, less than 50mW, as shown in Figure 3.21. In terms of C_{oss} loss, eGaNFET has a little bit more loss than Si MOSFET due to higher C_{oss}. However, the on-state resistance of GaN device is lower than Si device, which gives eGaNFET the chance to compete with Si MOSFET. Although the benefits that GaN's lower $R_{ds(on)}$ brought cannot neutralize its weakness on Q_g and C_{oss} at low power, it allows GaN-based converter has higher efficiency than Si-based

converter when the converter works at heavy load. In summary, EPC GaN is preferred over Si due to its low $R_{ds(on)}$.

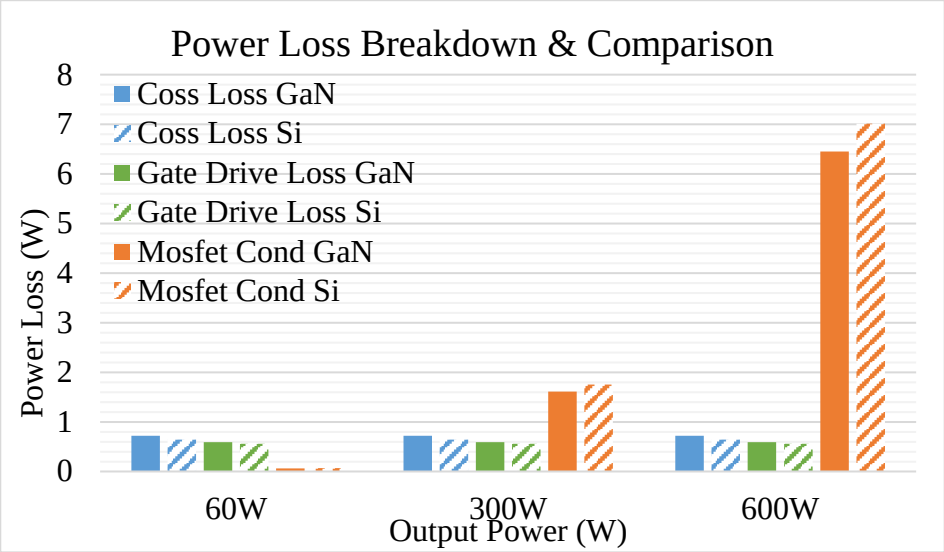

Figure 3.21. Power loss estimation and power loss breakdown comparison between GaN and Si based converter

3.4.3. Planar Inductor Design and Other Losses

In addition to selecting proper switching devices and estimating power loss on semiconductors, passive components' power loss optimization and estimation are also very important. This section focuses on inductor power loss optimization and estimation, capacitor power loss estimation and PCB power loss estimation. After all the power loss information, total loss of the converter can be calculated. At last, a power loss breakdown will be presented to interpret loss distribution of the proposed 6x STC. Inductor design is the key part to achieve high power density and high efficiency of the proposed STC.

In order to achieve superior performance, our main targets should be minimizing the core loss and copper loss. Also, low profile and small footprint occupation are the first priorities during the design. Because these two aspects directly affect the power density of the proposed converter. Unlike DC inductors in traditional dc-dc converters, the inductors in the proposed converter are

AC inductors. Thus, traditional DC inductor design method won't work in our case. In order to use the minimum size of magnetic components, inductors with less than 100nH inductance are preferred. Thus, there are two options, surface-mount inductor and planar inductor. In Figure 3.22, surface-mount inductors and planar inductor cores have been placed together to carry out a volumetric comparison. Although surface-mount inductor is 23.73mm^3 smaller than planar inductor (UI core), it makes the prototype 3.8mm thicker since it can only be placed on one side of the PCB. As a result, the planar inductor will be used in the prototype design. Furthermore, planar inductors with less than 100nH inductance allow us to use half-turn winding, which brings benefits of minimum copper loss and PCB area usage.

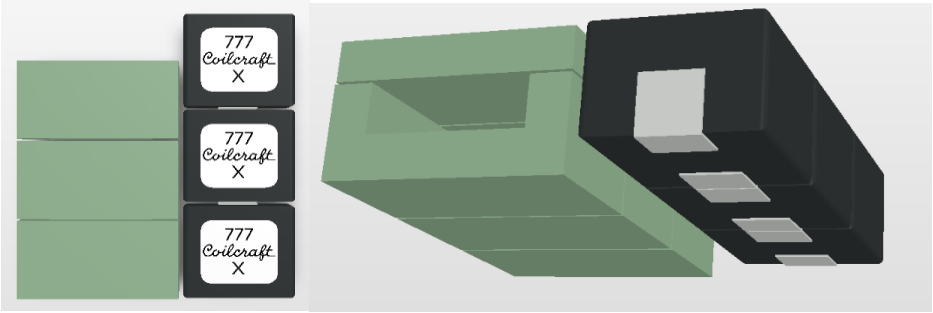

Figure 3.22. Volumetric comparison between surface-mount inductor and planar inductor

In Figure 3.23, a non-optimized planar inductor structure has been proposed in the first place. However, if there is no special optimization on the inductor winding, fringing flux spreading from the air gap will lead to significant copper loss. Therefore, the orthogonal winding structure has been adopted to remit the power loss due to fringing effect, as shown in Figure 3.24. By taking the air gap as the center of a circle, and take "r" as radius, then removing the inductor winding copper within this circle, the orthogonal winding structure has been realized. Since the orthogonal winding structure will increase DC copper loss in order to reduce AC copper loss, there should exist an optimal "r" that makes the total copper loss minimum. So FEA software has been used to

find out the optimal inductor winding design by sweeping “r” in FEA software. Figure 3.25 shows that when the radius equals to 1.65mm, total loss of the planar inductors become the lowest.

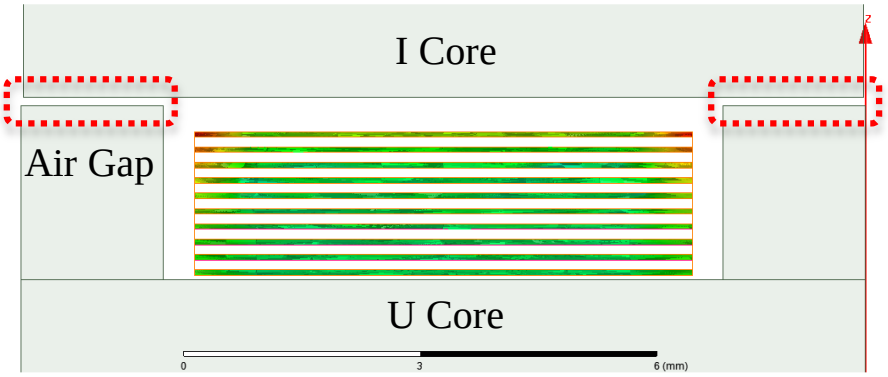

Figure 3.23. Planar inductor without orthogonal winding structure will lead to significant copper loss due to fringing effect

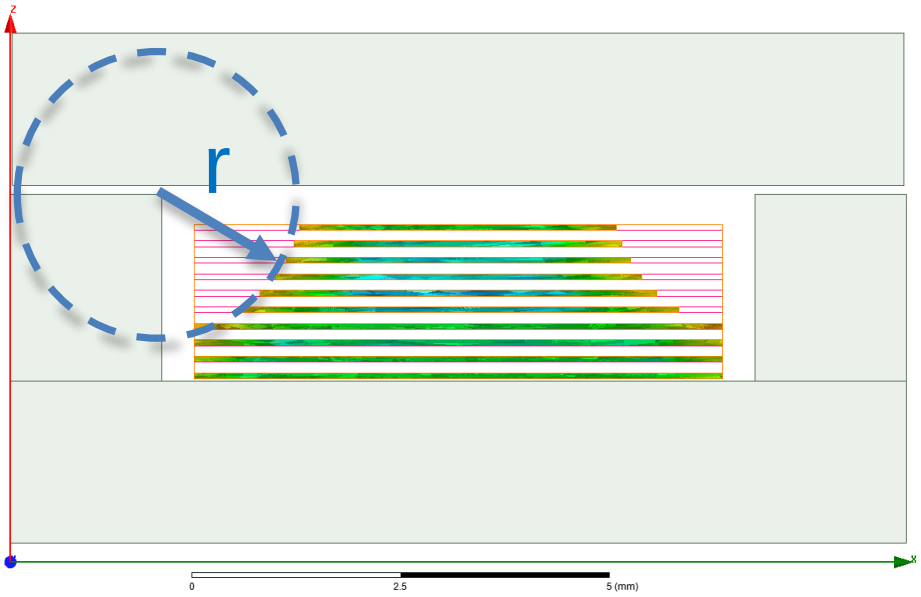

Figure 3.24. Planar inductor with orthogonal winding structure allows minimized power loss on inductor

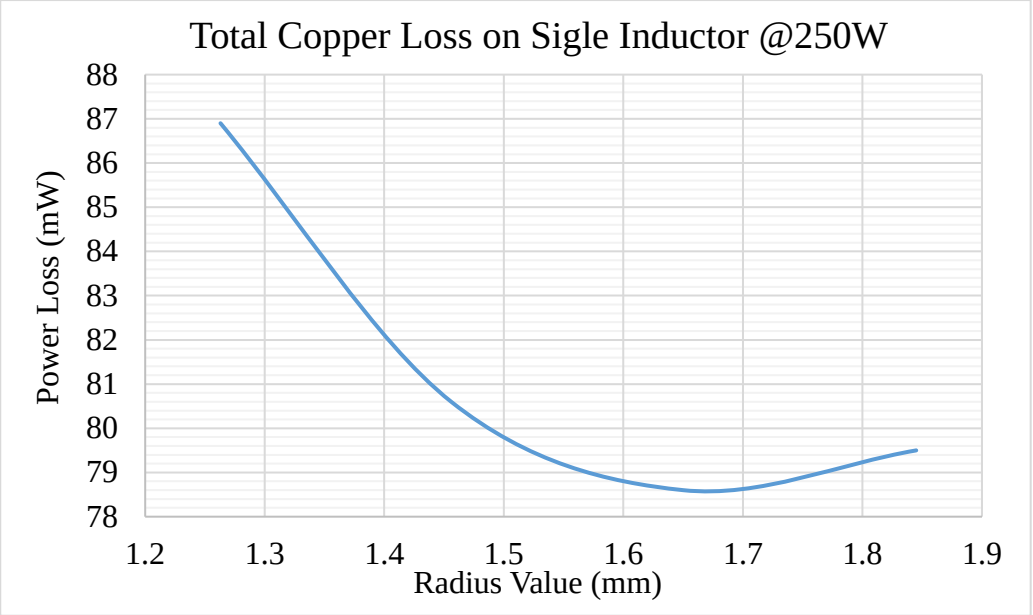

Figure 3.25. FEA software simulated total copper loss on single planar inductor

Power loss on ceramic capacitors is also a vital part of the total loss. Capacitor loss includes resonant capacitor loss, non-resonant capacitor loss, input capacitor loss and output capacitor loss. Assume r_{cap} is the ESR of a ceramic capacitor, N_{cap} is the capacitor number in one capacitor bank. And i_{rms_cap} represents the RMS value of current that flows through one capacitor bank. Then capacitor loss can be calculated through Eq.3.21. The ESR is affected by DC bias of the capacitor and frequency of the current that flows through it, and its value can be obtained via different manufactures' online simulation tools such as K-SIM (Kemet), SimSurfing (Murata) and SEAT (TDK).

At last, PCB loss is also a source of total power loss. Figure 3.26 shows a typical layout of the proposed 6x STC. In this layout, high-frequency AC current exists on more than 80% area of the board. So it is reasonable to concern that all these high-frequency current loops may result in considerable power loss on PCB. Hence, PCB power loss estimation is necessary. Further, in order to make sure that the board can meet the requirement of current capability, hotspot inspection has been performed along with the power loss estimation. As shown in Figure 3.27, power loss

distribution and estimation have been carried out via FEA software. According to the simulation result, when the GaN-based prototype operates at 450W, power loss due to PCB is around 4.1W. And there is no obvious hot spot can be observed on the board.

$$P_{cap} = i_{rms\_cap}^2 * \frac{r_{cap}}{N_{cap}} \qquad \text{(Eq. 3.21)}$$

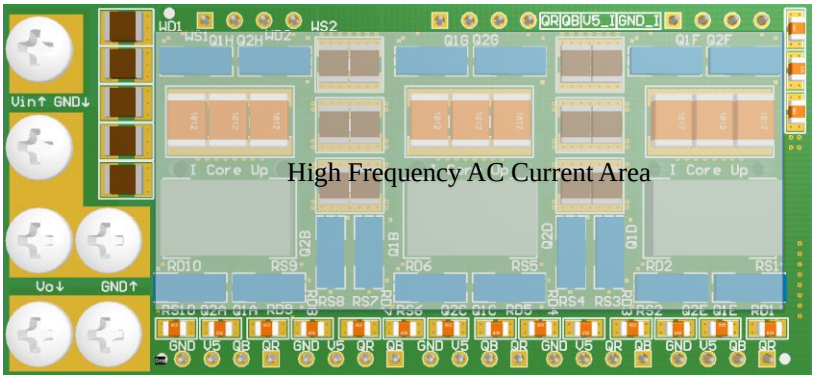

Figure 3.26. High frequency AC current exists all over the PCB

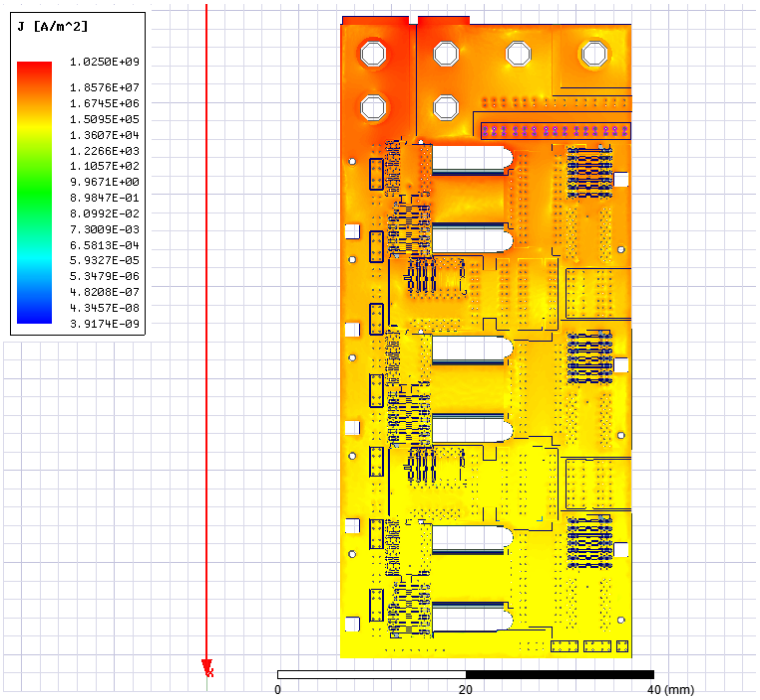

Figure 3.27. FEA software simulated PCB power loss distribution for GaN based

So far, both active components' and passive components' power loss have been estimated. The total power loss of the designed prototype can be calculated using Eq.3.22. In Figure 3.28, the

total power loss breakdown elaborates that the major contributors to total loss are MOSFET conduction loss, PCB loss and planar inductor core loss. In terms of inductor core loss, the selected UI core is the smallest off the shelf core that can be found during the design. This means with customized core and proper core shape optimization in the future, inductor core loss can be minimized. On the other hand, because the designed prototype only uses 10 layer PCB, which is much less than standard industry design, the PCB loss is not optimized.

$$P_{loss\_total} = P_{semi} + P_{cap} + P_{inductor} + P_{pcb} \quad \text{(Eq. 3.22)}$$

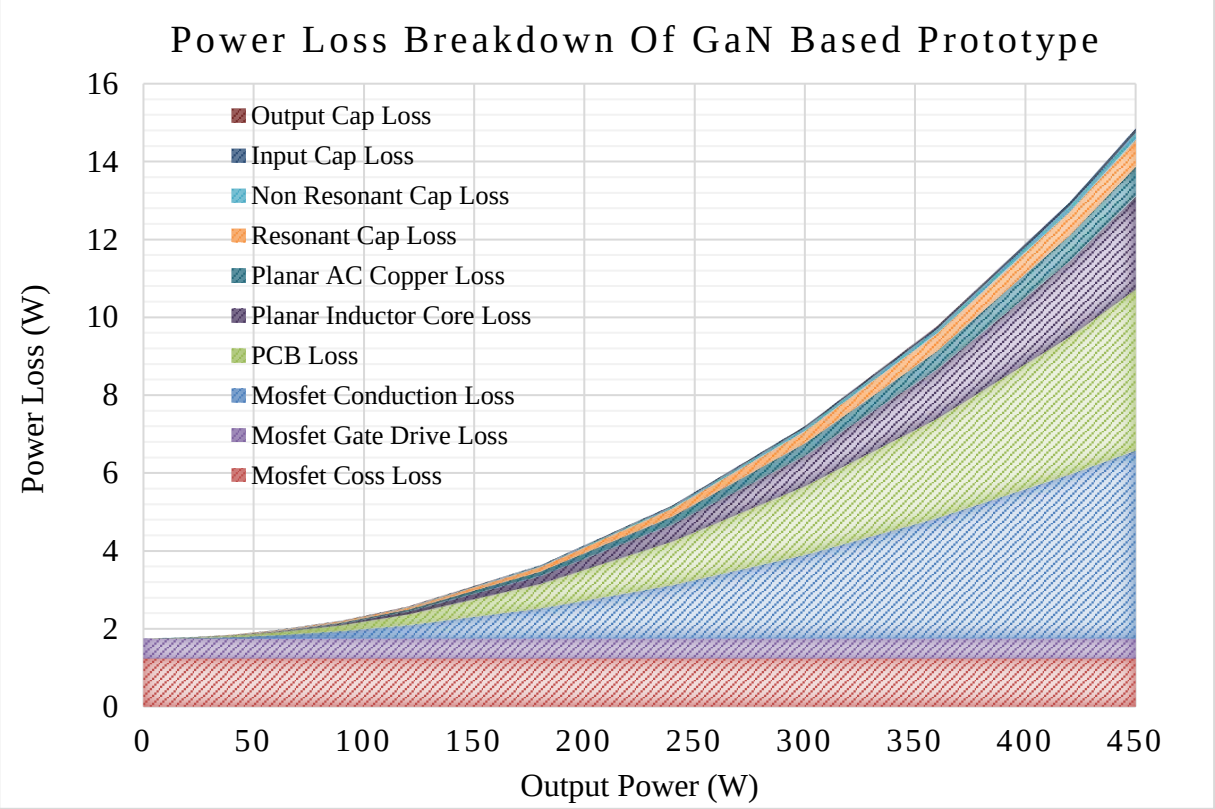

Figure 3.28. Power Loss Breakdown of GaN Based Prototype

3.5. Simulation and Experimental Results

Simulation has been performed to validate the operating principle of the proposed STC with six times conversion ratio. Table 3.3 shows the key parameters used to simulate the circuit. When the circuit operates at steady state, all MOSFET current waveforms are half sine and all the

inductor current waveforms are sinusoidal AC current without any DC bias, as shown in Figure 3.29. Figure 3.30 shows the resonant capacitor and non-resonant capacitor voltage waveforms. When there is 60V at the input of the proposed 6x STC, the average DC voltage on capacitors C_5 to C_1 are 50V, 40V, 30V, 20V and 10V, respectively. In Figure 3.31 and Figure 3.32, voltage stresses on both synchronous rectifier side and wing side devices are observed. According to the simulation, all the rectifier side MOSFETs have the same voltage stress, which is 10V. On the contrary, wing side MOSFETs have two different stresses, namely 10V and 20V.

Table 3.3. Parameters Used in The Simulation

Description	Items	Values
Input voltage	V_{in}	60 V
Output voltage	V_{out}	10 V
Resonant capacitor	C_r	4.7 μF
Non-Resonant capacitor	C_{nr}	100 μF
Resonant inductor	L_r	50 nH
Resistor Load	R_{load}	0.167 Ω
Resonant frequency	f_r	367.1kHz
Switching frequency	f_s	359.7kHz

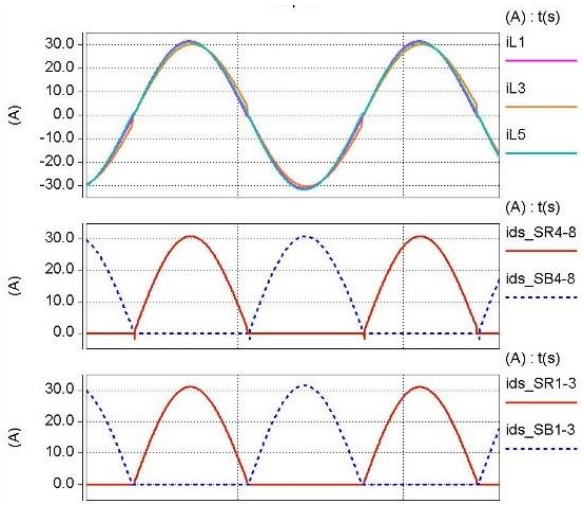

Figure 3.29. Inductor and MOSFET current waveform

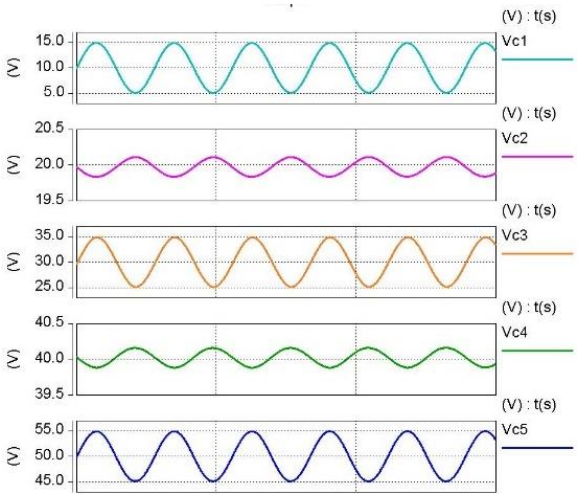

Figure 3.30. Capacitor voltage waveform

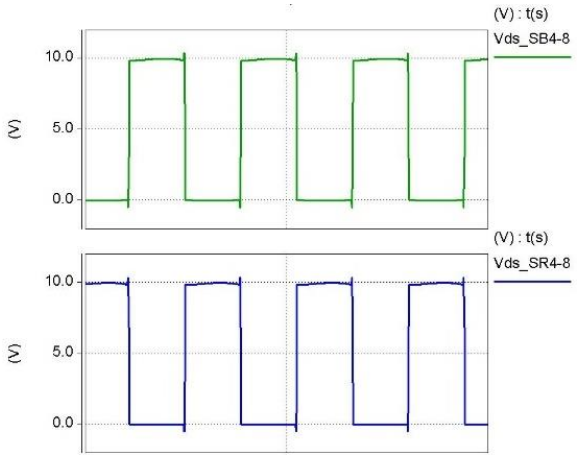

Figure 3.31. Synchronous rectifier side device voltage waveform

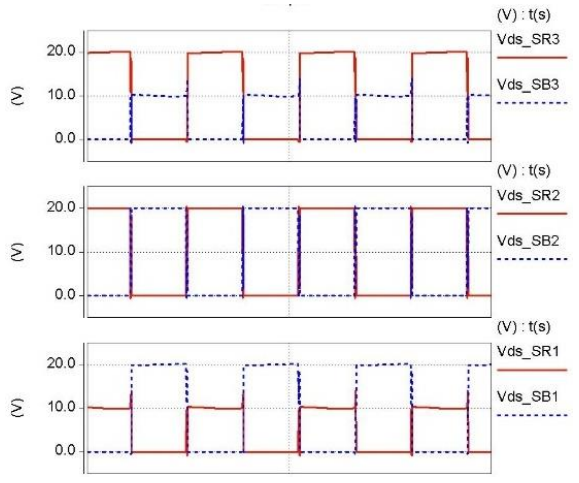

Figure 3.32. Wing side device voltage waveform

A first version prototype based on the traditional resonant switched-capacitor topology (with five resonant inductors) has been built to verify the ZCS operation of both traditional and derived switched-tank converter. By replacing two resonant tanks with non-resonant tanks, the circuit configuration can switch from traditional circuit to derived STC. The top and bottom view can be found in Figure 3.33 and Figure 3.34. The voltage conversion ratio of this prototype is 6:1. With nominal/maximum voltage 54V/60V, the designed converter is capable of delivering 450W nominal and 600W maximum power. Because the main purpose of building this converter is to validate the functionality of the proposed circuit, its efficiency and power density will not be evaluated. With the experience from the first prototype, a second GaN-based 450W (600W max) switched-tank converter has been designed to achieve high power density and high efficiency, as shown in Figure 3.35. And Table 3.4 shows the detailed list of the components that have been used in both prototypes.

Figure 3.33. Top view of the prototype

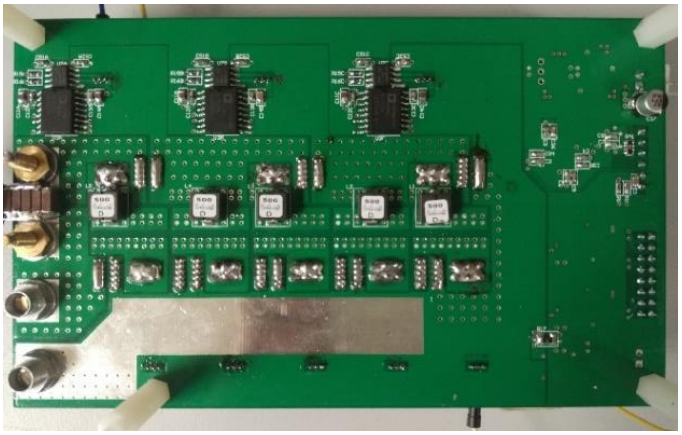

Figure 3.34. Bottom view of the prototype

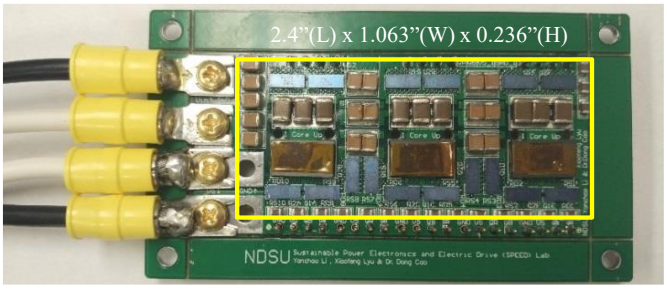

Figure 3.35. Second version prototype (main power area size: 2.4” x 1.063” x 0.236”, power density 750W/in^3 assuming 450W nominal power)

Table 3.4. Specifications of the Prototypes

Description	Part#	Manufacture
Digital controller	TMS320F28335	TI
Resonant capacitor	C2220C334J1GAC	Kemet
Resonant inductor	SLC7649S-700	Coilcraft
Switching device	EPC2023	EPC
Level shifter	ADUM6200CRWZ	ADI
Gate Driver	LM5113	TI
Digital Isolator	Si8620BB	Silicon Labs

To validate the theoretical analysis and design methodology of the proposed 6x STC, experiments have been performed based on the second version prototype. Also, efficiency curves are measured under different operating frequency. Note that frequency is changed by varying resonant capacitance. In order to get the most accurate measurement results, Fluke 87V

multimeters (high-resolution mode) are used to measure input voltage, output voltage and input current. Chroma programmable load is used to measure the output current.

Table 3.5. Parameters Used in The Experiment @ 387kHz

Description	Items	Values
Input voltage (nominal/max)	V_{in}	54 V / 60 V
Output voltage (nominal/max)	V_{out}	9 V / 10 V
Output Power (nominal/max)	P_{out}	450 W / 600 W
Resonant capacitor	C_r	2.58 μF
Non-Resonant capacitor	C_{nr}	120 μF
Resonant inductor	L_r	70 nH
Resistor Load	R_{load}	0.167 Ω
Resonant frequency	f_r	398 kHz
Switching frequency	f_s	387 kHz
Deadtime	t_d	40 ns

In Figure 3.36, a photo of the experimental platform has been exhibited. DSP TMS320F28335 is used to generate the PWM control signals. A docking board that has the same size as the main power board is developed to provide isolated power for wing side gate drivers.

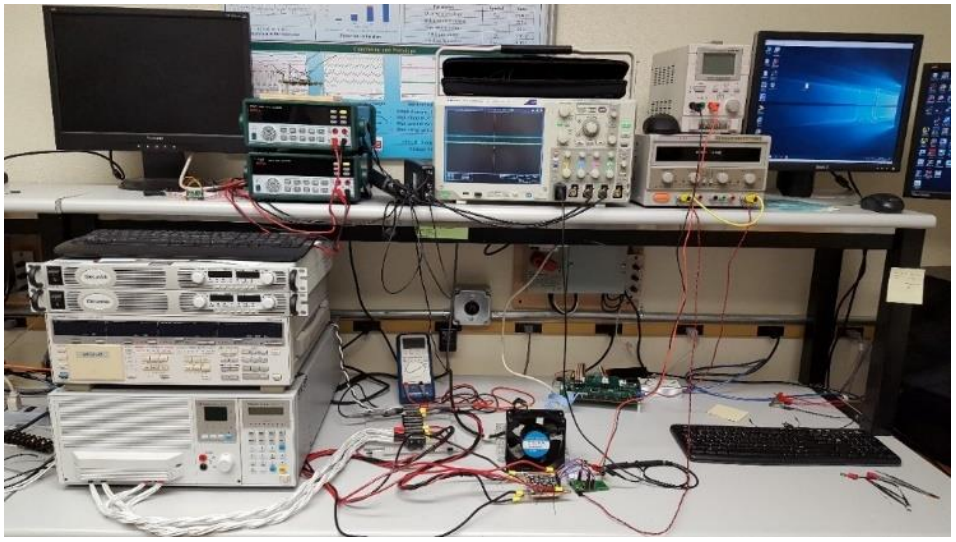

Figure 3.36. Experimental Platform

As shown in Figure 3.37, when the converter has 54V nominal input, its output voltage and power are 8.82V and 450W, respectively. The 0.18V voltage droop is caused by the ESR in the resonant loops. Figure 3.38 shows three inductor current waveforms. Since the resonant loops in the proposed circuit have almost the same parameters, all the current waveforms match each other very well. In Figure 3.39, the voltage waveforms on resonant capacitors have been measured, the peak-to-peak value is 8.6V. Non-resonant capacitor voltage waveforms are also captured, as shown in Figure 3.40. The peak-to-peak voltage on these capacitors is less than 0.5V, which is much smaller than that on the resonant capacitors due to much larger capacitance. In order to validate the ZCS operation of the proposed circuit, Figure 3.41 shows drain-source voltage across one of the eGaNFETs and corresponding inductor current (MOSFETs current cannot be directly measured due to its LGA package).

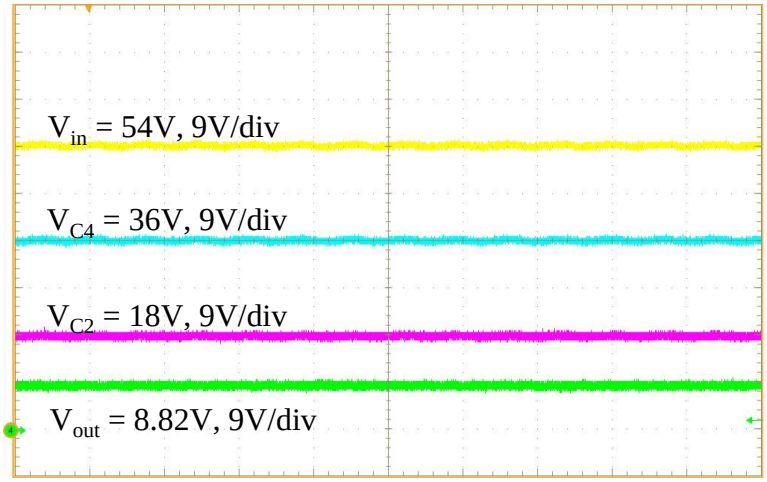

Figure 3.37. Capacitor and input/output waveforms

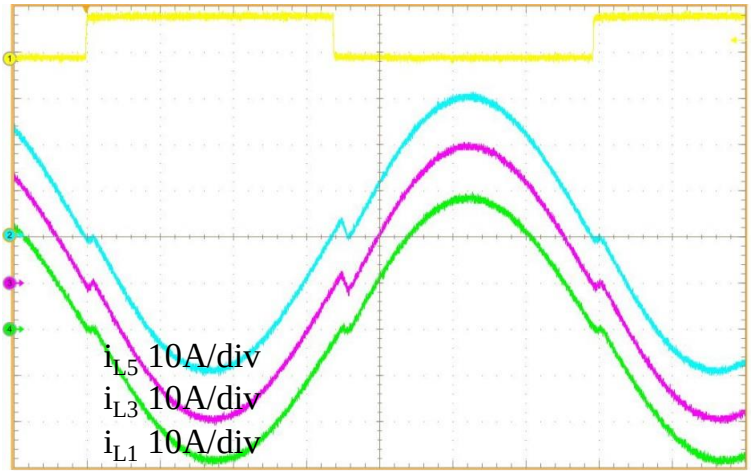

Figure 3.38. Inductor current waveforms

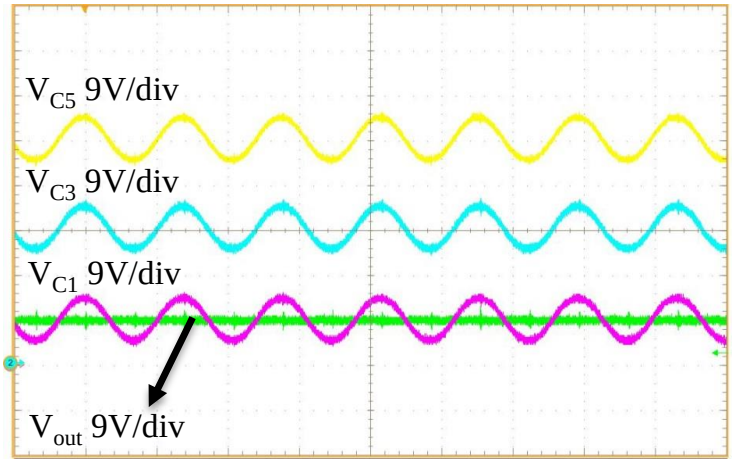

Figure 3.39. Resonant capacitor voltage waveforms

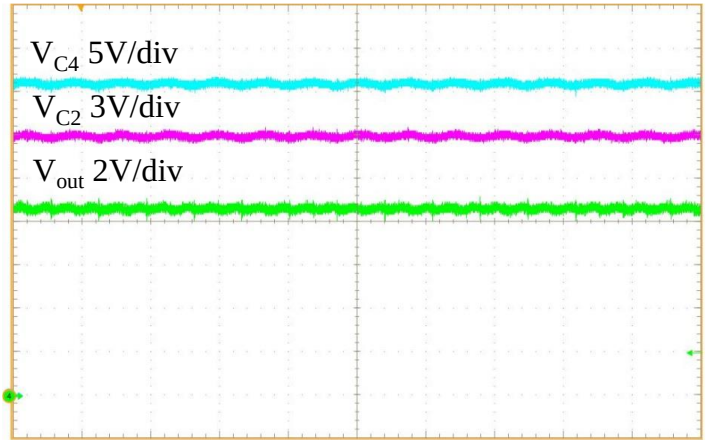

Figure 3.40. Non-resonant capacitor voltage waveforms

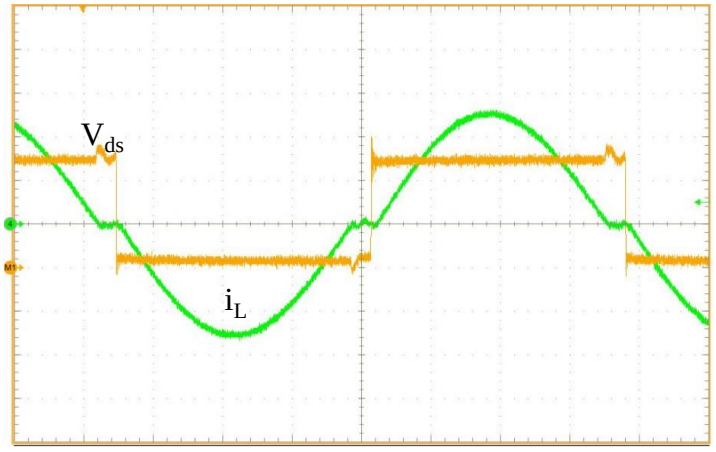

Figure 3.41. ZCS operation of the proposed 6x STC

The efficiency of the proposed converter has been measured under different operating frequency. By adjusting the capacitance of resonant capacitor banks, different resonant frequencies can be achieved. Note that the adjustment will not affect power density. In Figure 3.42, the efficiency of the converter is not as high as expected when it operates at 387kHz. This is because although the inductor winding loss has been improved, core loss is still significant the magnetic core is the smallest off the shelf core that can be found so far. If there is an opportunity to design a customized core shape, the core loss can be minimized. When the operating frequency decreases to 253kHz, peak efficiency of the proposed 6x STC reaches 98.55%.

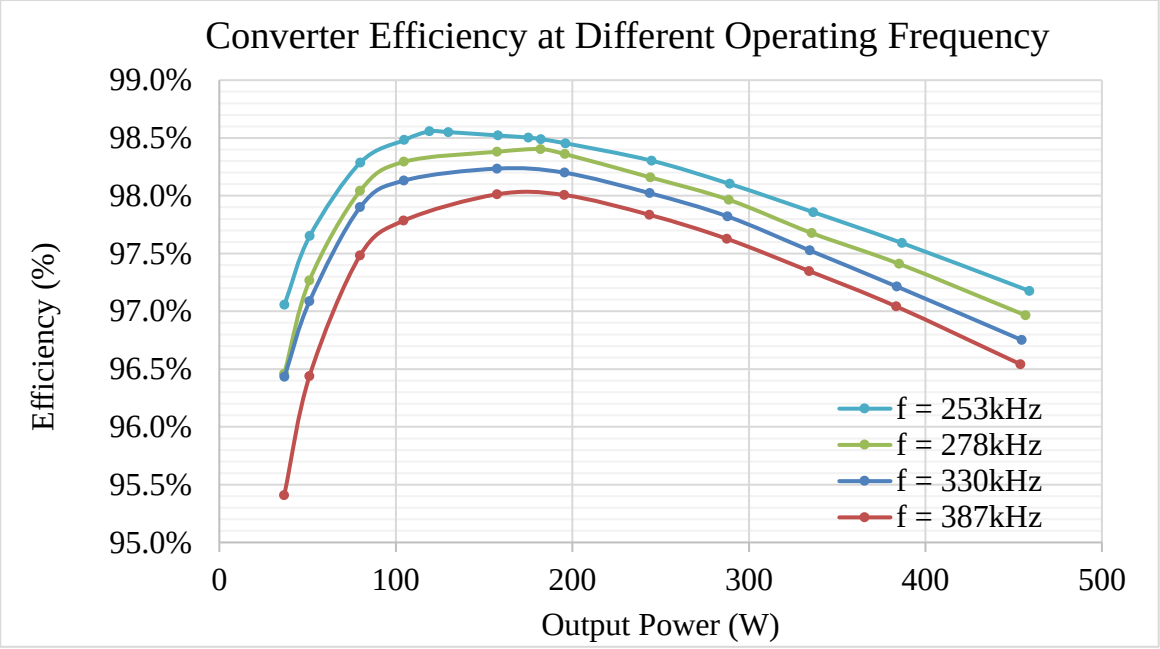

Figure 3.42. Efficiency of the second version prototype

Figure 3.43 shows the thermal performance of the proposed 6x switched-tank converter operating at 450W. The ambient temperature is 25˚C. And for cooling purposes, a small regular 12V DC fan has been used. The highest temperature observed on the board is 57˚C and it occurs on the PCB near the rectifier side devices. At this operating point, the typical temperature over the board is around 53˚C. And there is no significant temperature difference over the board. In a word, the thermal performance of the proposed converter is excellent because of high-efficiency design that has been achieved by following the design procedure for the proposed STC.

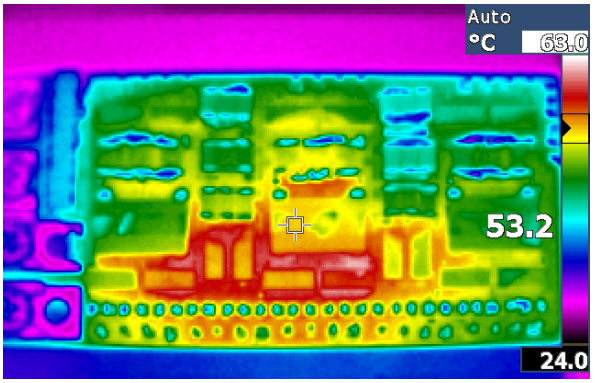

Figure 3.43. Thermal performance of the GaN based prototype at 450W

Compared to the other state of the art bus converters, the proposed converter can achieve much higher efficiency, as shown in Figure 3.44. What's more, the proposed converter has the highest power rating among the compared converters. And when the power output of the STC is less than 450W, its efficiency is always above 97%. Although the highest efficiency curve has been measured under 253kHz, higher efficiency can still be achieved under higher operating frequency by adopting customized core shape design and more layers of PCB. In addition, Table 3.6 shows that the proposed converter can achieve higher peak efficiency and density than the existing isolated commercial IBCs, which means removing isolation stage from the IBCs is an effective way to increase the performance of the IBCs.

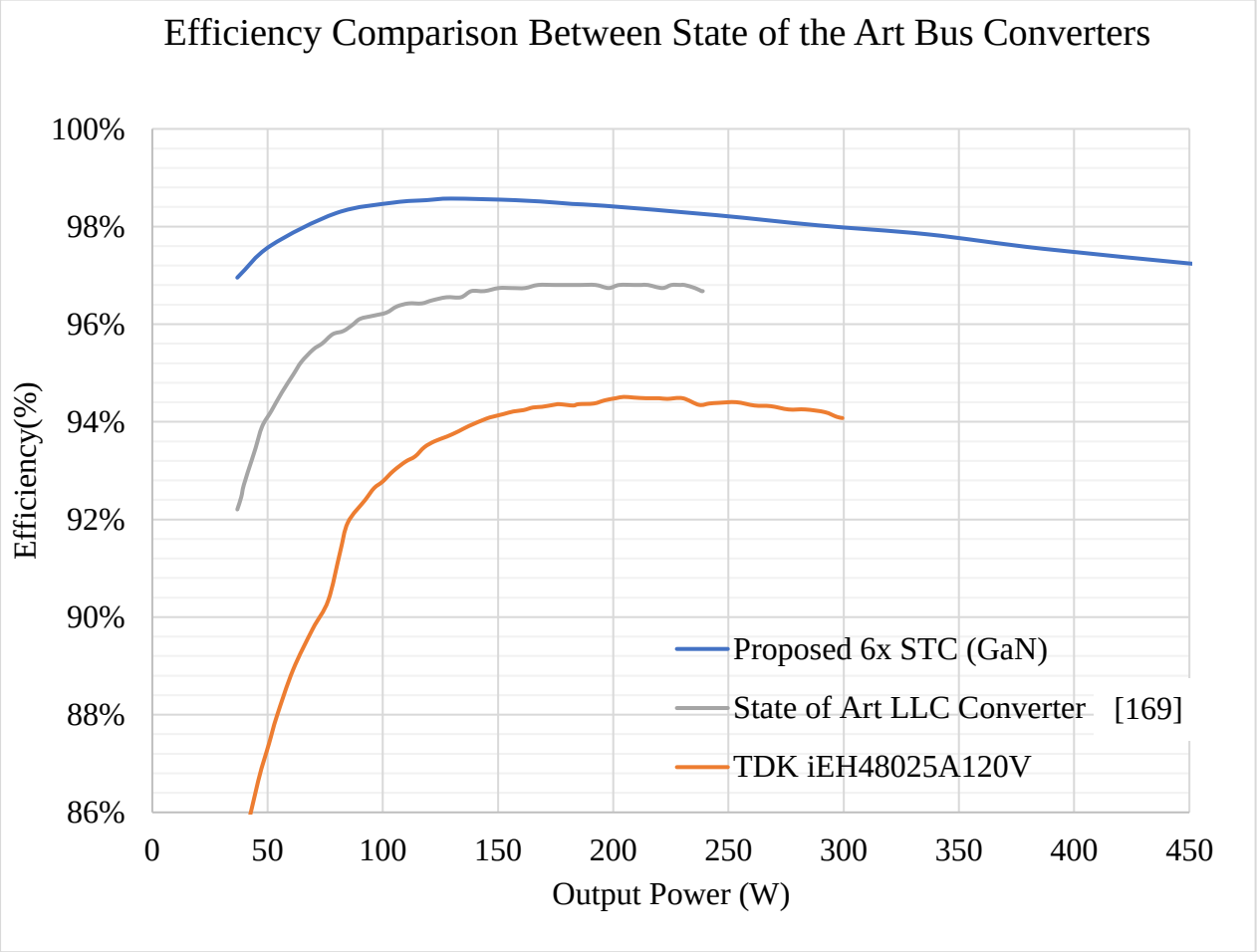

Figure 3.44. Efficiency comparison

Table 3.6. Comparison with Existing Eighth-Brick Converters

Prototype	Power Rating	Peak Efficiency	Full-Load Efficiency	Power Density
Proposed Converter	450W	98.55%	97.2%	750 W/in^3
TDK iEH48025A120V	300 W	95.5%	94%	289.9W/in^3
CUI NEB-300DMA	300 W	95.2%	94.8%	366.3 W/in^3
Murata DBE0125V2NBC	300 W	95%	94.6%	278.8 W/in^3
Vicor IB048E120T40Px	500 W	97.8%	97.4%	635.3 W/in^3
Ericsson PKB4413D	450 W	96%	95.6%	424.5 W/in^3
Delta E48SC12025	300W	95.7%	95%	337.1 W/in^3
Reference [54]	250 W	97.3%	97%	870 W/in^3

The transient performance and parallel operation performance are two very important factors of an IBC. In Figure 3.45, the prototype's transient waveform shows that when the load changes from 250W to no load, converter's output current changes from 28A to 0A in 26.5μs. Similarly, Figure 3.46 shows that when the load changes from 250W to 160W, it takes about 10μs for the output current to drop from 28A to 18A. Figure 3.47 shows that the output voltage is very stable during the transient. It's worth mentioning that the slew rate of the DC load has been set to 10A/μs, which is faster than the dynamic response of the prototype. A prototype that has two paralleled 6x STCs has been built to verify the parallel operation of the proposed converter, as shown in Figure 3.48. STC#1 and STC#2 of the prototype operate in parallel. By comparing two phases' inductor waveforms, one can tell the output current of the paralleled converters is balanced, as shown in Figure 3.49. The measured inductors are circled in Figure 3.48. Note that each of the STC on this prototype is built with the same parameters (i.e.V_{in}, V_{out}, L_r, C_r, C_{nr}, C_{in}, and C_{out}) as

the GaN prototype. The only difference is that this converter uses Si devices instead of GaN devices.

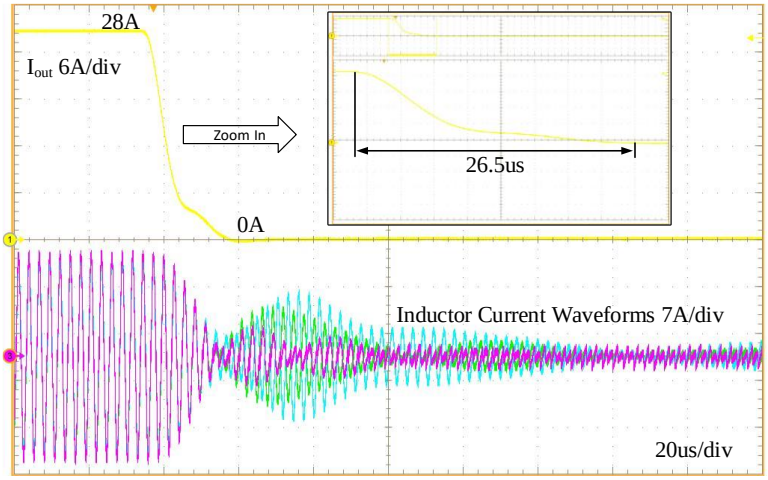

Figure 3.45. Converter 28A to 0A transient performance at V_{in}=54V

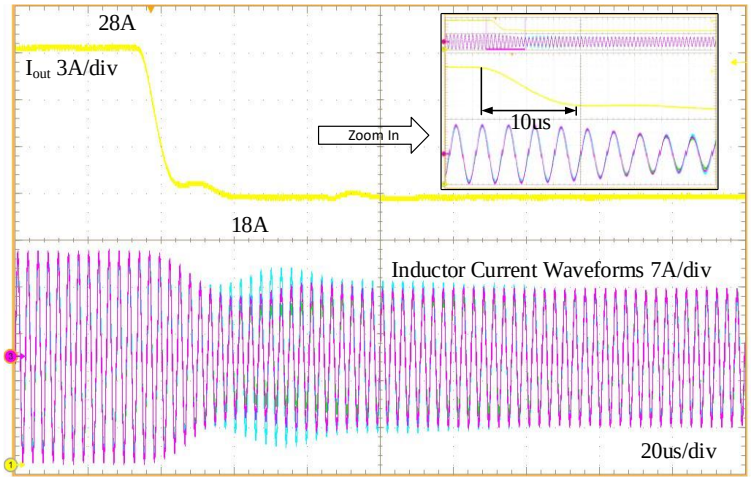

Figure 3.46. Converter 28A to 18A transient performance at V_{in}=54V

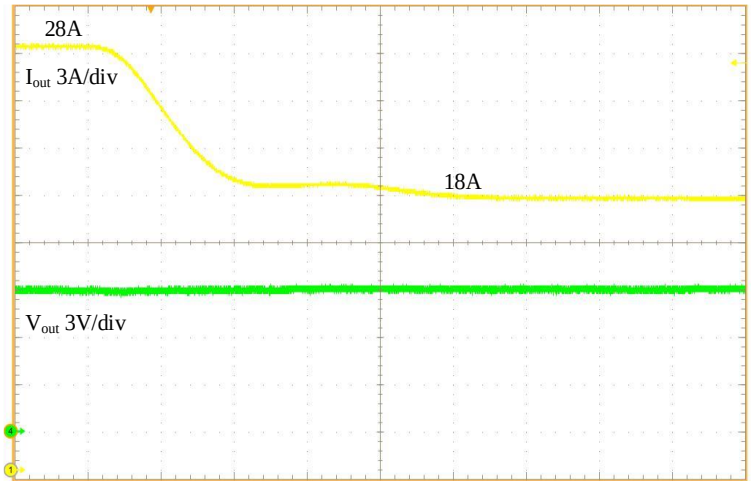

Figure 3.47. Converter 28A to 18A transient performance at V_{in}=54V

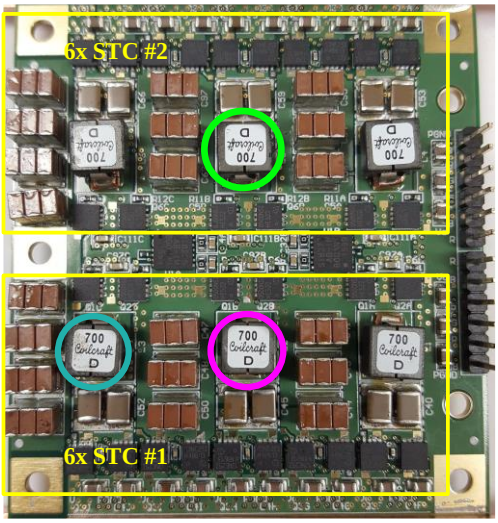

Figure 3.48. Prototype of two paralleled 6x STCs

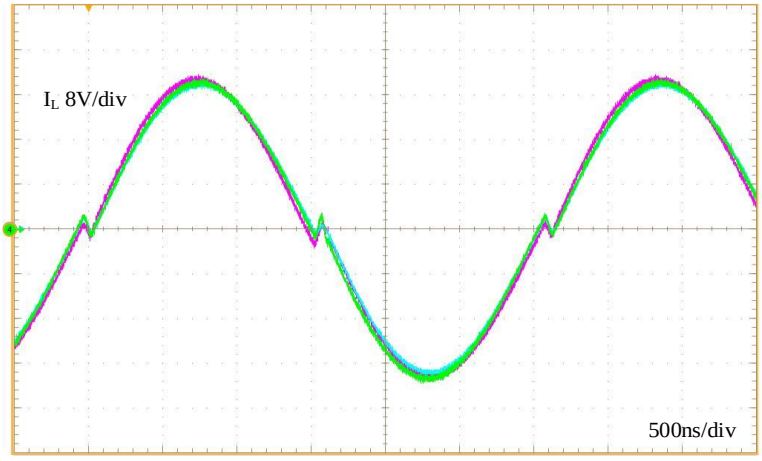

Figure 3.49. Parallel operation of the proposed 6x STC

3.6. Conclusion

In data center application, power density and efficiency of the bus converter is very critical. However, traditional topology and magnetic components used for isolation become the main barrier to achieving high efficiency and density. So a switched-tank converter has been proposed and its design procedure is demonstrated in this work.

Unlike conventional DC-DC converter, the proposed STC topology does not need high capacitance or inductance in the converter to achieve high efficiency. The underdamped resonant operation feature allows the proposed converter uses resonance between small capacitors and inductors to ensure the low loss in the circuit. Also, by utilizing high switching speed feature of low voltage rating MOSFETs, the passive components' size in the proposed converter can be minimized. The scalability of proposed topology is also one of the advantages. If we want to design an STC with different conversion ratio, there is no need for us to perform the inductor design and optimization again. This feature will significantly reduce the cost and time for an industrial product design. Furthermore, the proposed STC solves the issue that additional voltage clamping circuit for wing side device is needed for traditional resonant switched-capacitor converter shown in Figure 3.2.

With the proposed design procedure in this work, total power loss on semiconductors has been minimized by selecting proper switching device and gate drive voltage. Optimization on inductor is performed to minimize the copper loss when the off-the-shelf planar core is adopted. Also, the loss estimation and power loss breakdown support the successful design of the proposed converter and provide guidance in further efficiency improvement of the proposed converter.

Simulation has been carried out to verify the functionality of the proposed converter. Two versions of prototypes are built to verify the theoretical analysis. The first version focuses on

experimentally validating the operating principle. While the second version is designed to achieve high efficiency and high density. The experimental results shown in this work are based on the second prototype. When the proposed converter operates under 54V nominal (40Vmin/60Vmax) input voltage, 8.82V/450W has been generated at the output. The measured peak efficiency of the designed 6x STC is 98.55%. And its power density reaches 750W/in^3 (calculated with 450W power). In the future, with customized core shape design and more layers of PCB, efficiency and power density can be further improved.

4. ADAPTIVE ON-TIME CONTROL FOR HIGH EFFICIENCY SWITCHED-TANK CONVERTER

4.1. Introduction

As the rapid development of internet-based services such as cloud computing and big data, data center owners are trying to increase computing capacity of servers to meet the massive computing tasks. Energy usage in data center is expected to increase in the future. Based on the recent report, 73 billion kWh electricity will be consumed by U.S data center in 2020 [109]. As a result, the electricity bill takes more and more proportion among the overall cost. Therefore, the demand of high-efficiency and high-density power conversion solutions is increasing dramatically.

During the past years, wide-bandgap devices are becoming the new choice for more and more power electronics applications[110]–[112]. Because the switched-capacitor converter possesses the ability to leverage the advantages of Wide-bandgap devices, switched-capacitor concept has been used in many areas [59], [84], [113], [114], especially in DC-DC power conversion area. Based on the switched-capacitor concept, switched-tank converter concept was first introduced by Google in 2017. In [115], a comparison between STC and voltage divider shows that STC is more suitable for low voltage high current application. In [89], resonant switched-capacitor converters are implemented on PV application. Many control methods for switched-capacitor circuits are proposed to achieve different functions. In [101]–[103], hybrid switched-capacitor circuits and phase-shifted control are proposed to achieve high efficiency and voltage regulation function. In [116] and [117], new control methods allow the converters to achieve variable voltage conversion ratio. In [118], two control methods are proposed to enable dynamic variation in converter gain. In [119], an adaptive on-time control method is proposed to improve the light-load efficiency of switched-capacitor converters. In [75], split-phase control

method are proposed to avoid large transient current spikes in Dickson switched-capacitor converter.

In [105], a STC is demonstrated to show that it can achieve very high efficiency and power density. In ideal case, all resonant inductor and capacitor in the switched-tank converter are identical, thus two complementary control signals all over the board is sufficient. However, in order to deploy switched-tank converter into real application, only study on the ideal case is not enough. For example, component tolerance is an issue that cannot be eliminated during power converter mass production process. In order to commercialize this concept, issues caused by component tolerance have to be studied and addressed. When all the resonant tanks in STC are not identical due to component tolerance, efficiency will be pulled down and zero-current-switching (ZCS) cannot be maintained. As a result, a solution to solve the issues caused by component tolerance is desired.

The focus of this work is twofold: first, analyze the operation of switched-tank converter proposed in [105] when its resonant parameters in different resonant loops are not the same; second, propose an improved STC circuit and adaptive on-time control method to solve the issues that caused by tolerances of resonant inductance and capacitance. In order to fully evaluate the seriousness that unmatched resonant inductance and capacitance may lead to, worst case is considered in the study. Simulation has been performed to demonstrate the effectiveness of the proposed circuit and control method. A 1.2kW prototype has been built to validate the principle of the proposed control method. The prototype with nominal 900W, 54V input and 9V output achieves 98.71% peak efficiency and 97.7% efficiency under full-load (0.5% improvement).

4.2. Circuit Operation, Analysis and Proposed Control Method

4.2.1. Issues Caused By Component Tolerance in STC

Figure 4.1 shows the circuit configuration of the existing two-phase 6X switched-tank converter proposed in [105]. This converter has two types of tanks: resonant tank and non-resonant tank. The resonant tank includes both capacitor and inductor. The non-resonant tanks only have capacitors, such as C_{2a}, C_{4a}, C_{2b} and C_{4b}. The capacitance value of the non-resonant tanks is much larger than that in resonant branches. This circuit can achieve voltage step-down function, which converts 54V nominal voltage to 9V in our case. The input voltage could range from 40V to 60V. In ideal case, all switching devices in the circuit have the same current stress. However, their voltage stresses are different. When the input voltage is 60V, voltage stress on switching devices S_{R1a}, S_{R2a}, S_{B2a}, and S_{B3a} in the upper phase is 20V, while the stress on other devices is 10V. Similarly, the current stress and voltage stresses apply to lower phase.

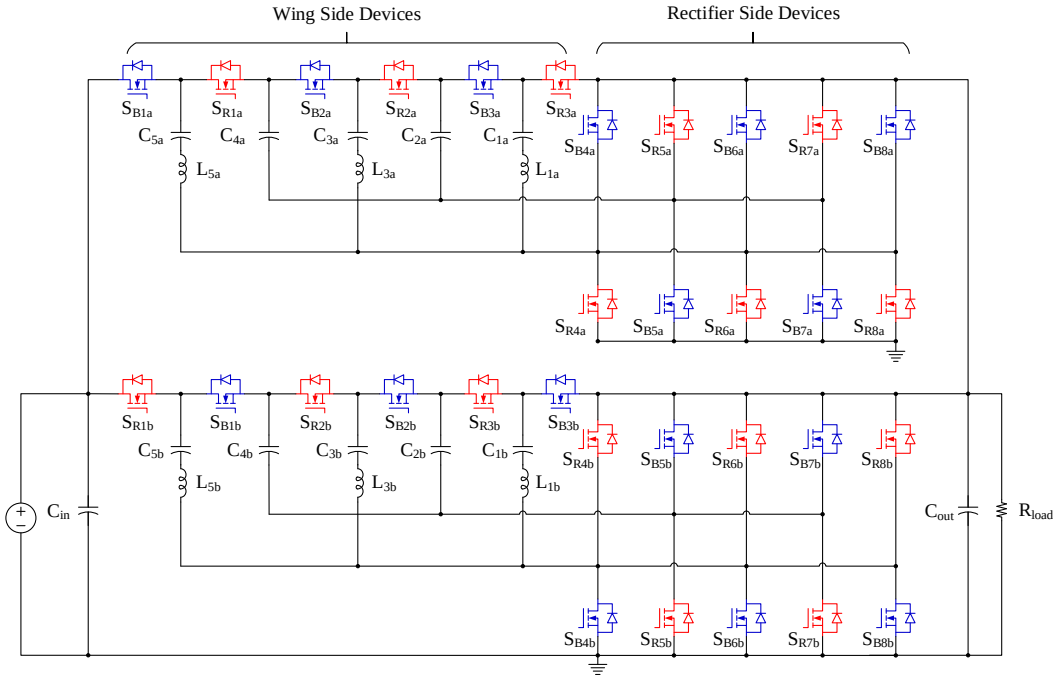

Figure 4.1. Previously proposed two-phase 6x STC [105]

In ideal case, the parameters of the resonant tanks and non-resonant tanks in the circuit are identical, respectively. When the converter operates under steady state, all the resonant loops in the circuit have the same resonant frequency. This means that all the switching devices can achieve ZCS with the same conduction time, namely, on-time. However, component tolerance is an issue that cannot be eliminated during power converter mass production process. And potential problems that may caused by component tolerance need to be studied. In order to study the issues caused by tolerance of inductors and capacitors in the circuit, it is necessary to know the tolerance range of the components first. In general, the tolerance of inductors and capacitors can range from -10% to +10% [20] [21]. The resonant frequency of each resonant loop can be calculated using Eq.4.1. Because the capacitance of non-resonant capacitance is much larger than that of resonant capacitors (eg. ten times larger), the tolerance of non-resonant capacitors has very limited effect on the resonant frequency. As a result, the resonant frequency of the resonant loops will be mainly affected by tolerances of resonant inductors and resonant capacitors.

$$f_r = \frac{1}{2\pi\sqrt{L_r \frac{C_r * C_{nr}}{C_r + C_{nr}}}} \qquad \text{(Eq. 4.1)}$$

In this work, an example based on single phase STC is used to demonstrate the issues that are caused by component tolerance. In order to fully understand the problems that are caused by tolerance of resonant inductors and capacitors, this analysis considers the worst case that there are -10% inductance change on L_3 and -10% capacitance change on C_3 from their nominal values. Under this condition, when the converter has 40V input and works under full-load, the effect of the unmatched resonant branch to converter is most obvious. In Figure 4.2 and Figure 4.4, all the three resonant loops are transferring power to the output of the converter. Because the resonant branch that includes C_3 and L_3 has higher resonant frequency than the other two branches, the

current in this branch will go across zero point and change its direction, as shown in Figure 4.3 and Figure 4.5. Operation mode 3 and mode 6 in Figure 4.7 show that when deadtime of the control signal is not long enough, the inductor current does not have enough time to reset the current back to zero before next operating state starts. Then the converter will operate under a new steady state that has a considerate among of circulating energy in the circuit. As a result, the conversion ratio of the converter will shift far away from 6:1. Furthermore, current sharing on the three paralleled resonant branches will become a problem. In this scenario, it is possible that the converter could be damaged due to high RMS current flowing through switching devices. One solution to ensure safe operation and mitigate current sharing issue of the converter is to increase deadtime of the control signals. However, although longer deadtime allows the inductor current reset back to zero, it still cannot totally solve energy circulating problem in the circuit or ensure soft-switching of the MOSFETs. What's more, current resetting procedure through MOSFETs' body diode during deadtime will also sacrifice efficiency of the proposed converter. So, new control strategy is necessary.

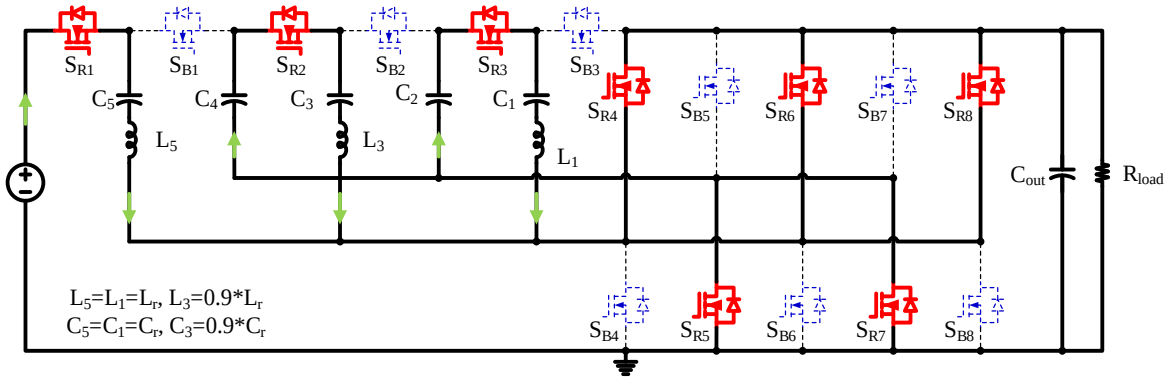

Figure 4.2. State 1a (Mode 1)

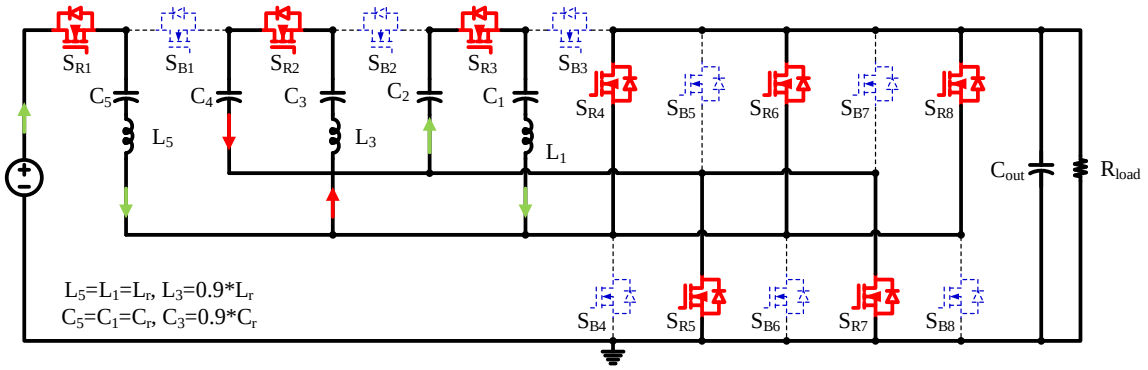

Figure 4.3. State 1b (Mode 2)

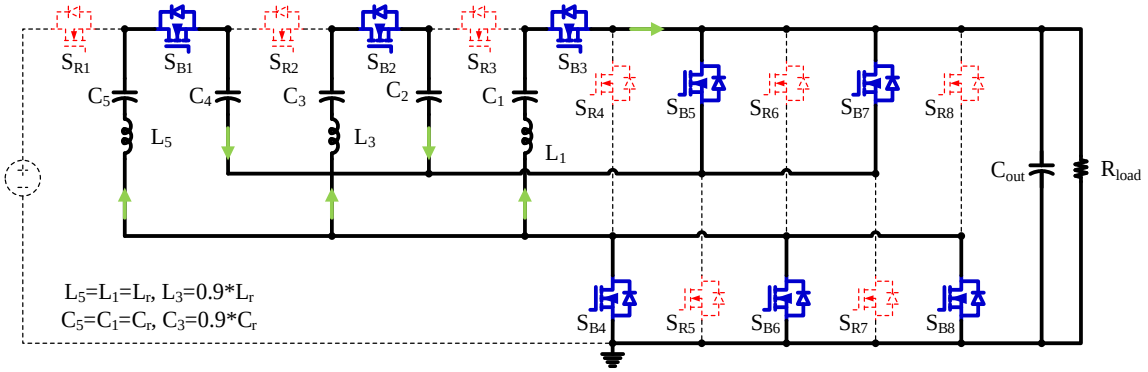

Figure 4.4. State 2a (Mode 4)

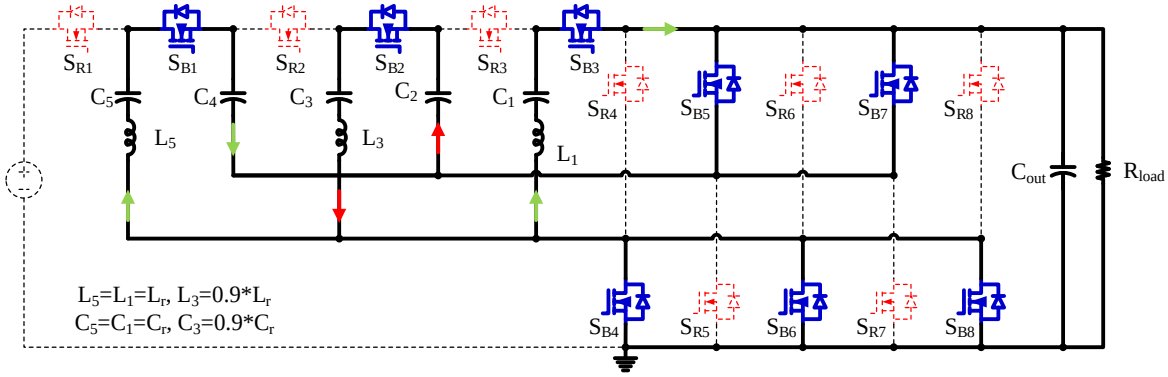

Figure 4.5. State 2b (Mode 5)

4.2.2. Improved Circuit Configuration and Proposed Adaptive On-Time Control Method

In Figure 4.1, due to the limitation of circuit structure, although all the wing side switching devices in the circuit can have different conduction time, the conduction time of all rectifier side

devices is the same. By connecting the node of different inductors to separate synchronized rectifiers, more flexible control strategy can be implemented.

Figure 4.6 shows the improved 6x STC with separate resonant branches. The improved circuit configuration allows us to control the operation of different resonant loops independently. Since the resonant parameters in the second resonant loop is different in this example. The proposed adaptive on-time control ensures that switches in the proposed converter can achieve zero-current switching by adjusting the conduction time of different MOSFETs in different resonant loops. In other words, all the devices in the circuit have the same switching frequency and different on-time. As shown in Figure 4.8, because L_3 and C_3 are 10% lower than nominal values, the conduction time of S_{B2} and S_{R2} is controlled to be less than the other MOSFETs. As a consequence, the ZCS on MOSFETs have been achieved, circulating energy is avoided and therefore conversion ratio is not shifted. The three paralleled resonant branches transfer the same amount of power to the output. In Figure 4.9 to Figure 4.12, circuit operating states using the proposed control method are demonstrated. Figure 4.9 and Figure 4.10 show that when the zero-current point in the resonant loop that includes L_3 and C_3 is reached, S_{R2} and S_{R6} are turned off to prevent current in this branch from flowing in the other direction and leading to energy circulation. As a result, compared to the current waveforms shown in Figure 4.7, ZCS is achieved on S_{R2} with the proposed control method. Similarly, Figure 4.11 and Figure 4.12 show the circuit's operating states during the other half switching period.

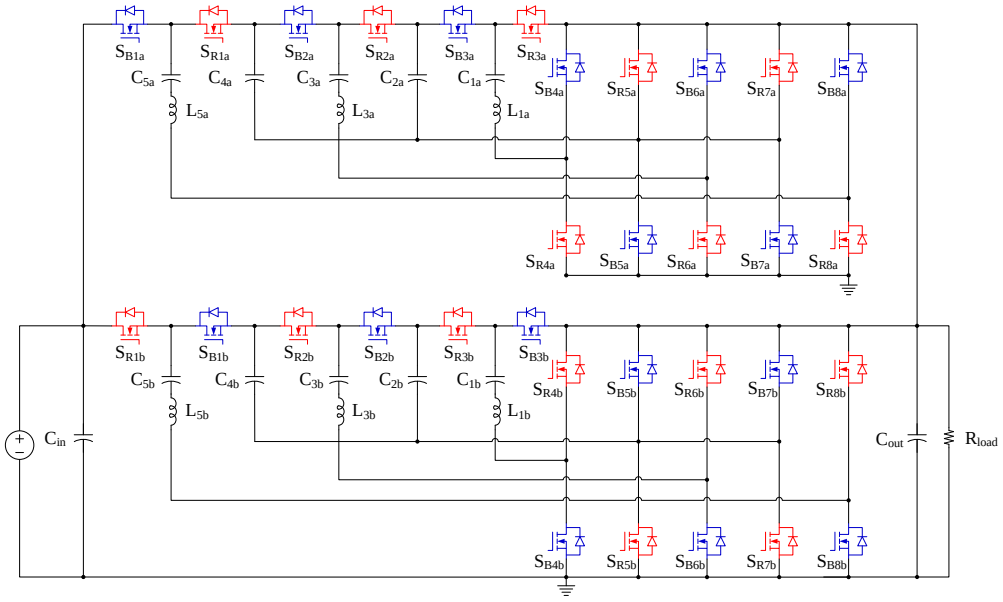

Figure 4.6. Proposed two-phase 6x switched-tank converter with separate resonant branches

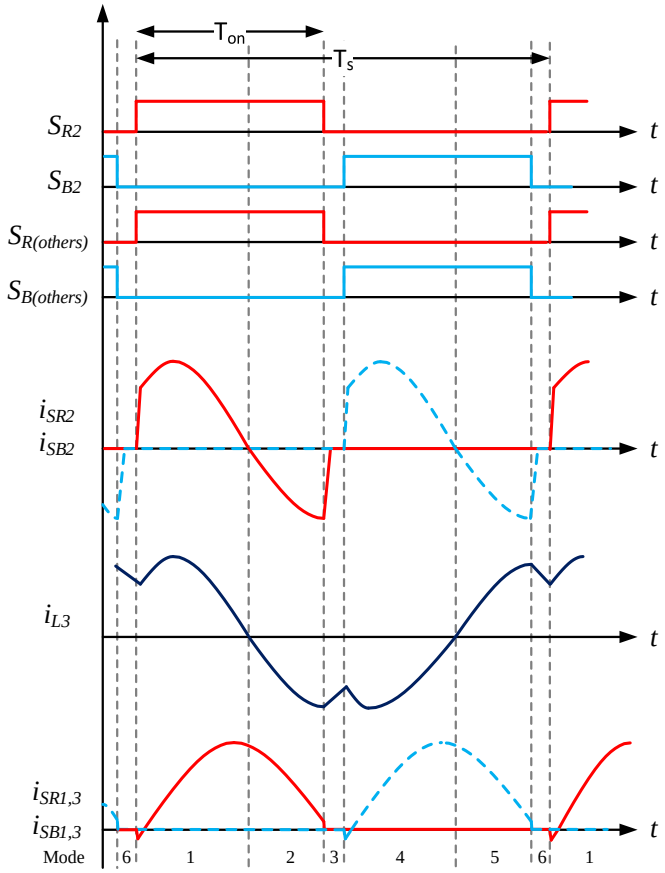

Figure 4.7. Waveforms without adaptive on-time control

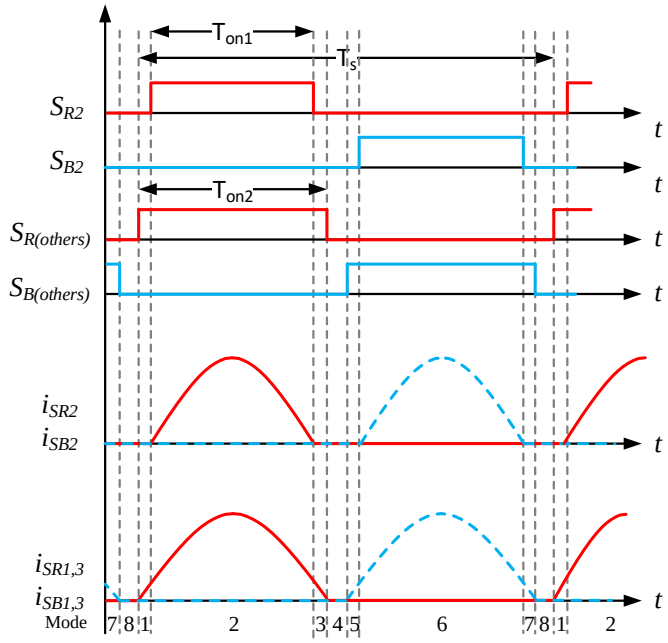

Figure 4.8. Waveforms with adaptive on-time control

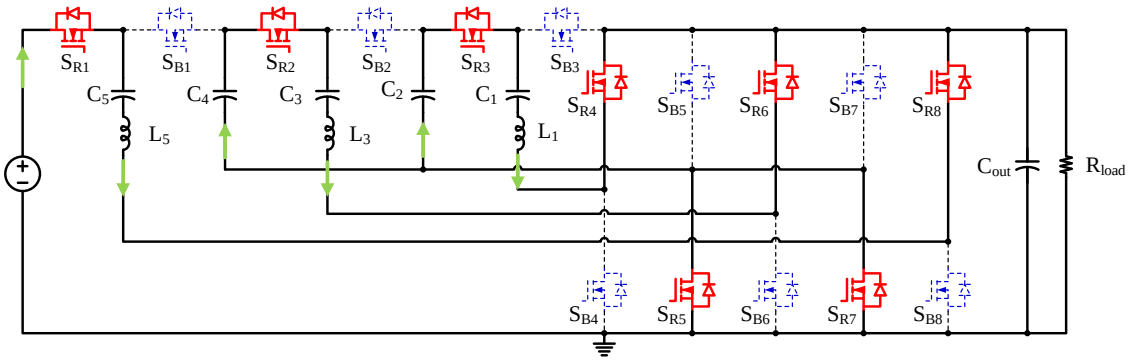

Figure 4.9. State 1a (Mode2)

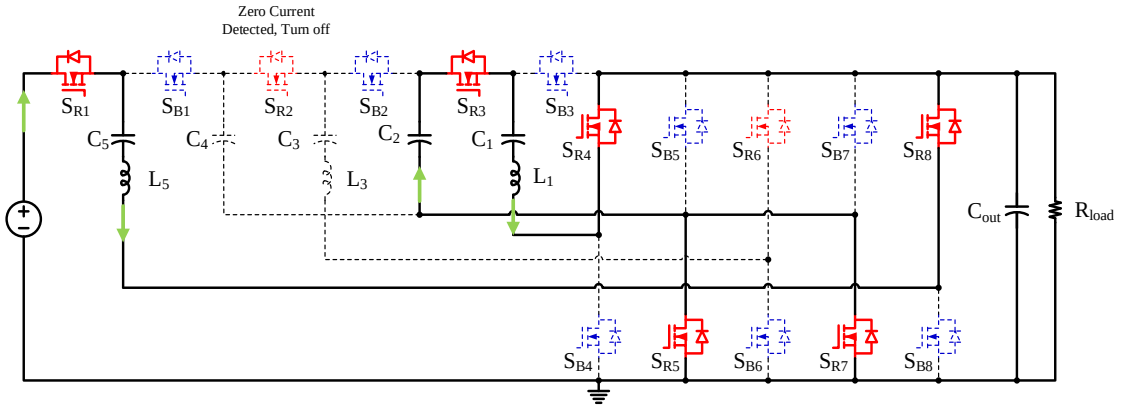

Figure 4.10. State 1b (Mode1,3)

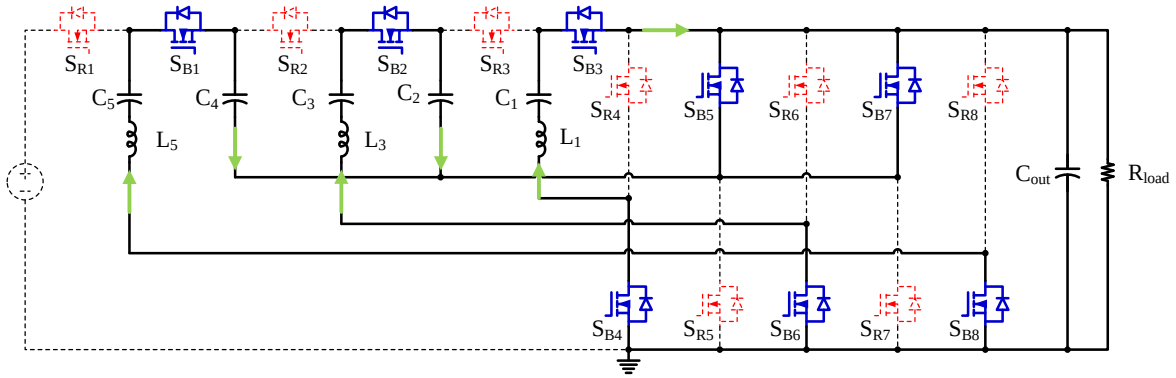

Figure 4.11. State 2a (Mode 6)

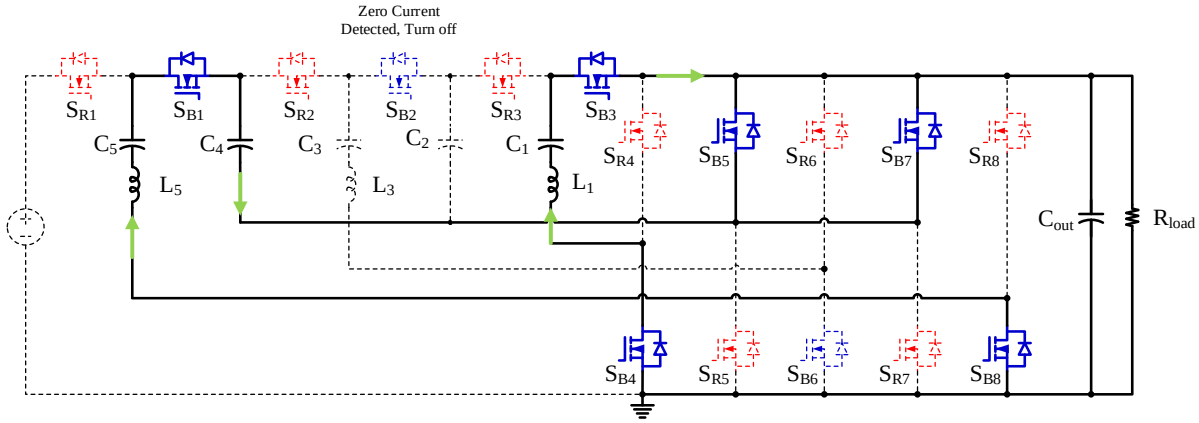

Figure 4.12. State 2b (Mode 5,7)

4.3. Simulation Results

Simulation has been performed to show the issues caused by unmatched resonant tanks and the effectiveness of the proposed control method. In order to simulate the worst case when one resonant tank is unmatched with nominal value, a one-phase STC with 40V input voltage and 450W power output is considered. Because the current stress on all devices is the highest under this condition. And this condition is the most difficult one for the inductor current to be reset back to zero. Table 4.1 shows the parameters used in the simulation. In this simulation, L_3 and C_3 are set to be 10% smaller than their nominal values, deadtime are set to 50ns.

Table 4.1. Parameters Used In The Simulation

Description	Items	Values
Input voltage	V_{in}	40V
Output voltage	V_{out}	6.67 V
Output Power	P_{out}	450 W
Resonant capacitor	C_1, C_5	2.82 μF
	C_3	2.54 μF
Resonant inductor	L_1, L_5	70 nH
	L_3	56 nH
Resistor load	R_{load}	0.0987 Ω
Deadtime	t_{dead}	50 ns
Resonant frequency	f_{r1}, f_{r5}	358 kHz
	f_{r3}	422 kHz
Switching frequency	f_s	365 kHz

As shown in Figure 4.13, without using the adaptive on-time control method, the inductor current fails to return back to zero during the deadtime. Therefore, the converter has reached a new steady state. In this new steady state, the proposed converter has severe current sharing issue between resonant branches and considerable conversion ratio shift. Current stress of switches S_{R2} and S_{B2} is three time as the other devices. The output voltage drops from 6.67V to 6.05V, which means conversion ratio shifts from 6:1 to 6.6:1. Figure 4.14 shows that with the proposed circuit and control, the currents flowing through three paralleled resonant branches are balanced. And energy circulation within the circuit is mininized. It's worth mentioning that since all the devices turn off at zero current point, there is no need of long deadtime to allow inductor current to be reset to zero. As a result, the theoretical analysis is validated through simulation and issues caused by component tolerence has been sloved with proposed control method. And ZCS are realized on all the switching devices.

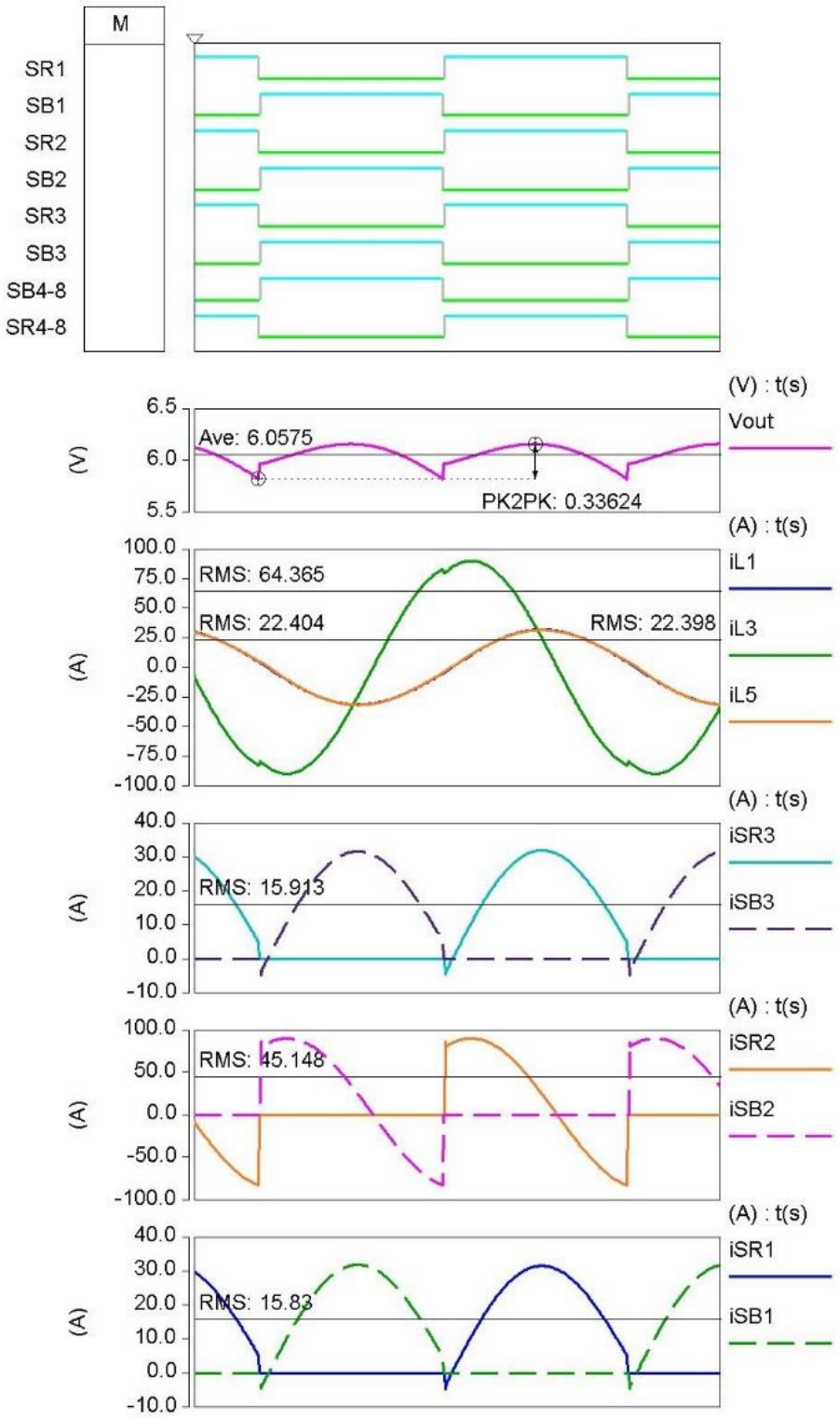

Figure 4.13. Simulation results of proposed converter without proposed control (450W power output, 40V input voltage)

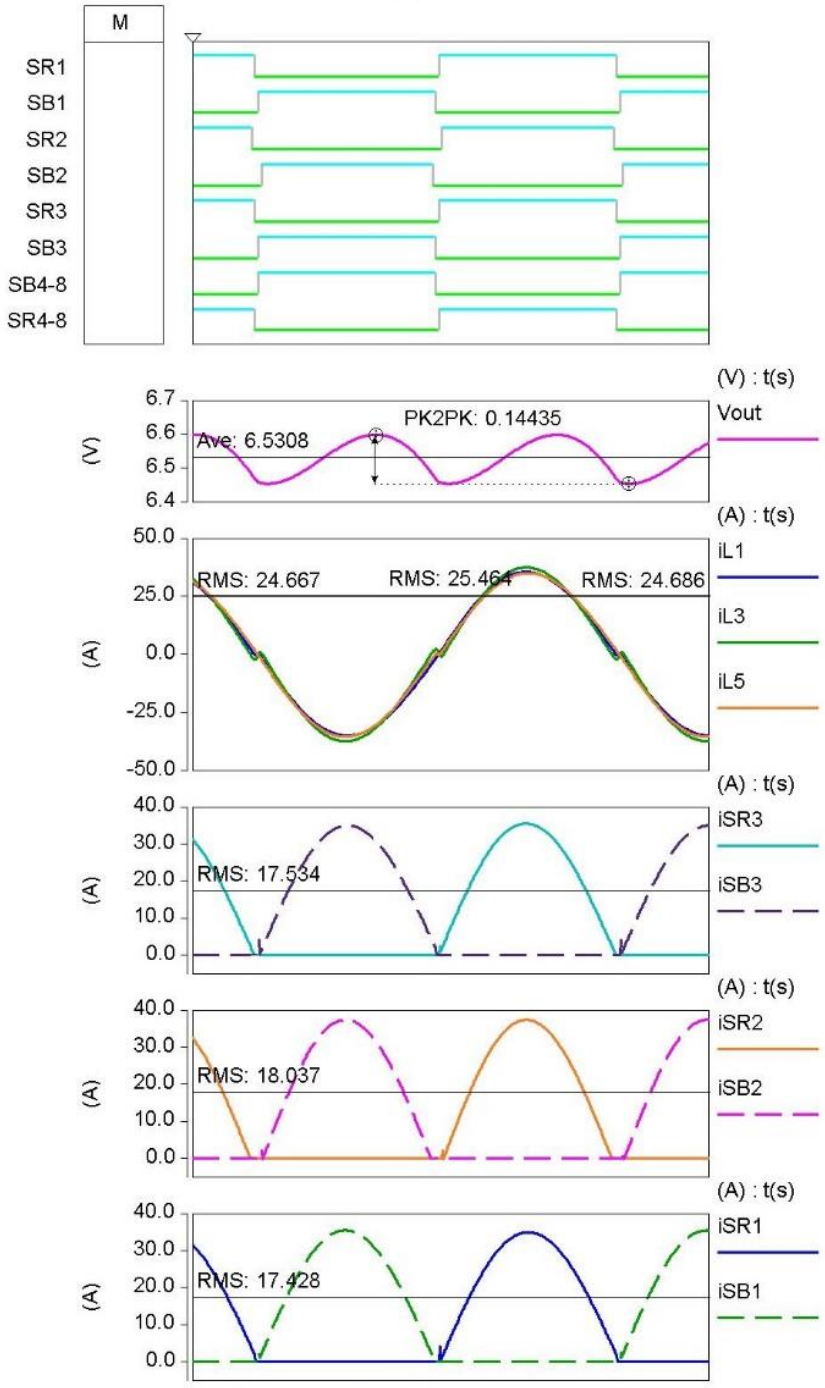

Figure 4.14. Simulation results of proposed converter with proposed control (450W power output, 40V input voltage)

4.4. Experimental Results and Prototype

A 1.2kW (nominal 900W) interleaved STC has been built to verify the effectiveness of the proposed control method, as shown in Figure 4.15 and Figure 4.16. Detailed hardware information can be found in Table 4.2. Due to component tolerance issue, resonant frequency of three loops are different. The switching frequency is set to 260kHz.

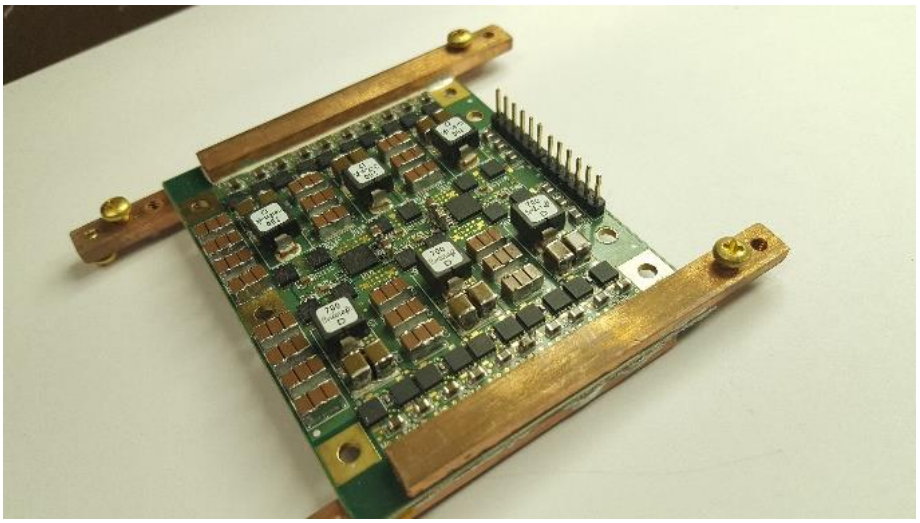

Figure 4.15. 1.2kW 6x STC Prototype Top View

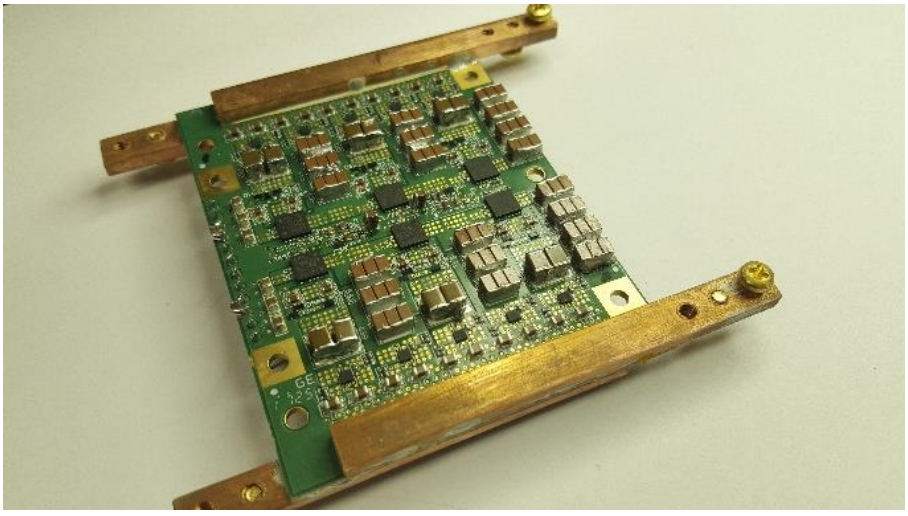

Figure 4.16. 1.2kW 6x STC Prototype Bottom View

Table 4.2. Specification of the Prototype

Description	Part#	Manufacture
Digital controller	TMS320F28335	TI
Resonant capacitor	C2220C334J1GAC	Kemet
Non-resonant capacitor	GRM32EC72A106KE05	Murata
Resonant inductor	SLC7649S-700	Coilcraft
Gate Driver	LM5113	TI
	Si8274	Silicon Labs
Digital Isolator	Si8620BB	Silicon Labs

Figure 4.17 and Figure 4.18 shows the inductor current waveforms without proposed control, which means all MOSFETs have the same switching frequency and conduction time. Without the proposed control, a relatively long deadtime (~100ns) is used to ensure the inductor current to have enough time to be reset back to zero during this time. However, the currents flowing through the three resonant branches are still not balanced and ZCS on the switches is not properly achieved. On the other hand, after using the proposed control method, currents flowing through all the resonant branches in the 6x STC are balanced and no circulating energy can be observed. This means the RMS values of currents flowing through all devices are identical. As a result, soft-switching has been achieved according to inductor current waveforms, as shown in Figure 4.19 and Figure 4.20.

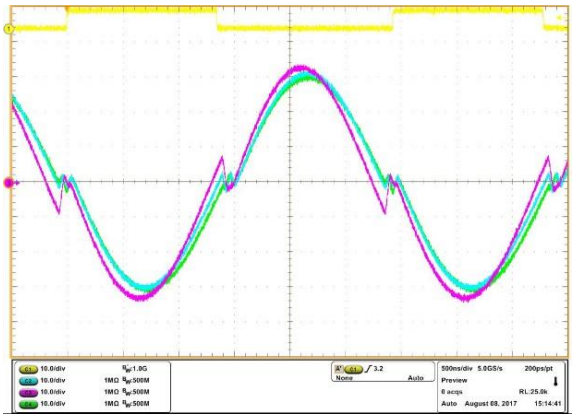

Figure 4.17. Overlapped inductor waveforms

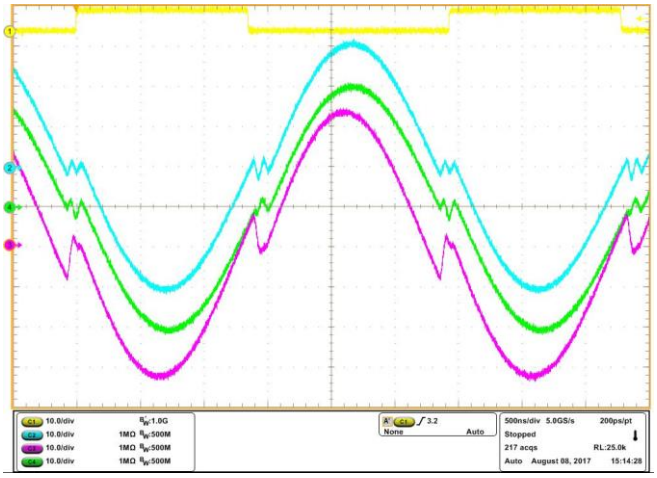

Figure 4.18. Inductor waveforms

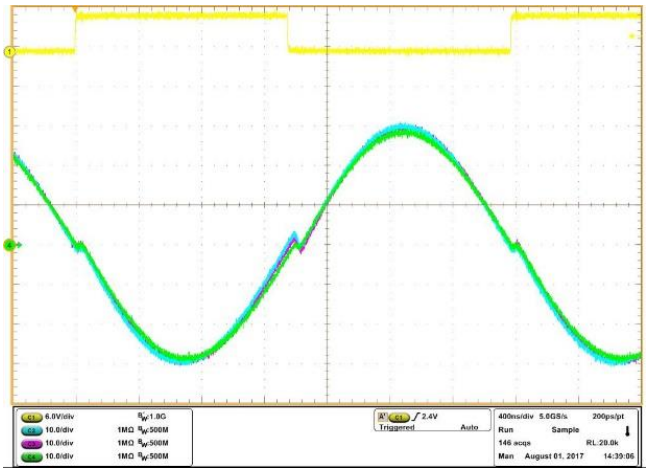

Figure 4.19. Overlapped inductor waveforms

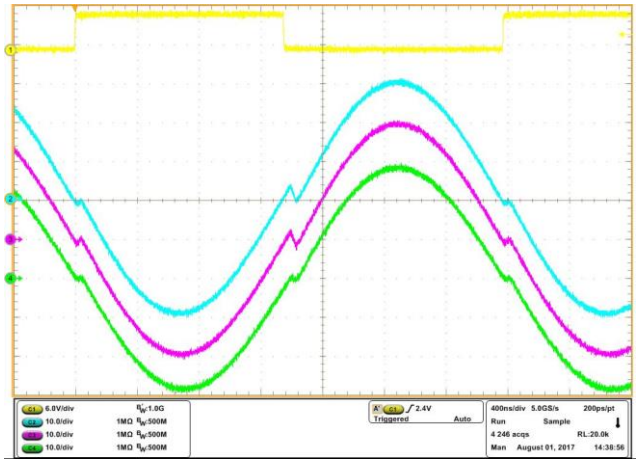

Figure 4.20. Inductor waveforms

In order to further validate the effectiveness of the proposed control method. Efficiency of the 6x STC using old control method and the proposed adaptive on-time control method are measured, as shown in Figure 4.21. The experimental results show that the proposed circuit and control method can improve the efficiency of the 6x STC by 0.5% at 900W, which means power loss is reduced by 16.77%. And the peak efficiency reaches as high as 98.71%.

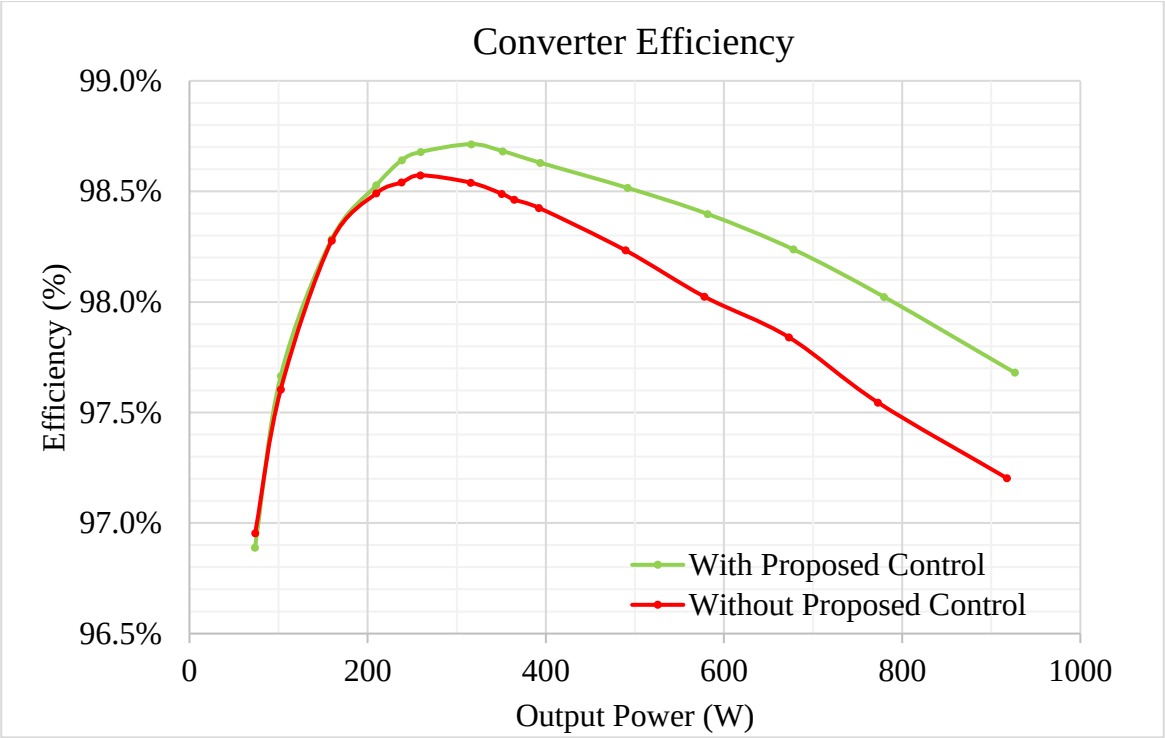

Figure 4.21. Converter efficiency increased with the proposed control method (98.71% peak efficiency)

4.5. Conclusion

This work presents an STC with separate resonant branches and on-time control method to improve the efficiency of STC. By identifying issues caused by unmatched resonant tanks in different resonant loops, an improved STC circuit and adaptive on-time control method are proposed. The proposed control method ensures ZCS operation and solves current sharing issue between the paralleled resonant branches in the STC. Simulation and experiments have been performed to verify the effectiveness of the proposed control method. The experimental results

show that with the proposed control method, efficiency of the proposed 6x STC with separate resonant branches is increased by 0.5% at 900W, which means power loss is reduced by 16.77%. And 98.71% peak efficiency has been achieved.

5. A HIGH-EFFICIENCY SWITCHED-CAPACITOR RESONANT CONVERTER WITH ZVS OPERATION

5.1. Introduction

DC-DC power converters are widely used all over the world and covers a lot of important applications. On one hand, high power DC-DC converters have been used in photovoltaic (PV) applications [120]–[123] to interface the PV arrays with high voltage DC-Link. In electric vehicle (EV) application, a boost converter is usually used to step-up the low battery voltage to high DC-Link voltage [124]–[126]. On the other hand, the low power DC-DC converters are used in applications such as DC motor drive, intermediate bus converter (IBC) [81], [127]–[130]. As the rapid development of DC-DC power conversion technology, the conventional inductor-based switching mode power supplies (SMPS) can no longer meet the high-efficiency and high power density requirement from the market. In order to improve the performance of the DC-DC converters, wide bandgap devices are widely used to replace traditional silicon devices because they have better thermal performance, reliability and lower switching loss than the conventional semiconductor devices [131]–[133]. Because the inductor-based topologies are heavily relying on magnetic components to achieve their functions, there is no very optimal solutions to solve the problems that they are bulky and heavy. This means the fundamental issues of the traditional inductor-based converters cannot be solved.

Switched-capacitor converters are famous for their magnetic-less feature. The capacitors are used in the circuits to transfer energy as well as achieve voltage conversion function. Because the capacitors have much higher energy density than inductors [134], the switched-capacitor converters have great potential to surpass the traditional inductor-based converters in terms of

power density and weight [135]. Therefore, switched-capacitor converters are widely used in different applications.

The traditional switched-capacitor concept has been widely used in low power applications, such as charge pump circuits. And intensive research efforts have been conducted to apply the traditional switched-capacitor concept to medium and high power application during the past decades [74], [83], [136], [137]. In these circuits, the capacitors directly charge/discharge each other to transfer the energy. Although the power density of the switched-capacitor converters is increased when comparing to inductor-based converters, they still suffer from low efficiency and severe electromagnetic interference (EMI) issues. In order to solve the low efficiency issue, increase switching efficiency and capacitor capacitance turn out to be very effective solutions [138]. However, increasing capacitance will lead to large passive component volume again, which is against the essential concept of switched-capacitor converters. Therefore, resonant switched-capacitor concept has been applied the switched-capacitor circuits to provide better converter performance. With resonant operation, the switched-capacitor can achieve soft-switching, which significantly alleviates the generation of EMI and semiconductor switching loss. Most importantly, the volume of passive components can be kept at a very low level. As a result, high power density and high efficiency can be achieved. In low power area, the converters based on resonant switched-capacitor concept can have fully integrated feature [63][139] and therefore have very low form factor [61], [65], [86]–[88], [140], [141]. In medium and high power area, solution such as utilizing stray inductance to achieve soft-switching was proposed to eliminate magnetic components [77], [79], [117]. Besides, tiny planar inductor or surface mount inductor is used to provide superior circuit integration[129][142].

The switched-tank converter (STC) concept is initially proposed by Google in 2017 [128][143]. And the zero-current switching (ZCS) operation of STC has been fully investigated in [142]. The STC is modified from the SCRC for ZCS operation. This work proposed a SCRC with zero-voltage switching capability. By analyzing the circuit's operating principle, mathematical model that can be used to represent all the devices' current waveforms have been developed. The design procedures of an example converter that can be used in data center application is demonstrated, which has 54V input and 9V output. The further analysis shows that designed SCRC with ZVS operation can achieve higher efficiency and density than the SCRC with ZCS operation. Simulations and experiments have been carried out the validate the developed mathematical model and ZVS operation. The proposed high-density prototype has predicted peak efficiency of 99.1%. And its power density can achieve 800W/in^3.

This work is organized as follows: section II demonstrates the circuit configuration and the converter's operation mode, which is ZVS operation. This section also clarifies how to get the current waveforms and voltage stress of all converter components. And this section also provides mathematical method to calculate the RMS value of the current flowing through all the devices. Section III uses a design example to show that how to use the information obtained from section II to design the proposed converter. Also, a guideline for selecting desired deadtime based on the presented converter is provided to ensure the high-efficiency operation of the presented converter. Section IV presents the simulation results of the designed converter. Multiple operating points are simulated to show that the mathematical calculation matches the simulation results very well. ZVS operation are validated through the simulation. Section V presents the experimental results based on designed lab prototype. Furthermore, a high-density prototype is proposed in this section.

Efficiency of the prototype has been estimated and power loss breakdown is provided in this section. At last, section VI concludes the proposed converter.

5.2. Circuit Configuration and Operation of The Proposed Converter

In this section, circuit architecture of the analyzed converter will be introduced at first. Then, the operation mode of the converter, which is zero-voltage switching operation mode, will be demonstrated. Furthermore, a mathematical model is provided to calculate the current waveform of all the components in the circuit. And voltage stress of all the components is analyzed. At last, the RMS values of the currents flowing through all the components are analyzed.

5.2.1. Circuit Configuration and Operation States of the Analyzed Converter

Figure 5.1 shows the generalized circuit architecture of the analyzed converter. This architecture has two parts. On one hand, the devices that are floating in reference to the ground are called wing side devices. On the other hand, the other devices in the half-bridges that are connected to the ground or output directly are called rectifier side devices, they work as synchronous rectifiers in the circuit. Figure 5.2 shows a converter with six times voltage conversion ratio based on the presented circuit architecture. It is composed by 16 switching devices, 10 devices on the rectifier side and 6 devices on the wing side. Figure 5.3 shows a converter that achieves the same function, but with different voltage clamping strategy. In this converter, all the devices have the same current stress and voltage stress. Since the basic circuit operation principle of both circuits are the same, this work uses the converter shown in Figure 5.2 as an example.

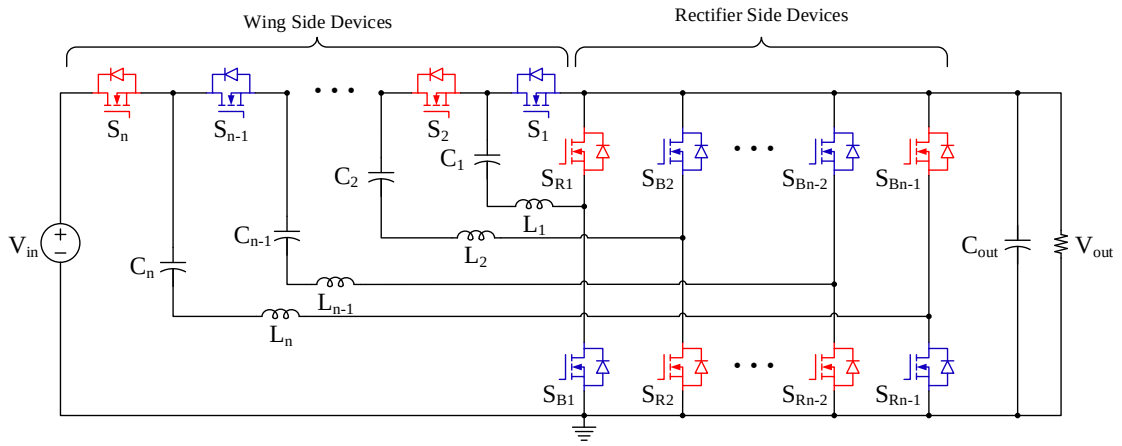

Figure 5.1. System level configuration of the proposed converter

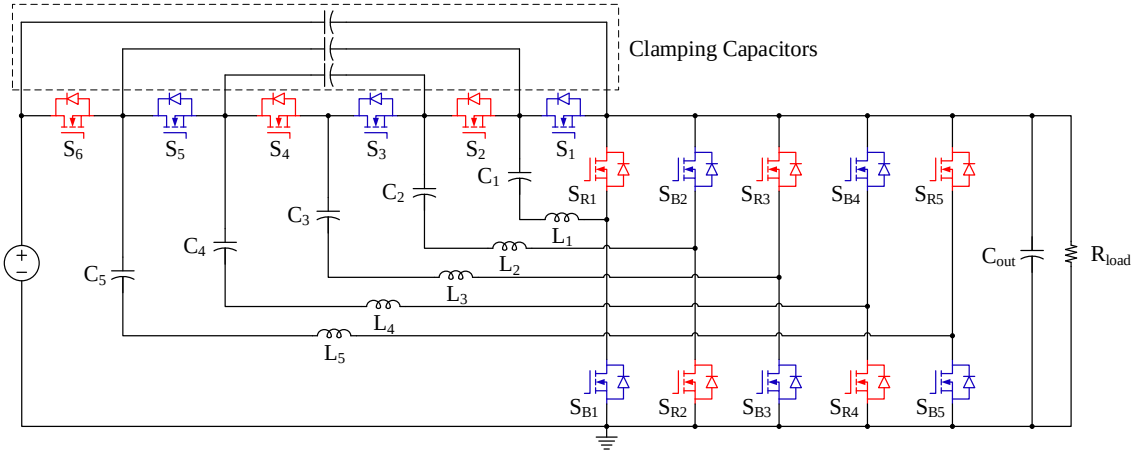

Figure 5.2. The proposed converter with both 2x and 1x devices

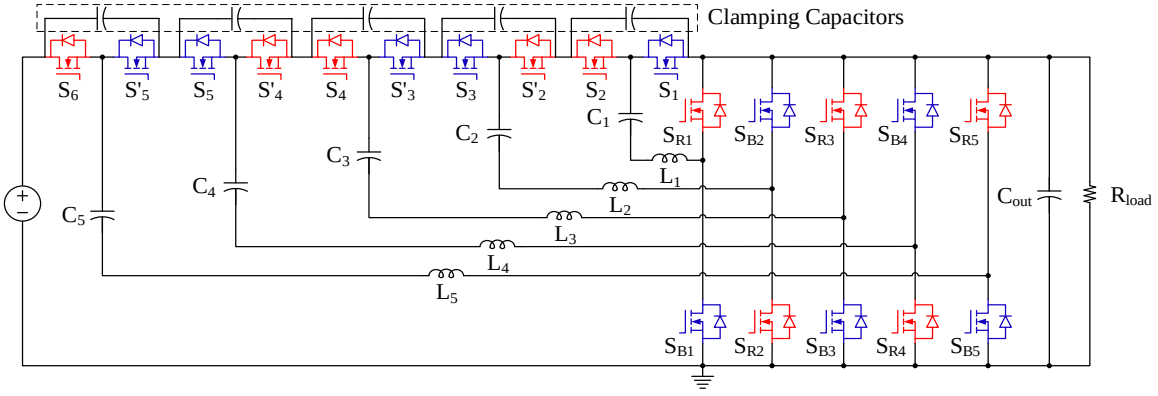

Figure 5.3. The proposed converter with only 1x devices

The presented converter can operate at two operation modes, which are zero-current switching mode and zero-voltage switching mode. In the zero-current switching mode, all the

switching devices can achieve zero-current turn-on and turn-off. In the zero-voltage switching mode, all devices can achieve zero-voltage turn-on through phase-shift control. The converter design and optimization method for zero-current switching operation is accomplished in [105], [142], [144]. This work focuses on analyzing and designing the converter that is operating at zero-voltage switching mode. Note that the switches that have the same color on wing side turn-on and turn-off at the same time, so does the switches on the rectifier side. Figure 5.4 to Figure 5.7 shows the four switching states of the analyzed converter. The four switching states can be classified into two parts, which are two phase-shift states and two non-phase-shift states. When the switches that have the same color on the wing side and rectifier side are conducting simultaneously, as shown in Figure 5.4 and Figure 5.5, the two switching states are called non-phase-shift states. On the other hand, Figure 5.6 and Figure 5.7 shows the two phase-shift states.

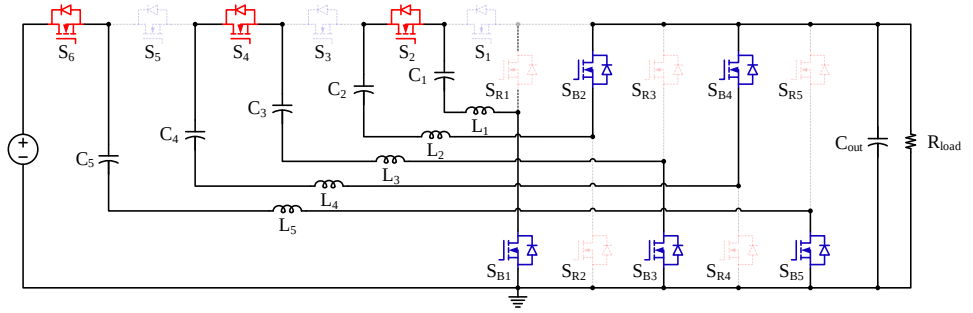

Figure 5.4. State 1

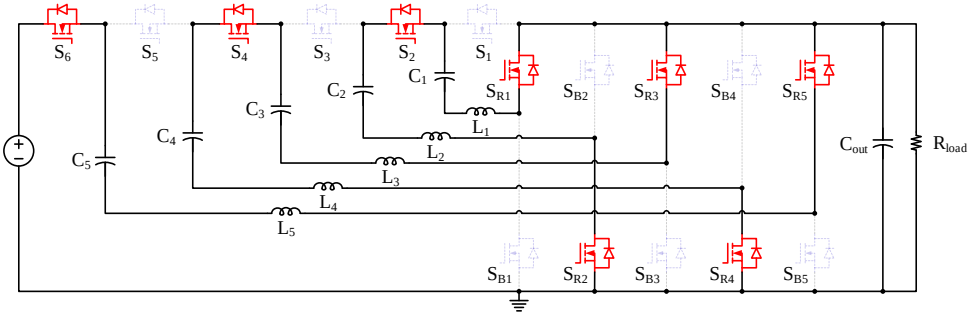

Figure 5.5. State 2

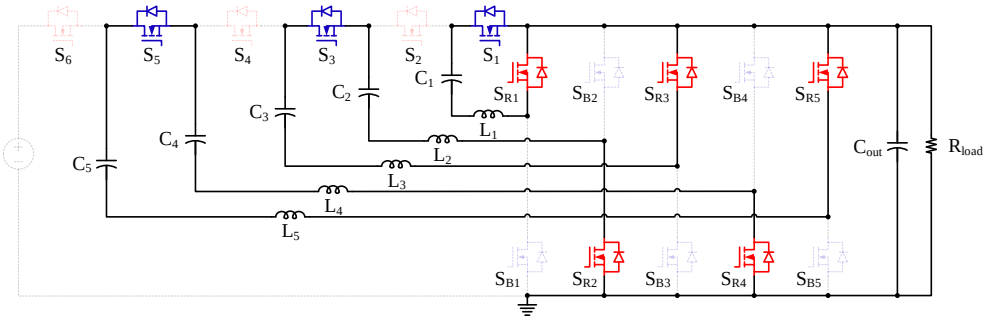

Figure 5.6. State 3

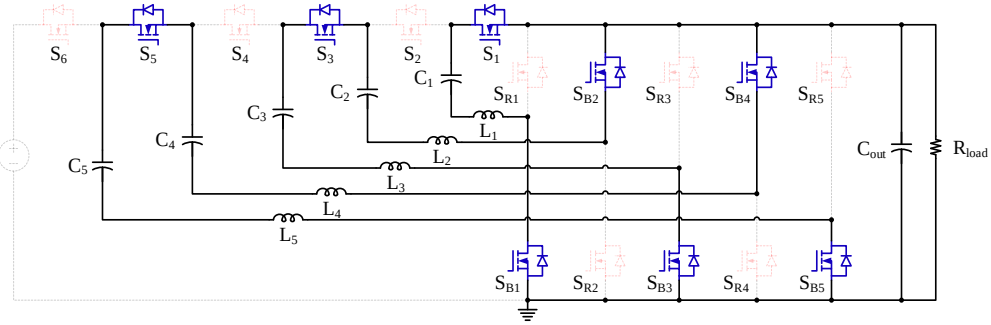

Figure 5.7. State 4

According to volt-second balance relationship on all the resonant inductors, one can easily tell that the DC voltage values across the capacitors C5 to C1 are $5V_{out}$, $4V_{out}$, $3V_{out}$, $2V_{out}$ and V_{out}. The voltage stress of S_6, S_1 and all the rectifier side devices is V_{out}. And switch S_2, S_3, S_4, S_5 have a stress of $2V_{out}$. In general, for a converter with N times conversion ratio, the DC voltage bias on capacitor C_n is (N-1/N) times the voltage of the input voltage, this means $V_{Cn} = (N - 1/N) * V_{in}$. In the circuit architecture shown in Figure 5.1, two different voltage stress can be observed on the switching devices. For the devices that are located on the wing side, the voltage across devices S_1 and S_n is two times the output voltage ($2V_{out}$), while the other wing side devices have a voltage stress of V_{out}. For the devices that are located on the rectifier, their voltage stress is V_{out}.

For more detailed analysis, the current waveforms of all the components will be analyzed. To simplify the analysis, the following assumptions have been made:

- All the switching devices in the analyzed circuit are ideal, their dynamic switching behavior and on-state resistance are not considered in the analysis.
- Voltage ripples across the input capacitor, output capacitor and resonant capacitor are small enough, which means $V_{Cin} = V_{in}, V_{Cout} = V_{out}, V_{Cn} = (N - 1/N) * V_{in}$.
- Deadtime is not considered in this analysis.
- The parameters of all resonant branches are identical. Thus, all the resonant tanks have the same current waveforms.

In order to achieve zero-voltage switching on all of the switching devices, the switching frequency should set to be higher than the resonant frequency of the resonant tank in the ZVS operation mode, which means the resonant circuit should operates at inductive impedance region of the LC tank, as shown in Eq.5.1.

$$f_s = \frac{1}{T_s} > \frac{1}{2\pi\sqrt{L_r C_r}} \quad \text{(Eq. 5.1)}$$

Here, L_r and C_r are the resonant inductance and resonant capacitance in the circuit, respectively. The f_s means switching frequency, and T_s represents the switching period.

Figure 5.8 shows the switch and inductor current waveforms of presented converter when it is operating at ZVS mode. When the switches in red on the wing side turn on, their current waveform can be divided into two parts. For the first part, the circuit is in phase-shift state, which is the state 1 in Figure 5.8. The equivalent circuit of this state is shown in Figure 5.4. During this state, the rectifier side devices S_{Bx} is conducting. And the drain-source current of the wing side devices S_2, S_4 and S_6 change from negative to positive with a slope of V_{out}/L_r. Note that the amplitude of positive part and negative part of the current are the same. For the second part, the circuit operates in non-phase-shift mode, the equivalent circuit of this state can be found in Figure 5.5. With the assumption that voltage ripple across all the capacitors is small enough, the voltage

across the inductors is close to zero. Thus, the inductor current can be considered to be a relatively constant value throughout this state. Similarly, the components' current waveforms of equivalent circuits Figure 5.6 and Figure 5.7 are corresponding to the waveforms during state 2 and state 3 in Figure 5.8, respectively.

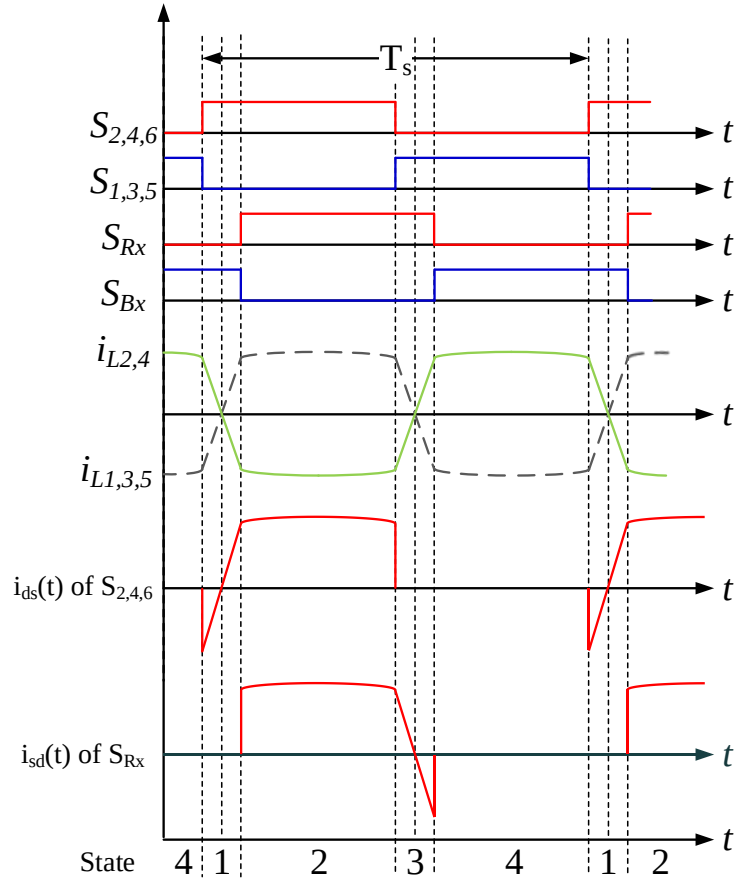

Figure 5.8. Waveforms of inductors and switching devices

5.2.2. ZVS Operation of the Presented Converter

The presented converter can operate at ZVS mode with or without closed loop phase-shift control. By utilizing the resonant inductor in the resonant circuit, the phase-shift control enables zero-voltage switching on all the switching devices. In half a switching period, the detailed converter operation can be divided into eight states in order to show the realization of ZVS. Figure 5.9 shows the detailed switching transient waveforms of the eight states. And the equivalent

circuits of these eight states are shown in Figure 5.10 to Figure 5.17. Note that we assume the converter already reaches the steady state in this study.

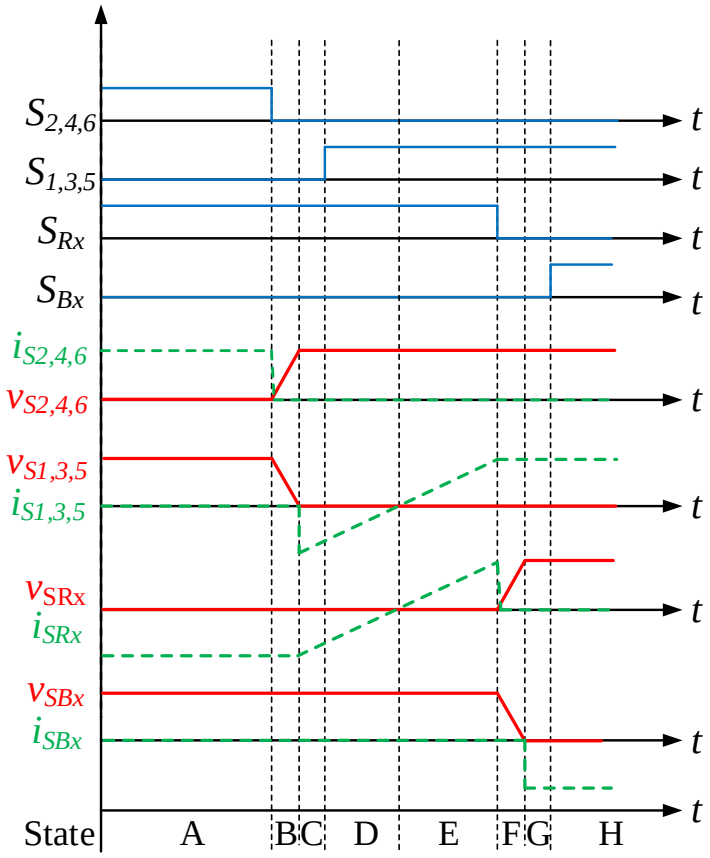

Figure 5.9. Commutation waveforms of ZVS operation

State A: In this state, MOSFETs S_2, S_4, S_6 and $S_{R1\text{-}5}$ are conducting. Capacitor C_1, C_3 and C_5 are charging, while C_2 and C_4 are discharging. The C_2, C_4 and the source are providing energy to the output during this state.

State B: MOSFETs S_2, S_4 and S_6 turn off at the beginning of this state. The inductor currents commute from the MOSFETs to the output capacitors of S_1 to S_6. Therefore, the inductors will interact with the output capacitors of the MOSFETs on the wing side, which are C_{s1} to C_{s6}. The inductor currents discharge the MOSFETs' output capacitors C_{s1}, C_{s3}, C_{s5}, and charges

capacitors C_{s2}, C_{s4}, C_{s6}. Note that after the MOSFETs' output capacitors are fully discharged, they will not be charged again in ideal case.

State C: After the capacitors C_{s1}, C_{s3} and C_{s5} are fully discharged the correspoinding device body diodes will kick in and keep the voltage accorss the devices equal to the diode forward voltage. During this state, all the inductor currents start approaching zero, because the voltage across the inductors is the output voltage.

State D: MOSFETs S_1, S_3 and S_5 turn on at the beginning of this state. Because their output capacitors C_{s1}, C_{s3} and C_{s5} are fully discharged in last state, the zero-voltage switching of these devices has been achieved. At the end of this state, all the inductor currents reaches zero.

State E: All the inductor currents keep increasing in the other direction. In this state, Capacitor C_1, C_3 and C_5 are discharging, while C_2 and C_4 are charging. The C_1, C_3 and C_5 are providing energy to the output during this state.

State F: At the beginning of this state, rectifier side MOSFETs S_{R1} to S_{R5} turn off. The inductor currents commute from switches S_{R1}~S_{R5} to the rectifier side devices' output capacitors C_{SR1}~C_{SR5} and C_{SB1}~C_{SB5}. The inductors will interact with all these capacitors in order to charge or discharge them. Thus, we can recycle the energy that is stored in the capacitors.

State G: Similar to the state C, once the MOSFET output capacitors of S_{B1}~S_{B5} are fully discharged, all the currents will commute to their body diodes. After this point, the voltage across them are the same, which is the diode forward voltage.

State H: MOSFETs S_{B1}~S_{B5} turn on at the beginning of this state. Because the voltage across them is almost zero (diode forward voltage), the zero-voltage switching of these devices has been achieved.

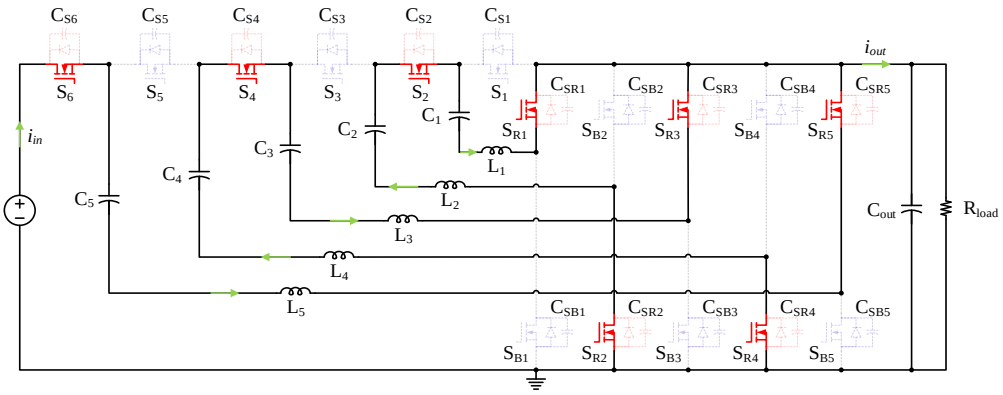

Figure 5.10. State A

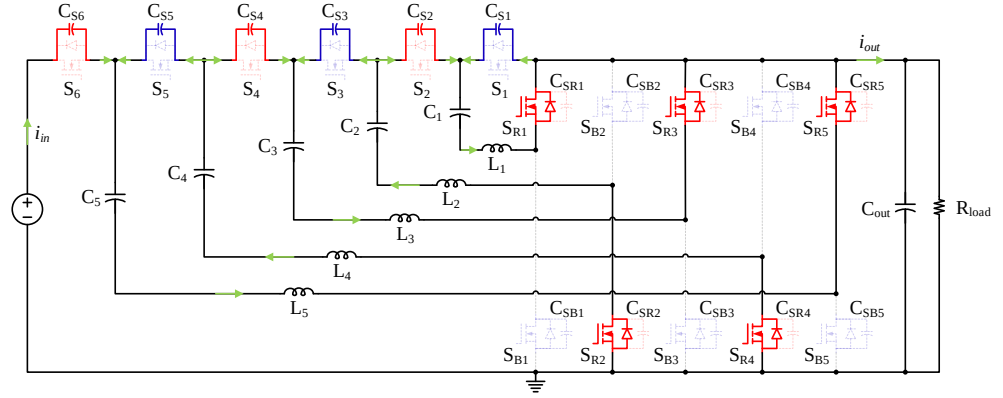

Figure 5.11. State B

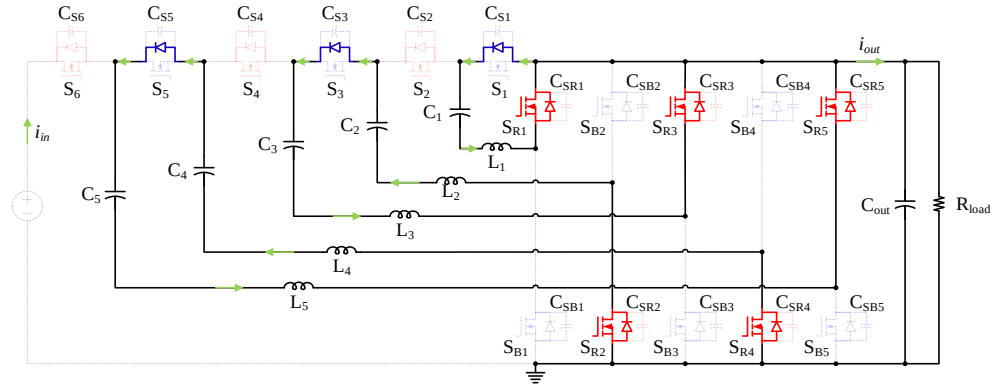

Figure 5.12. State C

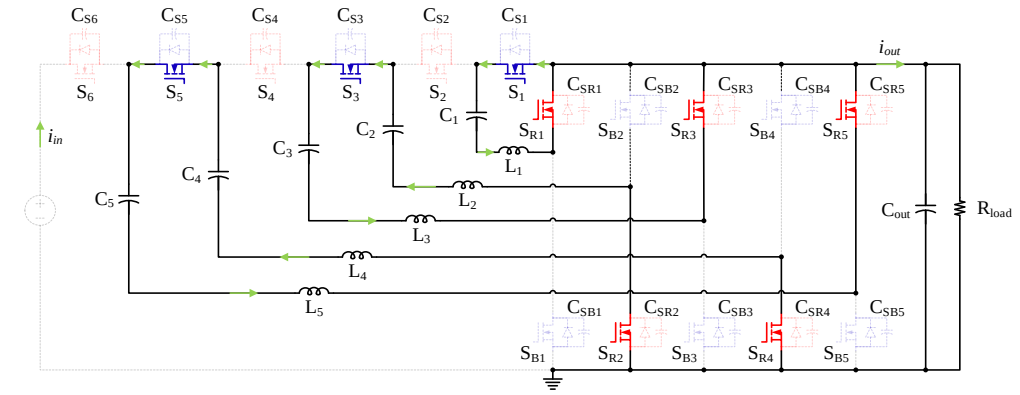

Figure 5.13. State D

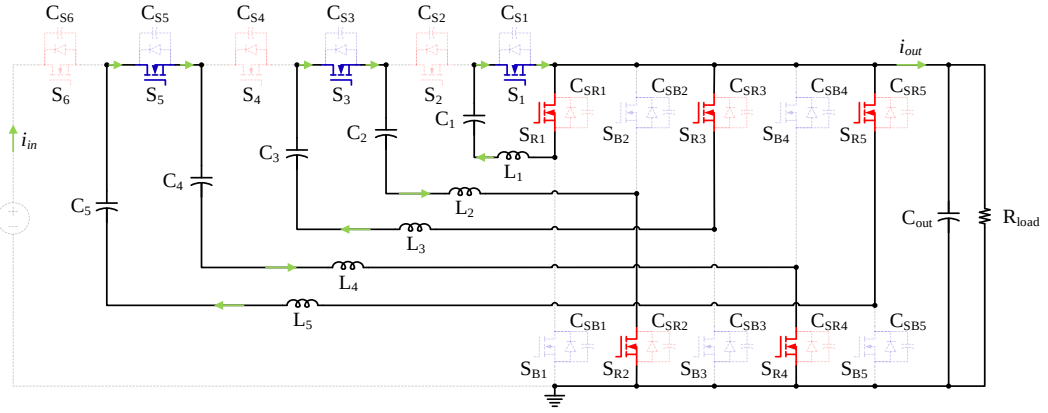

Figure 5.14. State E

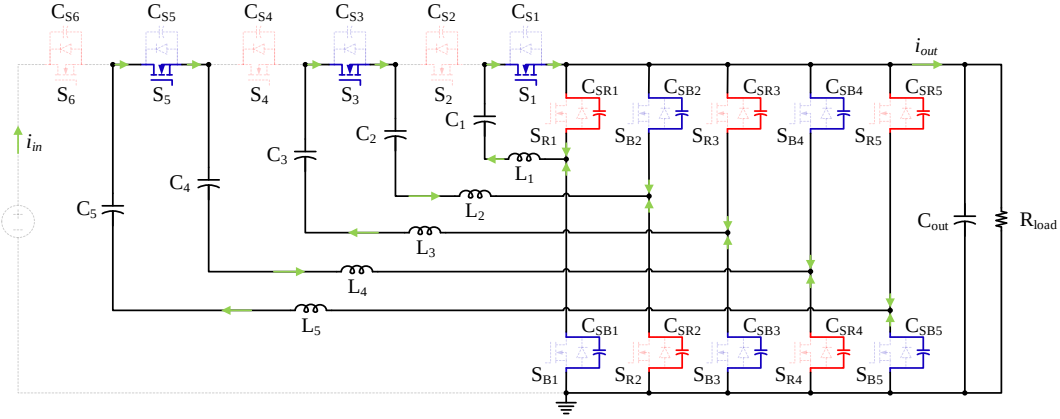

Figure 5.15. State F

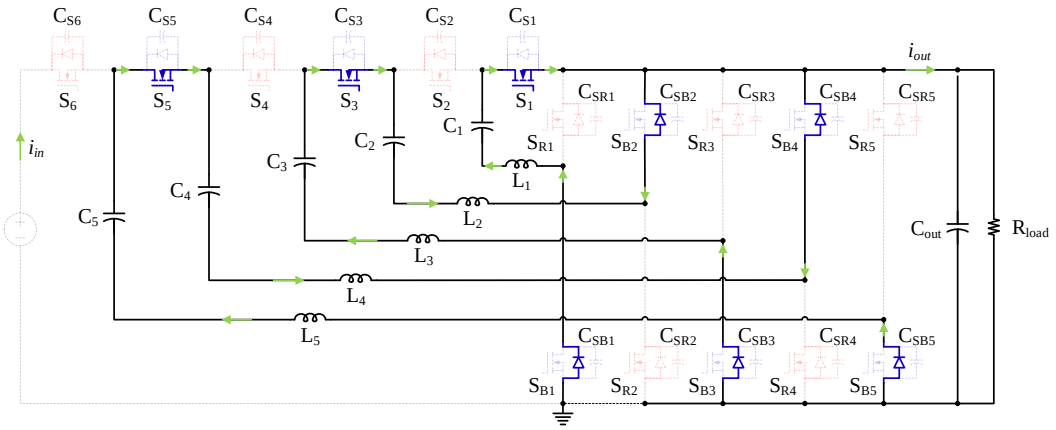

Figure 5.16. State G

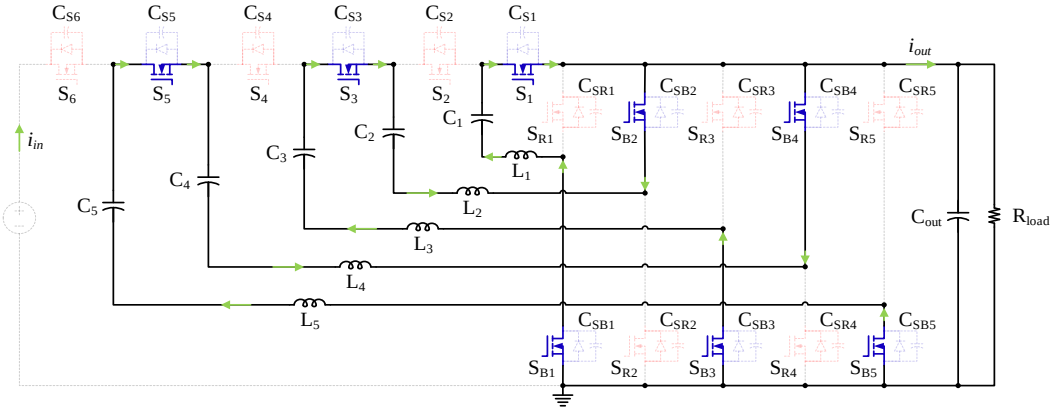

Figure 5.17. State H

So far, the switch current waveforms at ZVS operation have been analyzed according to the equivalent circuit. And zero-voltage switching mechanism is introduced in this section. Because the implementation of ZVS operation is closely related to the resonant tank design, more detailed information regarding zero-voltage switching mechanism will be discussed in the future section.

5.2.3. The RMS Value of the Current Flowing Through All the Components

In order to calculate the RMS value of the current flowing through the switching devices, the average current flowing through them has to be figured out as the first step. According to the four operating states shown in Figure 5.7, we can tell that there are always three branches

delivering power to the output at the same time. Because the conduction time of all the switching devices are the same, the average current flowing through all the switching should also be identical. Thus, the average current flow through each device I_{sw_avg} can be calculated according to the conversion ratio *N* and the output current of the presented converter I_{out}, as shown in Eq.5.2.

$$I_{sw\_avg} = \frac{I_{out}}{3} \quad \text{(Eq. 5.2)}$$

In general case, the average current flow through each switch in a converter with *N*:1 voltage conversion ratio can be calculated through Eq.5.3. Where the P_{out} represents the output power of the converter, V_{out} represents the output voltage.

$$I_{sw\_avg} = \frac{I_{out}}{N} = \frac{P_{out}}{V_{out} * N} \quad \text{(Eq. 5.3)}$$

According to Eq.5.3, the device average current is a function of converter output current I_{out} and voltage conversion ratio N. On the other hand, by analyzing the switch current waveform shown in Figure 5.8, one can tell that the average current during the phase-shift state is zero. This means the switch's average current value equals to its average current value during non-phase-shift state. Assume the phase-shift time is T_{shift}, the average value of the current flowing through each switching device can be calculated, as shown in Eq.5.4.

The next step is to figure out the current waveform of the switching devices. By plugging Eq.5.3 into Eq.5.4, the relationship between phase-shift time and other key parameters of the converter (switching frequency, resonant inductance, voltage conversion ratio, output voltage, output current) can be derived, as shown in Eq.5.5. With the phase-shift time information, the device current waveform can be calculated. Eq.5.6 shows the derived equation that represents the waveform of current flowing through S_2, S_4 and S_6. The current waveform shape of switches S_1, S_3 and S_5 is the same with that of S_2, S_4 and S_6. Similarly, the waveforms of the current flowing

through all the rectifier side devices can be also derived. Furthermore, the current waveform of all the resonant tank components can be derived, which can be found in Eq.5.7.

$$I_{sw\_avg} = \frac{V_{out} T_{shift}}{2 T_s L_r} * (\frac{T_s}{2} - T_{shift}) \quad \text{(Eq. 5.4)}$$

$$T_{shift} = \frac{T_s}{4} - \sqrt{\frac{T_s^2}{16} - T_s \frac{2 I_{out} L_r}{N * V_{out}}} \quad \text{(Eq. 5.5)}$$

$$i_{sw\_zvs}(t) = \begin{cases} -\left(\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right) + \frac{t}{\frac{L_r}{V_{out}}}, & 0 \le t \le T_{shift} \\ \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}, & T_{shift} \le t \le \frac{T_s}{2} \\ 0, & \frac{T_s}{2} \le t \le T_s \end{cases} \quad \text{(Eq. 5.6)}$$

$$i_{L\_zvs}(t) = \begin{cases} -\left(\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right) + \frac{t}{\frac{L_r}{V_{out}}}, & 0 \le t \le T_{shift} \\ \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}, & T_{shift} \le t \le \frac{T_s}{2} \\ \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2} - \frac{t - 0.5T_s}{\frac{L_r}{V_{out}}}, & \frac{T_s}{2} \le t \le T_s + T_{shift} \\ -\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}, & T_s + T_{shift} \le t \le T_s \end{cases} \quad \text{(Eq. 5.7)}$$

Finally, with the switch current waveform represented in Eq.5.6, the RMS value of the current flow through the switching devices can be calculated using Eq.5.8.

$$I_{sw\_zvs\_rms} = \sqrt{\frac{1}{T_s}\left[\int_0^{T_{shift}} (\frac{t}{\frac{L_r}{V_{out}}} - \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2})^2 dt + \int_{T_{shift}}^{0.5T_s} (\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2})^2 dt\right]} \quad \text{(Eq. 5.8)}$$

5.2.4. Design Target of the Presented Converter

Since the previous part has analyzed the device current waveform of when the converter operates at ZVS mode, we can easily tell that the device RMS current in ZVS operation is not only related to the output current and voltage conversion ratio of the converter, but also depends on switching period Ts, phase-shift time Tshift, and the value of L_r/V_{out}, which is shown in Eq.5.8.

According to Eq.5.5, the phase-shift time T_{shift} is decided by switching period T_s, converter output current I_{out}, converter voltage conversion ratio N and the value of L_r/V_{out}. If we consider Eq.5.5 and Eq.5.8 at the same time, the devices RMS current in ZVS operation mode is related to four factors, which are converter output current, converter voltage conversion ratio, switching frequency and the value of resonant inductance divided by output voltage.

In order to analysis the range of RMS value of switch current when the presented converter has a certain output current value, current waveform with square shape is analyzed at first. There are two reasons of doing this. First, we assume the two different current waveforms shown in Figure 5.18 have the same average value within a certain period. The RMS value of the square shape is the lowest among them, which can be verified through the following analysis. Second, the device current waveform in ZVS operation mode is close to square shape when the di/dt of phase-shift part current waveform is very high, as shown in Figure 5.19. Therefore, the waveforms appear in Figure 5.18 and Figure 5.19 represent the switch current waveforms in ZVS operation and switch current waveforms in ZVS operation with extremely low phase-shift time.

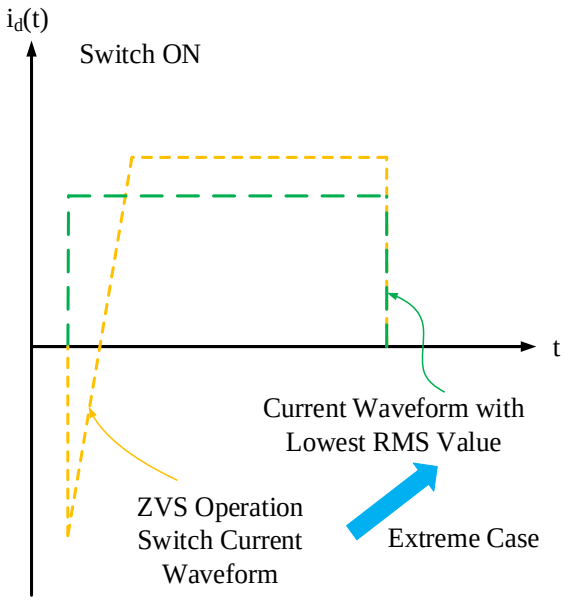

Figure 5.18. Two current waveforms that has the same average value

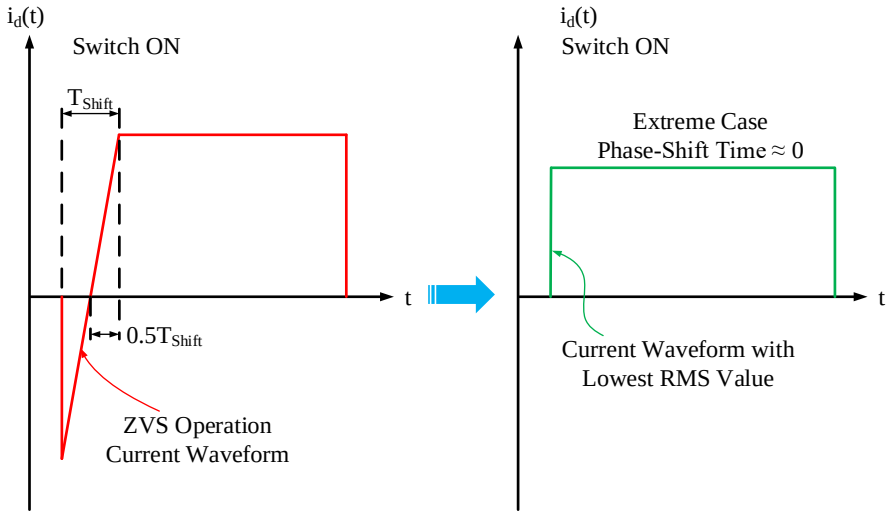

Figure 5.19. Switch current waveforms in ZVS operation (with/without phase-shift time)

Assume all the switching devices in the converter has square current waveform when the converter operates at steady state, then the switch current waveform can be derived accordingly, as shown in Eq.5.9. We can tell that the magnitude of the square waveform is a function of converter output current and conversion ratio. And Eq.5.10 calculates the RMS value of the square shape current waveform. With the same converter output current, the calculation based on Eq.5.8

and Eq.5.10 shows that when the converter operates at ZVS operation and has extremely low phase-shift time, the device RMS current is minimum. Note that the switch current waveform in ZVS operation mode can only infinitely close to a square waveform, which means it cannot be square shape and the RMS value of the square waveform is theoretically the lowest RMS value of switch current in ZVS operation. In Figure 5.20, the possible design region for ZVS operation of the presented 6x converter is demonstrated. This means in order to keep the conduction loss of the switching devices at a minimum level, the switch current waveform should as close to square shape as possible. For example, if the switching device RMS current can be reduced by 10%, the semiconductor conduction loss of the converter can be reduced as high as 19%, which is a big improvement of a converter for low voltage high current application. With the benefit of reducing conduction loss, the presented converter with ZVS operation has the potential to achieve superior efficiency. Therefore, a comprehensive analysis of converter parameters for ZVS operation is very meaningful. And the design procedure will be provided in the following section.

$$i_{square}(t) = \begin{cases} \frac{2I_{out}}{N}, & 0 \le t \le \frac{T_s}{2} \\ 0, & \frac{T_s}{2} \le t \le T_s \end{cases} \quad \text{(Eq. 5.9)}$$

$$I_{sw\_square\_rms} = \frac{\sqrt{2}I_{out}}{N} \quad \text{(Eq. 5.10)}$$

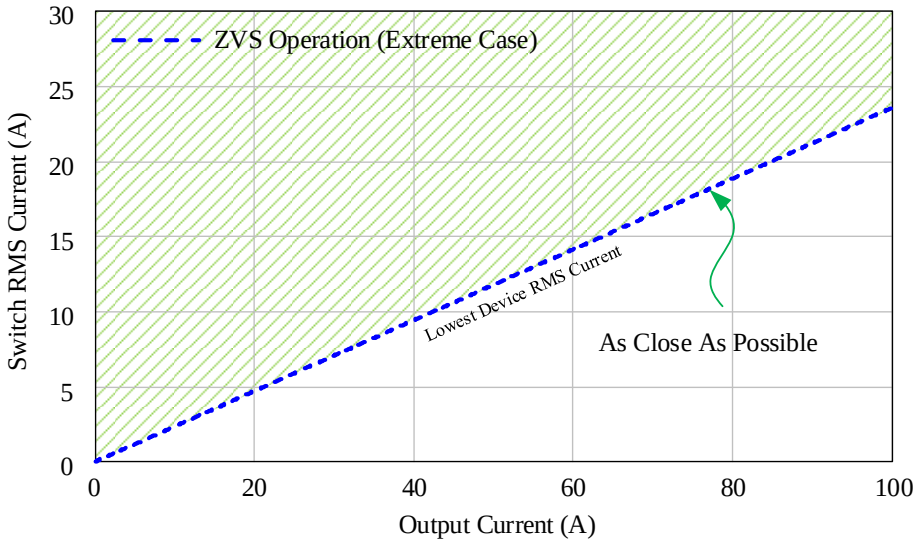

Figure 5.20. Theoretical lowest RMS current value of switching device

5.3. A Design Example of the Proposed Converter

The zero-voltage switching feature is enabled by the phase-shift control method, in order to fully leverage the advantages of the phase-shift control method, this section uses an example to show how to properly select the parameters for ZVS operation of the presented converter. For the presented converter with given power rating, voltage conversion ratio and input voltage, its output voltage and maximum output current are fixed. Based on the information obtained from previous analysis, there are three essential aspects need to be considered in terms of the converter design. First, the phase-shift time of the control signals. Second, the switching frequency of the switching devices. Third, the inductance value of resonant inductors in the circuit.

In Table 5.1, the basic converter specification in this design example is provided. In this example, the 6x multilevel modular resonant switched-capacitor converter with 54V input and 9V output will be analyzed and designed. The typical and maximum output power of the converter is 450W and 600W, respectively. And the output current capability of the converter is 66.6A. It is worth mentioning that the specification of this converter is a representative specification of

intermediate bus converter that are used in data center application. And we can tell that the converter has low voltage and high current output.

The design procedure is divided into two parts. The part-one focuses on preliminarily determining the key parameters of the converter and make sure it has enough power delivery capability. The part-two focuses on further selection of the converter parameters so that it can achieve superior performance.

Table 5.1. Basic Converter Specification Used in the Design Example

Description	Items	Values
Voltage Conversion Ratio	N	6
Typical Input Voltage	V_{in}	54 V
Typical Output Voltage	V_{out}	9 V
Typical Output Power	P_{out_typ}	450 W
Typical Output Current	I_{out_typ}	50 A
Maximum Output Power	P_{out_max}	600 W
Maximum Output Current	I_{out_max}	66.6A

5.3.1. Design Constrains

Because the ultimate goal of the phase-shift control method is to control the output current of the converter by adjusting the phase-shift time, there is no doubt that the determination of the key parameters (e.g.T_{shift}, f_s and L_r) needs to ensure the designed converter delivers enough power to the output.

The first step of the design procedure is to find the relationship between the converter output current and phase-shift time. According to Eq.5.2, when the converter delivers maximum current within its output current capability, the average value of current flow through switching devices is maximum. Therefore, when the derivative of switch average current shown in Eq.5.4 equals to zero, the phase-shift time that allows the converter generates the maximum output current

can be found, as shown in Eq.5.11. As a result, when the phase-shift time T_{shift} equals to 1/4 of the switching period T_s, the presented converter has the highest output current. With this information, we use the maximum converter output current as the base value, the relationship between the normalized output current and phase-shift time can be calculated using Eq.5.12. Figure 5.21 shows the calculated results. When $0 < T_{shift} < 0.25T_s$, the converter's output current capability increases as the increase of phase-shift time. On the other hand, when $0.25T_s < T_{shift} < 0.5T_s$, the converter's output current capability and phase-shift time has negative relationship. This means for a certain output current value, there are two corresponding phase-shift time. Figure 5.22 shows two example device current waveforms that have the same average value in ZVS operation mode and their equivalent waveforms that are used to calculate the RMS values. According to Figure 5.22, we can tell that the waveform in solid line has lower RMS value. As a result, in order to allow the converter to achieve the best performance, the range of phase-shift time should vary from 0 to $0.25T_s$.

$$I'_{sw\_avg}(T_{shift}) = 0 \quad \text{(Eq. 5.11)}$$

$$I_{sw\_avg\_nom} = \frac{16T_{shift}}{T_s^2} * \left(\frac{T_s}{2} - T_{shift}\right) \quad \text{(Eq. 5.12)}$$

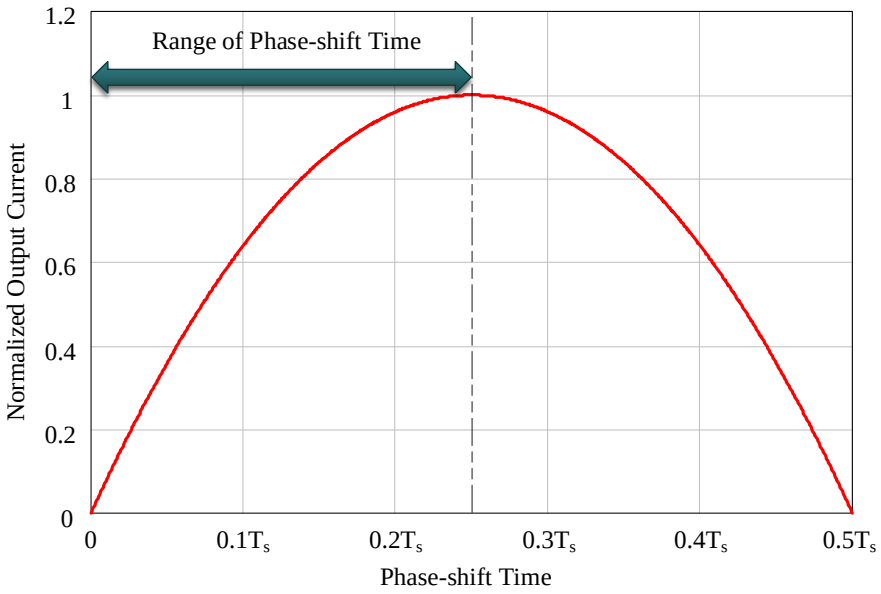

Figure 5.21. Relationship between the phase-shift time and converter normalized output current

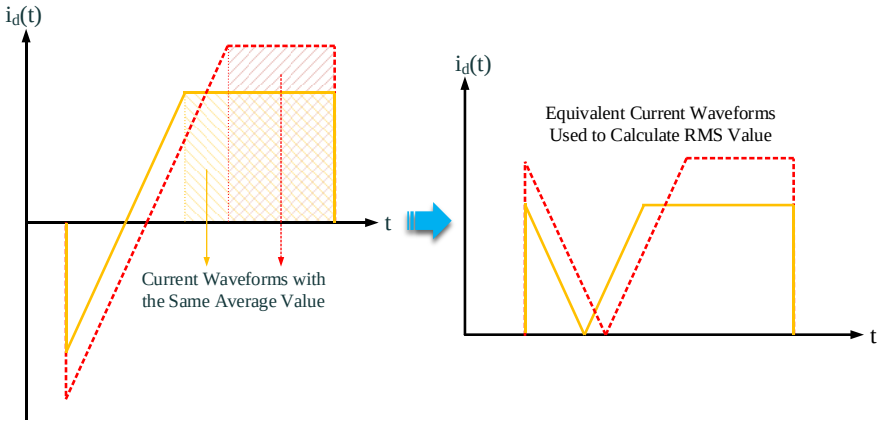

Figure 5.22. Lower phase-shift time enables lower device RMS current

With the information that the presented converter generates the most output current within its current output capability when $T_{shift} = 0.25T_s$, the next step is to find out the relationship between switching frequency and the output current capability of the converter. By plugging $T_{shift} = 0.25T_s$ into Eq.5.4, we can derive the maximum average current flow through each switching device under different conditions, which is shown in Eq.5.13. Consequently, the output current capability of the converter can be calculated using Eq.5.14. We can tell that the converter's maximum output current is a function of input voltage, switching frequency and resonant

inductance. Figure 5.23 shows the converter's normalized output current capability when the switching frequency sweep from 10kHz to 1MHz. In this normalization, the base value is the converter's maximum output current when it operates at 10kHz. Note that the normalized output current is only a function of switching frequency. We can tell that the converter's normalized output current capability drops significantly as the increase of switching frequency at the low frequency range. In other words, the maximum output current relies on the switching frequency a lot when the converter operates at low frequency (e.g. less than 100kHz). For example, the converter's output current capability deceases 90% when the switching frequency of the converter increases from 10kHz to 100kHz. From 100kHz to 1MHz, the change of converter's output current capability is less than 10%. Although low switching frequency enables high output current capability of the converter, it requires large volume of passive components. And for intermediate bus converter, power density is a very important factor. Therefore, high switching frequency is preferred in this design example.

$$I_{sw\_avg(max)} = \frac{V_{out}}{32 f_s L_r} \quad \text{(Eq. 5.13)}$$

$$I_{out(max)} = \frac{N * V_{out}}{32 f_s L_r} = \frac{V_{in}}{32 f_s L_r} \quad \text{(Eq. 5.14)}$$

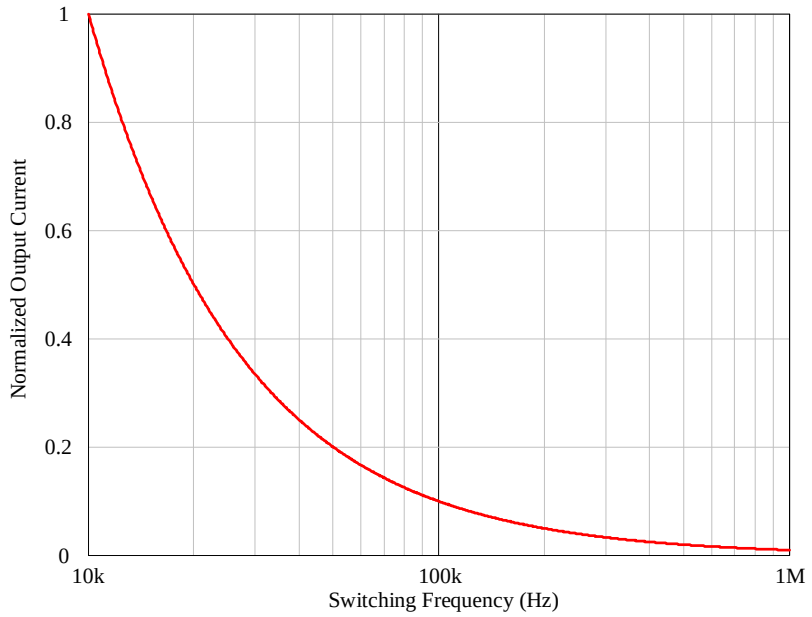

Figure 5.23. Relationship between the switching frequency and normalized converter output current

Finally, the inductance of resonant inductor needs to be properly selected in order to allow the converter has sufficient power delivery capability. It's worth mentioning that the inductors whose inductance value is within a few hundreds of nanohenry have been proven to be good choices in a similar design [142]. Because they have the potential to allow the converter to achieve both high power density and high efficiency at the same time. Therefore, we start from the off-the-shelf inductors shown in Table 5.2, whose inductance values are 36nH, 50nH and 70nH. In order to broaden the range of inductance in this analysis, we also assume that a customized 18nH inductor can be used in the design. In Figure 5.24, the four inductance values are evaluated. As the inductance value decreases, the converter's output current capability is significantly increased. Table 5.3 shows that the 18nH inductor allows the converter operates at above 1MHz, while the maximum switching frequency of the converters with 36nH, 50nH and 70nH inductors are limited to 696kHz, 498kHz and 359kHz, respectively. This also means that with the same switching

frequency, lower inductance value ensures higher output current capability of the presented converter.

Table 5.2. Inductor Candidates Used in the Design Example

Part Number	Values
Customized	18nH
SLC7649S-360KL	36nH
SLC7649S-500KL	50nH
SLC7649S-700KL	70nH

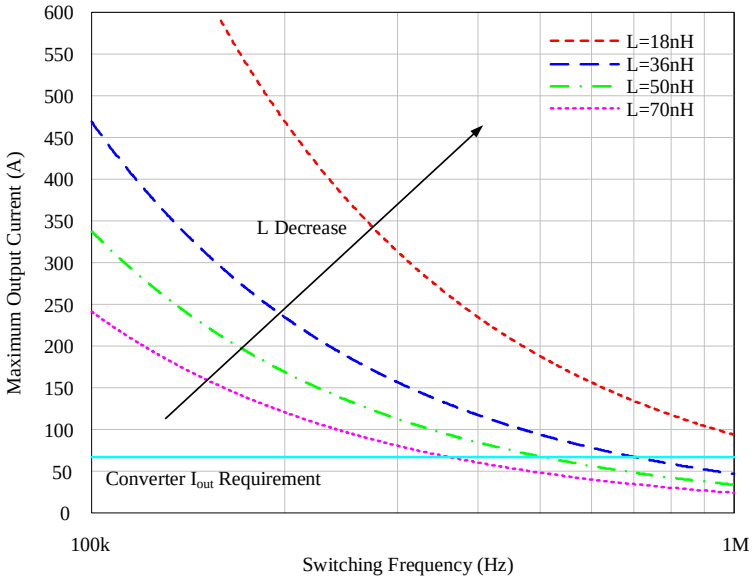

Figure 5.24. Maximum converter output current in terms of switching frequency and resonant inductance

Table 5.3. Relationship Between Resonant Inductance and Switching Frequency

Resonant Inductance Value	Maximum Switching Frequency
18 nH	>1 MHz
36 nH	696 kHz
50 nH	498 kHz
70 nH	359 kHz

5.3.2. Detailed Design Procedures

In addition to make sure that T_{shift}, f_s and L_r allows the converter to have enough power delivery capability, some other design criteria need to be further analyzed in order to achieve the optimized design. Because in the low voltage high current output application, one of the major power loss contributors is semiconductor conduction loss, the primary goal of the optimum design is to achieve low device RMS current in the ZVS operation.

By plugging Eq.5.5 into Eq.5.8, the parameter number that determines the RMS value of the current flow through switching devices can be reduced from five to four. We can tell that the device RMS current is a function of the converter output current if the resonant inductance, output voltage and switching frequency are determined. In order to evaluate the effect of inductance value on the RMS value of switch current, four inductance values shown in Table 5.3 are used to calculate the normalized switching device RMS current values. Because the maximum switching frequency is 359kHz when 70nH inductors are used in the circuit, we assume the switching frequency is 350kHz. So all the four inductance values shown in Table 5.3 can be included in the evaluation. Here we define the normalized switching device RMS current as follows:

$$i_{sw\_zvs\_norm}(V_{out}, I_{out}, L_r, f_s) = \frac{i_{sw\_zvs\_rms}(V_{out}, I_{out}, L_r, f_s)}{i_{sw\_square\_rms}(I_{out})} \qquad \text{(Eq. 5.15)}$$

In Eq.5.15, the base value used in the normalization is RMS value of square current waveform, which is represented by $i_{sw\_suqare\_rms}$. And the RMS values of current flowing through switching devices in the converter are represented by $i_{sw\_zvs\_rms}$. The term $i_{sw\_zvs\_norm}$ means the normalized switching device RMS current of the converter.

According to Figure 5.25, as the increase of converter output current, low inductance value allows the switching devices in the converter has lower RMS current due to higher di/dt of the switch current during the phase-shift state. In order to maintain low conduction loss on the switching

devices, the normalized switching device current ranges from 1 to 1.1 over whole operating range is desired in this example. Hence, 36nH and 18nH resonant inductance are preferred among the four inductance values. However, it is worth mentioning that the resonant inductance cannot be too small. There are two reasons. First, although the low resonant inductance can make sure the high output current capability as well as low device conduction loss of the presented converter, the inductance value cannot be too low in order to ensure the inductor have enough energy to charge and discharge the MOSFETs' output capacitors. In other words, a proper inductance value needs to be selected to achieve reasonable low semiconductor RMS current and soft-switching at the same time. Second, small inductance will create challenges for controller because high-resolution PWM signals and very fine phase-shift time are required. When switching frequency is 350kHz and resonant inductance is 36nH, the superior performance as well as high-density of the converter have been reached.

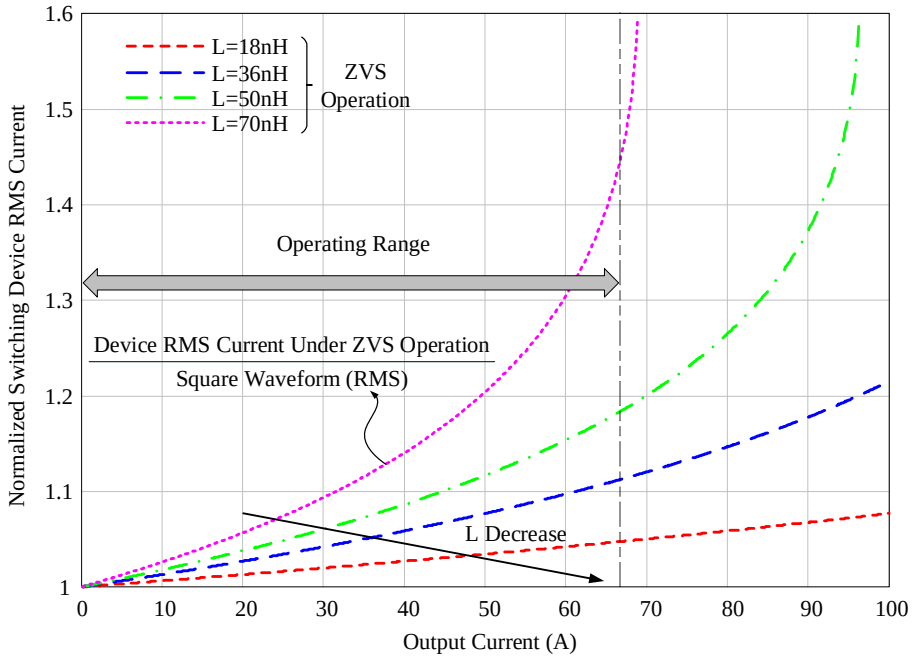

Figure 5.25. Normalized switching device RMS current when different resonant inductance are used (f_s=350k)

5.3.3. Deadtime

According to previous analysis, the inductor current value during the deadtime is the key to achieve ZVS operation. And the MOSFETs' body diodes will kick in upon the accomplishment of the zero-voltage switching process. Because the conduction of the diodes will lead to considerable power loss, the conduction time of the diodes should be minimized. Hence, proper deadtime should be estimated in order to ensure minimized power loss on the body diode. Figure 5.26 shows the circuit used to predict the deadtime. Assume the capacitances of the MOSFETs' output capacitors are Coss1 and Coss2, and the voltage stress of the two switches are Vds1 and Vds2. In order to calculate the correct deadtime, the total charge stored in MOSFETs' output capacitors is calculated by using Eq.5.16 as a first step. Assume the average inductor current during the deadtime is IL_avg, the integral of the current over the deadtime should equal to the total charge stored in Coss1 and Coss2, which is represented by Eq.5.17. Finally, the deadtime could be calculated, as shown in Eq.5.18.

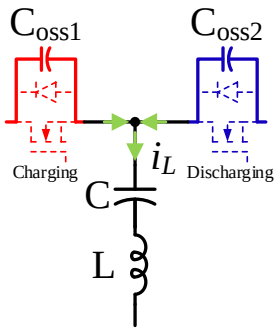

Figure 5.26. The circuit used to calculate the deadtime

$$C_{oss1}V_{ds1} + C_{oss2}V_{ds2} = Q_{coss} \quad \text{(Eq. 5.16)}$$

$$I_{L\_avg}t_{dead} = Q_{coss} \quad \text{(Eq. 5.17)}$$

$$t_{dead} = \frac{C_{oss1}V_{ds1} + C_{oss2}V_{ds2}}{I_{L\_avg}} \quad \text{(Eq. 5.18)}$$

5.4. Simulation Results

Simulation has been performed to verify the analytical analysis of the converters. Table 5.4 shows the parameters that are used in the simulation. The parameters of the switching devices are based on Infineon 25V device BSZ013NE2LS5I. The operating frequencies of the converter is 350kHz, which is aligned with the previous design example. The input voltage and output voltage are 54V and 9V. Two operating points are simulated in this section. First, the light load operation has been simulated. This operating point is the critical point that all the MOSFET's output capacitors are discharged. Second, full load is simulated to verify the theoretical RMS current calculation.

Table 5.4. Parameters Used in The Simulation

Items	Symbols	Values
Switching Frequency	f_s	350 kHz
Resonant Inductance	L_r	36 nH
Resonant Capacitance	C_r	120 uF
Output Power	P_{out}	450 W
Switch On-state Resistance	R_{ds_on}	1.25 mOhm
Switch Output Capacitance (1x Stress)	C_{oss1}	1.61 nF
Switch Output Capacitance (2x Stress)	C_{oss2}	1 nF

Figure 5.27 shows the current waveform of switching devices in the converter. The RMS value of switch current is 2.4A when the converter outputs 91W power. Figure 5.28 shows all the inductor current waveforms, which are very close to square waveforms. The peak-to-peak and RMS values of the current flow through the inductors are 7A and 3.41A, respectively. All the current values are aligned with the calculated values very well. In Figure 5.29, the voltage waveforms of all the switches are provided. The voltage stress of S2, S3, S4 and S5 is 18V, while all the other switches' stress is 9V. In Figure 5.30, ZVS waveform of one wing side device is

presented. In order to fully recycle the energy stored in the MOSFET's output capacitor, the corresponding inductor current needs to keep its flowing direction unchanged before the output capacitor is fully discharged. Similarly, Figure 5.31 shows the MOSFETs' current waveforms of the converter at full load. The simulated RMS value of current flow through all the switching devices is 12.45A. And the calculated value is 12.5A. The inductor current waveforms of the simulated converter are shown in Figure 5.32. Their peak-to-peak value and RMS value of the waveforms are 37.28A and 17.67A, respectively. And the calculated values are 37.2A and 17.8A. We can tell that the simulated converter's switch RMS current values matches the theoretical analysis.

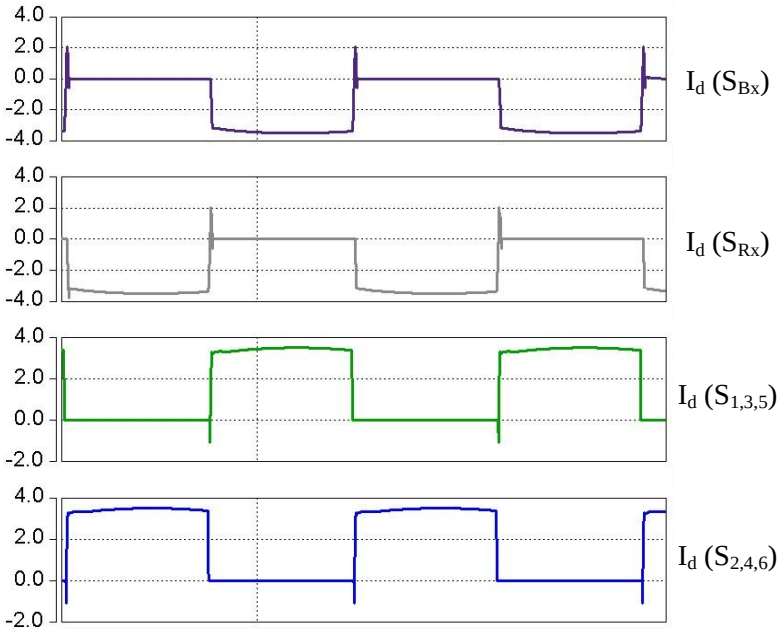

Figure 5.27. ZVS current waveforms of converter (light load)

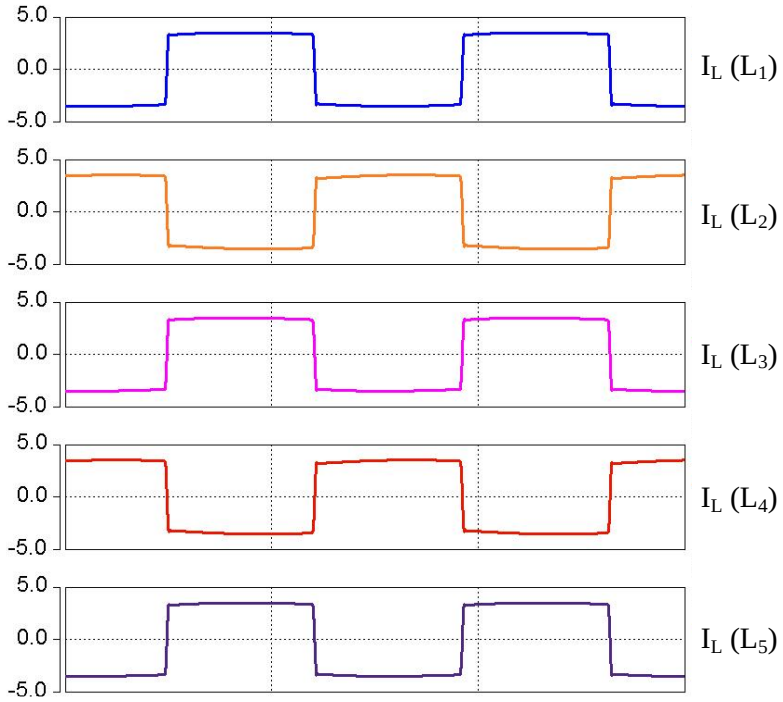

Figure 5.28. Inductor current waveforms of converter (light load)

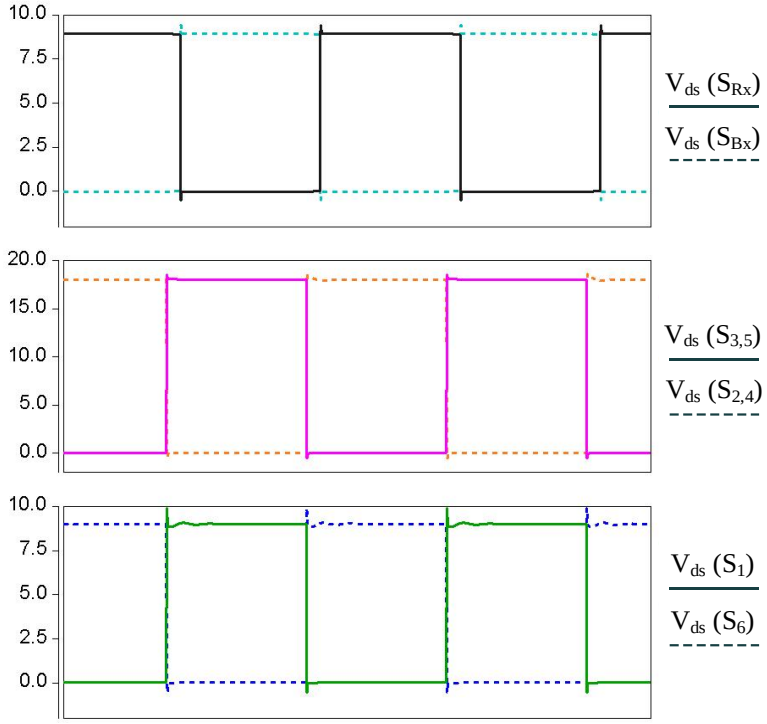

Figure 5.29. Voltage stress of switching devices (light load)

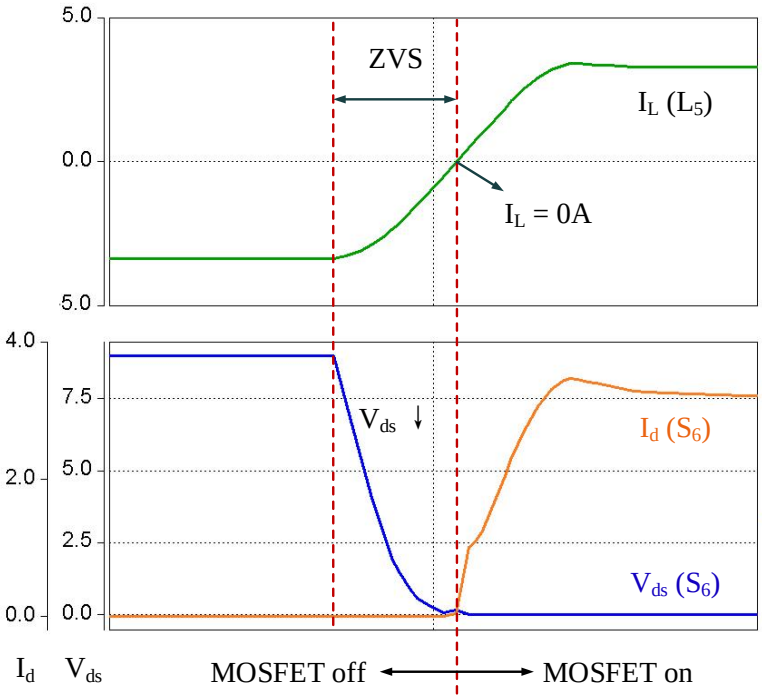

Figure 5.30. ZVS waveforms of converter (light load)

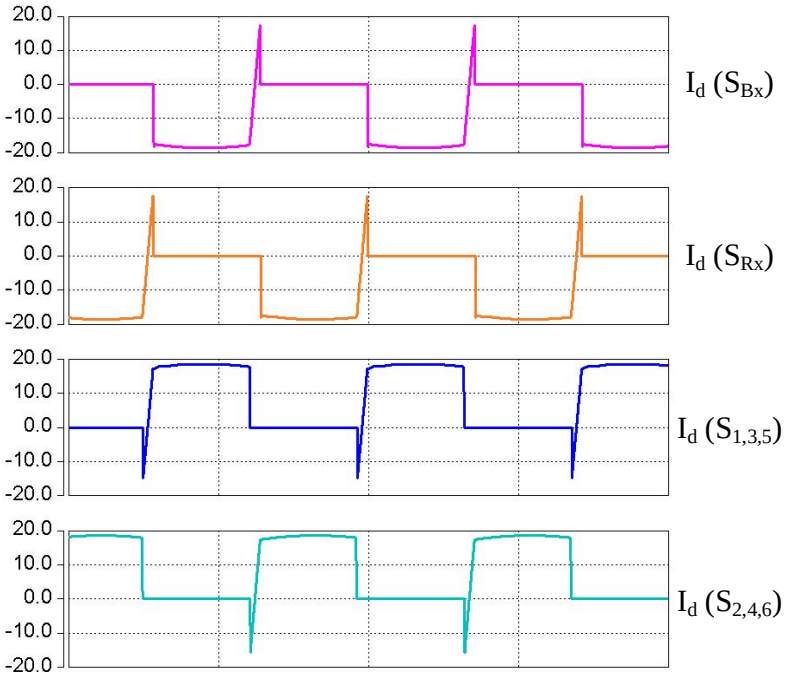

Figure 5.31. MOSFET current waveforms of converter (full load)

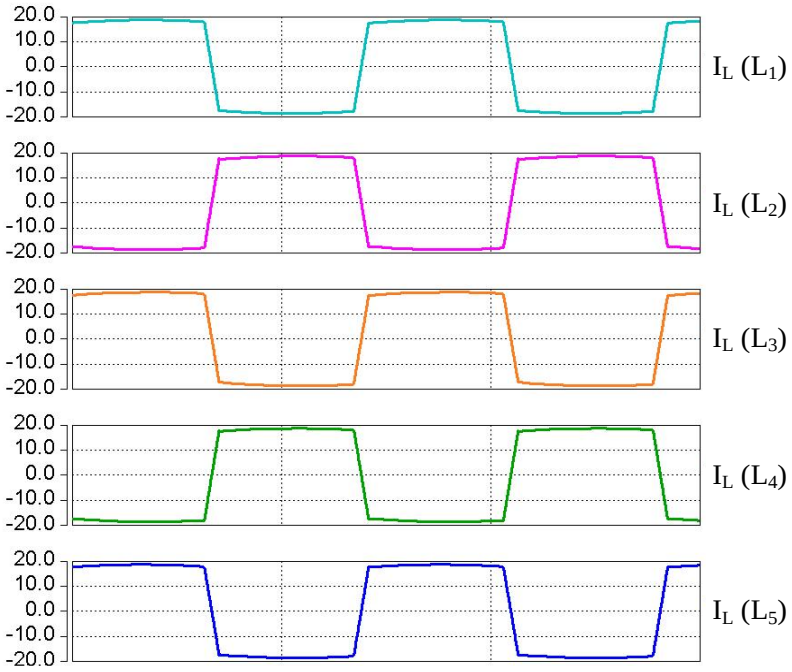

Figure 5.32. Inductor current waveforms of converter (full load)

The zero-voltage switching operation of the converter under full load has also been verified through the simulation. Figure 5.33 shows the voltage and current waveforms of all the wing side devices. According to Figure 5.33, we can tell that the two devices are fully discharged before they are turned on. Similarly, Figure 5.34 shows that zero-voltage switching is also achieved on rectifier side devices. As a result, the zero-voltage switching has been achieved on all the semiconductors devices in the presented converter. Furthermore, the time that takes to discharge the MOSFETs' output capacitors in the simulation is matched with the calculated value.

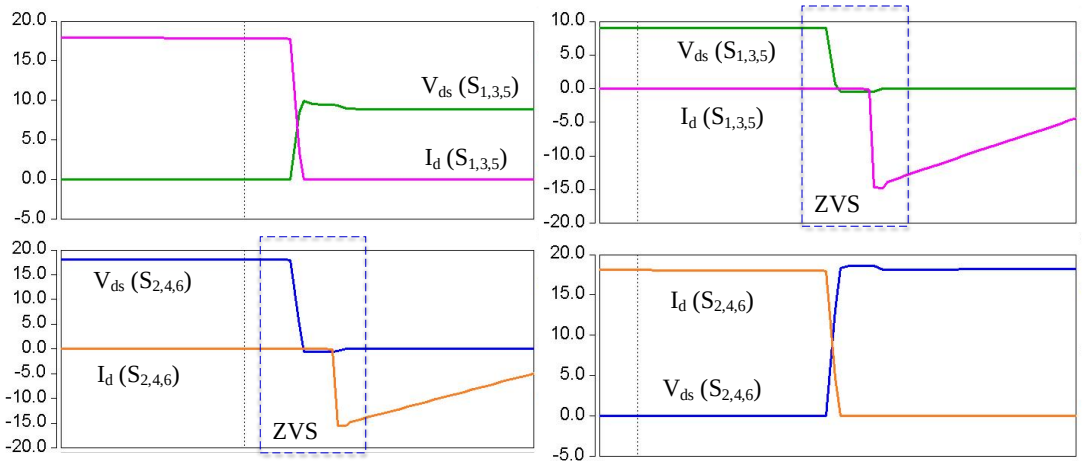

Figure 5.33. ZVS waveforms of the wing side switches

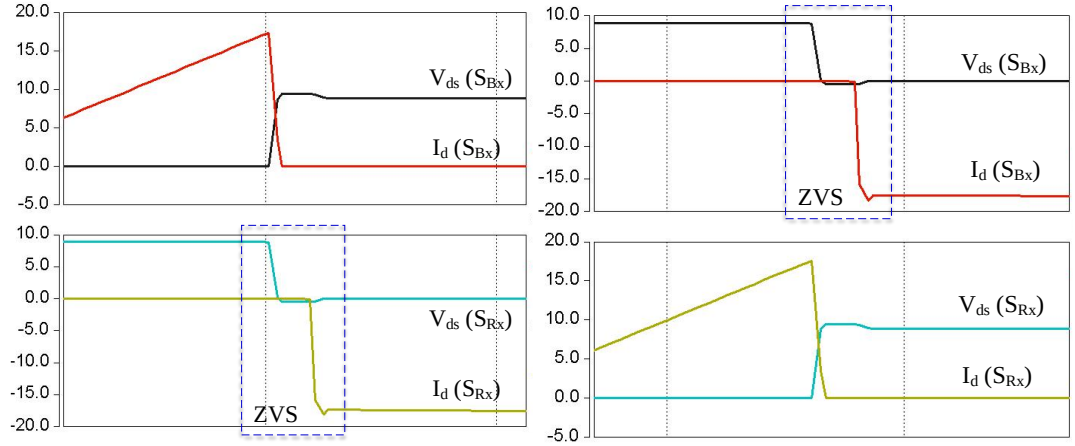

Figure 5.34. ZVS waveforms of the rectifier side switches

5.5. Experimental Results

A low power lab prototype with 6:1 voltage conversion ratio has been built to verify the operation of the presented converter. Detailed specification of the converter can be found in Table 5.5. The inductance of the inductor is 36nH, and capacitance used in the resonant tank is 120uF. And the operating frequency of the converter is set to be 350kHz, according to the design example. Table 5.6 illustrates the actual parts and theirs part numbers that are used in the lab prototype.

Table 5.5. Parameters Used in The Simulation

Items	Symbols	Values
Typical input voltage	V_{in}	54V
Typical output voltage	V_{out}	10V
Inductor inductance	L_r	36nH
Capacitor capacitance	C_r	120uF
Switching frequency	f_s	350kHz

Table 5.6. Parts Used In The Prototype

Items	Part#
Switching devices	EPC 2023
Gate Driver	LM5113
Resonant Inductor	SLC7649S-360
Resonant Capacitor	CGA9N3X7S2A106K230KB
Micro-controller	TMS320F28335
Level-shifter	ADUM6200CRWZ

Figure 5.35 shows the prototype that is used to verify the theoritical analysis. Eight modular boards are used to build the prototype, each board contains a half-bridge. Device RMS current and ZVS operation have been verified when the presented conveter has 54V input, 9V output and 100W output power. Figure 5.36 shows the inductor current waveforms of L_1, L_3 and L_5, all of them have the same RMS value, which is 3.85A. In Figure 5.37, the three inductor current waveforms are overlamped each other to show that the current flow through all the resonant branches are balanced. Furthermore, ZVS operation of the converter has been verified through the experiment. In Figure 5.38, the MOSFET's drain-source voltage decrease at first, which indicates the MOSFET's output capacitor has been discharged. Then the diode kicks-in when the MOSFET's output capacitor is fully discharged. After this point, the MOSFETS's gate-source voltage start rising and the switch turns on in a short time. As a result, the zero-voltage switching of the device has been achieved. In Figure 5.39, the voltage across capacitors C_5, C_3 and C_1 are

measured, which are 45V, 27V and 9V, respectively. The results match with the theoritical analysis and simulation results.

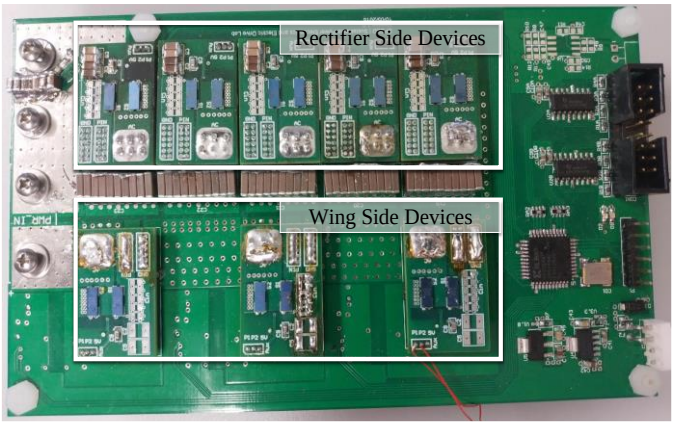

Figure 5.35. Lab prototype with 6:1 voltage conversion ratio

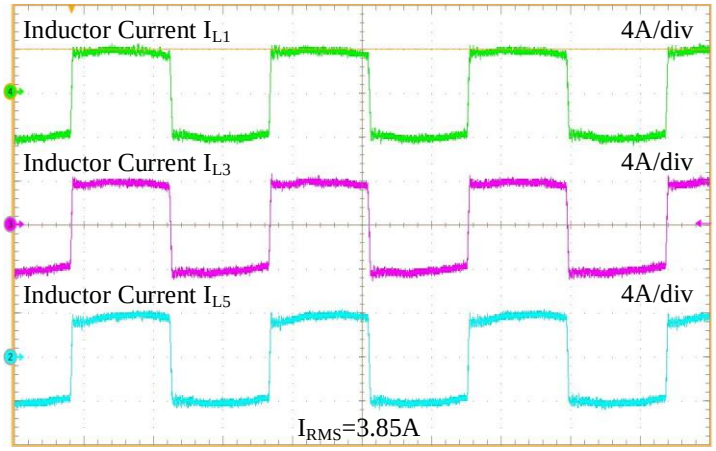

Figure 5.36. Inductor current waveforms when V_{in}=54V, V_{out}=9V, P_{out}= 100W

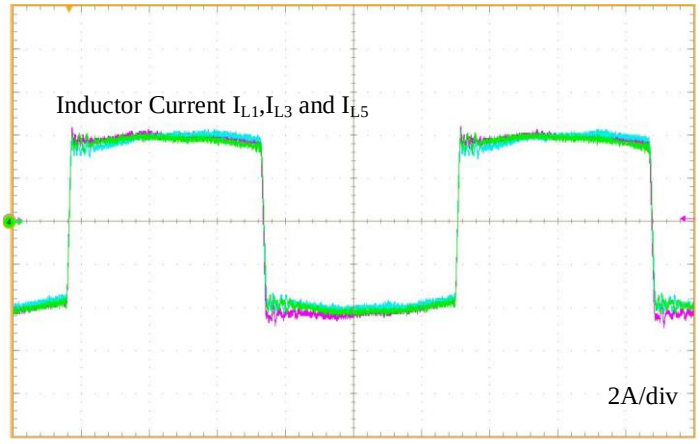

Figure 5.37. Inductor current waveforms when V_{in}=54V, V_{out}=9V, P_{out}= 100W

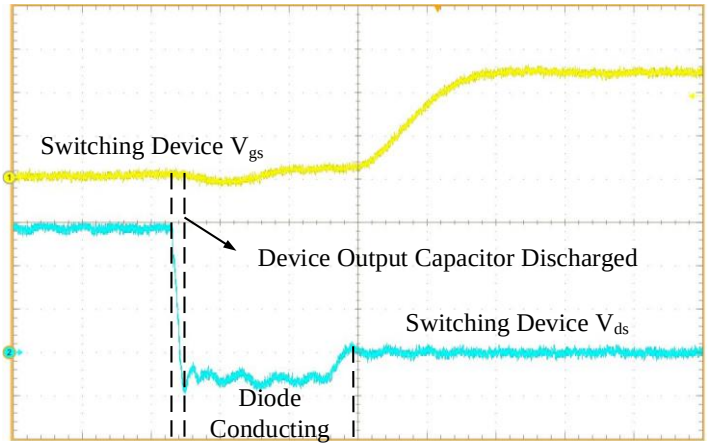

Figure 5.38. ZVS operation V_{in}=54V, V_{out}=9V, P_{out}= 100W

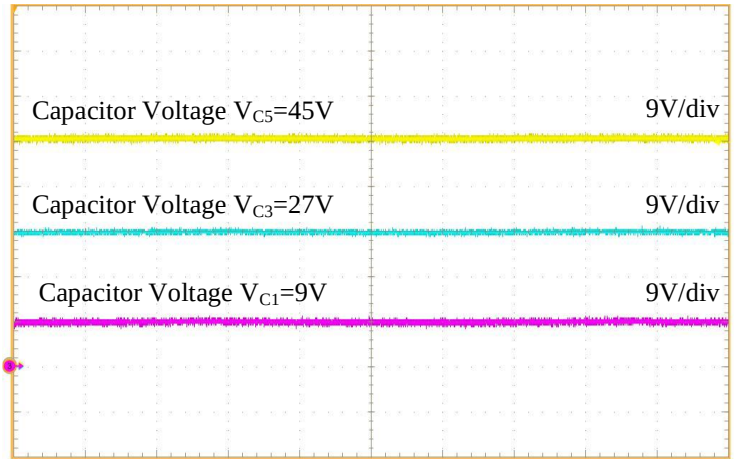

Figure 5.39. Capacitor voltage waveforms when V_{in}=54V, V_{out}=9V, P_{out}= 100W

The main purpoase of this prototype is to verify the zero-voltage switching capability of the converter and the theoritical analysis on the RMS value of the current that flow through switching devices. Power density and meansured efficiency are not provided in this work. Because the integration level of the prototype used for the experiment is not high enough. The power loss due to large PCB area and connectiors could significantly affect the converter's efficiency. Therefore, a denser design is also proposed to show that the presented converter can achieve very high density and high efficiency, as shown in Figure 5.40. The proposed converter can achieve 800W/in^3 density, which is slightly higher than the converter presented in [142]. Furthermore, the efficiency of the presented converter is estimated, it's peak effficiency can reach as high as 99.1%.

In order to prove the accuracy of the efficiency evaluation model, measured efficiency curve and estimated efficiency curve of the 6x switched-capacitor resonant converter are provided, as shown in Figure 5.41. The detailed efficiency prediction menthod is not within the scope of this work. Note that the PCB loss of the presented converter can be simulated thourgh finite element analysis (FEA) software.

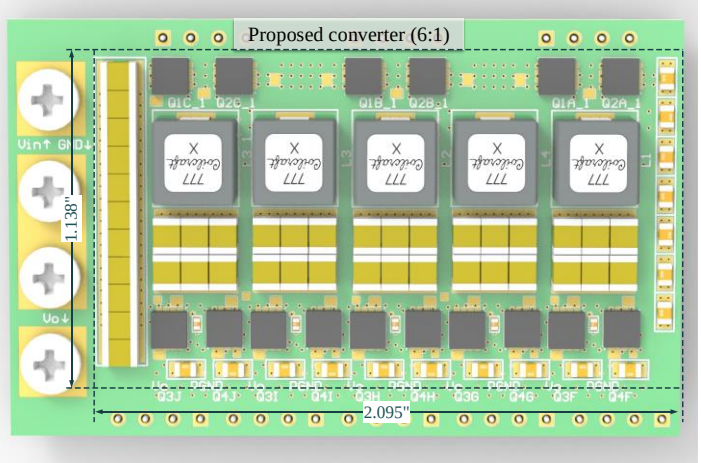

Figure 5.40. 3D view of the proposed converter with high density layout

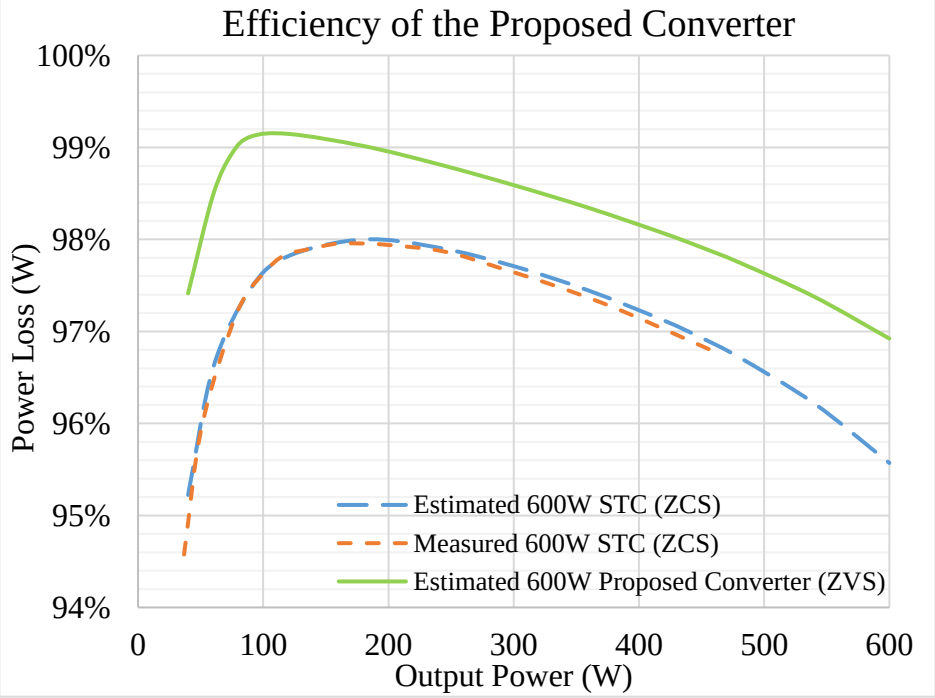

Figure 5.41. Estimated efficiency of the presented converter (f_s=350kHz)

Besides, a 48V to 12V prototype has been developed, which is also capable of deliver 600W power to the output. The prototype is shown in Figure 5.42. The efficiency of the presented 4:1 converter has been measured up to 450W (typical power). The measured efficiency curve of this prototype can be found in Figure 5.43. Its peak efficiency can achieve 99.5% when it is switching at 200kHz. And its efficiency is always above 98% before 450W.

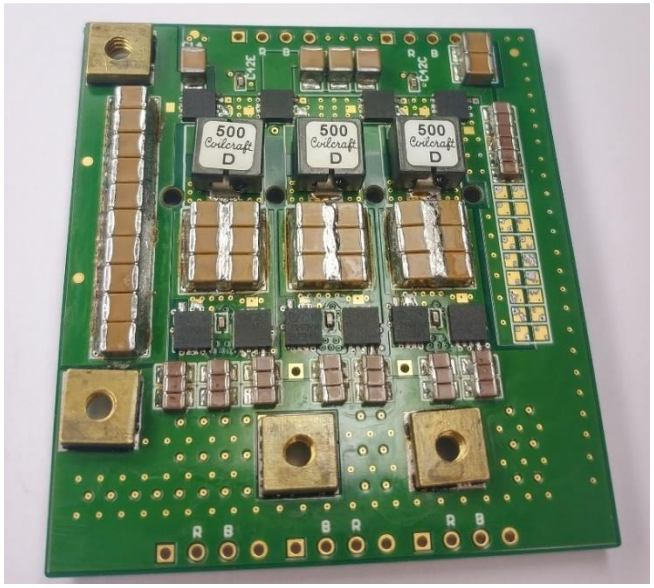

Figure 5.42. Designed high-density prototype (48V-12V)

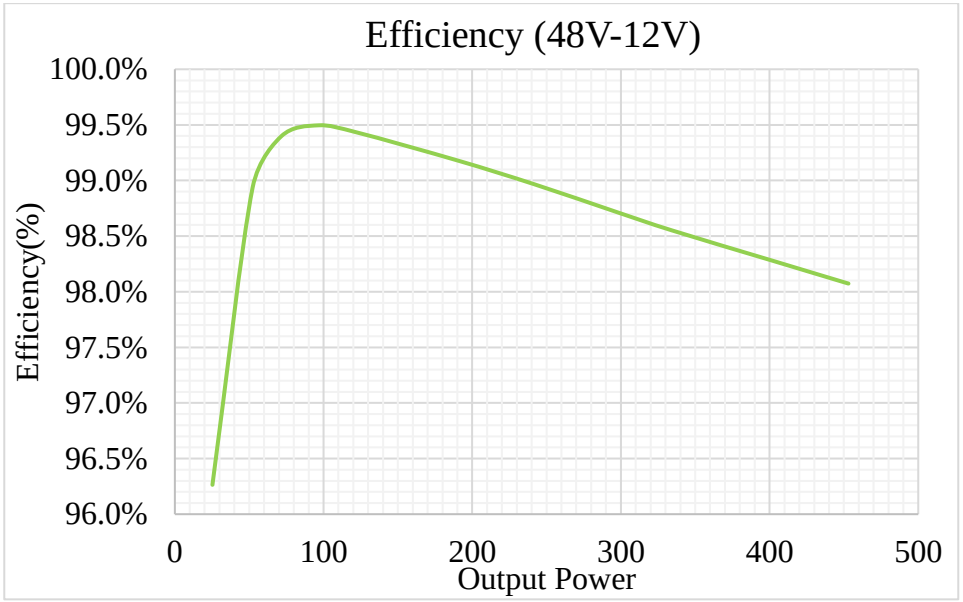

Figure 5.43. Efficiency of the designed density prototype (48V-12V)

5.6. Conclusion

A high-efficiency new SCRC has been proposed in this work. The basic operating principle as well as the ZVS operation of the presented circuit is demonstrated. Mathematical analysis of the components' RMS current is performed in this work. A design example shows the design constraints based on the given converter specifications. Within the design constraints, detailed design procedures that ensure high efficiency operation of the new SCRC is presented. In addition, the correct deadtime that should be used during the ZVS operation of the converter is analyzed in this work. Based on the design example, both light load and full load simulations are carried out to verify the theoretical calculated switch RMS current values and deadtime. A low power lab prototype with 6:1 voltage conversion ratio has been built to verify the operation of the presented converter. The ZVS operation is verified through the experimental results. The measured RMS values of device currents match with the theoretical calculation. A high-density prototype is also proposed in this work, the predicted peak efficiency is 99.1%. And its power density can achieve 800W/in^3. Experiment based on a design 4:1 prototype has been performed, the meansured peak efficiency can reach 99.5%. And it's power density is higher than 2kW/in^3.

6. ANALYTICAL EVALUATION ON TWO SOFT-SWITCHING MECHANISMS OF THE SWITCHED-TANK CONVERTER

6.1. Introduction

By the end of 2017, there are more than eight million operating datacenters all over the world. As the development of internet of things (IoT), self-driving cars and many other internet-based services, the total power consumption of the data centers is increasing rapidly. This trend forces the business leaders to start looking for solutions that can help their data centers operate more efficiently and keep their competitive advantages. As a result, the efficiency of data center power delivery architectures starts drawing more and more attention. One very straight forward way is to adopt intermediate bus architecture (IBA) in the data center[50], [52], [145]. This architecture brings a lot of flexibilities to the data center power delivery path. By carefully selecting the intermediate bus voltage and designing corresponding converters, the energy can be delivered from 48V bus to CPU effectively. Note that the typical voltage value on the 48V bus could be either 48V or 54V [128].

The key to ensure the success of the intermediate bus architecture is the intermediate bus converter (IBC), which converters from the intermediate bus voltage (eg.54V, 48V) to a lower voltage, which typically ranges from 5V to 14 V [50]. In the past years, a lot of research have been carried out to provide innovative solutions to push the efficiency and density of the intermediate bus converters to a new level that existing commercial products have never reached before. In summary, there are two types of intermediate bus converters, which are the isolated converters and non-isolated converters.

In terms of the isolated ones, this type of converter relies on magnetic components such as transformer to achieve voltage conversion function. In [146], leakage inductance of the

transformer has been utilized to help achieving the ZVZCS feature of the proposed converter. In [147], the circuit uses a full-bridge on primary side and half-bridge on the secondary side. ZVS operation has been achieved on both sides' devices. Its peak efficiency is around 94.4% when it operates at 250kHz switching frequency. In [148], the proposed converter uses composite resonant multilevel converter concept and partial power voltage regulation concept to make the power loss of the converter minimum, which is similar to but beyond the famous sigma converter concept [149].

As the development of IBC, the bulky magnetic components in the circuits are becoming the bottleneck of improving converter efficiency and density. In [53], [150], although the power loss and volume of the transformer is greatly optimized, it still take around 30% of the total converter power loss. Besides, isolation is not a rigid requirement for the IBC [52]. This gives researchers an opportunity to develop transformerless IBCs. Therefore, the non-isolated converter designs start to emerge, which is the second type. The key design goal of the non-isolated IBCs is to use very minimum magnetic components to help the circuit achieving voltage conversion function and soft-switching at the same time. The hybrid switched-capacitor circuits are very representative candidates that can help us achieve this goal [151][76]. In [129], a 4-to-1 cascaded voltage divider are proposed for datacenter application. It achieves 98.9% peak efficiency when it operates at 100kHz switching frequency. In [142], a switched-tank converter with 98.55% peak efficiency and 250kHz switch frequency is proposed. The switching devices in both converters achieve ZCS operation. Except the datacenter application, the hybrid switched-capacitor circuits are also widely used in many other applications. Such as integrated circuits [60], [86], [152], photovoltaic application [141], [153], [154], inverters [84], [113], [155]–[157], hybrid electric vehicles [158] and voltage balancing circuits in multilevel converters[90], [159].

Switched-tank converters are celebrated for their high power density and high efficiency features when they are used as intermediate bus converter [143]. This work shows a switched-tank circuit that is capable of both zero-current switching and zero-voltage switching operation. The main focus of this work is to analyze and compare the two operation modes of the presented circuit. By analyzing the equivalent circuit of each operation mode, mathematical models used to estimate the current waveforms of all the components under both zero-current switching and zero-voltage switching operation modes are developed. Design procedures of two example converters, one for ZCS operation and one for ZVS operation, are performed to show how to use the theoretical to guide the practical converter design. Furthermore, the power loss and efficiency of the designed converters are estimated and compared. The analysis shows that the converter designed for ZVS operation can achieve higher efficiency and density.

This work is organized as follows: The section II introduces the presented circuit and analyzes the principle of its ZCS and ZVS operation. In addition, the mathematical models used to predict the components' current waveforms are developed in this section. Section III demonstrates the design procedures of two example converters, one for ZCS operation and one for ZVS operation. Section IV compares the power loss and efficiency of two example converters. At last, section V shows the simulation results and shows a low power prototype that has been built to verify the theoretical analysis.

6.2. Circuit Configuration and Comparative Study of Two Soft-Switching Mechanisms

In this section, the standard module for switched-tank converter and general circuit architecture will be demonstrated at first. Then a 6-to-1 switched-tank converter that is derived from the generalized circuit configuration is presented, which is the analyzed circuit in this work.

At last, the ZCS operation and ZVS operation of the presented circuit are analyzed, mathematical models have been developed based on the theoretical analysis.

6.2.1. Circuit Configuration of the Presented Converter

Figure 6.1 shows the circuit configuration of the basic module that is used to compose the STC. The module contains two half-bridges and one tank. For the most common case, there are two types of tanks. It could be an inductor-capacitor (LC) resonant tank or just a single capacitor. It's worth mentioning that the circuit configuration of the tank is not limited to the aforementioned ones. The Figure 6.2 and Figure 6.3 shows two STC topologies that are composed by the basic module shown in Figure 6.1. In Figure 6.2, both resonant tank (LC) and non-resonant tank (C) are used in this topology. The main advantage of this topology is that the non-resonant tank (eg.C_2) in the circuit can help clamping the voltage of the floating switching devices. Therefore, this topology does not need additional clamping circuit, which is beneficial for achieving high power density of the converter. In Figure 6.3, the topology only contains tank#2, which is composed by one inductor and one capacitor. Comparing with the topology shown in Figure 6.2, this topology needs more inductors and additional voltage clamping circuit. At a glance, the latter topology is not as good as the former topology. However, notice that the latter topology can operates under either ZVS mode or ZCS mode. While the former topology can only operate at ZCS mode. And the components' current waveforms are quite different when the converter operates at different mode. Hence, the components' current stress and semiconductor loss will be different, especially the conduction loss.

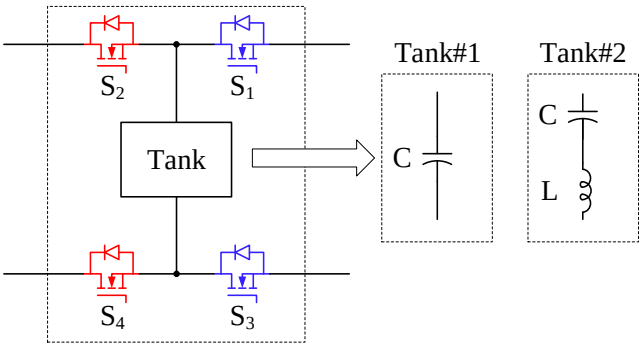

Figure 6.1. Basic module for the switched-tank converters

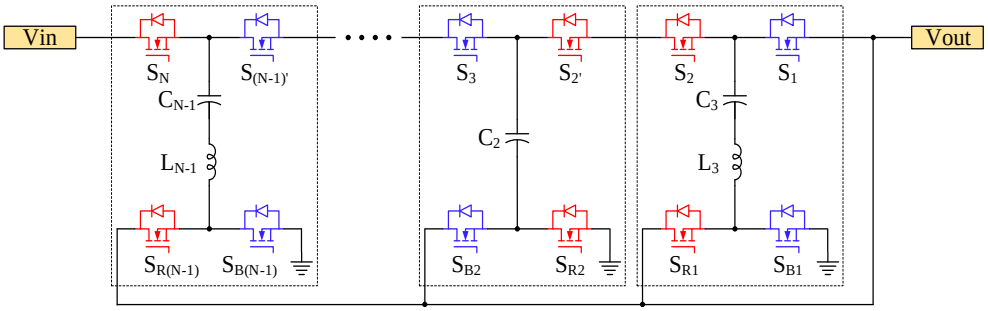

Figure 6.2. The generalized STC topology contains both type#1 and type#2 tanks

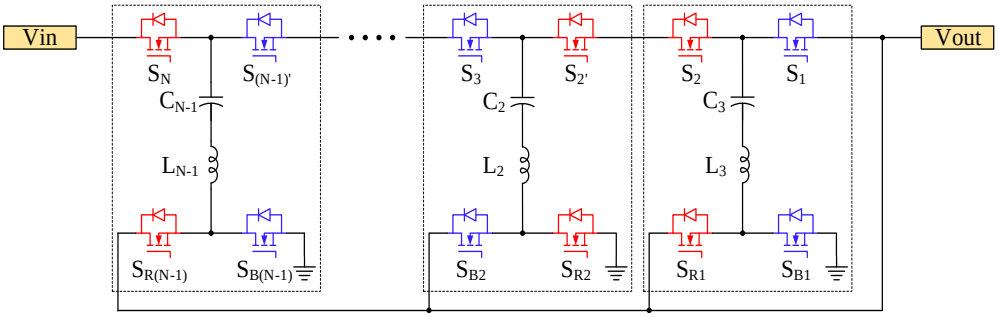

Figure 6.3. The generalized STC topology contains only type#2 tank

In Figure 6.2 and Figure 6.3, the voltage stress for all the switching devices is the same, which is V_{out}. During the operation of the converter, the switching devices S_N and $S_{N'}$ (N=1,2,3…) have the same switching behavior. In other words, they turn on and turn off at the same time. As a result, every two low voltage rating switches S_N and $S_{N'}$ (N=1,2,3…) can be combined to one device that has higher voltage rating. Here, we name the combined devices S_N. And the voltage stress of these devices is $2V_{out}$. Figure 6.4 shows the switched-tank converter with 6-to-1 voltage

conversion ratio, which is the circuit that will be analyzed in this work. Table 6.1 shows the voltage stress of all the key components in the circuit. The DC bias voltage of the capacitors in the presented converter ranges from $5V_{out}$ to V_{out}. Note that the DC bias voltage will be recognized as one of the capacitor design consideration in the future sections.

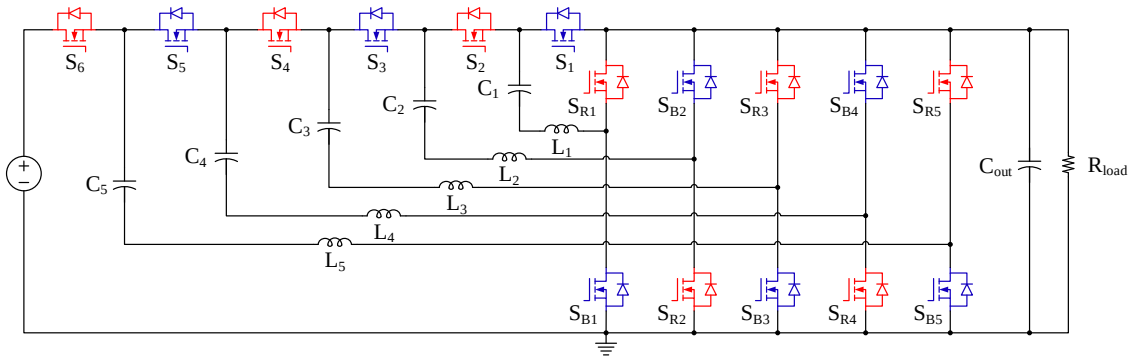

Figure 6.4. The presented switched-tank converter with 6-to-1 voltage conversion ratio (S_N and $S_{N'}$ combined to one switching device)

Table 6.1. Voltage Stress of the Key Components

Description	Items	Values
Resonant Capacitors (DC Bias)	C_5	$5V_{out}$
	C_4	$4V_{out}$
	C_3	$3V_{out}$
	C_2	$2V_{out}$
	C_1	$1V_{out}$
Switching Devices	S_1, S_6, S_{Rx}, S_{Bx}	$1V_{out}$
	$S_2 \sim S_5$	$2V_{out}$

For the following analysis, we assume all the resonant tanks are identical. Thus, all the resonant tanks' current waveforms are the same. Also, all the switching devices are identical.

6.2.2. ZCS Operation

The presented circuit has zero-current switching capability. All the switching devices in this circuit can achieve both zero-current turn-on and zero-current turn-off. In order to achieve

ZCS operation, the switching frequency of all the MOSFETs should be set to the same as the resonant frequency of the resonant tank, as shown in Eq.6.1.

$$f_s = \frac{1}{T_s} = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad \text{(Eq. 6.1)}$$

In Eq.6.1, L_r is the inductance value of the resonant inductor and Cr represents the resonant capacitance in the resonant circuit. The parameter Ts represents the period of one switching cycle. Figure 6.5 and Figure 6.6 show the equivalent circuits of the ZCS operation mode. As shown in Figure 6.5, all the red switches are conducting at the same time during the first state. Similarly, all the blue devices turn-on and turn-off at the same time, as shown in Figure 6.6. In Figure 6.7, the current waveforms of switching devices and inductors are provided. When the devices S2, S4, S6 and SRx turn on, their drain-source current start increasing from zero. And the current waveforms follow sinusoidal shape because of the LC resonant tank. After Ts/2, the device current resonant back to zero. Then all the red switches turn-off. Thus zero-current turn-on and zero-current turn-off on devices S_2, S_4, S_6 and S_{Rx} are achieved. Similarly, the devices S_1, S_3, S_5 and S_{Bx} achieve ZCS turn-on at $T_s/2$ and ZCS turn off at T_s.

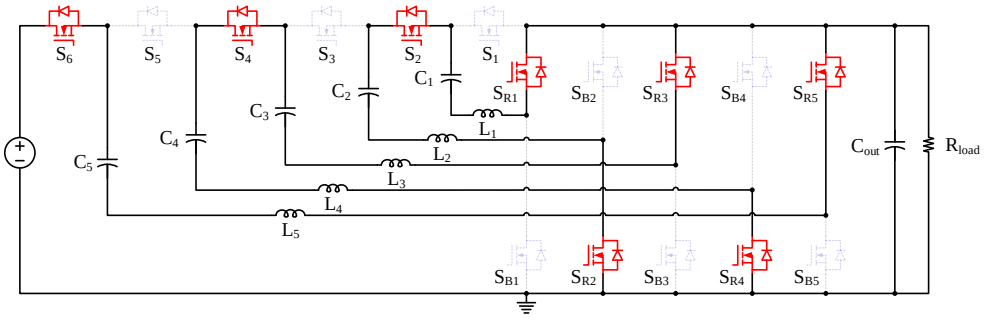

Figure 6.5. State 1

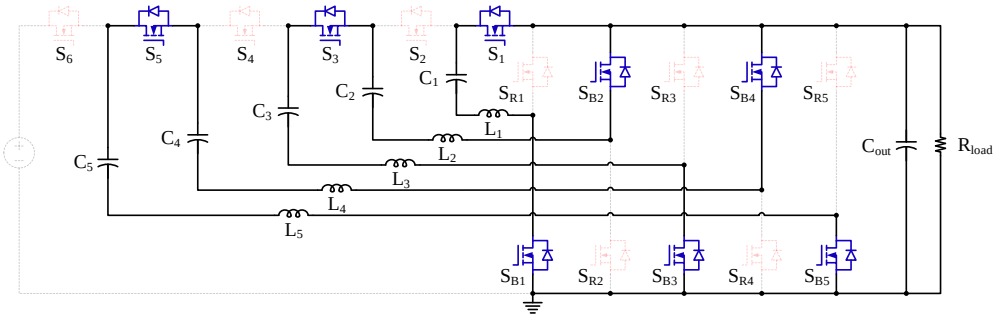

Figure 6.6. State 2

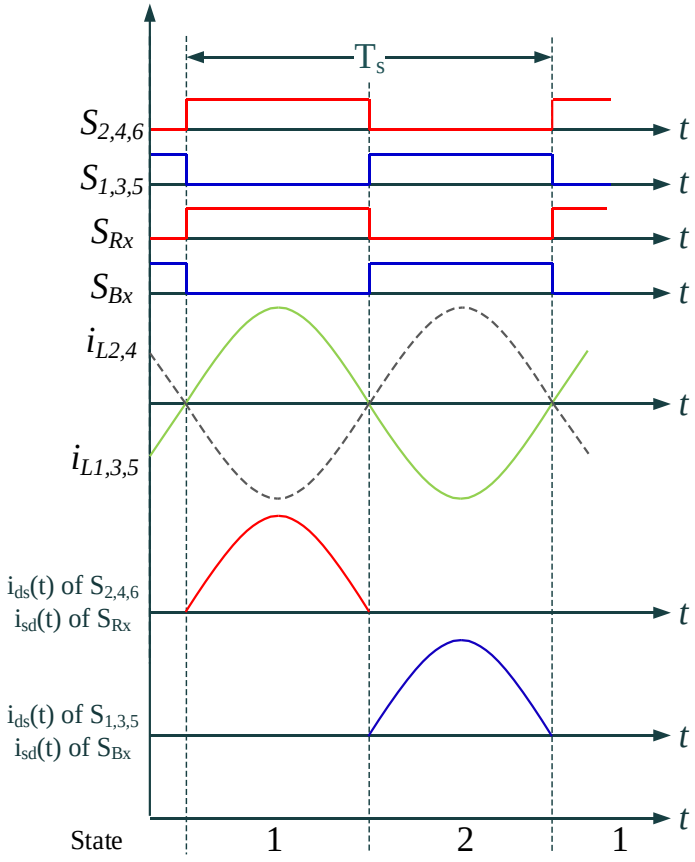

Figure 6.7. Switch and inductor waveforms of the ZCS operation mode

According to the equivalent circuit shown in Figure 6.5 and Figure 6.6, the average current flow through each MOSFET is 1/6 of the converter output current. Therefore, the average current flow through each device I_{sw_avg} can be calculated, as shown in Eq.6.2.

$$I_{sw\_avg} = \frac{I_{out}}{6} = \frac{P_{out}}{6V_{out}} \quad \text{(Eq. 6.2)}$$

Where the P_{out} represents the output power of the converter, V_{out} represents the output voltage. According to Figure 6.7, the current waveform of the switching device is sinusoidal shape, with the frequency calculated in Eq.6.1. We assume the peak value of the switch current is I_{sw_pk}. The switching devices' current waveform can be presented by Eq.6.3.

$$i_{sw\_zcs}(t) = I_{sw\_pk} sin\left(\frac{1}{\sqrt{L_r C_r}} t\right) \quad \left(0 \le t \le \frac{T_s}{2}\right) \quad \text{(Eq. 6.3)}$$

On the other hand, the average value of the switch current can also be calculated based on Eq.6.3, which shown in Eq.6.4. As a result, the peak value of the switch current waveform I_{sw_pk} can be derived as a function of converter output current I_{out} by plugging Eq.6.1, Eq.6.2 and Eq.6.3 into Eq.6.4, which is I_{out}*π/6.

$$I_{sw\_avg} = \frac{1}{T_s} \int_0^{0.5T_s} i_{sw\_zcs}(t)\, dt \quad \text{(Eq. 6.4)}$$

$$i_{sw\_zcs}(t) = \begin{cases} \frac{I_{out}\pi}{6} sin\left(\frac{1}{\sqrt{L_r C_r}} t\right), & 0 \le t \le \pi\sqrt{L_r C_r} \\ 0, & \pi\sqrt{L_r C_r} \le t \le 2\pi\sqrt{L_r C_r} \end{cases} \quad \text{(Eq. 6.5)}$$

Since the Isw_pk is Iout dependent in this case. The current flow through switching devices during one switching cycle can be obtained, as shown in Eq.6.5. As a result, the root mean square (RMS) current flow through switching devices can be calculated, as shown in Eq.6.6. Similarly, the RMS value of current flowing through the resonant tank can also be calculated, as shown in Eq.6.7.

$$I_{sw\_zcs\_rms} = \sqrt{\frac{I_{out}^2 \pi}{72\sqrt{L_r C_r}} \int_0^{\pi\sqrt{L_r C_r}} sin^2\left(\frac{1}{\sqrt{L_r C_r}} t\right) dt} \quad \text{(Eq. 6.6)}$$

$$I_{L\_zcs\_rms} = \sqrt{\frac{I_{out}^2 \pi}{36\sqrt{L_r C_r}} \int_0^{\pi\sqrt{L_r C_r}} sin^2\left(\frac{1}{\sqrt{L_r C_r}} t\right) dt} \qquad \text{(Eq. 6.7)}$$

6.2.3. ZVS Operation

The presented circuit also has zero-voltage switching capability. All the switches in the circuit can achieve ZVS turn-on in this mode. In order to achieve the ZVS operation, the switching frequency of all the MOSFETs should be higher than the resonant frequency of the resonant tank, as shown in Eq.6.8.

$$f_s > \frac{1}{2\pi\sqrt{L_r C_r}} \qquad \text{(Eq. 6.8)}$$

For the ZVS operation, the converter control algorism is different with the ZCS operation. A shift time is introduced between the control signals of the 6 floating switches and the 10 half-bridge rectifier devices. This control method is call phase-shift control. In contrast to the ZCS operation mode, the phase-shift control method generates two more operation states for the converter, which are called phase-shift states. Figure 6.8 to Figure 6.11 shows the four switching states when the converter is operating at ZVS mode. The two phase-shift states in the ZVS operation mode can be found in Figure 6.8 and Figure 6.10. Note that the following analysis assumes that the voltage ripple across all the capacitors in this circuit is small enough (e.g. Less than 5%).

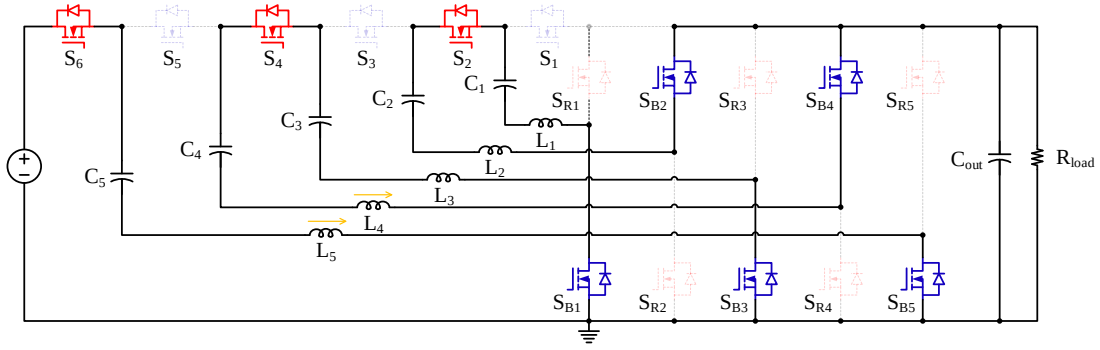

Figure 6.8. State 1

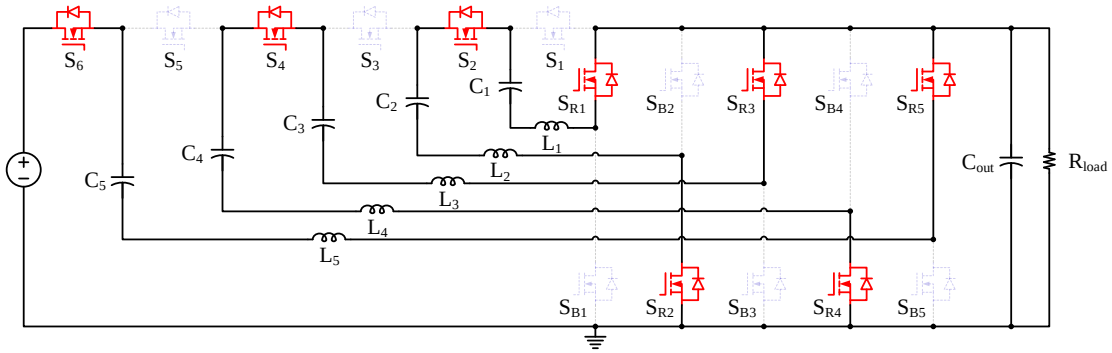

Figure 6.9. State 2

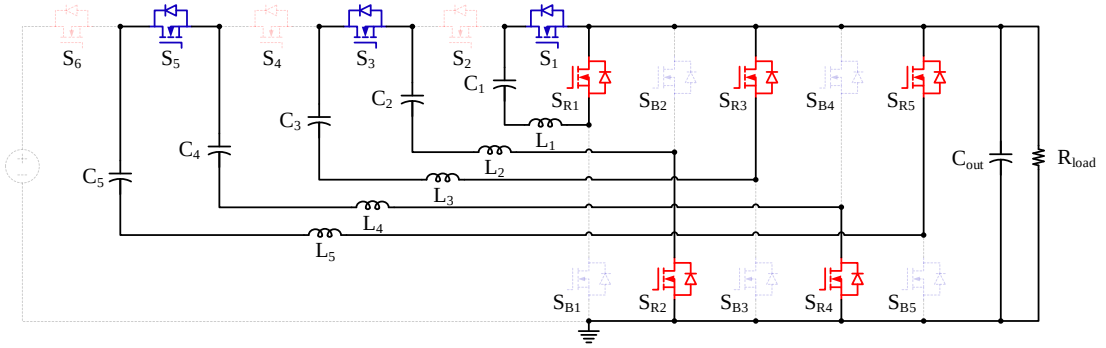

Figure 6.10. State 3

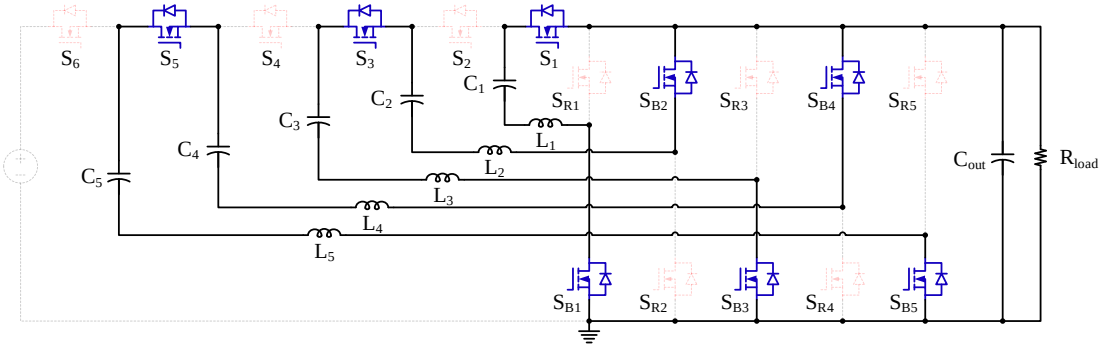

Figure 6.11. State 4

In Figure 6.12, state 1, the output capacitors of S_2, S_4, S_6 will be discharged by the negative drain-source current before they turn on. Thus, the ZVS for S_2, S_4, S_6 is achieved. During the state 1, the switches S_2, S_4, S_6 and S_{Rx} are conducting, the converter is working at phase-shift state. According to Table 6.1, we can calculate the voltage across the inductors, which is V_{out}. Therefore, the changing rate of the MOSFET current is V_{out}/L_r. During this state, the drain-source current of

S_2, S_4, S_6 alternates from negative to positive. At the end of state 1, the switches S_{Bx} turn off, the resonant currents commutate from S_{Bx} to S_{Rx} and make the drain-source current of switches negative. At the beginning of the state 2, the switches S_{Rx} turn on with their output capacitors been fully discharged. In other words, the ZVS for S_{Rx} is achieved. During the state 2, the voltage across the inductors is very close to zero. The inductor current waveforms can be considered as a constant value during this state. For the state 3 and state 4, the behavior of the presented converter is similar to state 1 and state 2. So that the ZVS for the S_1, S_3, S_5 and S_{Bx} is also achieved. More detailed analysis on achieving ZVS operation can be found in [103].

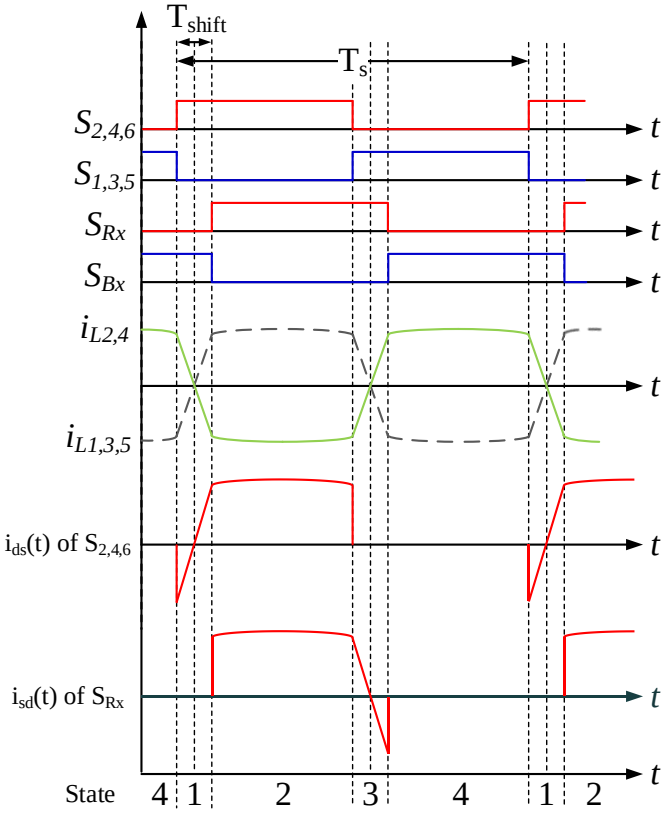

Figure 6.12. Switch and inductor waveforms of the ZVS operation mode

According to Figure 6.12, because the negative part and the positive part of the inductor current waveform are symmetric, the peak current value of the switching devices S_2, S_4 and S_6 can

be calculated, as shown in Eq.6.9. As a result, the current waveform of S_2, S_4 and S_6 can be represented by Eq.6.10.

$$I_{sw\_zvs\_pk} = \frac{V_{out}}{L_r} * \frac{T_{shift}}{2} \quad \text{(Eq. 6.9)}$$

$$i_{sw\_zvs}(t) = \begin{cases} -\left(I_{sw\_zvs\_pk}\right) + \dfrac{t}{\dfrac{L_r}{V_{out}}}, & 0 \le t \le T_{shift} \\ I_{sw\_zvs\_pk}, & T_{shift} \le t \le \dfrac{T_s}{2} \\ 0, & \dfrac{T_s}{2} \le t \le T_s \end{cases} \quad \text{(Eq. 6.10)}$$

In Eq.6.10, the T_{shift} represents the phase-shift time. In order to find the relationship between the MOSFET's current waveform and the converter output current, the Tshift needs to be derived as a function of Iout. With the analyzed device current waveforms shown in Figure 6.12, the I_{sw_avg} can be calculated by using Eq.6.11. According to Figure 6.11, the average current flowing through each MOSFET I_{sw_avg} is 1/6 of the converter average output current I_{out}, which is the same as the ZCS operation mode, as shown in Eq.6.2. By plugging Eq.6.2 into Eq.6.11, the T_{shift} can be described as a function of V_{out}, L_r, T_s and I_{out}. The Eq.6.12 shows the derived equation.

$$\frac{V_{out}T_{shift}}{2T_sL_r} * \left(\frac{T_s}{2} - T_{shift}\right) = I_{sw\_avg} \quad \text{(Eq. 6.11)}$$

$$T_{shift} = \frac{T_s}{4} - \sqrt{\frac{T_s^2}{16} - T_s\frac{I_{out}L_r}{3 * V_{out}}} \quad \text{(Eq. 6.12)}$$

With the switch current waveform derived above, one can calculate the RMS value of the current flowing through the switching devices, as shown in Eq.6.13. Note that the RMS current of all the switching devices in the circuit are the same.

$$I_{sw\_zvs\_rms} = \sqrt{\frac{1}{T_s}\left[\int_0^{T_{shift}} \left(\frac{t}{\frac{L_r}{V_{out}}} - \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right)^2 dt + \int_{T_{shift}}^{0.5T_s} \left(\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right)^2 dt\right]} \quad \text{(Eq. 6.13)}$$

6.3. Design Considerations of the Presented Converter

Because the two operation modes of the presented converter have different control strategy, the design consideration for the converter's ZCS operation mode and ZVS operation mode would be quite different. Based on the circuit analysis in the last section, this section illustrates the design consideration by providing two converter design examples.

The specifications of the converters that will be designed can be found in Table 6.2. The input voltage and output voltage of the converter are 54V and 9V, respectively. The maximum converter output current is 66.6A and the typical output current is 50A. In order to avoid the confusion, we call the converter designed for ZCS operation converter #1. And the converter designed for ZVS operation is called converter #2, as shown in Table 6.3. In order to make the designs comparable, the switching frequencies of the two converters are set to be the same value.

Table 6.2. Basic Converter Specification Used in the Design Example

Description	Items	Values
Typical Input Voltage	V_{in}	54 V
Typical Output Voltage	V_{out}	9 V
Typical Output Power	P_{out_typ}	450 W
Typical Output Current	I_{out_typ}	50 A
Maximum Output Power	P_{out_max}	600 W
Maximum Output Current	I_{out_max}	66.6A
Switching Frequency	f_s	~350 kHz

Table 6.3. Two Converters Used in the Design Example

Converters	Operation Mode
Converter #1	ZCS Operation
Converter #2	ZVS Operation

6.3.1. Converter Design for ZCS Operation

First of all, the resonant capacitor design is one of the most important aspects to ensure the reliable converter operation. In the ZCS operation mode, the switching frequency of the presented converter is determined by the inductance and capacitance values of the resonant tanks. And the resonant frequency of all the tanks should be identical or as close as possible. Therefore, class I ceramic capacitors are required for this design. According to the standard EIA RS-198, the class I ceramic capacitors are highly stable and their ESR is very low. When a DC bias voltage is observed on this type of capacitors, their capacitance change is very minimum. For example, for capacitor C1812C474K5JAC from Kemet, the capacitance change is within 0.5% when there is a DC bias voltage across it, according to the K-SIM simulation tool. In order to ensure the capacitor bank can flow through enough current, we assume each of the capacitor have 5A current capability. Thus, a minimum number of 6 capacitors should be selected.

Second, the inductor design is also very important. Because the volume of magnetic component will be increasing rapidly as the increasing of inductance when the saturation current of the inductor is unchanged. According to the design shown in [142], customize designed planar inductors or off-the-shelf surface mount inductors whose inductance values are within 100nH could he very ideal candidates for this design.

By considering the capacitor current bank’s current capability and the approximate inductance value, the resonant capacitance of the resonant tank is designed to be 2.82uF. And the inductance is selected to be 70nH. One more thing that needs to be verified is the voltage ripple of

the resonant capacitors. We need to make sure the maximum voltage across the capacitor bank will not exceeds its voltage rating. According to the resonant current waveform shown in Figure 6.7, the charge that will be stored in the resonant capacitor can be calculated by using Eq.6.14. As a result, the resonant capacitor voltage ripple is derived, as shown in Eq.6.15. In this design, the maximum voltage is around 50V, which meets the requirement.

$$\Delta Q_{cap\_zcs} = \int_0^{\pi\sqrt{L_r C_r}} \frac{I_{out}\pi}{6} sin\left(\frac{1}{\sqrt{L_r C_r}} t\right) dt = \frac{I_{out}\pi\sqrt{L_r C_r}}{3} \quad \text{(Eq. 6.14)}$$

$$\Delta V_{cap\_zcs} = \frac{\Delta Q_{cap\_zcs}}{C_r} = \frac{I_{out}\pi}{3}\sqrt{\frac{L_r}{C_r}} \quad \text{(Eq. 6.15)}$$

In terms of the MOSFET selection, the proper switch that can be used in the presented circuit is selected by estimating and comparing the semiconductor loss of different MOSFETs. The detailed procedure and methodology can be found in [142].

6.3.2. Converter Design for ZVS Operation

Different with the ZCS operation, the ZVS operation mode does not have a very strong relationship between the switching frequency and the resonant frequency of the LC tank. Therefore, the tolerance requirement on consistence of the resonant frequency of the tanks is lower. To ensure the inductor current waveform very close to trapezoidal shape, the voltage ripple of the resonant capacitor should be as small as possible. This means there is a high requirement on the capacitance of the resonant tank, which is different with the capacitor design consideration for ZCS operation. According to the standard EIA RS-198, class II ceramic capacitors can provide very high volumetric efficiency. This means the capacitance density is much higher than the class I ceramic capacitor, even after considering the capacitance drop led by DC bias voltage across the capacitor. Note that the ESR of the class II capacitor is usually higher than the class I capacitors, but not necessarily. So, their current capability is usually slightly lower.

The inductor value is very critical for this design. It is closely related to the slope of the inductor current waveform during the phase-shift state. As shown in Figure 6.13, the inductor current waveforms for ZCS operation and ZVS operation are placed together for comparison purpose. When the inductor average current values of converter#1 and converter#2 are the same, the converter#2 could have lower RMS current flowing through the resonant tank. This indicates that it is possible to make the RMS current flowing through of the switching devices in converter#2 lower than that of converter#1. In order to achieve this goal, further analysis will be performed next.

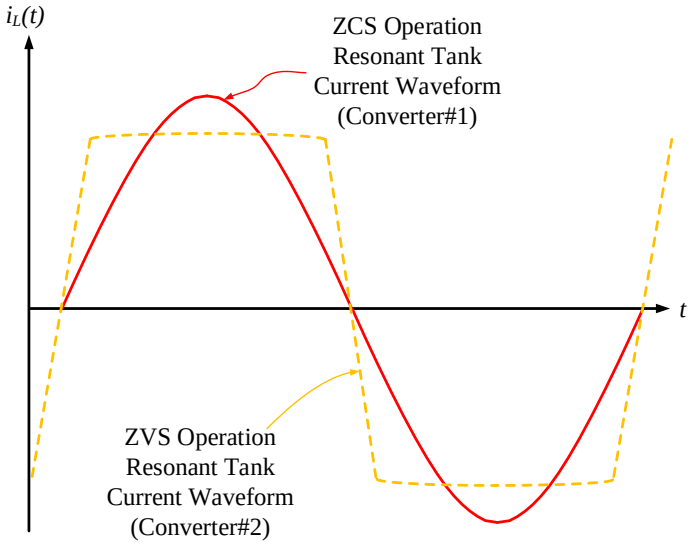

Figure 6.13. ZCS operation and ZVS operation inductor current waveforms

The inductor waveform in half of a switching period is shown in Figure 6.14, which shows effect of the phase-shift time to the inductor RMS current. When the average value of the inductor current during half a period is a fixed value, which means the area of shaded parts are the same, increasing the phase-shift time will lead to higher RMS value. On the contrary, the RMS value of the waveform is the lowest when phase-shift time is infinitely close to zero, we call this case extreme case.

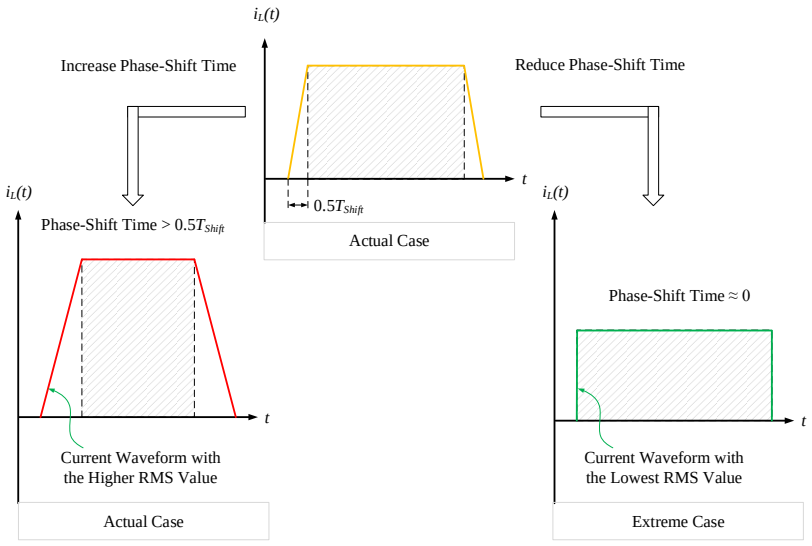

Figure 6.14. Effect of the Phase-shift time to the resonant waveform (half-cycle)

By calculating the RMS value of the square current waveform, we can obtain the lowest limit of the RMS current flowing through the inductor and switching device in converter#2. Assume the converter is operating under the extreme situation, the current flowing through the switches can be represented by Eq.6.16. At a result, the switching device RMS current can be calculated, as shown in Eq.6.17. Figure 6.15 shows that the RMS value of the square waveforms is always lower than the RMS current of the switches in the converter#1. If we want the converter#2 has lower switch RMS current than that of converter#1, the desired switch RMS current of the converter#2 should locate in the shaded area. As the increasing of the converter output current, the converte#2 will reveal more and more advantage in terms of semiconductor conduction loss.

$$i_{sw\_square}(t) = \begin{cases} \frac{I_{out}}{3}, & 0 \le t \le \frac{T_s}{2} \\ 0, & \frac{T_s}{2} \le t \le T_s \end{cases} \quad \text{(Eq. 6.16)}$$

$$I_{sw\_square\_rms} = \frac{\sqrt{2} I_{out}}{6} \quad \text{(Eq. 6.17)}$$

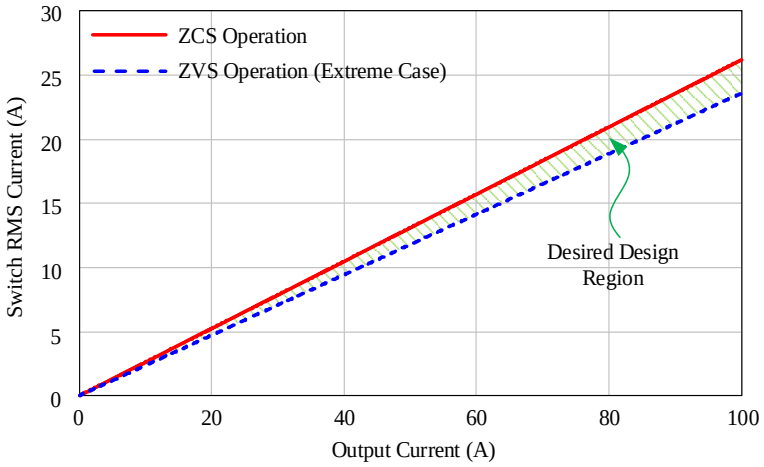

Figure 6.15. Desired design region for the converter#2

In Figure 6.16, the normalized switching device RMS current values of both converter#1 and converter#2 are calculated. The base value used for the normalization is RMS value of the square waveform. Four inductor values, 18nH, 36nH, 50nH and 70nH, are used for the calculation. The 36nH, 50nH and 70nH inductors can be found off the shelf. With the change of inductance value, the switching device RMS current is a constant value. On the contrary, the switching device RMS current is sensitive to the inductance values. Because the typical converter output current is 50A, we select the 36nH inductor in this design. Thus, the converter#1 and converter#2 have similar MOSFET conduction loss when they are operating at full load condition. It is worth mentioning that although the inductor with lower inductance enables lower switching device RMS current, a trade off between the semiconductor conduction loss and the implementability of the converter design must be made. First, low inductance will bring challenges to the controller under light load condition because very fine resolution of the phase-shift time is required. Second, the zero-voltage switching under light load will become hard to achieve since the energy used to discharge the output capacitors of the MOSFETs during the deadtime comes from the inductors.

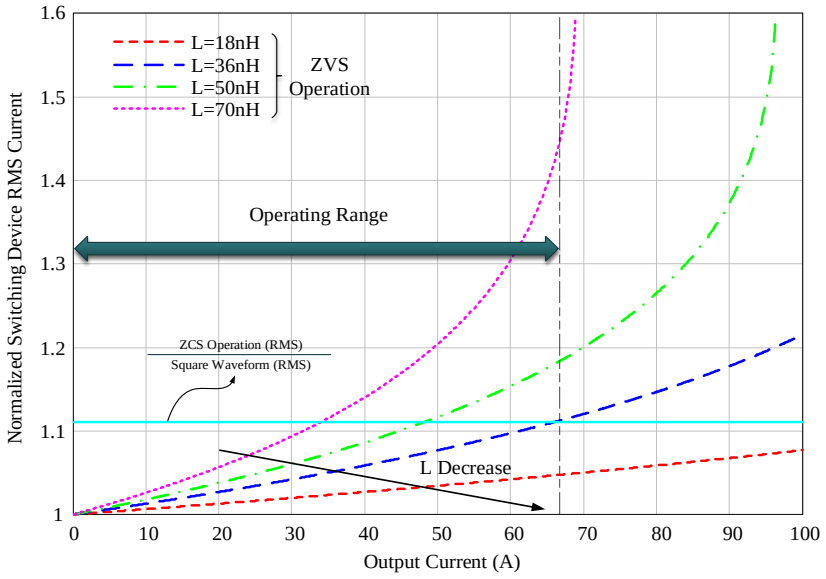

Figure 6.16. Relationship between normalized device RMS current value and resonant inductance (f_s=350kHz)

So far, the inductance of the resonant tank is design. Next step is to design the capacitance of resonant capacitor banks. Because the voltage ripple on the capacitor should be small enough to make the inductor current trapezoidal, 5% voltage ripple are assumed in this design. According to Eq.6.10, the charge that will be stored in the resonant capacitor can be calculated by using Eq.6.18. As a result, the required capacitance used in the resonant tank should be 70uF according to Eq.6.19.

$$\Delta Q_{cap\_zvs} = \int_0^{0.5T_s} i_{sw\_zvs}(t)_{dt} = \frac{V_{out}T_{shift}(T_s - T_{shift})}{4L_r} \quad \text{(Eq. 6.18)}$$

$$\Delta V_{cap\_zvs} = \frac{\Delta Q_{cap\_zvs}}{C_r} = \frac{V_{out}T_{shift}(T_s - T_{shift})}{4L_rC_r} \quad \text{(Eq. 6.19)}$$

In summary, the detailed part number of all the inductors, capacitors and MOSFETs that are used to design the converter#1 and converter#2 can be found in Table 6.4.

Table 6.4. Parts Used in the Design Examples

Converters	Description	Part Number
Converter#1 (ZCS Operation)	Resonant Inductor	SLC7649S-700KL
	Resonant Capacitor (U2J)	C1812C474K5JAC
	Switching Device	BSZ013NE2LS5I
Converter#2 (ZVS Operation)	Resonant Inductor	SLC7649S-360KL
	Resonant Capacitor (X7S)	GRM32EC72A106KE05
	Switching Device	BSZ013NE2LS5I

6.4. Power Loss and Efficiency Estimation of The Designed Converters

Power loss estimation of the converter#1 and converter#2 has been carried out. According to Eq.6.20, the total loss of each converter can be divided into the following part: semiconductor loss, resonant capacitor loss, resonant inductor loss and PCB loss. The PCB loss P_{pcb} can be estimated by using FEA (finite element analysis) software such as Ansys. The inductor loss $P_{inductor}$ can be estimated by using inductor loss calculation tools provided by the manufacture.

$$P_{conv\_loss} = P_{mosfet} + P_{cap} + P_{inductor} + P_{pcb} \quad \text{(Eq. 6.20)}$$

For the capacitor loss, it can be estimated by using the resistance of the capacitor and the RMS current flowing through the capacitor bank I_{rms_cap}, Eq.6.21 calculates the capacitor loss of each capacitor bank. Here, the R_{cap} means the resistance of each capacitor at the operating frequency. And the N_{cap} represents the capacitor number in each capacitor bank.

$$P_{cap} = i_{rms\_cap}^2 * R_{cap}/N_{cap} \quad \text{(Eq. 6.21)}$$

The semiconductor loss is composed by several parts. First, the gate drive loss. The MOSFETs need power from the gate driver to turn on and turn off. The power that is used to turn on and turn off each MOSFETs can be calculated by using Eq.6.22. Note that the power consumption due to the gate drive IC is not included in this calculation. Here, the Vg is the gate

voltage, Qg is the amount of charge that is used to drive the MOSFET's gate. fs is the MOSFET's switching frequency.

$$P_{gate} = V_g Q_g f_s \quad \text{(Eq. 6.22)}$$

Second, the power loss due to the output capacitance of the MOSFETs. When one MOSFET is turned off, it will be charge to voltage Vd, which is the voltage stress of the device. When it turns on, the energy stored in the MOSFET Coss will be discharged. The power loss of each switch due to the switching behavior can be calculated with Eq.6.23.

$$P_{coss} = C_{oss} V_d^2 f_s \quad \text{(Eq. 6.23)}$$

Third, the semiconductor conduction loss. Assume the RMS value of the current flowing through each switch is i_{rms_mos}. And the on-state resistance of the MOSFET is R_{on}. Then the semiconductor conduction loss can be estimated by using Eq.6.24.

$$P_{cond} = i_{rms\_mos}^2 * R_{on} \quad \text{(Eq. 6.24)}$$

With the power loss estimation methodology provided above and the device information shown in Table 6.4, the power loss of both converter#1 and converter #2 can be obtained. First, the power loss of the passive components is calculated and compared, as shown in Figure 6.17. Because the converter#2 has lower RMS value of the current flowing through the resonant tank, the capacitor loss of converter#2 is 50% lower at the full load condition. Furthermore, the converter#1 uses 70nH inductor and converter#2 uses 36nH inductor. When the two converters use the same core, the inductors used in converter#2 have more air gap than the ones used in converter#1. In addition, the resonant current of converter#2 has smaller peak value than converter#1's peak value of the resonant current. Therefore, the inductors used in converter#2 has less flux swing than that in converter#1. As a result, the inductor loss of converter#2 is significantly smaller than the inductor loss of converter#1.

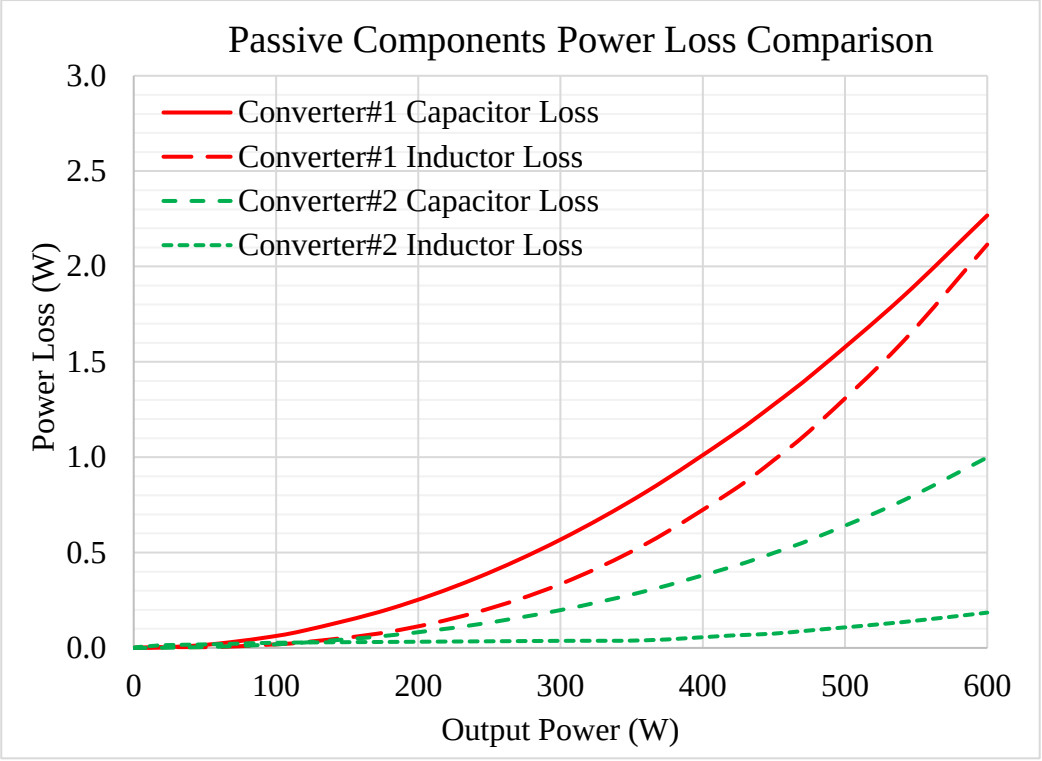

Figure 6.17. Passive components power loss of the designed converters (f_s=350kHz)

The MOSFET loss of converter#1 and converter#2 is shown in Figure 6.18, which includes the gate drive loss, MOSFET output capacitor loss and conduction loss. On one hand, as the increasing of converter output power, the MOSFET loss of converter#1 keeps increasing. On the other hand, the MOSFET loss of converter#2 decreases first. Because the recycling rate of energy stored in MOSFET output capacitors is higher than the increasing rate of MOSFET conduction loss. Then, the MOSFETs power loss increases when the switching device conduction loss becomes the main contributor. At full load condition, the converter#1 and converter#2 have similar RMS current, they have similar MOSFET conduction loss. However, the converter#2 still has less loss because it can recycle the energy stored in MOSFET output capacitors.

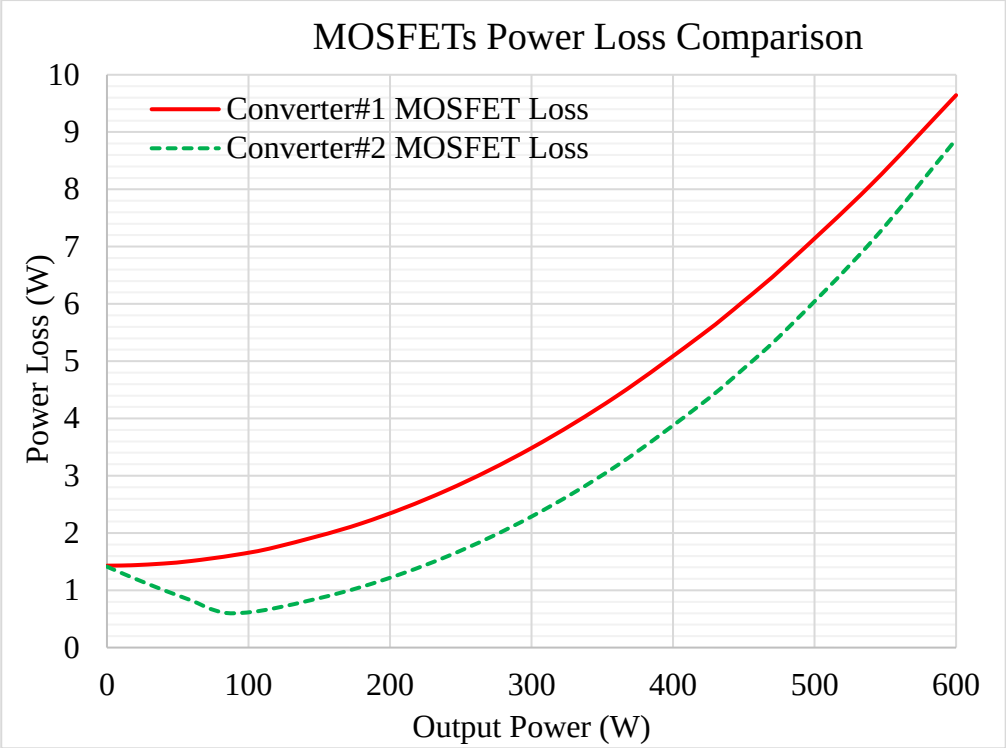

Figure 6.18. MOSFET power loss of the two designed converters(f_s=350kHz)

In Figure 6.19, the efficiency of the two designed converters have been calculated. We can tell the peak efficiency of the converter#1 is 98.31%. With the advantage of lower RMS current and zero-voltage switching, the converter#2 can achieve 99.1% efficiency. Note that the operating frequency of the converters is 350kHz. The efficiency can be further increased when the converters are operating at lower frequency. It is worth mentioning that the accuracy of the loss prediction method is proved in [142].

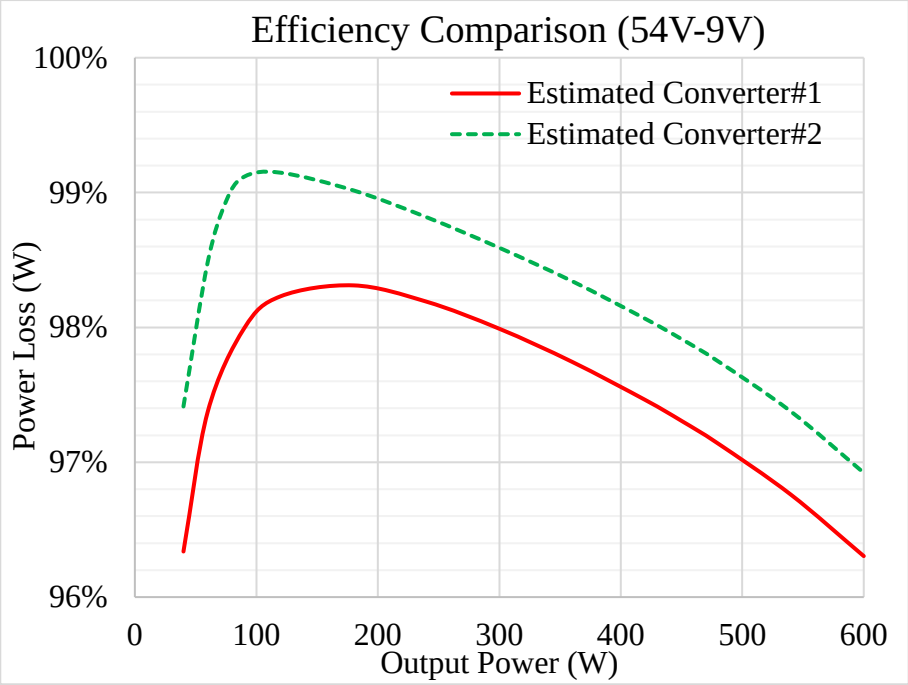

Figure 6.19. Estimated efficiency of the presented converter (f_s=350kHz)

6.5. Simulation and Experimental Results

Simulation has been carried out to validate the theoretical analysis shown in previous sections. Both of the designed converters are simulated. A comparison is performed based on the simulation results. Table 6.5 shows the parameters of the simulated switched-tank converter that is operating at ZCS mode. Table 6.6 shows the specification of designed converter that is operating at ZVS mode. For fair comparison, the switching frequencies of both converters are designed to be around 350kHz. Their input voltage and output voltage are 54V and 9V. The converter#1 uses 2.82uF capacitor banks in the resonant tanks. Different from the converter#1, the converter#2 uses 70uF capacitor banks in the resonant tanks.

Table 6.5. Parameters Used in The Simulation (Converter #1, Switched-Tank Converter, ZCS Operation)

Items	Symbols	Values
Typical Input Voltage	V_{in}	54 V
Typical Output Voltage	V_{out}	9 V
Switching Frequency	f_s	354 kHz
Resonant Inductance	L_r	70 nH
Resonant Capacitance	C_r	2.82 uF
Output Power	P_{out}	600 W

Table 6.6. Parameters Used in The Simulation (Converter #2, Presented Converter, ZVS Operation)

Items	Symbols	Values
Typical Input Voltage	Vin	54 V
Typical Output Voltage	Vout	9 V
Switching Frequency	fs	350 kHz
Resonant Inductance	Lr	36 nH
Resonant Capacitance	Cr	70 uF
Output Power	Pout	600 W

Figure 6.20 shows the current waveform of switching devices in converter#1. When the switching frequency is the same with the resonant frequency, all the switches achieve ZCS operation. The RMS value of switch current is 17.3A when the converter outputs 600W power. Figure 6.21 shows the current waveforms of inductors L1, L3 and L5, which are sinusoidal waveforms. The peak-to-peak and RMS values of the current flow through the inductors are 70.24A and 24.6A, respectively.

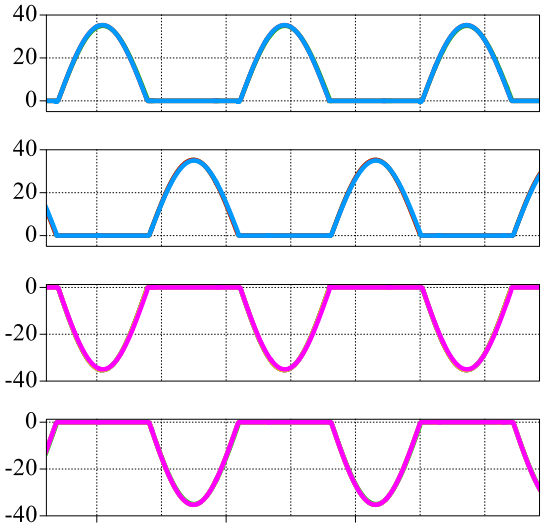

Figure 6.20. ZCS current waveforms of converter#1

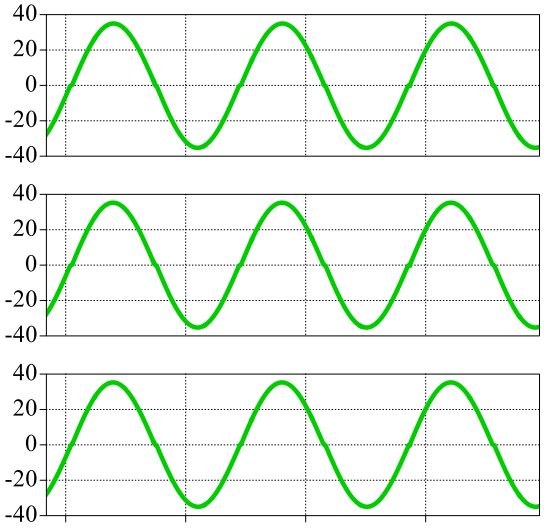

Figure 6.21. Inductor current waveforms of converter#2

Similarly, Figure 6.22 shows the current waveforms of the switching devices in converter#2. The RMS values of the four current waveforms are identical, which are 17.2A. We can tell that the two converter's switch RMS current values are the same at Pout=600W, which matches the theoretical analysis. The inductor current waveforms of converter#2 are closer to square waveforms compared with that of converter#1, as shown in Figure 6.23. The peak-to-peak value and RMS value of the waveforms are 51.6A and 24.4A, respectively. We can tell that

although the RMS values of the currents flowing through the inductors in both converters are the same, the inductors in converter#2 meet 26.7% less peak-to-peak current compared with that in converter#1. This means if the two converters use the same magnetic cores to build the inductors, the inductor loss of converter#2 will be lower than that of converter#1. And this statement is validated through the power loss estimation shown in Figure 6.17. The ZVS operation of the converter#2 is also verified through the simulation. In Figure 6.24, the voltage and current waveforms across two wing-side devices, S5 and S6, are captured. According to Figure 6.24, we can tell that the voltages of the two devices decrease to zero before the increase of their currents. This means the ZVS for the wing-side devices is achieved. Likewise, the ZVS is also achieved on rectifier side devices, which is shown in Figure 6.25. In summary, the ZVS operation of all switches in the converter#2 is verified.

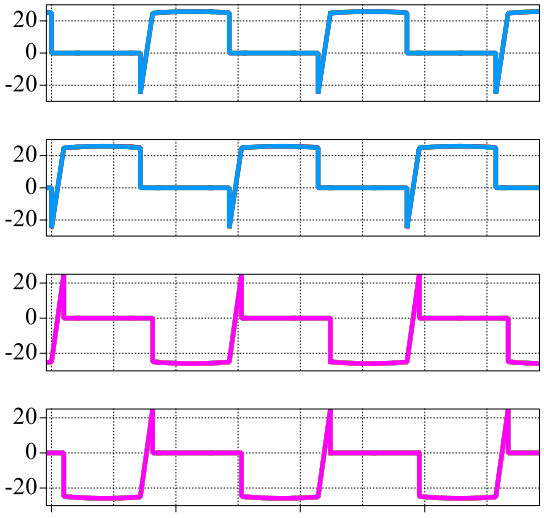

Figure 6.22. MOSFET current waveforms of converter#2

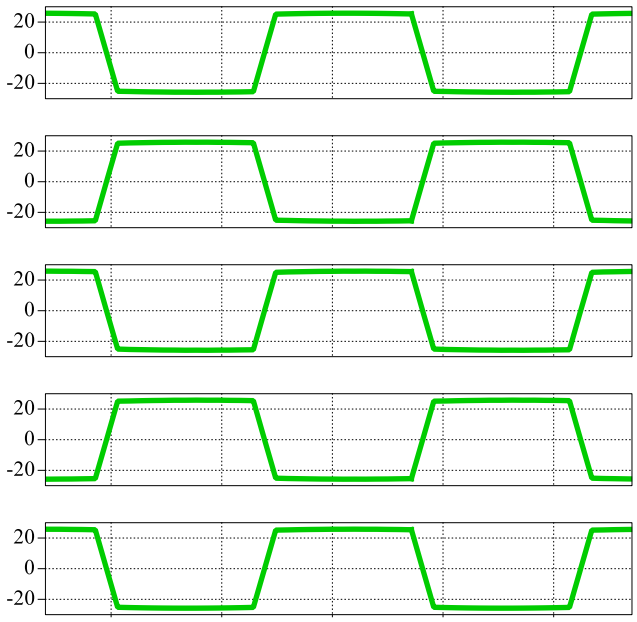

Figure 6.23. Inductor current waveforms of converter#2

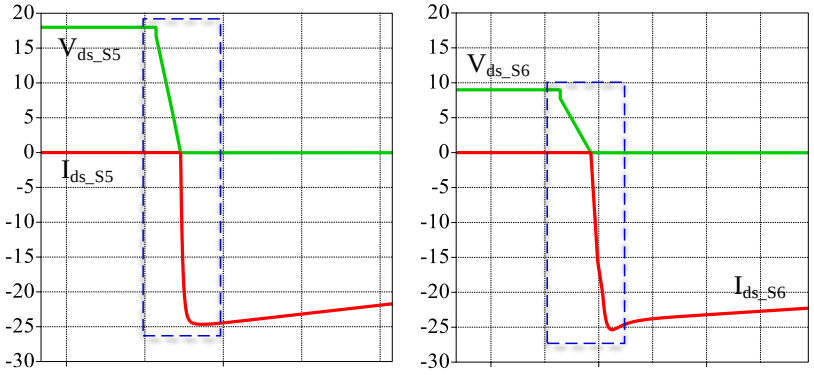

Figure 6.24. ZVS achieved on wing-side devices

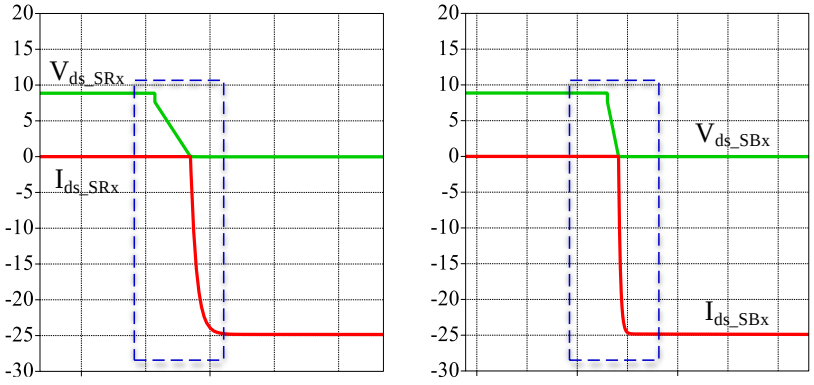

Figure 6.25. ZVS achieved on rectifier-side devices

A low-density lab prototype with 6:1 voltage conversion ratio has been built to verify the operation of the presented converter, as shown in Figure 6.26. The detailed information about the parts used in this prototype is shown in Table 6.7. The switching frequency of the prototype is 350kHz. By changing the parts in the resonant tank, the theoritical analysis for both converter#1 and converter#2 can be validated. Note that the major target for this prototype is to verify the mathematical models that are used to estimated the RMS value of the resonant current. Since the density of the presented converter is low, the PCB loss and connector loss cannot be ignored. Therefore, the efficiency of the protype is not representative.

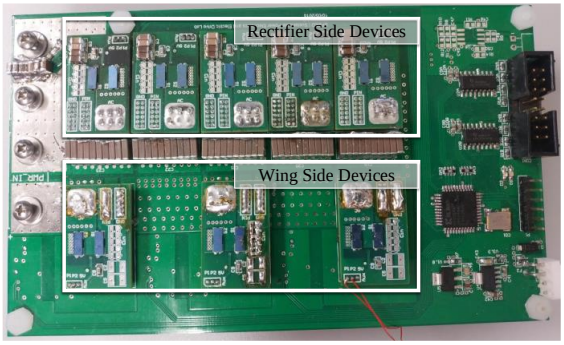

Figure 6.26. Low density lab prototype

Table 6.7. Parts Used In The Prototype

Items	Part#
Switching devices	EPC 2023
Gate Driver	LM5113
Micro-controller	TMS320F28335
Level-shifter	ADUM6200CRWZ

In Figure 6.27, two high density prototypes are proposed. The part numbers of all the key parts that are used to build the two converters are shown in Table 6.4. For the converter#1, the resoant capacitance and inductance is shown in Table 6.5. For the converter#2, considering the utilization of PCB space and capacitance drop due to DC bias voltage, 120uF is used in each resonant bank. The previouly estimated efficiency of the two converters are based on the high

density prototypes. In terms of the power density, the designed converter#1 and converter#2 can achieve 975W/in^3 and 1055W/in^3, respectively.

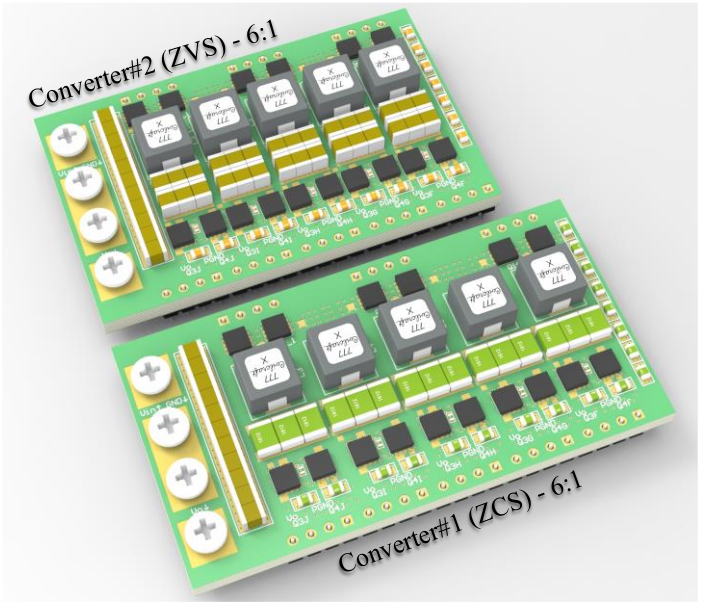

Figure 6.27. 3D view of the high-density prototypes

Experiments have been conducted on the low-density lab prototype with 54V/9V voltage input/output and 100W power output. In Figure 6.28, the current waveforms of inductor L1, L3 and L5 have been captured. The RMS values of the currents flowing through them are identical, which are 4.49A. The Figure 6.29 shows the three waveforms that are overlapped with each other, this further proves the identity of the three currents. In Figure 6.30, the voltage waveforms of the resonant capacitors C1, C3 and C5 are measured. They have 45V, 27V and 9V DC voltage, respectively. According to the waveforms, the voltage ripple of the capacitors is 2V. Figure 6.32 shows the inductor current waveforms of the converter#2. In Figure 6.31, the RMS values of the three currents are measured. They have the same value, which is 3.85A. When we overlap the three current waveforms together, they matched with each other very well, as shown in Figure 6.32. This means the power flowing through each resonant loop is balanced. In Figure 6.33, the voltage waveforms of three resonant capacitors are measured. Because the resonant capacitance of

converter#2 is much higher than that of converter#1, the voltage ripples of the capacitors are very minimum. In summary, all the measurement results match with the theoretical analysis and simulation results very well.

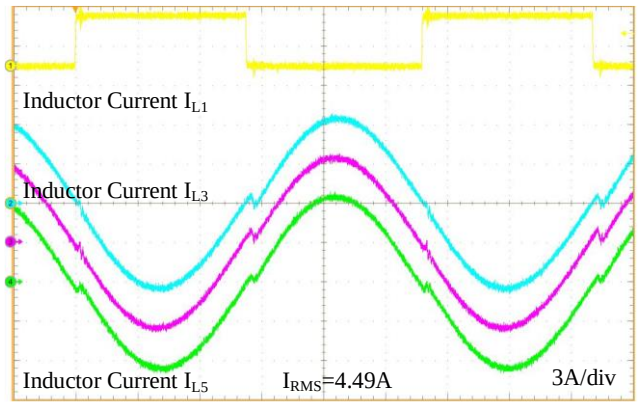

Figure 6.28. Converter#1 inductor current waveforms (V_{in}=54V, V_{out}=9V, P_{out}= 100W)

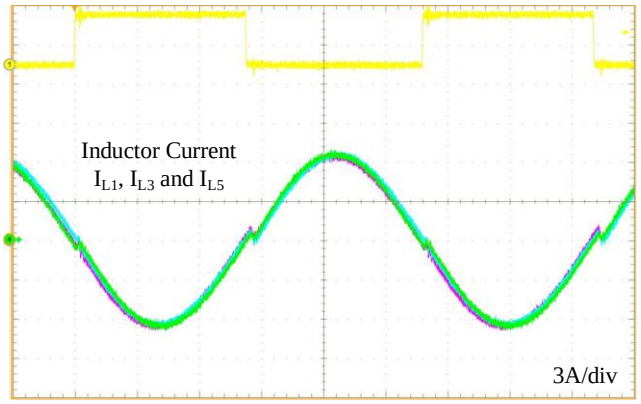

Figure 6.29. Converter#1 inductor current waveforms (V_{in}=54V, V_{out}=9V, P_{out}= 100W)

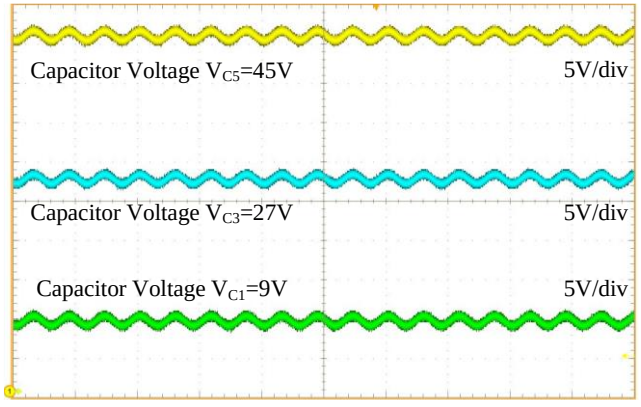

Figure 6.30. Converter#1 capacitor voltage waveforms (V_{in}=54V, V_{out}=9V, P_{out}= 100W)

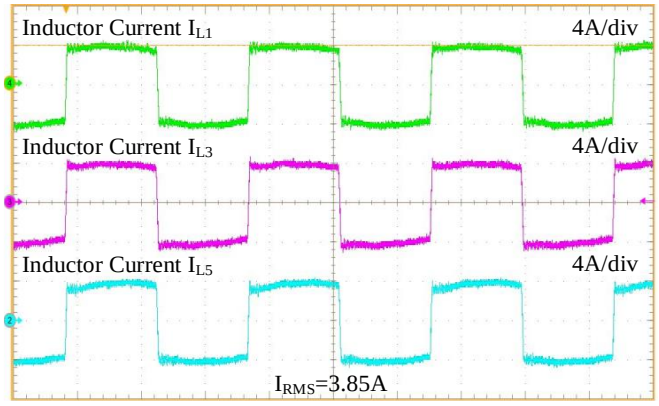

Figure 6.31. Converter#2 inductor current waveforms (V_{in}=54V, V_{out}=9V, P_{out}= 100W)

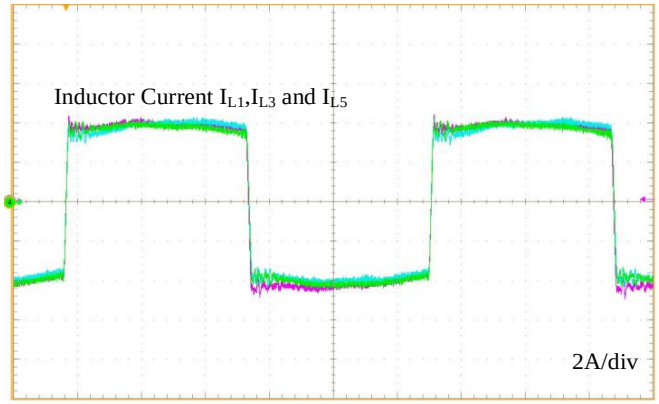

Figure 6.32. Converter#2 inductor current waveforms (V_{in}=54V, V_{out}=9V, P_{out}= 100W)

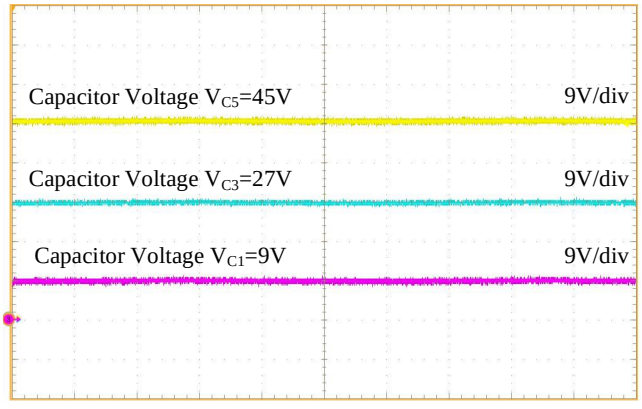

Figure 6.33. Converter#2 capacitor voltage waveforms (V_{in}=54V, V_{out}=9V, P_{out}= 100W)

6.6. Conclusion

A switched-tank topology that can achieve either zero-current switching or zero-voltage switching operation is presented in this work. The operation principle of these two modes is analyzed. Based on the analysis, mathematical models that can be used to predict the RMS values of resonant current and MOSFET current are developed. Furthermore, two converter design examples, one for ZCS operation and one for ZVS operation, are provided to show the design considerations and the procedures. The efficiency estimation of two high-density prototype has been carried out. When the converter operates at 350kHz, the peak efficiency of the ZVS version converter can reach 99.1%. And this prototype reaches 1055W/in3 density. Besides, a power loss comparison between the ZCS version converter and the ZVS version converter is carried out. At last, a low-density lab prototype is built to verify the presented mathematical models. The simulation and experimental results show that the theoretical analysis and measured results match with each other very well.

7. AN ISOLATED COMPOSITE RESONANT MULTILEVEL CONVERTER WITH PARTIAL POWER VOLTAGE REGULATION FOR TELECOM APPLICATION

7.1. Introduction

Over the years, the number of telecommunication and data center power delivery systems are growing rapidly. As a result, total power consumption of these systems is also significantly increased during the past years. In order to reduce energy waste, the efficiency improvement of these power systems becomes very important. Therefore, new architecture level topology called intermediate-bus architecture (IBA) becomes more and more popular since 1990s [50]. And the advantages of IBA relies on intermediate-bus converter (IBC) a lot. The functions of IBC is to generate an intermediate-bus voltage from higher voltage such as 48V and provide electrical isolation. Hence, the performance of IBC becomes a vital part of the power delivery systems' success. It's worth mentioning that although power system architectures with higher voltage level DC bus like 380V are claimed to be more efficient than that with 48V DC bus and they will become the trend of future datacenters [160]–[163], the systems with 48V is still the most common architectures in the world right now.

A lot of novel dc-dc converters have been proposed during the past years. In [105], a very high efficiency switched-capacitor DC-DC converter has been proposed for data center application. Although this converter has low power stress on semiconductors, it cannot meet the requirement that IBC in telecom system needs isolation [149]. And, its voltage conversion ratio is fixed. Therefore, in order to use this converter in telecom application, an isolation stage with voltage regulation capability is needed, either before or after the converter. However, using the additional stage is not an ideal solution because it leads to additional power consumption. In [164], a MultiTrack architecture has been proposed for application that needs wide range voltage

conversion ratio and isolation. This architecture uses switched-inductor concept to achieve the voltage regulation function and switched-capacitor concept to balance the capacitor voltage in the circuit. Besides, although there are many resonant converters that are proposed during the past years [165]–[167], these converters does not use partial power processing concept in the design. In [149], sigma converter that uses partial power processing concept has been proposed, with this concept, one can achieve very high efficiency and power density. Other than the converters' architecture level improvements, optimization on magnetic components also helps increase the performance of IBC. For example, optimized matrix transformer design in [168]–[170] help the converters to achieve very high efficiency and density.

This work proposed an isolated composite resonant multilevel converter with partial power voltage regulator. In order to achieve high density and efficiency, the proposed converter that utilizes partial power processing concept from [149] and keep the good features from [105]. In the proposed converter, the partial power voltage regulator allows the proposed converter have capability to regulate the output voltage. In order to show the advantages of the proposed converter, a comparison study of the novel DC-DC converter has been performed. As a result, the proposed converter has the lowest total semiconductor power stress and lowest semiconductor loss among the compared converters.

This work is organized as follows: The second section will demonstrate the topology of the proposed circuit as well as its operation modes under different input voltage. The third section states the advantages of the proposed circuit in terms of total semiconductor power stress. Furthermore, detailed power loss analysis and power loss breakdown are performed to show that the proposed converter has the lowest semiconductor power loss. Section IV shows the simulated

results and estimated efficiency. Simulation and experimental results are provided in Section IV. At last, section V concludes the proposed design.

7.2. Circuit Configuration and Operating Principle

Intermediate bus architecture is widely used in data center and telecommunication power system. For telecom application, the IBC accomplishes two functions, which are provides electrical isolation and converts intermediate bus voltage to a lower voltage, such as from 48V to 12V. For data center application, the IBC only takes care of voltage conversion, isolation is not a mandatory requirement nowadays [52]. This work proposed an IBC that is suitable for telecom applications. In this section, circuit configuration as well as operating principle will be introduced.

7.2.1. Circuit Configuration

The structure of the proposed converter is shown in Figure 7.1. For a converter with N:1 voltage conversion ratio, its primary side has N+2 switching devices and secondary side has 2N devices. Figure 7.1 shows the proposed converter with 4:1 conversion ratio. In the proposed converter, the primary side circuit contains two parts. The first part has four floating MOSFETs and three resonant branches. This part of circuit has relatively fixed conversion ratio, which is 3:1. When the switch S_2 operates at bypassing mode, 2:1 conversion ratio can be achieved. More details will be mentioned in the following work. The second part of the circuit is the partial power voltage regulator. Unlike the first part circuit, the circuit structure of this part is very flexible. It could be any isolated circuit that is capable of performing continuous and fine voltage regulation. This work uses LLC resonant converter as an example. The secondary side of the proposed circuit has N synchronous rectifier that is composed by 2N MOSFETs. In summary, the ICRMC and PPVR in the proposed converter accomplish rough voltage regulation (3:1 / 2:1) and fine voltage regulation

(continuous conversion ratio), respectively. And the secondary side circuit accomplishes current and voltage rectification function.

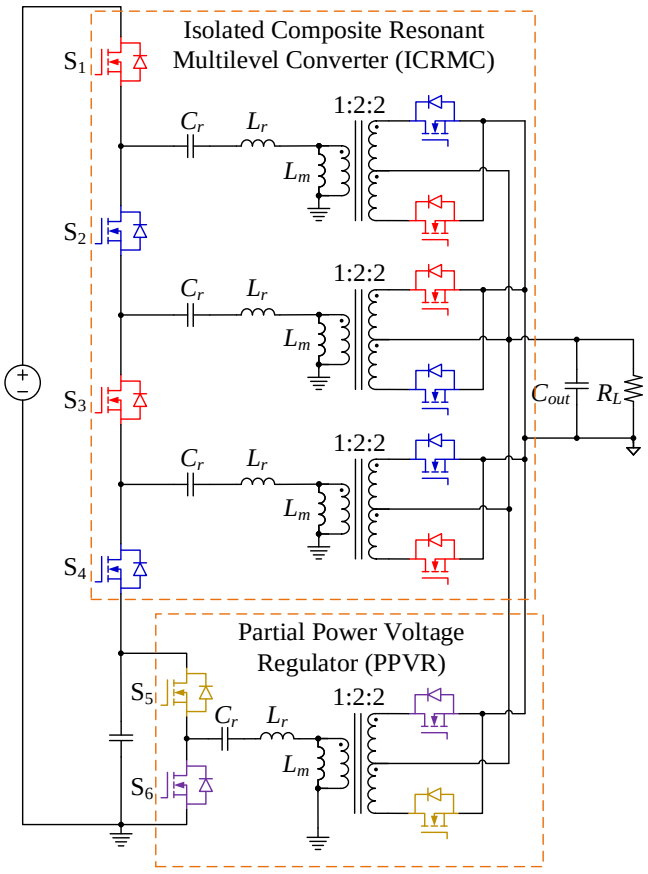

Figure 7.1. Structure of the proposed converter

7.2.2. Circuit Operation Under Different Input Voltage

In order to meet the high efficiency requirement as well as make sure the converter can operate when input voltage ranges from 36V to 60V, two operation modes has been proposed for ICRMC. Note that the highest gain of PPVR is assumed to be 1. The power processed by the isolated composite resonant multilevel converter and differential power processing module can be calculated using Eq.7.1 and Eq.7.2, respectively. Here P_{total} means the total power processed by the proposed converter.

$$P_{ICRMC} = \frac{1 - V_{C1}}{V_{in}} * P_{total} \quad \text{(Eq. 7.1)}$$

$$P_{DPP} = P_{total} - P_{ICRMC} \quad \text{(Eq. 7.2)}$$

By using the proposed two operation modes, the proposed converter uses less effort to regulate the output voltage than that without the proposed control method.

- Unregulated mode: When $V_{in} \geq 48V$, the ICRMC operates in unregulated mode. The voltage conversion ratio of this circuit is 3:1. This means the DC voltage across this module is constantly 36V. Thus, the DC voltage across PPVR will be (V_{in}-36V). For the circumstance that V_{in} ranges from 48V to 60V, the maximum voltage of the devices in PPVR is 24V. The equivalent circuits of this operation mode are shown in Figure 7.2 and Figure 7.3.
- Bypassing mode: When $V_{in} < 48V$, the ICRMC operates in bypassing mode, which means switch S_2 is always turned on. In this mode, the voltage conversion ratio is 2:1 instead of 3:1. The DC voltage across the ICRMC is 24V. And this means the DC voltage across capacitor C_1 is (V_{in}-24V). Also, the maximum voltage of the devices in PPVR is 24V when the input ranges from 36V to 48V. The equivalent circuits of this operation mode are shown in Figure 7.4 and Figure 7.5.

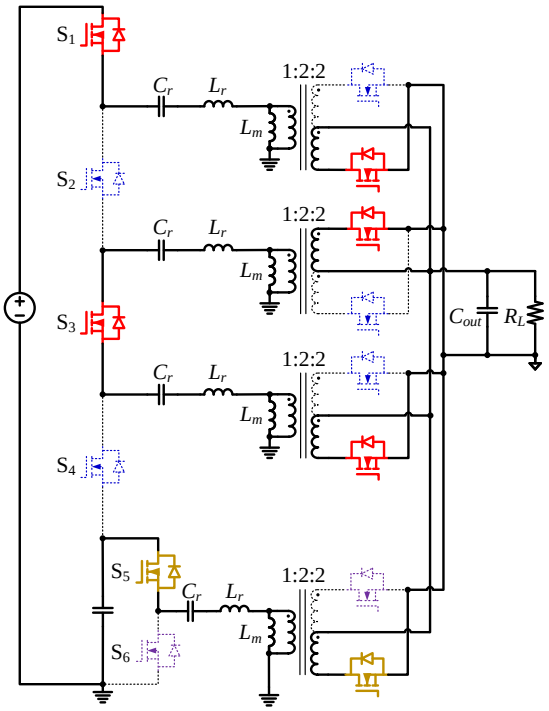

Figure 7.2. Equivalent circuit of state 1

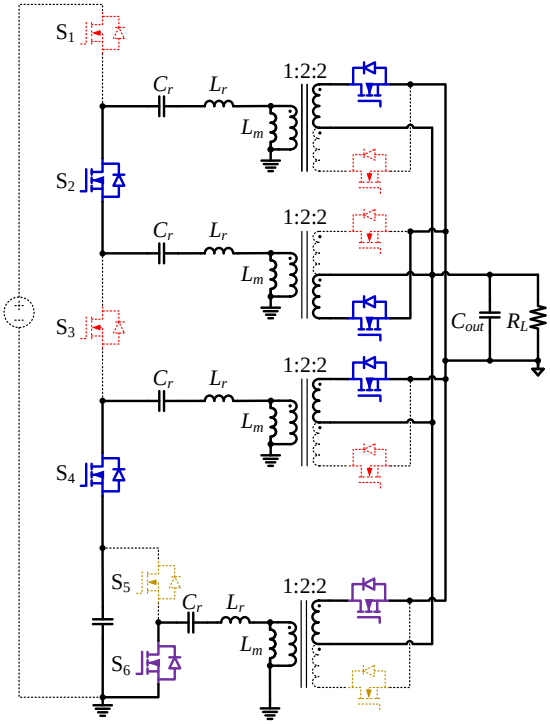

Figure 7.3. Equivalent circuit of state 2

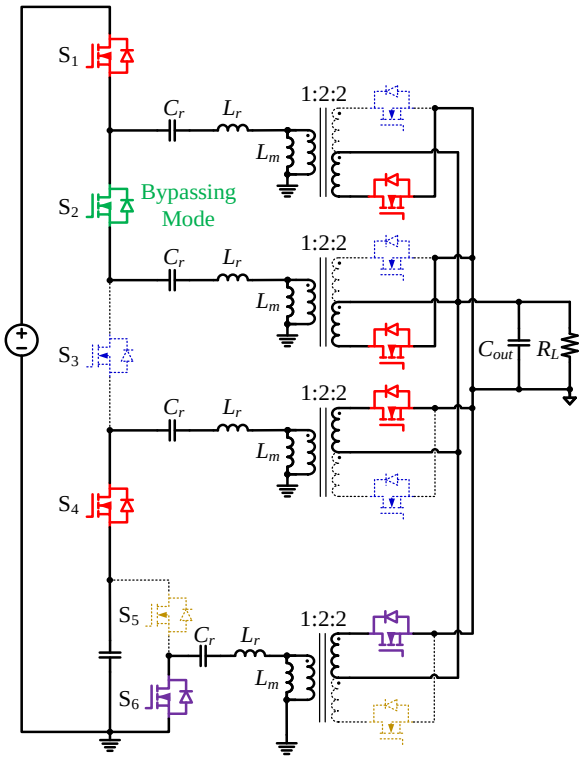

Figure 7.4. Equivalent circuit of state 1 (bypassing mode)

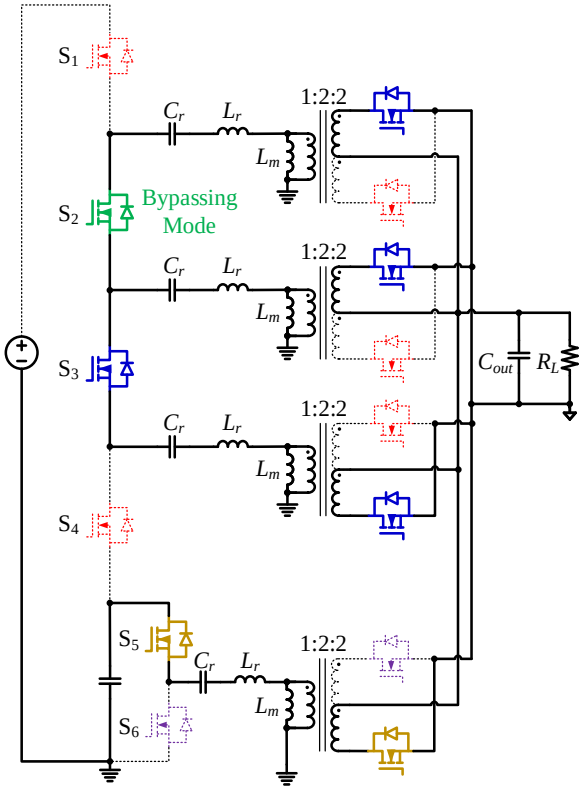

Figure 7.5. Equivalent circuit of state 2 (bypassing mode)

Assume the PPVR uses LLC resonant converter, and all the L_r and C_r in the circuit are identical. Thus, there is no doubt that the switching devices in PPVR can achieve soft-switching. Besides, the ICRMC also processes soft-switching capability. In the case that $V_{in} \geq 48V$, when switching frequency of all switching devices in the ICRMC is very close to or matches the resonant frequency of the resonant tanks and is within the ZCS operation region of the LLC resonant tanks, ZCS operation of the ICRMC has been achieved. Similarly, in the case that $V_{in} < 48V$, all of the switches in ICRMC still achieve ZCS except the switch operates in bypassing mode. The resonant frequency of the resonant tank can be calculated using Eq.7.3.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad \text{(Eq. 7.3)}$$

It is worth mentioning that when the input voltage is not 36V or 48V, the PPVR achieves buck function. As a result, zero voltage switching is achieved instead of zero current switching regarding the devices in PPVR.

7.3. Comparison Between Different Solutions

7.3.1. Advantage of the Proposed Converter

One state of the art architecture for telecom application is shown in Figure 7.6 to Figure 7.8. Similarly, this structure has two parts, unregulated module and regulated module. When applying this architecture to dc-dc power conversation application that needs high voltage gain, its highly efficient unregulated module can process more than 90% of total power. And the less efficient regulated module only processes very minimum amount of power (e.g. less than 10%). However, for 48/12V application whose input voltage ranges from 36V to 60V, the regulated module will need to process up to 60% of the total power. Thus, the benefit of this architecture is not obvious anymore. The proposed converter, on the other hand, utilizes composite converter concept and replace the traditional unregulated module with ICRMC. The new topology shown in Figure 7.9 to

Figure 7.11 can reduce the power need to be processed by regulated module and reduce converter's total semiconductor power stress. This means less power loss on switching devices.

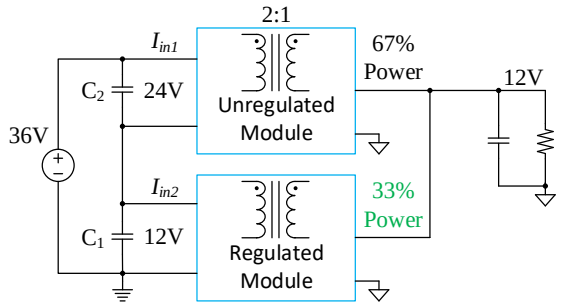

Figure 7.6. Input voltage is 36V

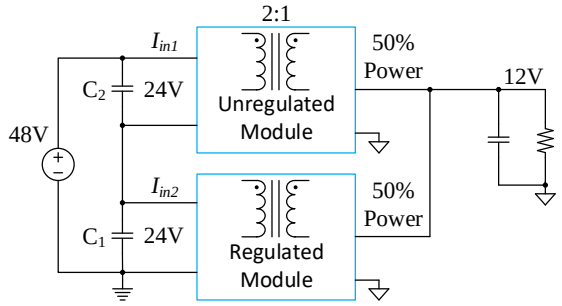

Figure 7.7. Input voltage is 48V

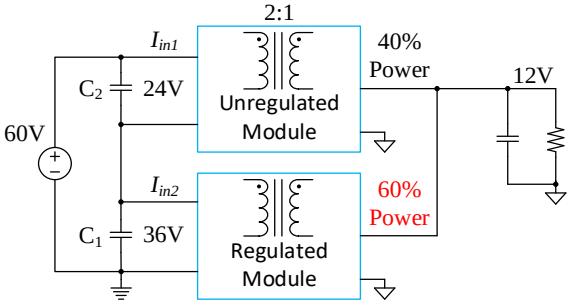

Figure 7.8. Input voltage is 60V

The total semiconductor power stress of multiple state of the art converters are compared, as shown in Figure 7.12. In this comparison, three scenarios are considered, which are $V_{in} = 36V$, $V_{in} = 48V$ and $V_{in} = 60V$. One can tell that when input voltage is 36V, the proposed converter, converter with input-series-output-parallel (ISOP) architecture and the converter shown in [149] have the lowest total power stress. When input voltage changes to 48V and 60V, the total stress of

proposed solution is always the lowest and almost unchanged under different input voltage. However, the total stress of other converters become higher as input voltage increases. Note that in this comparison, stress of the secondary side devices for all solutions are assumed to be the same and is not included in the comparison.

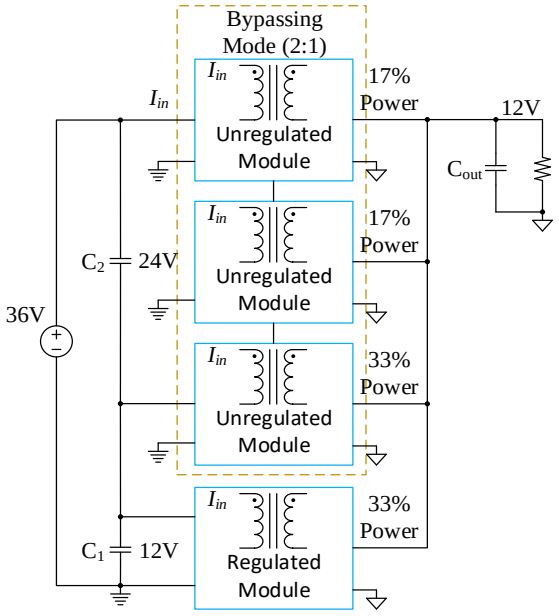

Figure 7.9. Input voltage is 36V

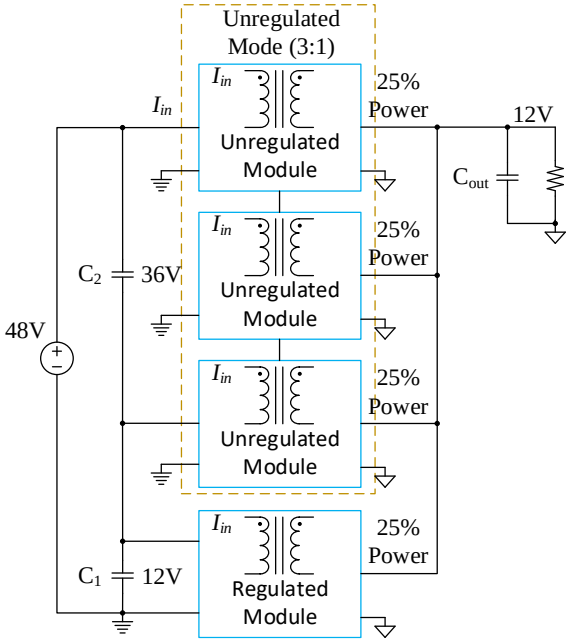

Figure 7.10. Input voltage is 48V

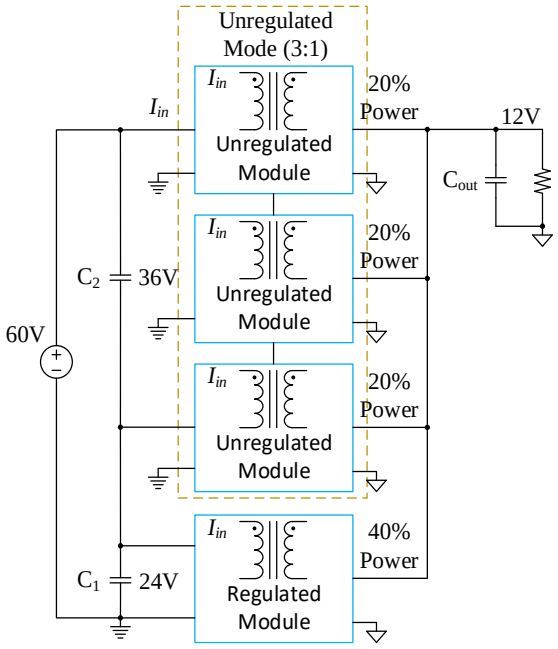

Figure 7.11. Input voltage is 60V

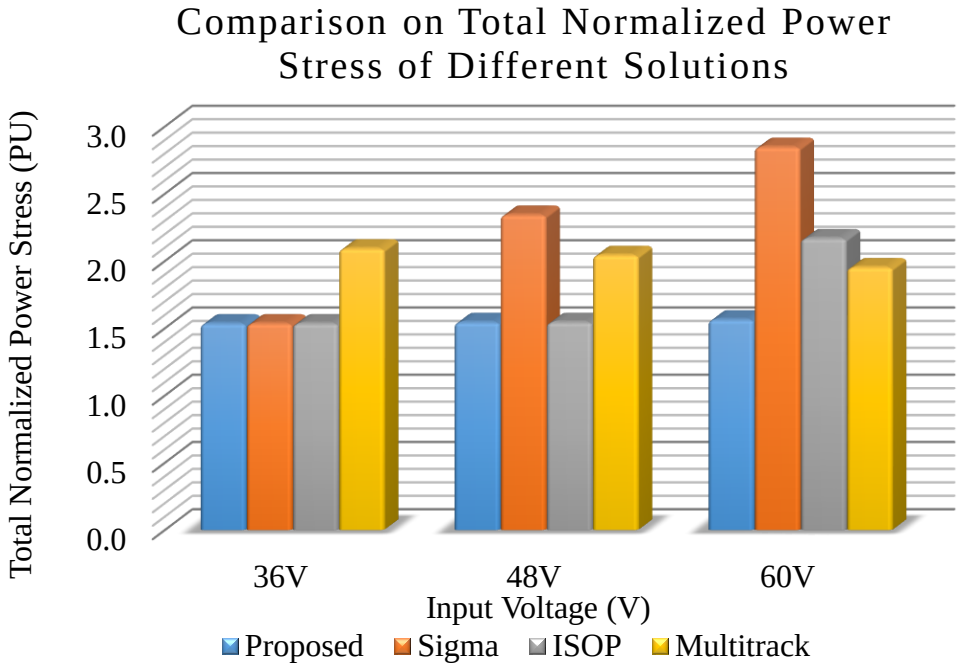

Figure 7.12. Comparison on total normalized power stress of different solutions

7.3.2. Detailed Power Loss Analysis and Power Loss Breakdown

Power loss analysis and loss breakdown has been performed when input voltage is 48V since this would be the nominal input voltage. Table 7.1 shows the information of GaN devices that

are used to perform the switching devices power loss estimation. Table 7.2 shows that the proposed converter and the converter with input-series-output-parallel (ISOP) architecture can use lower voltage rating device than that in the other two converters.

Table 7.1. Parameters of GaN Devices Used in Analysis

Part#	Q_g (nC)	V_{gs} (V)	f_s (kHz)	R_{ds_on} (mΩ)	Coss (pF)
EPC2023 (30V)	19	5	328	1.15	1724@12V
					1174@24V
EPC2024 (40V)	18	5	328	1.2	2169@12V
					1381@24V
EPC2020 (60V)	16	5	328	1.5	1820@12V
					1175@24V
					939@36V

Table 7.2. Voltage Stress of Switching Devices in Different Converters

Converter	Voltage Stress	Switching Device Used
Proposed	12V, 24V	EPC2023, EPC2024
Converter [149]	36V	EPC2020
ISOP	12V, 24V	EPC2023, EPC2024
Converter [164]	36V	EPC2020

Figure 7.13 shows the calculated total switching device power loss using different converter architectures. The proposed solution has the best performance among all the solutions. It is worth mentioning that switching loss is not included in the calculation since there is not a very accurate way to predict it. And under the nominal condition, all switching devices in the proposed solution as well as the ISOP solution achieve ZCS. On the other hand, the other two solutions can only achieve ZCS on part of the devices, as shown in Table 7.3. Also, power loss breakdown has been performed to show the loss difference between different converters, as shown in Figure 7.14. The detailed loss information can be found in Table 7.3.

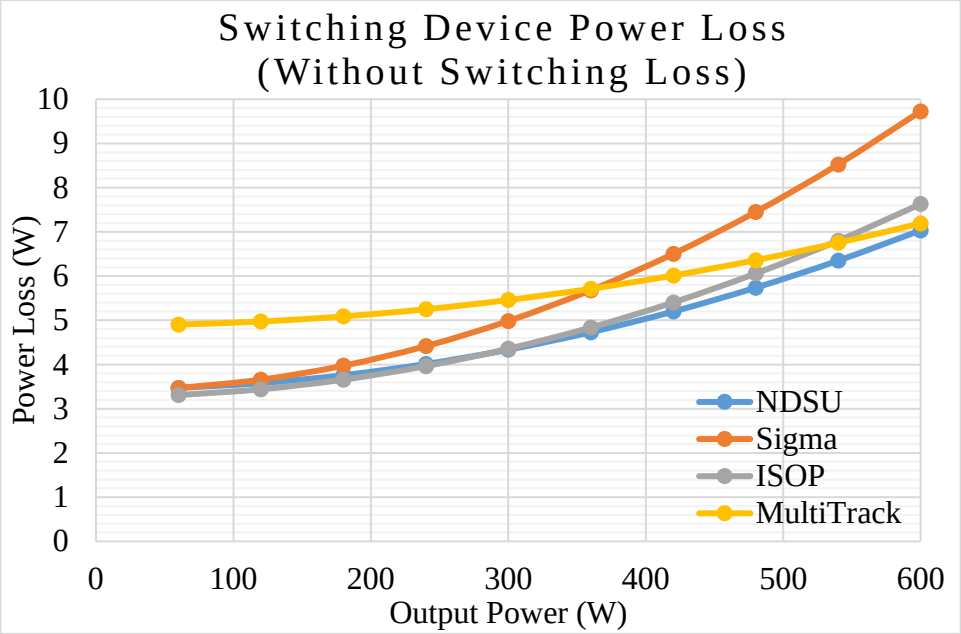

Figure 7.13. Semiconductor power loss of different analyzed converters

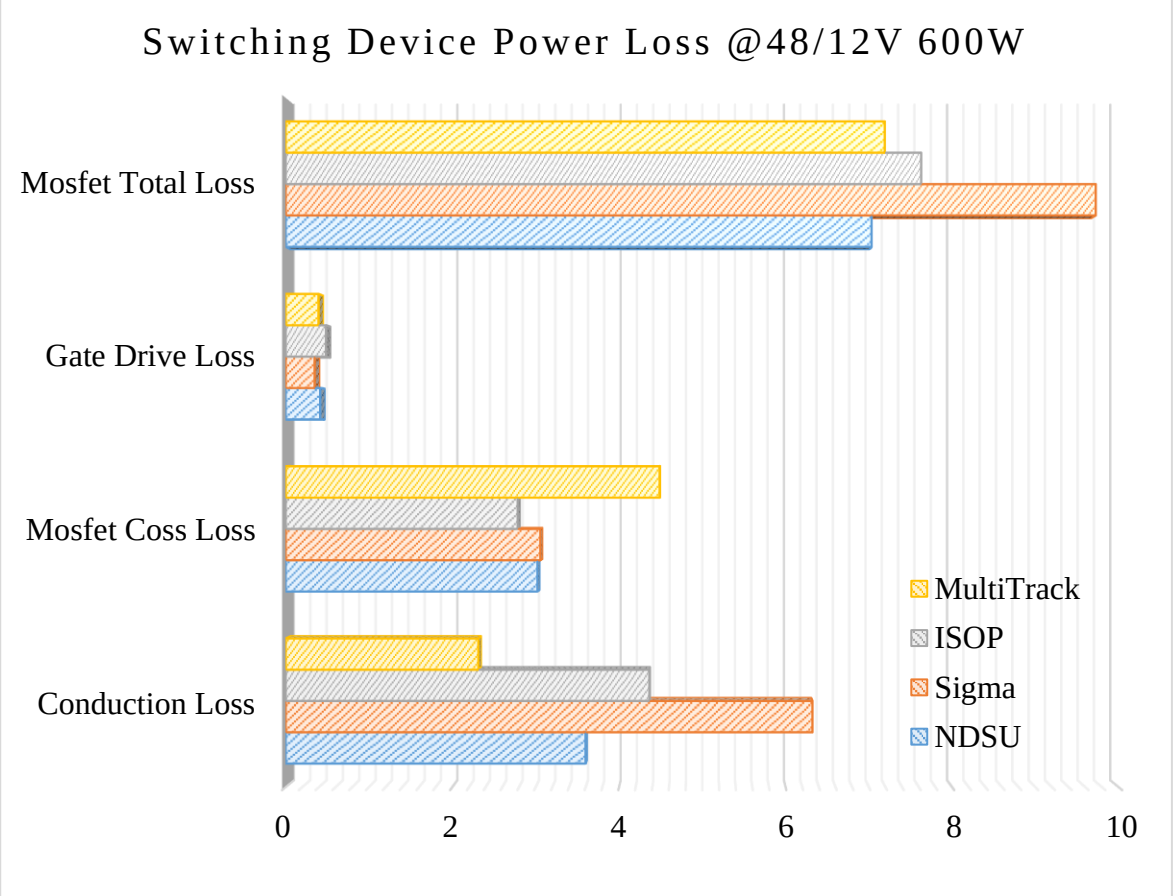

Figure 7.14. Power loss breakdown of different analyzed converters

Table 7.3. Power Loss Information when V_{in}=48V, P_{out}=600W, F_s=328kHz

Converters	Proposed	[164]	ISOP	[149]
Conduction Loss	3.60W	6.32W	4.36W	2.31W
GaN C_{oss} Loss	3.02W	3.06W	2.78W	4.49W
Gate Drive Loss	0.41W	0.35W	0.48W	0.39W
All Devices ZCS	Y	N	Y	N

7.4. Simulation Results and Efficiency of the Proposed Converter

Simulation has been performed to verify the theoretical analysis of the proposed converter operating at 600W. Table 7.4 shows the detailed parameters used in the simulation. Figure 7.15 shows that when the converter has 48V input, it generates 12V output. At this input voltage, ICRMC operates in unregulated mode. ZCS is realized on all the switching devices, as shown in Figure 7.16. Figure 7.17 shows that when the ICRMC is working in bypassing mode, the converter converts 36V to 12V. And ZCS is achieved on all switching devices, as shown in Figure 7.18.

Table 7.4. Parameters Used in The Simulation

Description	Items	Values
Input voltage Range	V_{in}	36V ~ 60 V
Nominal input voltage	V_{in_nom}	48V
Output voltage	V_{out}	12 V
Output Power	P_{out}	600 W
Resonant capacitor	C_r	2.35 μF
Resonant inductor	L_r	100 nH
Magnitizating Inductance	L_m	10 μH
Resistor load	R_{load}	0.24 Ω
Resonant frequency	f_r	328.3 kHz
Switching frequency	f_s	316.5 kHz

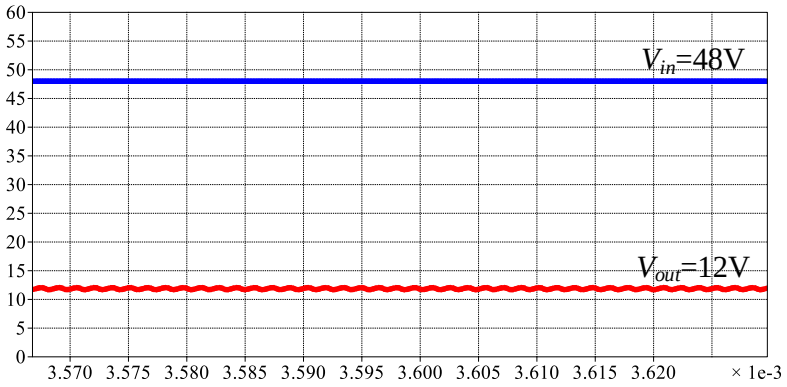

Figure 7.15. Input and output voltage

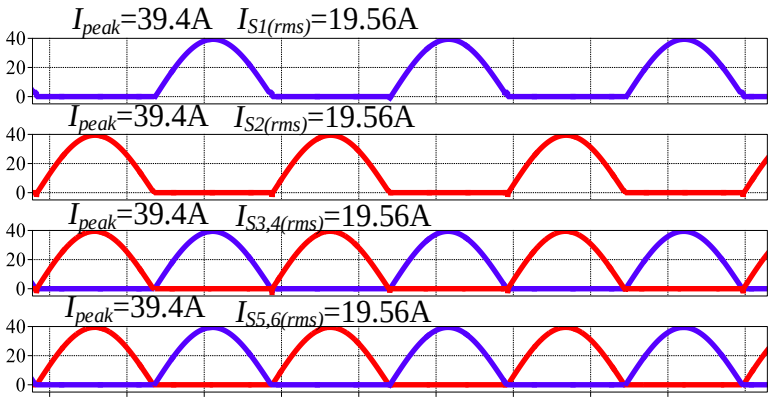

Figure 7.16. Switch devices' current waveforms

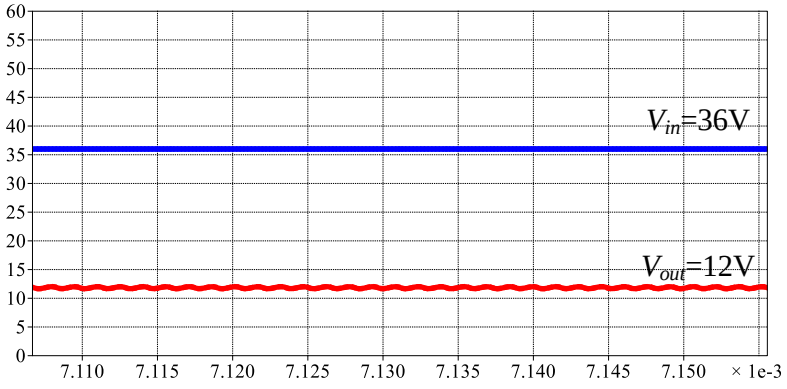

Figure 7.17. Input and output voltage

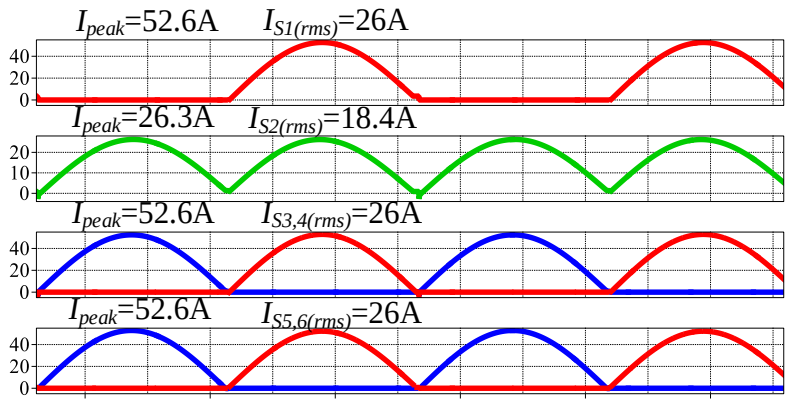

Figure 7.18. Switch devices' current waveforms

In Figure 7.19, the estimated efficiency curve shows that the proposed converter with 600W rating can reach 97.65% efficiency. Improvements regarding efficiency and power density can be further performed based on the power loss breakdown of the proposed converter that is shown in Figure 7.20.

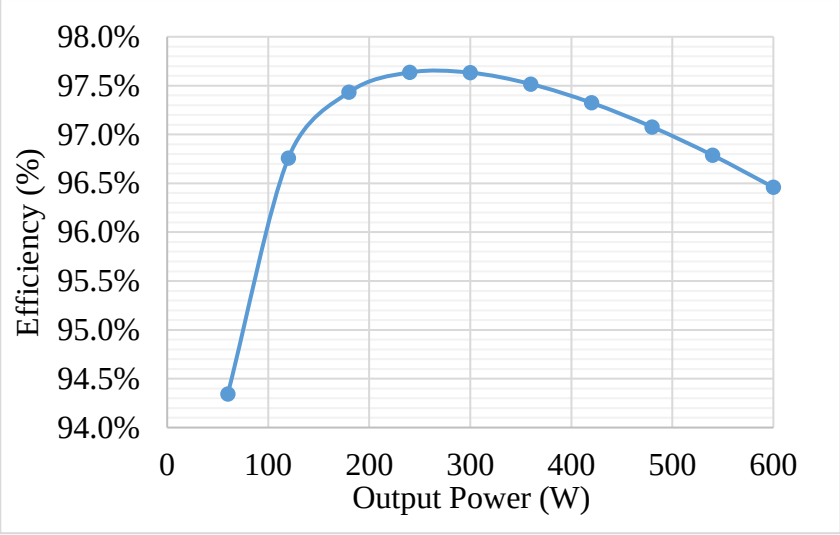

Figure 7.19. Efficiency estimation of the proposed converter (48V input)

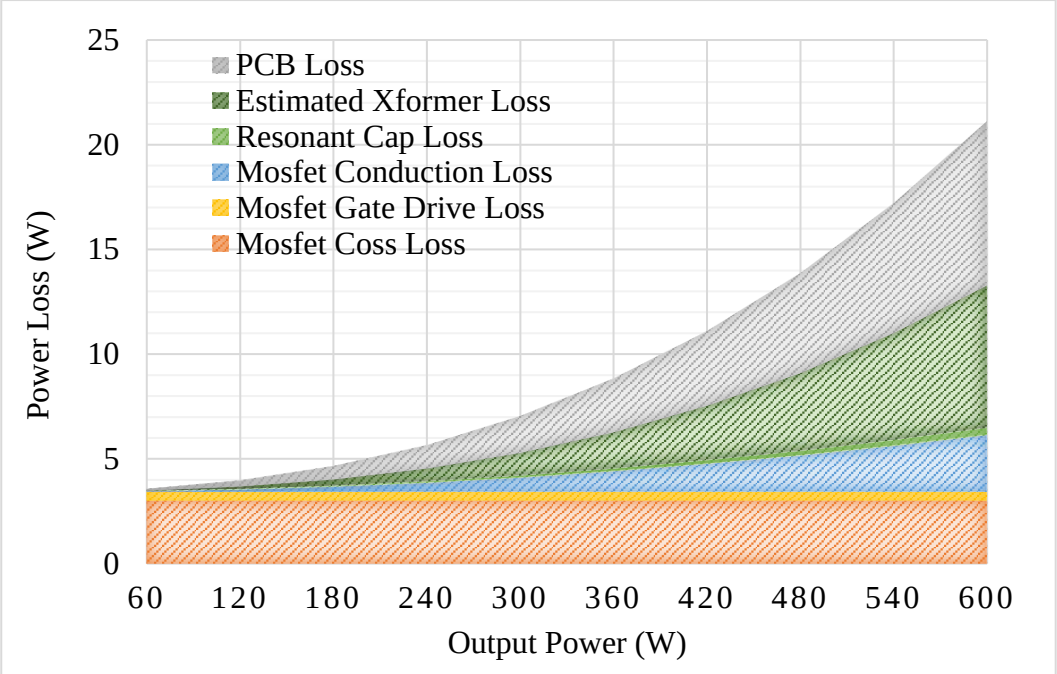

Figure 7.20. Power loss breakdown of the proposed converter (48V input)

A GaN based prototype has been developed to verify the theoretical analysis, as shown in Figure 7.21. Note that the maximum power of the prototype is limited to 300W due to limited PCB layers (4-layer). A planar transformer using ML95S material from Hitachi is used in the prototype. In Figure 7.22, when then input voltage of the converter is 48V, the converter generates 12V at the output side. And Figure 7.23 shows the current waveforms of resonant capacitor in the ICRMC and PPVR. According to this figure, soft-switching of the switching devices is validated. More detailed prototype design and experimental results will be included in future publications.

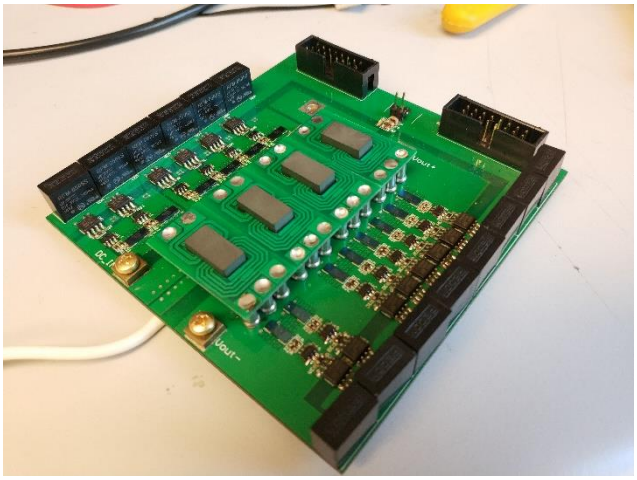

Figure 7.21. Designed 300W prototype

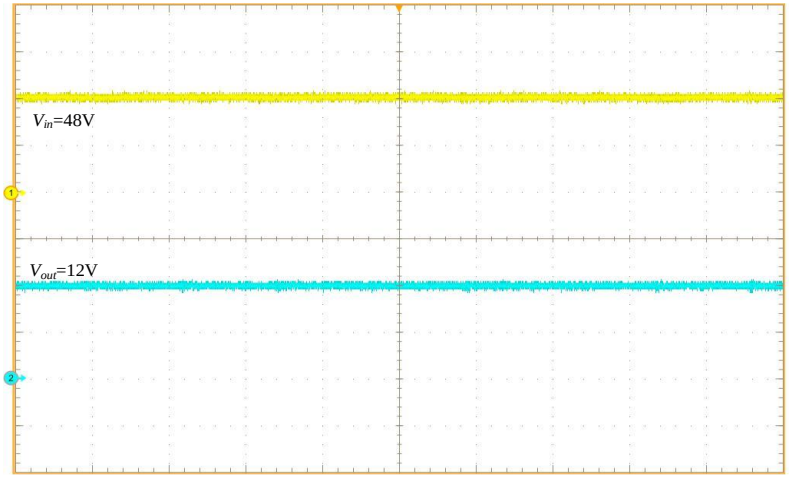

Figure 7.22. Input and output voltage

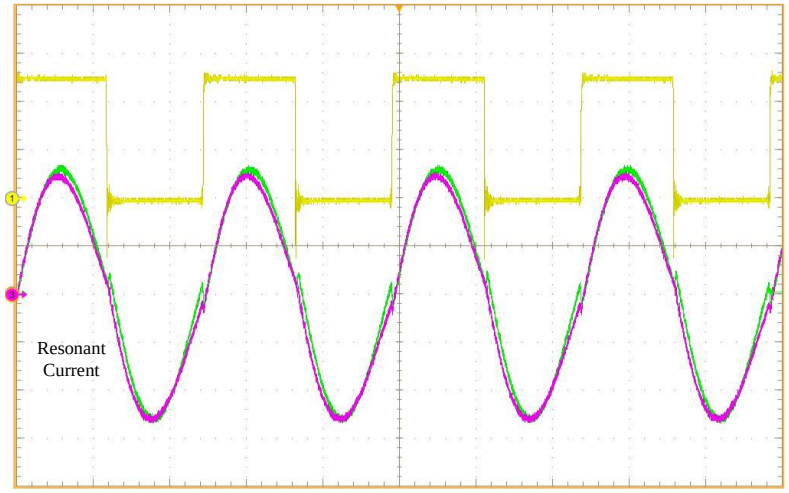

Figure 7.23. Resonant current of unregulated module and PPVR

7.5. Conclusion

This work presents an isolated composite resonant multilevel converter with partial power voltage regulation for 48/12V application. The contribution of this work are threefold. First, composite converter concept is used to effectively reduce total semiconductor power stress in the new converter to ensure its high efficiency operation. Second, the proposed topology allows the partial power voltage regulator to process less power than traditional solution. This means more power can flow through highly efficient ICRMC. Thus, power loss can be reduced. Third, the proposed converter has the capability to achieve fine voltage regulation. At last, A GaN based converter prototype is built to validate the theoretical analysis.

8. A 100KW SWITCHED-TANK CONVERTER FOR ELECTRIC VEHICLE APPLICATION

8.1. Introduction

As the growth of environmental awareness among the world, direct vehicle emissions of conventional vehicles are recognized to be harmful to human health and the major source of greenhouse gases. Battery electric vehicles start drawing more and more attention because they have zero direct vehicle emissions. And they could be the key solution to help improve the environment of the world. With the development of SiC technology, SiC devices are widely used in power electronics area, such as inverters[111], [171], [172], Also, how the leveraging the advantages of SiC devices in electric vehicle powertrain applications become hot topics in recent years[173]–[175].

As shown in Figure 8.1, the electric vehicle powertrain includes on-board charger, battery system, bi-directional dc-dc converter and motor drive system. The nominal battery voltage is usually around 300V, and the DC bus of the inverter is around 600~800V [124]. Thus, the bi-directional DC-DC converter will need to boost the battery voltage up to two times higher and feed to the motor drive system. In [176], a boost converter is optimized to achieve high power density and high efficiency. The volume of the converter is 9.15 liter and it achieves 6kW/L power density. In [177] and [126], a composite boost converter has been presented, it achieves lower loss than conventional boost converter. The predicted volume of the 39kW converter is 1.8 liter. In [178], a three-phase interleaved boost converter shows that interleaved topology can greatly reduce the volume of the converter. In [125], a 100kW boost converter with coupled inductor are presented. The converter achieves 27.9kW/L power density and 98% efficiency.

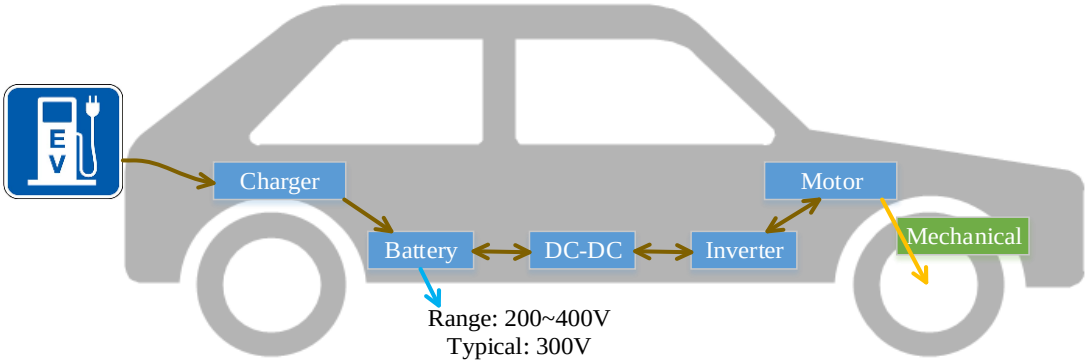

Figure 8.1. Powertrain of an electric vehicle

This work proposed a new evaluation method that evaluates different converter topologies show the advantages of the presented one-cell STC over the boost converter and 3-level flying capacitor multilevel (FCML) converter. This work also evaluates the potential converter size reduction by using interleaving concept. Compared with the state-of-art solution that still uses conventional boost converter in the circuit (22kW/L) [126], this work presents a 1-phase STC that can achieve higher density (45kW/L) with an estimated total volume of 2.2 liters in the second section. However, although the 1-phase converter achieves very high density, the size of passive components (e.g. input and output capacitors) is not optimized because of the high RMS current flowing through them. As a result, interleaved topology has been evaluated to reduce the size of passive components. Both ZVS operation mode and ZCS operation mode are studied in this work, which shows the ZCS operation mode is more suitable for the interleaved operation. With 3-phase interleaved operation, the estimated converter size reduction can be as high as 60%. Simulation results are provided to show that the RMS current of the passive components has been significantly reduced with 3-phase interleaved operation. At last, a 100kW 1-phase prototype and a 3-phase prototype are demonstrated for size comparison purpose.

8.2. Circuit Configuration and Analysis

8.2.1. Circuit Configuration and Topology Evaluation

Figure 8.2 shows the generalized circuit configuration of the new switched-tank converter. This structure is highly modular and scalable. Figure 8.3 shows the circuit configuration of the presented one-cell STC. This converter has two operation modes, which are ZCS mode and ZVS mode. Under ZCS operation mode, the conversion ratio of the converter is fixed, which is 2 to 1. Under ZVS operation mode, the output of the converter can be regulated. However, because the converter achieves the highest efficiency when its conversion ratio is 2 to 1 and the DC bus voltage of the inverter does not need to be regulated to a specific value in the existing electric vehicles [179], voltage regulation is not within the scope of this work.

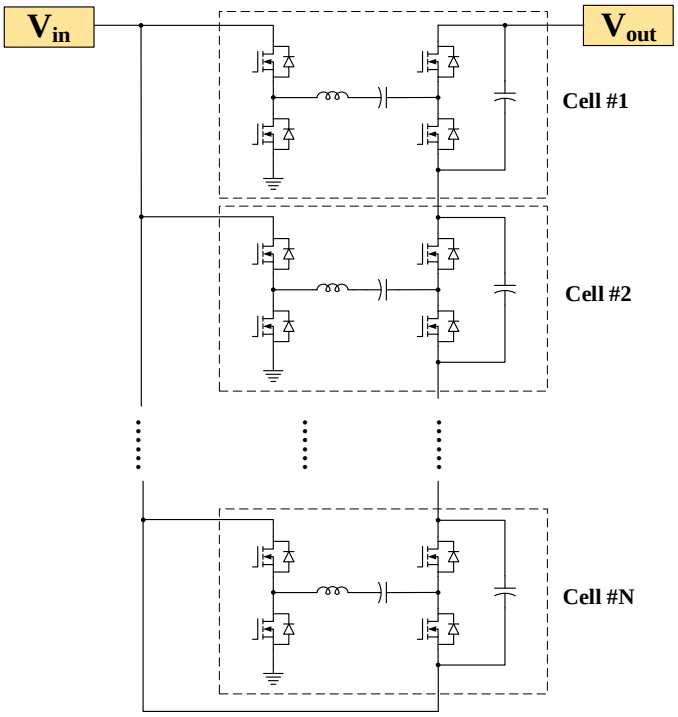

Figure 8.2. Generalized circuit structure of the new STC

First, three different converter topologies are compared, which are the one-cell switched-tank converter, 3-level FCML converter and boost converter, as shown in Figure 8.3 to Figure 8.5.

In this comparison, we assume the boost converter is operating at continues conduction mode (CCM) and the inductor current ripple is 30% of its average current value. So, semiconductor switching loss of the boost converter cannot be ignored in this topology evaluation part. Also, we assume the 3-level FCML converter and STC operating at ZCS mode. Thus, the semiconductor loss of this two converters is the same.

In order to ensure the fairness of the comparison, semiconductor loss index (SLI) is introduced to evaluate the utilization level of semiconductor devices in all the circuits, which is represented by $P_{loss\_norm}(A_{die})$. The semiconductor loss index $P_{loss\_norm}(A_{die})$ can be calculated by using Eq.8.1. Note that the $P_{cond}(A_{die})$, $P_{gate}(A_{die})$ and $P_{switching}(A_{die})$ means the total semiconductor conduction loss, total gate drive loss and total switching loss of the converter when the total semiconductor die area usage is A_{die} in a converter. They can be calculated by using equation Eq.8.2, Eq.8.3 and Eq.8.4. In the ZCS case, the total switching loss can be simplified as MOSFET output capacitor loss, as shown in Eq.8.5. The $P_{converter}$ is the power rating to the converter. According to Eq.8.1, we can tell that if the total semiconductor die area usage of two converters are the same, then the converter that has lower semiconductor loss index value is more efficient than the other one. In summary, the converter with lower semiconductor loss index can better utilize the switching devices.

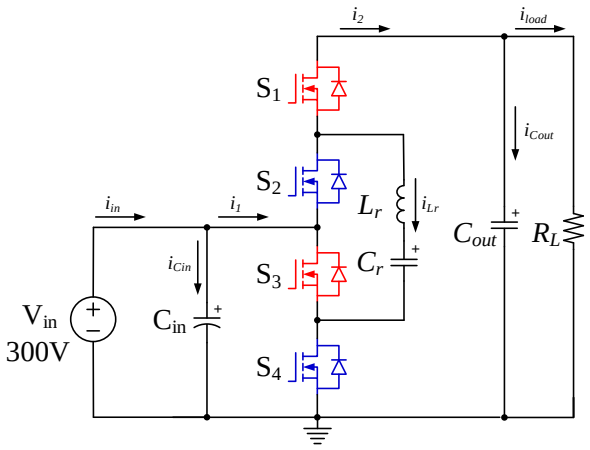

Figure 8.3. Presented one-cell switched-tank converter

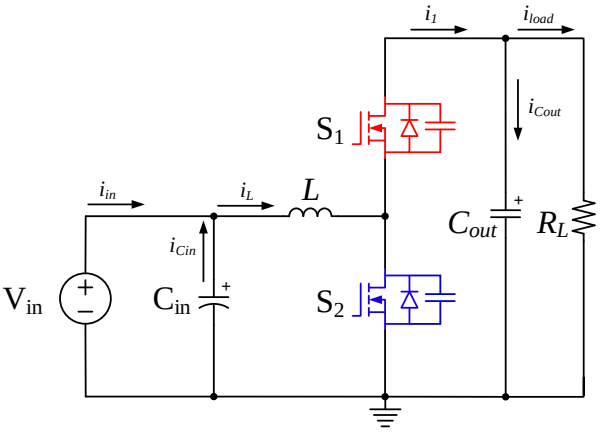

Figure 8.4. Boost converter

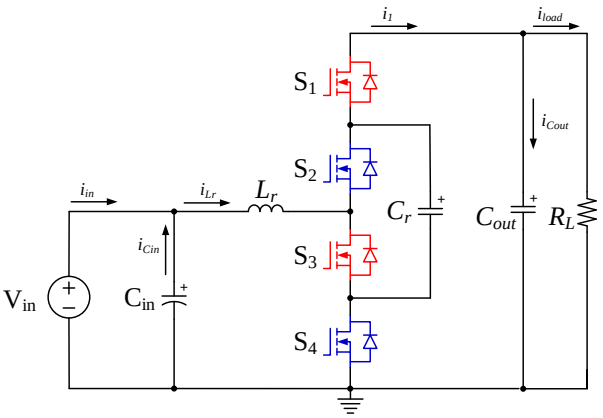

Figure 8.5. 3-level flying capacitor multilevel converter

$$P_{loss\_norm}(A_{die}) = \frac{P_{cond}(A_{die}) + P_{gate}(A_{die}) + P_{switching}(A_{die})}{P_{converter}} \quad \text{(Eq. 8.1)}$$

$$P_{cond}(A_{die}) = \sum_i I_{rms_i}^2 \frac{\alpha_i(\xi_i, V_{B_i})}{k_i A_{die}} \quad (\alpha_i(\xi_i, V_{B_i}) = R_{ds(on)} A_{die}(V_{B_i})) \quad \text{(Eq. 8.2)}$$

$$P_{gate}(A_{die}) = \sum_i V_{gs_i} f_{s_i} \beta_i k_i A_{die} \qquad (\beta_i = \frac{Q_{g_i}}{A_{die}}) \quad \text{(Eq. 8.3)}$$

$$P_{switching}(A_{die}) = \sum_i [E_{on_i}(A_{die}) + E_{off_i}(A_{die})] f_{s_i} \quad \text{(Eq. 8.4)}$$

$$P_{switching\_zcs}(A_{die}) = \sum_i V_{ds_i}^2 f_{s_i} \gamma_i k_i A_{die} \qquad (\gamma = \frac{C_{oss_i}}{A_{die}}) \quad \text{(Eq. 8.5)}$$

According to Figure 8.6, with the same semiconductor technology, the value of $R_{ds(on)}$*A_{die} is a fixed number when the breakdown voltage V_B is fixed. This means for a certain semiconductor technology, the $\alpha_i(\xi_i, V_{B_i})$ is a fixed value when V_{B_i} is determined. The ξ_i in Eq.8.2 represents the coefficient of the semiconductor technology of the ith device. In addition, we also assume the parameters β_i and γ_i shown in Eq.8.3 and Eq.8.5 are constant values. This means when we increase the total die area A_{die} by *N* times, the Q_g and C_{oss} will also be *N* times larger and the $R_{ds(on)}$ will reduce by *N* times, which is the same as connecting *N* dies in parallel. The parameter k_i means the ratio of the i^{th} die's area over the total die area A_{die} since there are multiple switches been used in a converter, and $\sum_i k_i = 1$. By tuning the parameter k_i, the switch conduction loss of a converter can be optimized. It's worth mentioning that the semiconductor loss index values are the same for 3-level FCML converter and STC.

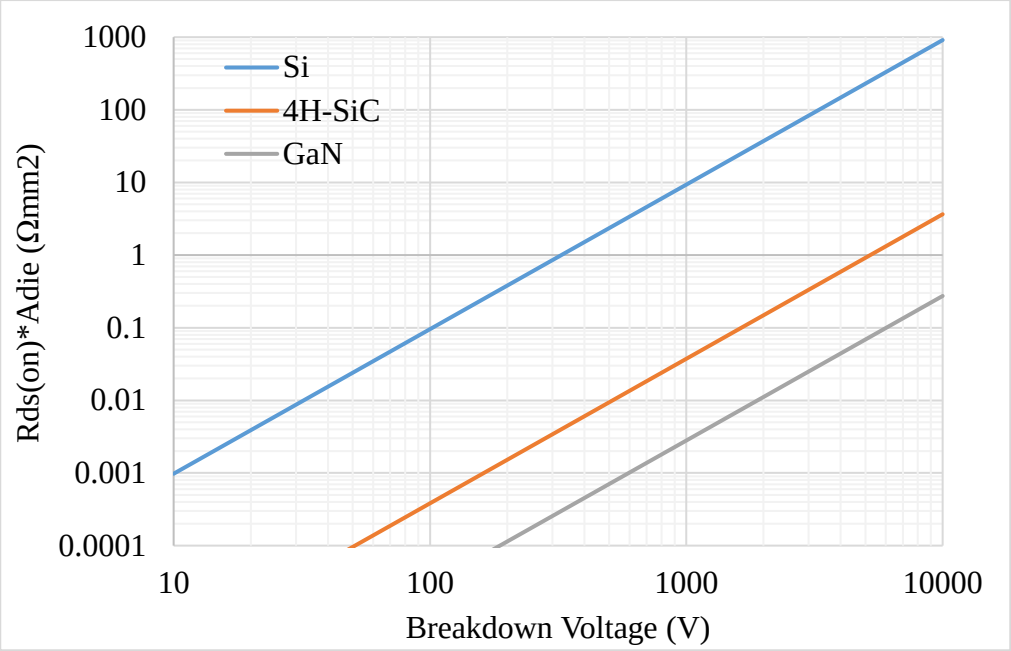

Figure 8.6. Theoretical on-resistance and blocking voltage relationship for silicon, silicon-carbide, and gallium nitride devices [180]–[183]

For converter with 300V input and 600V output, 1200V dies from both Rohm and Wolfspeed are used in the boost converter evaluation. And we assume the die area of the upper switch and the lower switch in the boost converter are the same, which means k_i=0.5. On the other hand, 900V die from Wolfspeed and 650V die from Rohm are used in the STC and 3-level FCML converter. Table 8.1 shows the SiC die information used for the evaluation. Figure 8.7 shows that the power loss of switching devices in STC and 3-level FCML converter is less than 50% the total semiconductor loss of the boost converter under full load. This is because the switching loss is a major contributor to the total semiconductor power loss in boost converter. Note that although the 3-level FCML converter and STC have the same semiconductor loss index, the mechanical layout of 3-level FCML converter is more challenging since its inductor, input and output capacitors are on the dc side.

Table 8.1. Die Information Used In the Comparison

Part#	Company	Voltage Rating	Current Rating
S4003	Rohm	650 V	118 A
S4103	Rohm	1200 V	95 A
CPM3-0900-0010A	Wolfspeed	900 V	196 A
CPM2-1200-0025B	Wolfspeed	1200 V	98 A

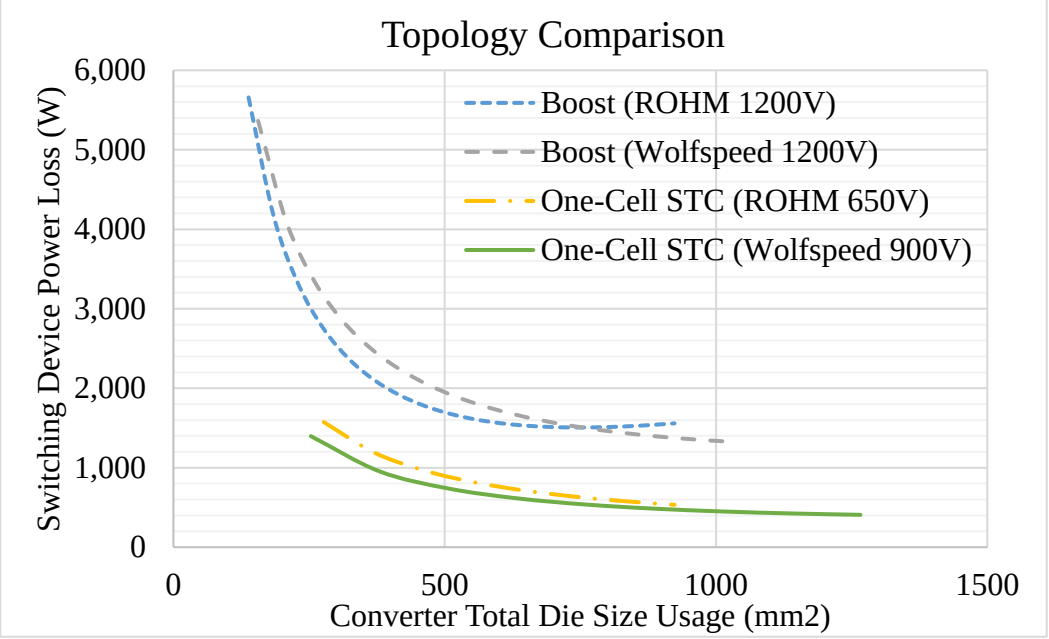

Figure 8.7. Topology comparison (300V input and 600V output, 100kW)

8.2.2. Design of Passive Components in 1-Phase Converter

Since the topology evaluation shows that the STC is a better choice than the other two converters, the next step is to figure out the potential improvement that can be done to reduce the passive component size of the one-cell STC, especially the input and output capacitors. Therefore, the current flowing through input and output capacitors should be analyzed. In order to analyze the current waveforms of passive components in the circuit, some assumptions have been made to simplify the analysis procedure. First, the voltage ripple across the input capacitor, output capacitor and resonant capacitor is small enough. Second, all the switching devices are ideal. It is worth

mentioning that the mechanisms to achieve ZCS and ZVS operation of the presented converter will not be included in this work since they have been analyzed in previous works [101]–[103], [105], [142]. This work only focuses on obtaining the current waveforms of different passive component under different operation modes. In Figure 8.11, state 1 and 3 shows the operation states of ZCS mode, while state 1 to 4 shows 4 operation states of ZVS mode. The waveforms of current flow through the passive components in both modes can be found in Figure 8.12 and Figure 8.13, respectively.

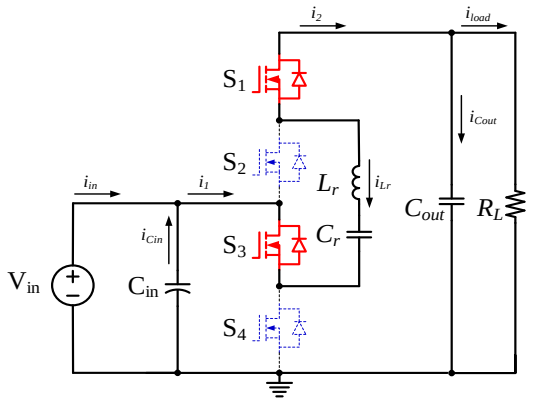

Figure 8.8. State 1

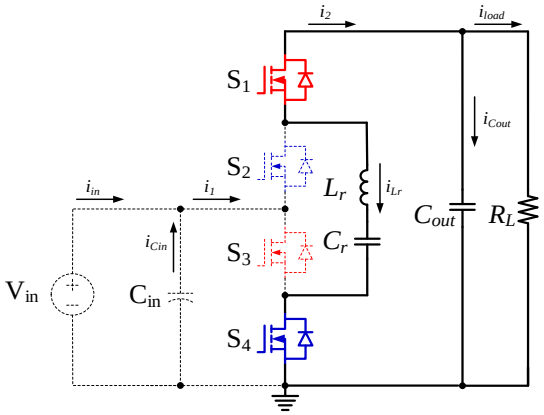

Figure 8.9. State 2

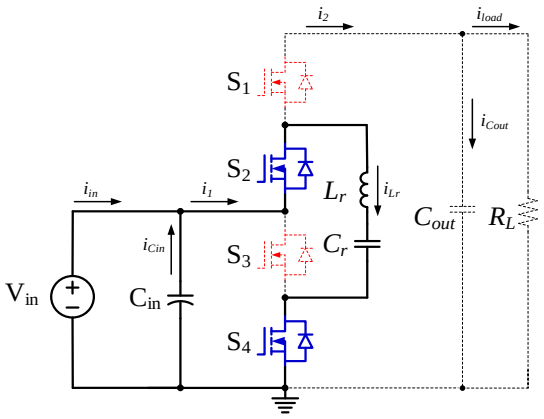

Figure 8.10. State 3

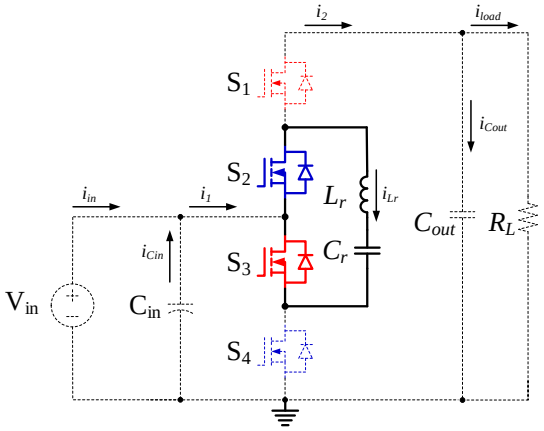

Figure 8.11. State 4

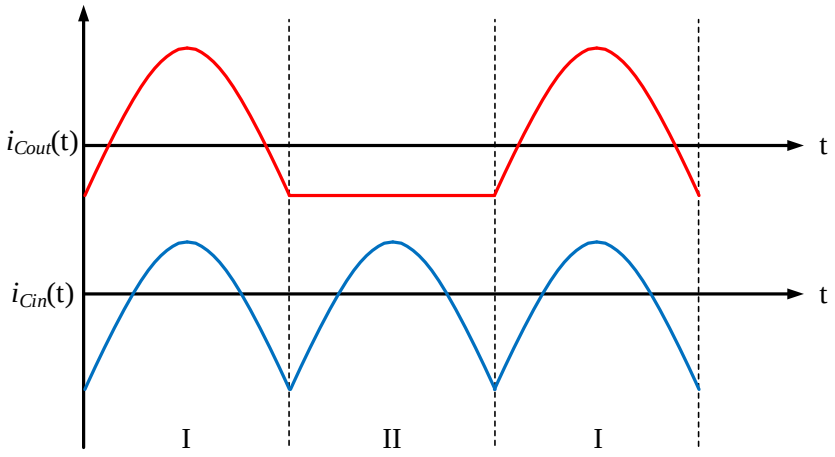

Figure 8.12. Current waveforms of ZCS operation

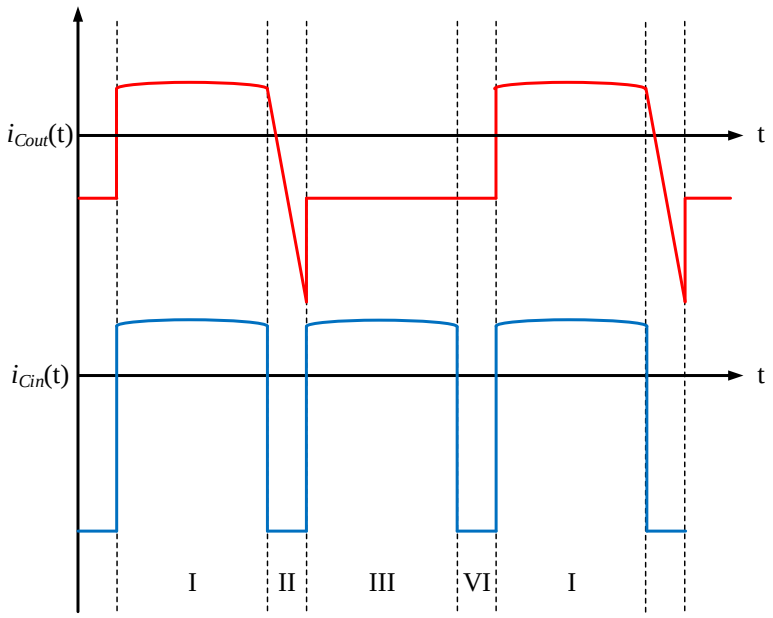

Figure 8.13. Current waveforms of ZVS operation

In order to study the actual size reduction that can be achieved by using interleaved topology. A 1-phase 100kW converter is developed at first. Table 8.1 shows the specifications of the designed 1-phase converter. The operating frequency of the designed converter is 100kHz. Table 8.2 shows the input and output capacitors that are used in the prototype. The capacitance of each input and output capacitor are 12uF and 5uF, respectively. According to Table 8.3, when we assume the voltage ripple of both input and output of the converter is less than 5%, then the minimum capacitance values of the input and output capacitor banks are 30uF and 40uF. On the other hand, the root mean square (RMS) values of the current flowing through input and output capacitors are 165A and 205.5A. As a result, in order to make sure the capacitor banks have enough current capability, the actual designed capacitance values of the input and output capacitors in the circuit are 120uF and 70uF, respectively. This means the capacitance in the circuit is over-designed. Therefore, the size of input and output capacitors are not optimized. A component

volume breakdown shows that the input capacitor and output capacitor take more than 30% of the total component size, as shown in Figure 8.14.

Table 8.2. Parameters of the Analyzed 1-Phase 100kW Converter

	Symbols	Values
Power Rating	P_{out}	100 kW
Input Voltage	V_{in}	300 V
Output Voltage	V_{out}	600 V
Resonant Capacitance	C_r	7.2 uF
Resonant Inductance	L_r	350 nH
Switching Frequency	f_s	100 kHz
Input Capacitor	C_{in}	120 uF
Output Capacitor	C_{out}	70 uF

Table 8.3. Capacitors Used In The 1-Phase Prototype

	Part#	Capacitance
Input Capacitor	B32674D3126	12uF
Output Capacitor	B32674D6505	5uF

Table 8.4. Capacitance and Current Capability Requirements of Input and Output Capacitors (Assume Voltage Ripple <5%)

	Current Capability Requirement	Capacitance Requirement
Input Capacitor	165 A	30 uF
Output Capacitor	205.5 A	40 uF

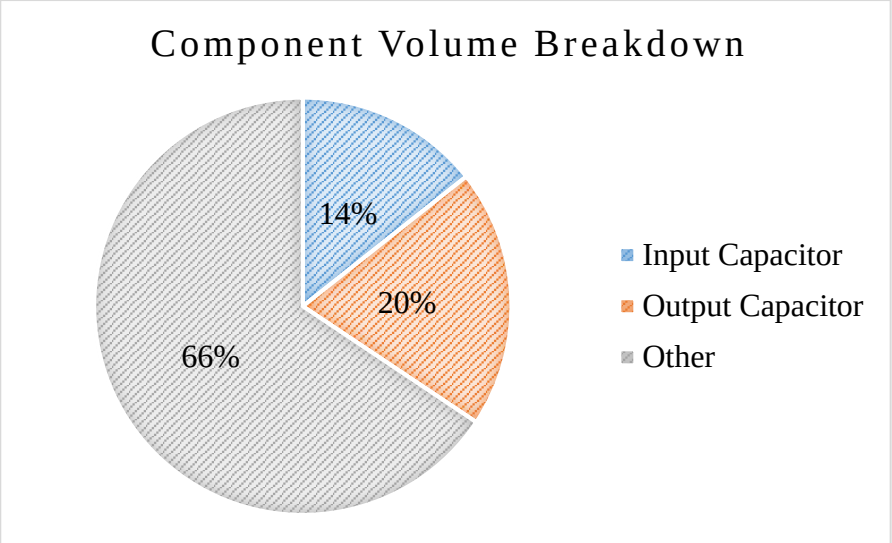

Figure 8.14. Capacitors take 34% of the total component volume

8.3. Interleaved Topology and Comparison

Interleaved concept provides a good solution to make use of the passive components in a more rational manner. In order to have a reasonable comparison between 1-phase converter, 2-phase interleaved converter and 3-phase interleaved converter, the values of resonant inductance and resonant capacitance frequency are always kept the same. This means switching frequency is always the same in the following analysis.

8.3.1. Current Stress of Passive Components

In the interleaved operation, the control signals of the converter in different phases shift 180-degree and 120-degree from each other in 2-phase interleaved connection and 3-phase interleaved connection, respectively. Figure 8.15 shows the 3-Phase interleaved circuit connection of the presented circuit. Figure 8.16 and Figure 8.17 shows the normalized capacitor RMS current when the converter operates at ZCS mode. Similarly, Figure 8.18 and Figure 8.19 shows the normalized current stress of the input and output capacitors when the converter operates at ZVS operation mode. According to these two figures, we can tell that the RMS values of the currents flowing through input capacitor bank and output capacitor bank are significantly reduced with the

interleaved operation. Especially when the converter operates at ZCS mode, the current stress of the input and output capacitors can be reduced by more than ten times. This means the size of the input capacitor and the output capacitor can be significantly reduced with interleaved operation.

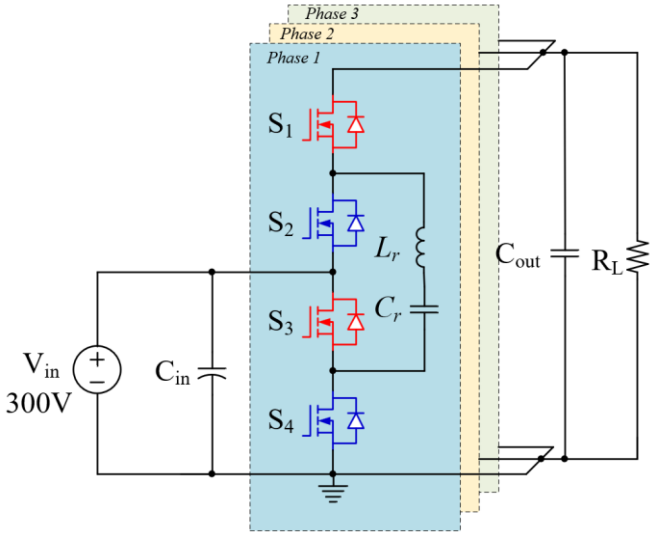

Figure 8.15. 3-Phase interleaved connection of the presented converter

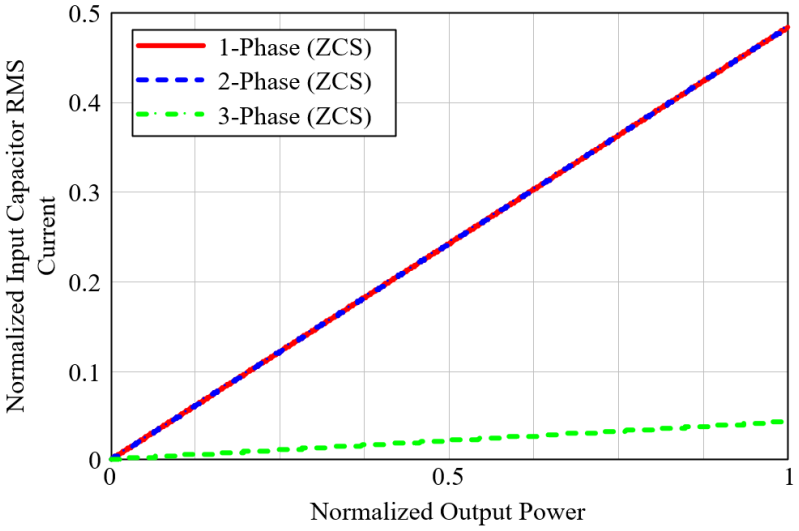

Figure 8.16. Input capacitor RMS current

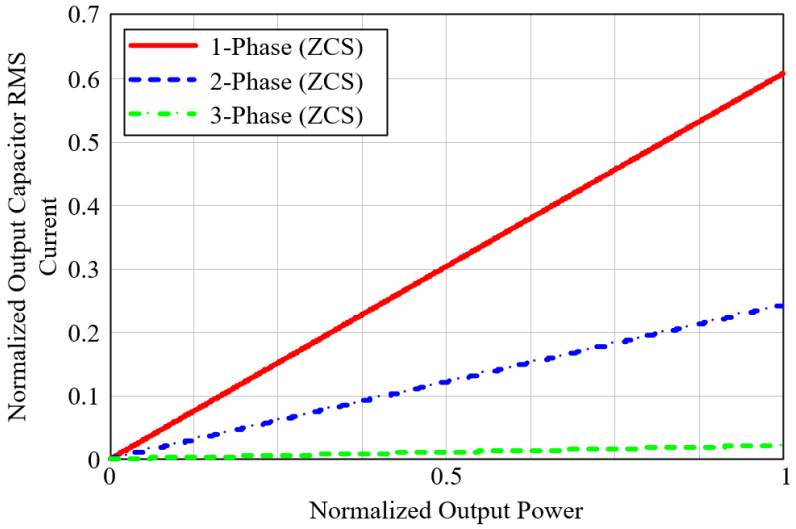

Figure 8.17. Output capacitor RMS current

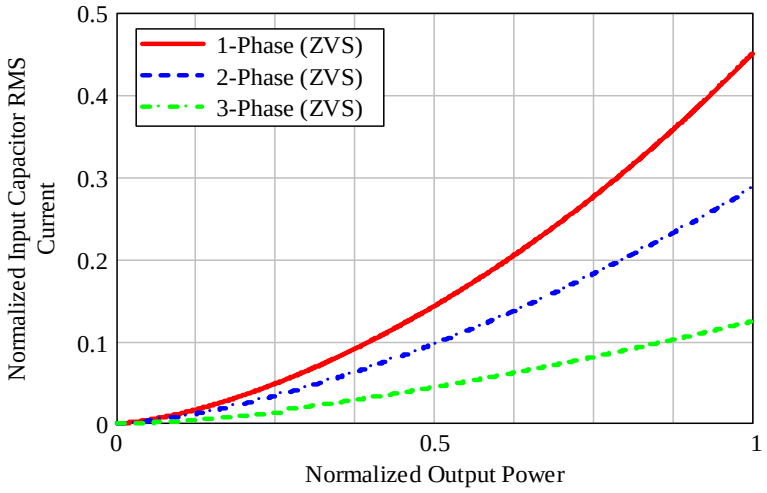

Figure 8.18. Input capacitor RMS current

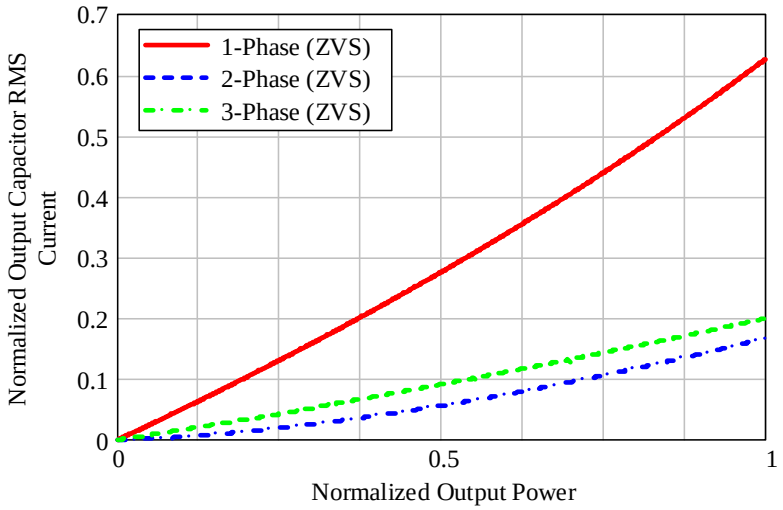

Figure 8.19. Output capacitor RMS current

8.3.2. Estimated Component Size and Inductor Size Reduction

The inductance of the resonant inductor can be calculated using Eq.8.6. And the relationship between the saturation current and the saturation flux density can be found in Eq.8.8. Based on Eq.8.8, the saturation current of a inductor can be represented by the mean length of the magnetic path l_m, length of the air gap l_g, inductor turn number N, permeability μ_0, relative permeability μ and the saturation flux density, as shown in Eq.8.8. Thus, Eq.8.9 has been derived from Eq.8.6 and Eq.8.8. According to Eq.8.9, resonant inductance value and saturation current value of an inductor are proportional to the core's cross-section area and magnetic path length. In our case, the peak current of the inductors will become 1/N times in an interleaved N-phase converter, this means that the size of magnetic component size can also be significantly reduced in interleaved structure (e.g. ~9 times in a 3-phase converter). It's worth mentioning that a similar inductor volume reduction analysis is also proposed in [184]. At last, an estimated component size reduction of 64.5% can be achieved by using 3-phase interleaved operation, as shown in Figure 8.20.

$$L = \frac{N^2 A_c}{\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}} \quad \text{(Eq. 8.6)}$$

$$H = N * I_{sat} = (\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}) B_{sat} \quad \text{(Eq. 8.7)}$$

$$I_{sat} = \frac{(\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}) B_{sat}}{N} \quad \text{(Eq. 8.8)}$$

$$L I_{sat}^2 = B_{sat}^2 A_c (\frac{l_g}{\mu_0} + \frac{l_m}{\mu * \mu_0}) \quad \text{(Eq. 8.9)}$$

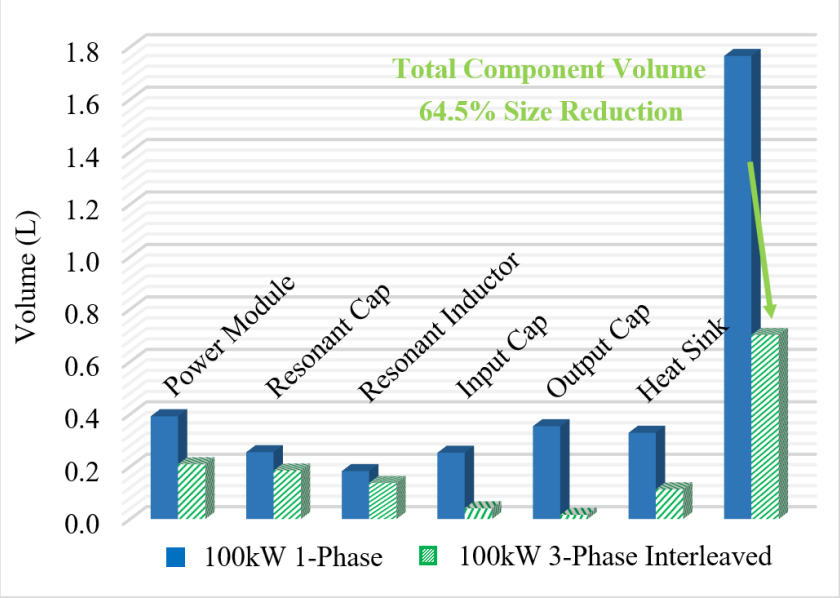

Figure 8.20. 64.5% component size reduction can be achieved by using 3-phase interleaved topology

8.4. Simulation Results and Prototype

Simulation has been performed to validate the theoretical analysis on the current stress of passive components in the circuit. In ZCS mode, the 3-phase interleaved operation allows the current stress of input capacitor drop from 163A to 14.25A, which is 11.5 times lower. And the current stress of output capacitor is reduced by 28 times, from 202A to 7.3A, as shown in Figure 8.21 and Figure 8.22. On the other hand, according to Figure 8.23 and Figure 8.24, the current

stress of input capacitor is 4.7 times lower in the 3-phase interleaved converter when it operates at ZVS mode, which is 25.4A. In comparison, the current stress of input capacitor in 1-phase converter is 120.6A. In addition, the current stress values of output capacitors in 1-phase converter and 3-phase interleaved converter are 191.5A and 38.4A, respectively. We can tell that the current stress of output capacitors is reduced by five times with the interleaved operation. The simulated current stress values of input and output capacitors match the theoretical analysis. And according to the simulation, one can tell that the interleaved operation can better mitigate the high current stress issue on input and output capacitors when ZCS operation mode is enabled, which also suggest that the ZCS operation is more suitable for interleaved operation. A 1-phase 100kW converter prototype based on Rohm SiC power module BSM600D12P3G001 is designed to verify the theoretical analysis of the capacitor current, as shown in Figure 8.25. The 1-phase converter achieves 45kW/L density. Furthermore, a 3-phase high power density converter based on Infineon CoolSiC FF11MR12W1M1_B11 is proposed. Both single side cooling and double side cooling method are considered. With the double side cooling layout, the 3-phase converter achieves 115kW/L power density. Compared with the 1-phase converter, the converter volume reduction is 60%. The magnetic material used to build the inductor is Hitachi ML29D, which is very suitable for the applications range from 50kHz~250kHz.

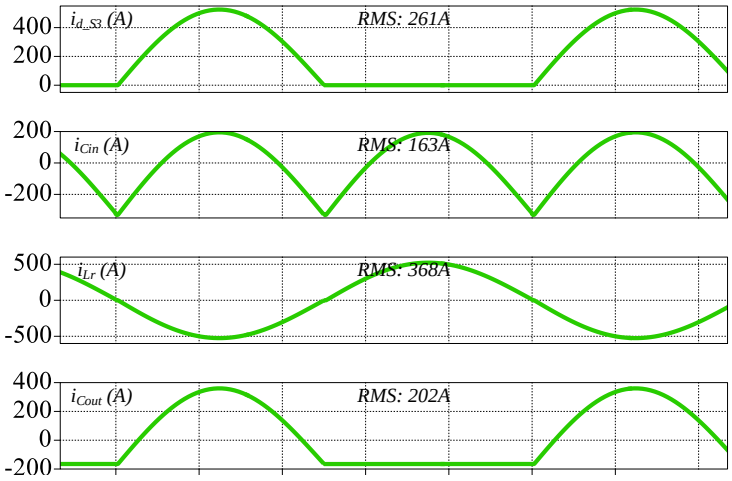

Figure 8.21. Current waveforms of 1-Phase converter

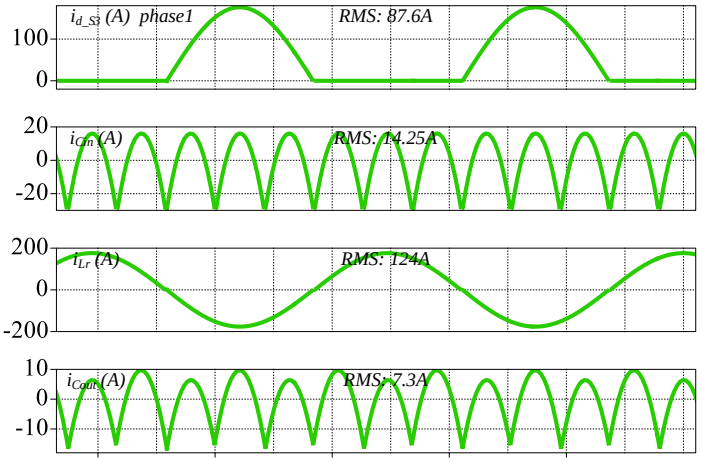

Figure 8.22. Current waveforms of 3-Phase converter

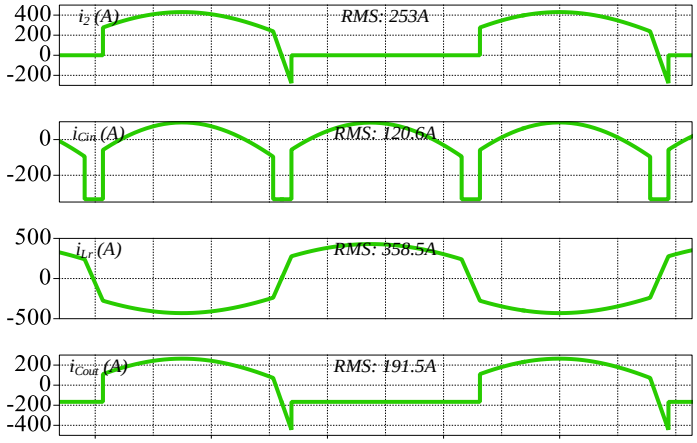

Figure 8.23. Current waveforms of 1-Phase converter

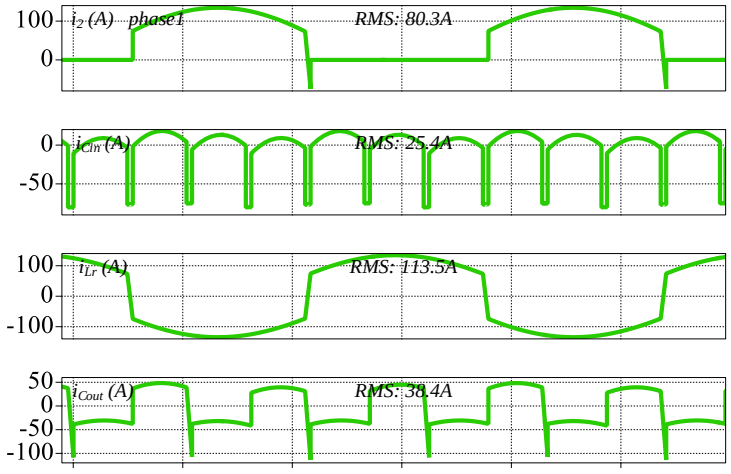

Figure 8.24. Current waveforms of 3-Phase converter

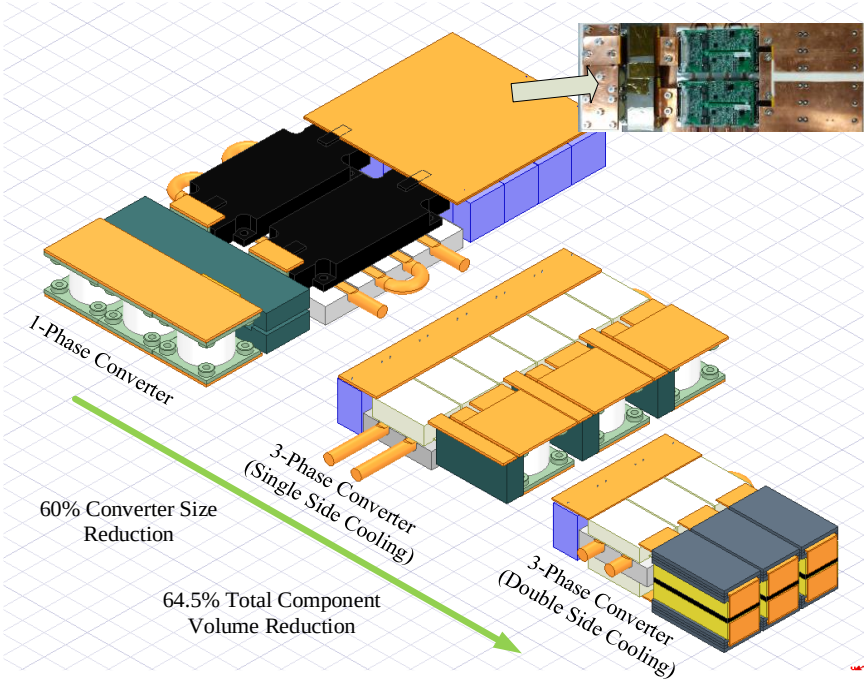

Figure 8.25. 100kW 1-phase converter and 3-phase converter under developing

8.5. Conclusion and Future Work

This work proposed a new topology evaluation method to evaluate different converter topologies. The study shows that the presented one-cell switched tank converter has the advantage of lower semiconductor index value and lower mechanical layout difficulty over the conventional boost converter and the 3-level FCML converter. Furthermore, this work evaluates the potential

of utilizing interleaving concept to optimize the volume of passive components, thus to achieve size reduction of the 100kW one-cell STC that can be used in electric vehicles. With the interleaved operation, the capacitor over-design issue led by high current stress can be alleviated. The volume of the input capacitor, output capacitor can be reduced by 6 times and 17 times, respectively. An estimated 60% size reduction based on 1-phase converter and a density of 115kW/L can be achieved on a 3-phase one-cell STC with interleaved operation.

9. CONCLUSION AND RECOMMENDATION

9.1. Contributions

This dissertation presents a series of wide bandgap semiconductors based high-power-density and high-efficiency DC-DC converters for data center, telecommunication, electric vehicle and MVDC applications. The contributions of this dissertation are as follows;

For the MVDC application, a modular multilevel converter with zero-current switching capability is proposed. By utilizing the parasitic inductance existed in the converter system, the magnetic components needed in the system can be minimized. Thus, high-density converter design can be achieved. In addition, by using different control method, the converter can achieve different voltage conversion ratios.

For the data center application, this dissertation proposed a switched-tank converter with zero-current switching capability. With the in-depth circuit analysis and proposed design method, the proposed converter can achieve 98.55% peak efficiency. Furthermore, the issues that may led by component tolerance during the mass production have been analyzed. And an adaptive control method is proposed to make sure the converter can operate at optimal condition. As a result, the peak efficiency of the presented switched-tank converter has been improved, which is 98.71%. Also, the converter's full load efficiency has been improved by 0.48%. This dissertation also proposed a switched-capacitor converter that is capable of zero-voltage switching. The proposed phase-shift control method for the converter is demonstrated. Furthermore, analytical analysis of the converter shows the design methodology to achieve high-density and high-efficiency design. At last, an analytical comparison between the switched-capacitor converter with ZVS operation and switched-capacitor converter with ZCS operation has been performed. The comparison study

shows that the converter with ZVS operation can achieve higher density and efficiency with proper design.

For the telecommunication application, although the removal of isolation stage shows great benefit in terms of power density and efficiency, the isolation is a mandatory requirement in telecom application. Therefore, a composite multilevel converter based on switched-capacitor concept is proposed in this this dissertation.

Finally, a 100kW switched-tank converter has been developed to validate that the high power- density and high-efficiency can be achieved by using the switched-capacitor concept. The successful development of this converter shows that the hybrid switched-capacitor converter is not only suitable for low-power application but also suitable for high-power application.

9.2. Recommendations for Future Works

Here are some recommendations for future works. For the proposed adaptive control method, a zero-current detection method could be developed to support the adaptive control method. Furthermore, how to regulate the voltage could be one of the meaningful topics for future work. For the switched-capacitor converter with ZVS operation, input/output voltage sensing circuits and closed-loop controller could be developed to ensure the proper operation of the converter.

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