BIT OPTIMIZED RECONFIGURABLE NETWORK (BORN): A NEW PATHWAY TOWARDS IMPLEMENTING A FULLY INTEGRATED BAND-SWITCHABLE CMOS POWER AMPLIFIER

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Seyyed Babak Hamidi Perchehkolaei

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Title

Bit Optimized Reconfigurable Network (BORN): A New Pathway Towards Implementing a Fully Integrated Band-Switchable CMOS Power Amplifier

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The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

DOCTOR OF PHILOSOPHY

SUPERVISORY COMMITTEE:

Dr. Debasis Dawn
Chair

Dr. Benjamin Braaten
Co-Chair

Dr. Kalpana Katti

Dr. Ivan Lima

Dr. Saikat Sarkar

Approved:

07/13/2020
Date

Dr. Benjamin Braaten
Department Chair

ABSTRACT

The ultimate goal of the modern wireless communication industry is the full integration of digital, analog, and radio frequency (RF) functions. The most successful solution for such demands has been complementary metal oxide semiconductor (CMOS) technology, thanks to its cost-effective material and great versatility. Power amplifier (PA), the biggest bottleneck to integrate in a single-chip transceiver in wireless communications, significantly influences overall system performance. Recent advanced wireless communication systems demand a power amplifier that can simultaneously support different communication standards. A fully integrated single-chip tunable CMOS power amplifier is the best solution in terms of the cost and level of integration with other functional blocks of an RF transceiver.

This work, for the first time, proposes a fully integrated band-switchable RF power amplifier by using a novel approach towards switching the matching networks. In this approach, which is called **B**it **O**ptimized **R**econfigurable **N**etwork (BORN), two matching networks which can be controlled by digital bits will provide three operating frequency bands for the power amplifier. In order to implementing the proposed BORN PA, a robust high-power RF switch is presented by using resistive body floating technique and 6-terminal triple-well NMOS.

The proposed BORN PA delivers measured saturated output power (Psat) of 21.25/22.25/ 23.0dBm at 960MHz/1317MHz/1750MHz, respectively. Moreover, the proposed BORN PA provides respective 3-dB bandwidth of 400MHz/425MHz/550MHz, output 1-dB compression point (P1dB) of 19.5dBm/20.0dBm/21.0dBm, and power-added efficiency (PAE) of 9/11/13% at three targeted frequency bands, respectively. The promising results show that the proposed BORN PA can be a practical solution for RF multiband applications in terms of the cost and level of integration with other functional blocks of an RF transceiver.

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DEDICATION

To My Beloved Parents,

Behnaz & Mehdi

&

My Amazing Siblings,

Bahareh & Behnam

&

My Wonderful In-Laws,

Maedeh & Babak

&

My Adorable Niece and Nephew,

Liana & Arta

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LIST OF ABBREVIATIONS

3GPP	Third-Generation Partnership Project
5G	The fifth generation
BW	Bandwidth
CG	Common Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CS	Common Source
DC	Direct Current
DNW	Deep N-well
DRC	Design Rule Checking
FDD	Frequency-Division Duplexing
FET	Field-Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSM	Global System for Mobile Communications
HEMT	High-Electron-Mobility Transistor
IC	Integrated Circuit
IMN	Input Matching Network
InGaAs	Indium-Gallium Arsenide
ISMN	Interstage Matching Network
Kf	Stability Factor
LC	Inductor and Capacitor
LTE	Long Term Evolution
LVS	Layout versus Schematic
mm-Wave	Millimeter-Wave

NMOS ..... N-channel Metal-Oxide-Semiconductor

NR ..... New Radio

OMN ..... Output Matching Network

P1dB ..... 1 dB compression point

PA ..... Power Amplifier

PAE ..... Power-Added Efficiency

PCB ..... Printed Circuit Board

Psat ..... Saturated Output Power

RF ..... Radio Frequency

RFIC ..... Radio Frequency Integrated Circuit

Rx ..... Receiver

SW ..... Switch

Tx ..... Transmitter

VCO ..... Voltage Control Oscillator

WLAN ..... Wireless Local Area Network

CHAPTER 1. INTRODUCTION

1.1. Motivation

The concept of wireless communications has tremendously evolved and become an integral part of our everyday life, influencing the way people live and interact with one another. The largest leap in the domain of wireless information transfer started with the invention of the transistor in 1947, as this allowed research and development of portable devices and led to the launch of the first commercially automated cellular network 1G (the first generation), which later evolved into the currently widespread 4G technology and is paving the way to the 5G realm [1]. On the electronics side, mobile user devices have become increasingly powerful over the years. Users can now make high-quality calls, read emails, download music and watch live streaming video, all from a single highly-integrated mobile device. The development of integrated circuits (ICs) is a major reason that the cost of these devices is relatively low and affordable for the public, giving rise to an explosive growth of the mobile phone market in the last few decades.

Accordingly, the inevitable task and ultimate goal of the modern wireless communication industry is the full integration of digital, analog, and even radio frequency (RF) functions. To this end, the industry has devoted great effort to designing wireless terminals using a common semiconductor process that utilizes a single chip; thus, true single-chip radio is now within the grasp of manufacturers. To date, the most successful solution for such demands has been complementary metal oxide semiconductor (CMOS) technology, thanks to its cost-effective material and great versatility.

Since power amplifier (PA) is the most power hungry component in an RF transceiver, it is important to minimize the power consumption to extend battery life-time of portable devices. In addition, recent advanced wireless communication systems demand a power amplifier that can

simultaneously support different communication standards. Thus, multiband power amplifiers covering different frequency bands are desired, where the operating frequency can be selectable to achieve the highest communication data rate.

1.2. Radio Frequency (RF) Transceiver

A transceiver is a blend of a transmitter and a receiver in a single package. The main application of an RF transceiver is to make information in the form of data/voice/video to be transmitted and received over the wireless medium.

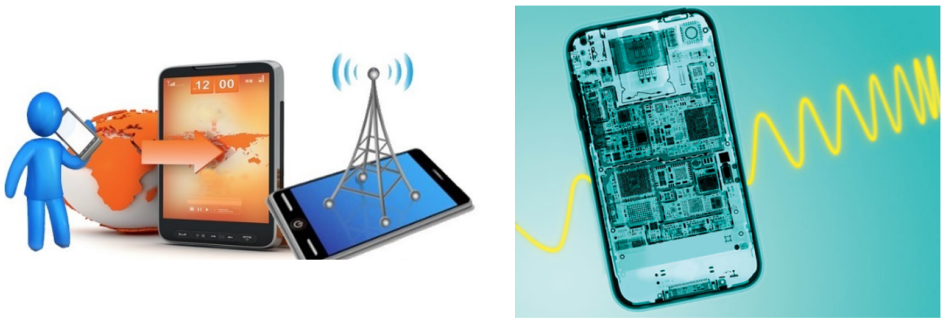


Figure 1.1. Modern wireless communication.

The RF front end (shown in Figure 1.2) is generally defined as everything between an antenna and a digital baseband system. Baseband is a low frequency signal. Data and information cannot be transmitted directly to the antenna. Moreover, a large antenna and also very high power level would be needed for low frequency. When the baseband signal is converted to high frequency by modulating the RF frequency, the antenna becomes small and power level becomes low. Thus, amplifier and oscillator are crucial in a transmission chain whatever standard is used. All transmitter and receiver front-ends are composed of various RF building blocks that carry out basic analog functions like frequency translation, frequency selection and power amplification.

An antenna provides an interface between a communication channel (e.g., free space) and a receiver front-end. The analog portion of the receiver chain takes an RF analog signal and

converts it into digital bit streams. In a receiver, it is required to bring the input signal to an acceptable level for processing with minimal noise to avoid degrading the quality of modulated data. A receiver requires a bandwidth selection filter and a low noise amplifier (LNA) to carefully select the right channel and get the signal at a detectable level. A down-converter mixer is used to translate the RF signal to intermediate frequency (IF). A local oscillator (LO) is a device that generates a reference signal to be used as one of the mixer inputs and serves for up- and down-conversion. The LO output is a large signal that drives the mixer and causes the generation of both fundamental frequency and various harmonics. An analog-to-digital converter (ADC) is a master component in modern wireless radios. It transforms an analog signal into digital words that can be used in baseband signal processing.

In a transmitter, digital I/Q signals are converted to an analog signal, then frequency-translated by an up-conversion mixer. The resulting RF signal is finally amplified by a power amplifier (PA) to the required power level before radiating through an antenna. A transmitter requires a matching circuit at the output of the power amplifier to allow the radiation of maximum power into the communication channel [2]-[3].

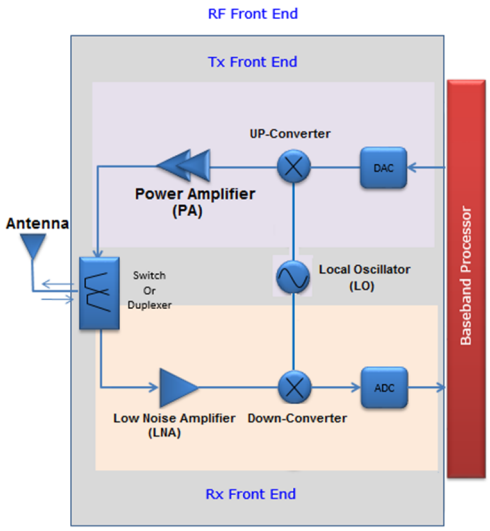


Figure 1.2. RF front-end.

1.2.1. Some Popular Examples of RF Transceiver Applications

- Mobile wireless communication including but not limited to mobile smart phones, tablets.
- Radio transmission, satellite communication, transmission/reception in wireless local area network (WLAN) via Wi-Fi, or long-term evolution (LTE) networks.
- Wireless health monitoring system in hospitals for patients
- Voice controlled home appliances such as fan speed control using RF Communication
- War field robot with night vision wireless camera
- RF controlled robotic vehicle in industries
- Wireless reckless driving detection
- Firefighting robotic vehicle
- Speed synchronization of multiple motors in industries
- Commercial and industrial uses of small unmanned air vehicles (UAV) such as package delivery, medical supply chains, mining, telecommunications, agriculture, commercial aerial photography, and air traffic reporting.

1.2.2. Global RF Transceiver Market Overview

Base on the design, the RF transceiver market is categorized into a single chip transceiver and a standalone chip transceiver. Out of these, the single chip transceiver category accounted or a larger revenue share in 2019. Single chip transceivers offer low power consumption and low voltage operations in wireless systems. Further, the single chip transceivers are increasingly used in the healthcare industry for wireless body area network (WBAN) and telemetry communication. The 4G cellular technology is poised to be replaced by 5G (the fifth generation) technology in the coming years. 5G wireless technology supports various frequency bands and can be used for cellular as well as Internet-of-Things (IoT) applications. With continuous technological advance-ments and growing demand for high-performance, area efficient transceivers, the advancement of

5G communication technology is expected to create huge opportunities for RF transceiver market players across the globe.

According to P&S Intelligence, the global RF transceiver market reached $10 Billion in 2019 and will exceed $18.5 billion by 2024 (shown in Figure 1.3), and half of that total will be for silicon-based amplifiers, by increasing demand for mobile devices and the rising adoption of the Internet-of-Things. Factors including 5G technology expansion, the massive adoption of smartphones, increasing penetration of IoT and automation, and growth of technology-intense industries such as manufacturing, telecommunication, automobile, aerospace, and defense are expected to boost RF transceiver market [4].

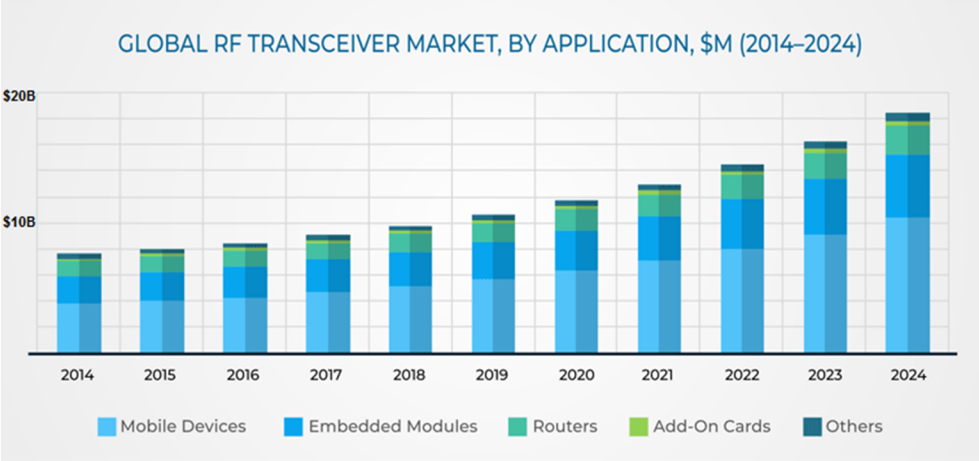


Figure 1.3. Global RF transceiver market [4].

1.3. RF Power Amplifier (PA)

Power amplifiers are among the most crucial functional blocks in a radio frequency (RF) frontend for reliable wireless communication. PAs amplify and boost the input signal to the required output power. The signal is amplified to make it sufficiently high for a transmitter to propagate it to the required distance to a receiver. An RF transmitter is composed of functional blocks, such as a digital-to-analog converter (DAC), an up-conversion mixer, an oscillator, and a

PA, as shown in Figure 1.4 [5]-[6]. Among all of these modules, the PA is the most vital block because its performance significantly affects the overall performance of the transmitter [7]-[9].

Figure 1.5 describes the basic block diagram of a power amplifier. The block diagram consists of two main stages, namely, driver and power stages. Both stages are biased with individual bias voltages. Different configurations are applied to the driver and power stages so that the PA operates properly [10]-[13]. Input and output matching networks are used to minimize the return losses to obtain a high gain and a high output power. However the interstage matching network is also required between the driver stage and the power stage.

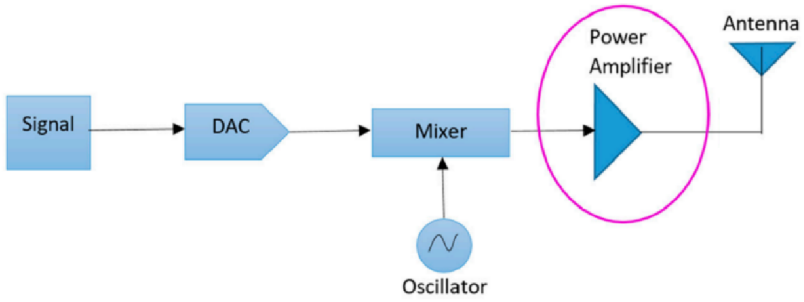


Figure 1.4. Block diagram of an RF transmitter [14].

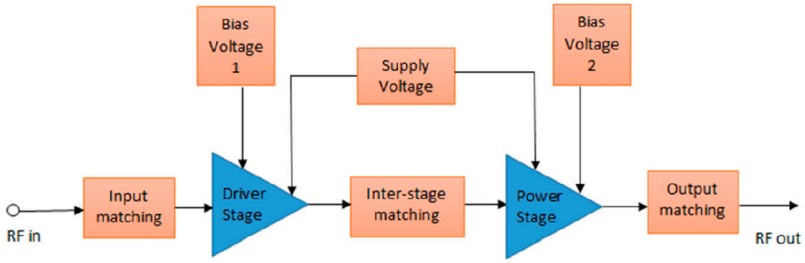


Figure 1.5. Block diagram of an RF power amplifier [10].

1.4. 5G New Radio (NR) Technology

The structure of the modern wireless network evolves rapidly, and maturing 4G networks paves the way to the next generation of communication (5G). Both indoor and outdoor wireless technologies are evolving very rapidly. 2G, 3G and 4G cellular wireless technologies have been

mass deployed throughout the world. 5G is used to designate fifth generation of mobile technologies. 5G is the next leap in the evolution of wireless communication which introduces many improvements to the existing telecommunications industry [15]. This emerging technology provides low latency, ultra-high-speed massive connectivity between devices with larger bandwidth possible. New 5G networks, which in the process, will unleash the greatest technological shifts in a generation. Indeed, experts predict this new tech will eventually replace almost every internet connection on earth. By 2022 alone there will be an estimated 29 billion devices hooked up to 5G, creating more than $1.5 trillion in market value for investors. That's why many legendary technology investors are calling it the #1 investment of the decade. Through a landmark 5G Economy study, it is found that 5G's full economic effect will likely be realized across the globe by 2035, supporting a wide range of industries and potentially enabling up to $13.2 trillion worth of goods and services, and the 5G value chain (including operators, content creators, application developers, and consumers) could alone support up to 22.3 million jobs.

1.4.1. 5G Technology Features and Advantages

The 5G technology makes use of all the existing cellular wireless technologies (2G, 3G and 4G), and provides following features to the users and providers of this technology.

- Interoperability will become feasible and easier
- Low battery power consumption.
- Better coverage and high data rates at the edge of cell.
- Multiple data transfer paths concurrently.
- More secure
- Better Quality of Service
- Ultimate download and upload speed

1.4.2. 5G Communications Frequency Bands and Operation Modes

The 3rd Generation Partnership Project (3GPP) is a standard organization which develops protocols for mobile telephony. The frequencies used by each nation are gradually becoming clearer for full-scale deployment of 5G mobile communications, and can be divided broadly into two groups. First is Frequency Range 1 (FR1) defined by 3GPP, from 410 MHz to 7125 MHz and is described as the sub-6 GHz band. It is used by the LTE/LTE-Advanced and WLAN technologies and has been extended in recent years. It has advantage of using the RF resources validated previously for 3G and 4G LTE. One disadvantage is that an orderly wide frequency band cannot be secured because most frequencies are already in use [16].

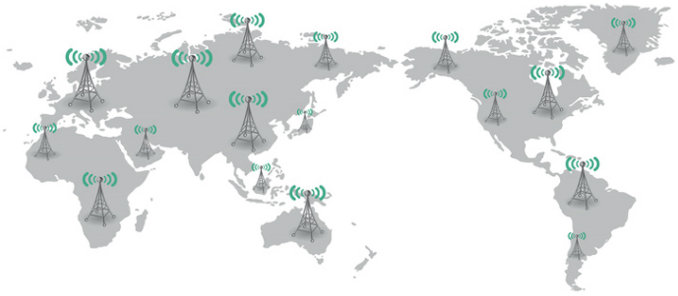


Figure 1.6. World 5G mobile communications.

For the second band, 3GPP defines the frequencies between 24250 MHz and 52600 MHz, called the millimeter band (mmWave), where a wideband can be assured because this frequency band is hardly used, offering the advantage of easy support for high-speed and large-capacity data transmissions. One disadvantage is the large over-the-air signal attenuation, presenting a number of technical issues that must be cleared due to the lack of actual usage by mobile operators [17].

As well as two frequency bands, there are also two operation modes: 1) The Non-Standalone (NSA) mode using a combination of a New Radio (NR) technology for 5G and LTE/LTE-A, and 2) The Standalone (SA) mode using a unique 5G NR technology where data is sent and received using control between base stations and mobile terminals.

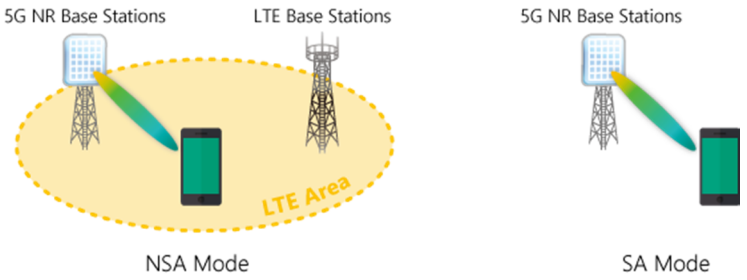


Figure 1.7. Non-standalone (NSA) and standalone (SA) operation modes.

On December 2017, in Lisbon, the 3GPP Radio Access Network (RAN) Plenary Meeting successfully approved first implementable 5G NR specification. The completion of the first 5G NR standard enabled the full-scale development of 5G NR for large-scale trials and commercial deployments as early as in 2019. This first specification was completed as part of 3GPP Release15. As per 3GPP release 15, the *frequency bands for 5G NR* have been designated and Technical Specification (TS 38.104 section 5.2) provides the list of bands in which 5G NR can operate. The specification defines the frequency bands as FR1 and FR2 shown in Table 1.1 and Table 1.3, respectively. Note that the NR bands are defined with prefix of "n". When the NR band is overlapping with the 4G LTE band, they share the same band number [18].

Table 1.1. FR1 frequency division duplex (FDD) frequency bands for 5G-NR

5G NR Band	Uplink Frequency	Downlink Frequency	Bandwidth
n1	1920-1989MHz	2110-2170MHz	60MHz
n2	1850-1910MHz	1930-1990MHz	60MHz
n3	1710-1785MHz	1805-1880MHz	75MHz
n5	824-849MHz	869-894MHz	25MHz
n7	2500-2670MHz	2620-2690MHz	70MHz
n8	880-915MHz	925-960MHz	35MHz
n20	832-862MHz	791-821MHz	30MHz
n28	703-748MHz	758-803MHz	45MHz
n66	1710-1780MHz	2110-2200MHz	90MHz
n70	1695-1710MHz	1995-2020MHz	15/25MHz
n71	663-698MHz	617-652MHz	35MHz
n74	1427-1470MHz	1475-1518MHz	43MHz

Table 1.2. FR1 supplementary downlink and uplink bands for 5G-NR

5G NR Band	Uplink Frequency	Downlink Frequency	Bandwidth
n75	-	1432-1517MHz	85MHz
n76	-	1427-1432MHz	5MHz
n80	1710-1785MHz	-	75MHz
n81	880-915MHz	-	35MHz
n82	832-862MHz	-	30MHz
n83	703-748MHz	-	45MHz
n84	1920-1980MHz	-	60MHz

Table 1.3. 5G-NR frequency bands in FR2

5G NR Band	Band Alias	Uplink Frequency	Downlink Frequency	Bandwidth
n257	28 GHz	26.5-29.5 GHz	26.5-29.5 GHz	3.0 GHz
n258	26 GHz	24.25-27.5 GHz	24.25-27.5 GHz	3.25 GHz
n260	39 GHz	37-40 GHz	37-40 GHz	3.0 GHz

Because the main specification for high-speed wireless communication for mobile phone and data terminals is the frequency band, future mobile terminals will be expected to function in all the required standard frequency bands. In frequency range of 700MHz to 1000MHz and 1400 MHz to 2100MHz, twenty five different frequency bands have already been defined by 4G LTE standard (as shown in Figure 1.8), and eighteen individual frequency bands have been defined by 5G NR (as listed in Table 1.1 and Table 1.2) in frequency-division duplexing (FDD) mode.

Furthermore, quad-band GSM at 850/900/1800/1900 MHz are the cellular frequencies designated for the operation of GSM mobile phones.

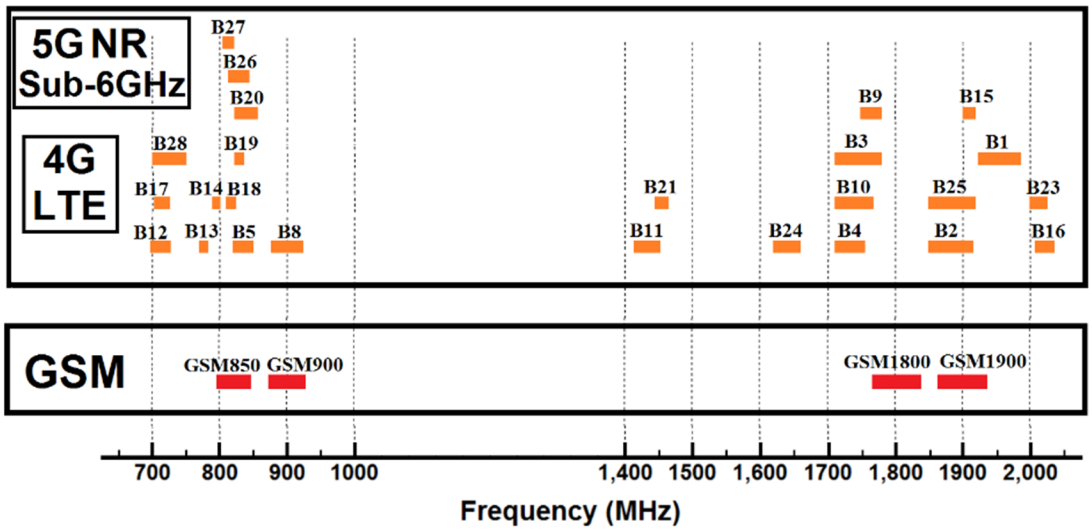


Figure 1.8. 4G LTE and 5G NR frequency bands in FDD mode, and GSM standards.

1.4.3. LoRa and ISM Bands

LoRa (**Lo**ng **Ra**nge) is a low-power wide-area network (LPWAN) technology. LoRa for Internet-of-Things (IoT) type devices uses license-free sub-gigahertz radio frequency bands like 433 MHz (Asia), 868 MHz (Europe), 915 MHz (North and South America). LoRa enables long-range transmissions (more than 10 miles in rural areas) with low power consumption [19].

The ISM radio bands are portions of the radio spectrum reserved internationally for industrial, scientific and medical (ISM) purposes other than telecommunications. The ISM band covering 902.2-927.8 MHz is used in North and South America. In recent years the fastest-growing use of these bands has been for short-range, low power wireless communications systems with low power transceivers, since these bands are often approved for such devices which can be used without a government license. Bluetooth devices, near field communication (NFC) devices, garage door openers, baby monitors and wireless computer networks (WiFi) may all use the ISM frequencies.

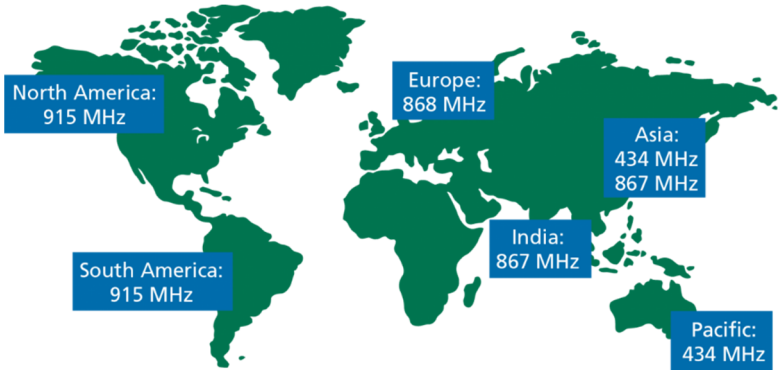


Figure 1.9. LoRa and ISM frequency bands.

1.5. Semiconductor Material Types

Gallium Arsenide (GaAs) and Gallium Nitride (GaN) are compound semiconductors. Known as III-V semiconductors, they fall into categories of elements with either three or five valence electrons. Boron, aluminum, gallium, indium, and thallium are Category III elements. Nitrogen, phosphorus, arsenic, antimony, and bismuth are Category V elements. Combining a Category III element with a Category V element produces a covalent bond with eight electrons, yielding a unique semiconductor. Such semiconductors have higher electron mobility than Silicon, hence they are more useful at higher frequencies [20]-[21].

As shown in Table 4, carrier velocity and mobility are higher for electrons than holes. The difference between electrons and holes is much larger in III-V devices (e.g. GaAs) than silicon devices [22], but the carrier velocity and mobility of electrons are lower for silicon devices. Due to the large difference in complementary III-V devices, and the lower carrier velocity and mobility for holes in GaAs, silicon technologies are better suited when it comes to high speed complementary logic.

Another important parameter is thermal conductivity as listed in Table 1.4. If the parameter is low, it implies issues to dissipate heating. Considering a billion-transistor processor in silicon, a good thermal conductivity of the substrate material is necessary in order to make sure that the

chip is not overheated. The comparable integration level is typically limited to approximately 1000 transistors in GaAs, and 50 transistors in GaN [22].

A parameter not beneficial in the silicon case is the substrate resistivity, which is relatively low compared to the III-V semiconductors, and degrades the quality factor of integrated passives. A common argument to use silicon-based technologies such as complimentary metal-oxide-semiconductor field effect transistor (CMOS) is cost, and the relative speed performance between electron and hole carriers makes silicon a preferable choice. Moreover in silicon-based process, the PA can be integrated with the CMOS transceiver. In other words, CMOS processes can use larger wafers, make CMOS processes favorable in mass fabrication. Thus, a major benefit of using CMOS PAs is the possibility of full integration [23].

Table 1.4. Comparison of silicon-based technology with III-V semiconductors

	Silicon	**InGaAs**	**GaAs**	**GaN**
Electron mobility at 300K [$cm^2/V.s$]	1500	10000	8500	2000
Hole mobility at 300K [$cm^2/V.s$]	450	250	400	400
Peak electron velocity [$10^7 cm/s$]	1.0	2.7	2.0	2.1
Bandgap [eV]	1.1	0.75	1.42	3.49
Thermal conductivity [W/(cm.K)]	1.5	1.4	0.5	1.5
Substrate resistivity [Ω.cm]	20	>1000	>1000	>1000
Number of transistors in IC	>1 billions	<500	<1000	<50
Costs	low	Very high	high	Very high

Even though wireless transceivers can be fully implemented using III-V group semiconductors, the low level of integration and small digital capabilities of these technologies leads to a high price to functionality ratio, hence III-V-based technologies are not suitable for portable low power cells [24]. CMOS, on the other hand, is scalable and provides a high level of

integration for both analog and digital circuits at a reasonable (compared to that of III-V group semiconductors) price [25]-[26]. Due to low breakdown voltage, CMOS is not suitable for very high power applications, but is perfect for low and medium power transceiver blocks, including low/medium power RF PAs.

To replace expensive III-V processes with the lower cost Si-based technologies such as CMOS, careful design methodologies should be developed not only by proposing novel circuit design techniques, but also by accurate understanding of device physics to overcome performance limitation. It is widely known that the RF PA is the most power-hungry component in radio transceivers and is also one of the most critical blocks in radio front-end applications. Hence, research in this area will drive overall 5G network costs down while achieving improved energy efficiency [27]. Pushing mobile devices to lower powers is useful from a design perspective as non-PA components (digital controllers, RF transceiver blocks, switches, etc.) can readily be integrated with the PA in a single chip [28]-[30]. As a result, agile CMOS RF transceiver ICs are dominating low power device market [31].

The CMOS power amplifier is a promising solution for modern wireless devices to satisfy the demand of a low-power, low-cost design [32]-[33]. Over the years, CMOS PA has been widely used in various wireless communication applications, including home automation, Radio Frequency Identification (RFID), industrial consumer electronics, TV transmissions, cell phones, medical ultrasonic applications, and ultrasonic images [34]-[36]. Silicon is much less expensive, more reliable and has a longer lifespan.

1.6. Literature Survey on Multi-Band Power Amplifier

The explosively growing demands on higher data rates in mobile communications is pushing a quick development of standards like 4G LTE and 5G NR. The use of multi-band

approach, where the frequency bands can be selectable to achieve the highest communication data rate, is therefore highly desired to reduce transceiver complexity and cost.

Research activities are in progress to develop multi-band power amplifier covering several frequency bands using a reduced number of PA blocks. A multi-band CMOS power amplifier by using a resistive feedback and a tunable capacitor array in [37], and a compact CMOS dual-band power amplifier by using tunable differential inductors both in the RF choke and the matching circuit in [38] have been presented. However an off-chip input matching network is used in both studies. Reference [39] utilizes two different power amplifiers for low and high frequency bands, and [40] uses off-chip matching network, and commercial components. Moreover in many studies, special fabrication processes, such as GaAs pseudomorphic high electron mobility transistor (PHEMT) in [41], high power GaAs heterojunction bipolar transistor (HBT) on printed circuit board (PCB) in [42]-[43], 10W Gallium Nitride (GaN) HEMT in [44]-[45], tunable transmission line in [46], PIN diode switches in [46]-[47], RF-MEMS (Micro-Electro-Mechanical-System) switches in [48]-[49], and barium-strontium-titanate (BST) varactors in [50] are required in order to design a multi-band tunable PA which are not suitable for implementing a fully integrated single-chip power amplifier in terms of the cost and level of integration with other functional blocks of a transceiver.

1.7. Proposed Work and its Significance

Designing modern wireless communication systems has been focused toward reduced complexity and power consumption along with increased data rate. Hence, it has raised the demand for radio-frequency integrated circuits (RFICs) handling multiple frequency bands at a low cost. The use of multi-band approach is therefore highly desired to reduce transceiver complexity and cost. Because the main specification for high-speed wireless communication for mobile phone and

data terminals is the frequency band, future mobile terminals will be expected to function in all required standard frequency bands. Power amplifier (PA), the biggest bottleneck to achieve a single-chip transceiver, significantly influences system performance in wireless communications. Depending on the number of bands designed in a device, various numbers of transceiver blocks (mixer, local oscillator, low-noise amplifier, analog-to-digital converter, duplexer, and power amplifier) are required in a system. Traditionally, a multiband RF power amplifier has been implemented by bringing together several PAs. Figure 1.10 (a) shows conventional multi-band PA scheme which is directly assembled by several single-band PAs in a single chip. Each path covers a narrow range of operating frequency.

As much as 60~70% of a smartphone's battery usage can go to the power amplifier, power amplifiers use transistors that operate in two basic modes: standby and output. If the cellphone is not actively being used, the amplifier stays in standby and uses less power. When the phone transmits data, the power amplifier switches from standby mode to a high-power mode. In this condition, the problem is that big spikes in power can cause signal distortion and damages to internal circuits. To prevent this problem, existing technologies set standby power at a higher level, thereby reducing the size of any sudden jumps. Figure 1.10 (b) shows the targeted architecture for multi-band transmitters, which consists of multiple/multi-band antenna, a multi-band duplexer, and a multi-band power amplifier. In this approach, only one multi-band PA covers multiple standards. In order to have a multi-band PA, a fully integrated single-chip tunable CMOS power amplifier is the best solution in terms of the cost and level of integration with other functional blocks.

In this research, a fully-integrated, single-chip, band-switchable CMOS power amplifier is being proposed, which can cover the frequency standards for 4G LTE and 5G NR shown in Figure

1.8 and Table 1, by using only one band-switchable PA (instead of three in traditional approach). As a result, the proposed architecture can reduce the power consumption of the today's smartphones by one-third, in other words, it can increase the battery life of a smartphone by three times.

A fully-integrated CMOS RF transceiver will result in a low production cost, a low power consumption, a better noise immunity, and the possibility of using digital signal processing (DSP) to improve RF performance.

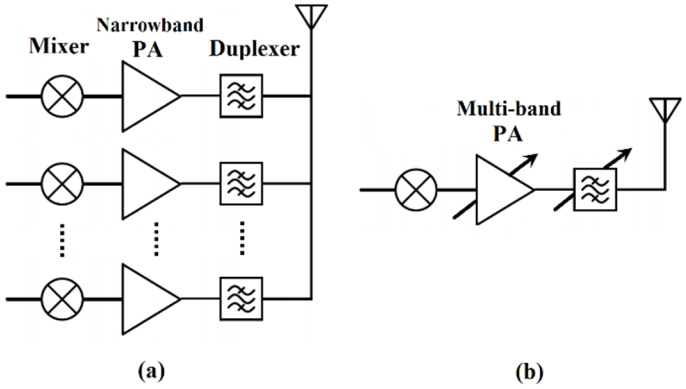


Figure 1.10. Architecture of (a) conventional, and (b) modern multi-band RF power amplifier.

CHAPTER 2. DESIGN AND IMPLEMENTATION OF A FULLY INTEGRATED TRIPLE-MODE TUNABLE POWER AMPLIFIER IN 130nm CMOS PROCESS

2.1. Design of Power Amplifier

A power amplifier is the key component in the design of a transmitter to use in wireless communication systems. PAs are characterized for being the most power consuming part of a transmitter, making the decision for an architecture and critical to the fulfillment of the system requirements.

2.1.1. Performance Metrics of a Power Amplifier

This Section introduces the most important characteristics of an RF power amplifier such as output power, gain, efficiency, linearity, stability, and other specifications. Inevitable trade-offs exist among these factors, and these trade-offs make PA design challenging, particularly, at CMOS downscaling.

2.1.1.1. Output Power

The output power is defined as the active power delivered to the load, i.e. the antenna, at the fundamental frequency [51]. Output power is the most important design aspect of a PA. In one sense, if the PA generates low output power, it loses its identity, making it hard to define.

To generate output power, the energy supply in a device should exceed the required output power because some power dissipates as heat. When the supply voltage has a constant value, the amount of current is critical in obtaining the output power. The output power is proportional to the efficiency of the PA and therefore, determines the performance of the PA.

In RF applications, the power level, usually defined as dBm, has a decibel value on a reference of 1mW (0 dBm), and expressed by Equation (2.1) as follows:

$$Pout = \frac{V_{out}^{2}}{2R_L} \tag{2.1}$$

where V_{out} is the output voltage, and R_L is the resistance load.

2.1.1.2. Gain

Power gain (G) is the ratio of the output and input powers, as expressed in Equation (2.2). This parameter describes how well a power amplifier can deliver a significantly higher power signal to a load compared to the input power [51]. The gain indicates the extent of the increase in the amplitude of a signal, usually expressed in dB.

$$G = 10\log(\frac{P_{out}}{P_{in}}) \tag{2.2}$$

where P_{out} is the output power, and P_{in} is the input power.

2.1.1.3. Power Added Efficiency

An important measure of a PA is the efficiency as it directly affects talk-time in handheld devices and has an impact on electricity bill in base stations.

When considering the input power, P_{in}, needed to drive the amplifier chain, an efficiency metric can be defined as Power-Added Efficiency (PAE). PAE is defined as the output power, P_{out}, gained subtracted by the input power and then divided by the DC power dissipation. PAE evaluates how efficiently the PA converts the DC power into RF power signal [51]. The DC power consumption includes the total DC power consumed by the amplifier stages. PAE is calculated as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.3}$$

As power amplifiers must often be able to deal with large signal swing, this type of circuit is frequently under operating conditions that lead to signal distortion, particularly when operating close to the maximum output power. High output power leads to high PAE.

2.1.1.4. P1dB Compression Point

Linearity is defined as the scenario in which the output of the device varies linearly with respect to the variations of the input [52]. Linearity has become increasingly important in current RF communication structures. The linearity of a system can be defined as a 1dB compression point (P1dB). As depicted in Figure 2.1, 1dB output power compression point is defined as a 1dB output power deviation from the ideal linear curve.

Under high input power levels, it is possible to observe that the output characteristics deviate from the ideal linear response. When the output power does not further increase due to a higher input power, the PA is said to be saturated and it cannot deliver more power regardless of the input power to PA. It is in the compression region that the amplifier's efficiency reaches its maximum, because the output power is maximum. For that reason, from the efficiency point of view it is interesting to work at that region most of the time.

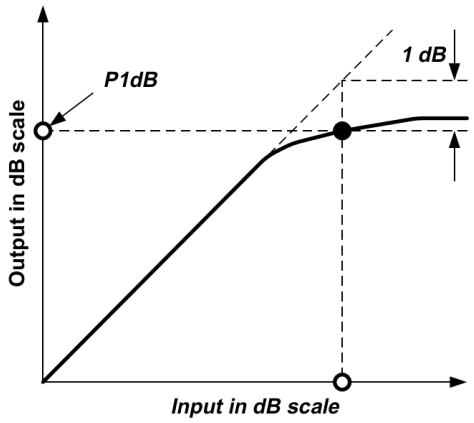


Figure 2.1. P1dB compression point in dB scale.

2.1.1.5. Stability

The stability of a power amplifier is a major issue in designing the PA. For a varying load, power amplifier should be stable. In other words, it should generate neither spurious signals nor

oscillation throughout the whole frequency band of interest. Stability is measured by the Rollet stability factor (Kf), can be defined in the following Equation (2.4) for any two-terminal device.

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \tag{2.4}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$, and K>1 and Δ>0 should be satisfied for unconditional stability [53]-[54].

The above criteria for stability should be fulfilled not only at the desired frequency range but also at other frequencies.

2.1.1.6. 3-dB Bandwidth

The half-power bandwidth is a point at which the output power has dropped to half of its peak value; that is, at a level of approximately -3 dB. The frequency at which the power level of the signal decreases by 3 dB from its maximum value is called the 3 dB bandwidth.

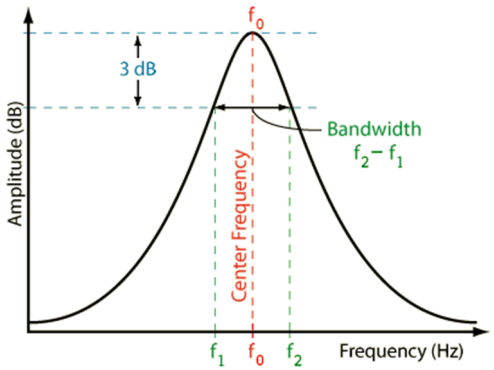


Figure 2.2. 3-dB bandwidth.

Therefore, to satisfy the current demand, power amplifiers should be designed to have low power consumption, high output power, high power gain, high PAE, and high linearity.

2.1.2. Impedance Matching Network

In electronics, impedance matching is the practice of designing the input impedance of an electrical load or the output impedance of its corresponding signal source to maximize the power

transfer or minimize signal reflection from the load. A source of electric power such as an amplifier has a source impedance which is equivalent to an electrical resistance in series with a reactance. An electrical load, such as an antenna similarly has an impedance which is equivalent to a resistance in series with a reactance. The maximum power theorem says that maximum power is transferred from source to load when the load impedance is equal to the complex conjugate of the source impedance. If this condition is met, the two parts of the circuit are said to be impedance matched.

Since a matching network is typically made of reactive components, it is frequency-dependent and changing the frequency will unmatch the circuit. Thus, a difficult challenge for an RFIC designer is to design a matching network that provides adequate match over a wide range of frequencies.

2.1.3. Classes of Operations of Power Amplifier

The main purpose of a power amplifier is to increase the power level of the signal. Power Amplifiers can be divided in several classes, depending on how the transistor is driven and the harmonic content of the drain voltage. The fundamental PA classes will be described in this section with the trade-offs between linearity and power efficiency. In order to be able to control the trade-off as a function of the desired specifications, it is possible to alter the biasing of the active device leading to different operating classes. The active device is used in an amplifier as a voltage-controlled current-source, where the input voltage controls the output current.

Power amplifiers have been traditionally categorized into different power classes of A, B, AB, C, and so on. As mentioned, the difference among these classes relates to the bias voltage at the gate of the transistor, which changes the current conduction angle. Classes A, B, and AB are labeled as linear amplifiers, whereas classes C is categorized as non-linear amplifier. These classes

are compared in Table 2.1 in terms of power efficiency and linearity, which are the most significant parameters for RF power amplifier design.

Table 2.1. Comparison of different power amplifier classes

Class	**A**	**AB**	**B**	**C**
Conduction Angle	360°	180°-360°	180°	<180°
Max. Efficiency	50%	50%-78%	78%	100%
Linearity	Excellent	Good	Moderate	Poor

Class-A amplifier is biased such that the output device of the amplifier conducts 360° throughout the full cycle and as a consequence, the power loss is also increased which in turn leads to have less efficiency.

Biasing the transistor at the threshold voltage (V_{th}), leads to 180° conduction angle, meaning that the transistor would conduct current for half a cycle. Reducing the conduction angle, reduces the DC power dissipation, potentially leading higher efficiency. As the current would be chopped in the half of the duty cycle, the output power is non-sinusoidal and harmonics are generated, polluting side bands. On the other hand, the class-AB amplifier is the combination of class-A and class-B amplifiers, and thus it has a better efficiency than class-A, and a better linearity than class-B. For non-linear amplifier, the class-C amplifier, conducts less than a half cycle, and experiences higher distortion and noise effect. Although the efficiency of class-C PA is good, it suffers from poor dynamic range [55].

2.1.4. Power Combining Techniques

In power amplifier design in CMOS technology, two main issues must be addressed: Oxide breakdown and hot carrier effect. The gate-oxide breakdown is caused by a high voltage drop

across the gate oxide, which results in an irreversible shortage of gate-to-channel capacitance. The oxide breakdown degrades the performance and the efficiency of the PA. Hot carrier effect refers to the acceleration of an electron by a high electric field in the MOS device, which generates a high kinetic energy. This effect increases the threshold voltage and degrades the performance of the device [56].

Due to the low breakdown voltages in CMOS technology, achieving a large output power with a single device requires to conduct a large drain current, making the power efficiency more sensitive to supply parasitics and leads to a high loss in the matching network. To overcome these problems, an alternative way is to use multiple devices which their powers can be combined to reach the required output power. Several approaches exist in the literature that can combine power of multiple devices in parallel [57]-[59].

1) Transformer-based techniques have been widely investigated recently with good results. However, most of these techniques are only suitable for nonlinear amplification while on-chip transformers require a large die area [60]-[63].

2) Current combining topology which a parallel combination of transistors is used to increase the overall output current while the individual transistors are subjected to an identical output voltage equal to the maximum allowable voltage across one device. Thus, the total output power at the device plane gets increased [64]-[65].

3) Voltage combining topology which two or more transistors are stacked so that the overall voltage swing is increased with the increase in output impedance, ultimately increasing the output power. Stacking of transistors helps to overcome the low breakdown voltage of CMOS technologies [66]-[69].

Figure 2.3 shows the proposed architecture for power combining which consists of both current and voltage combining techniques. The circuit is composed of common-source and common-gate transistors in series so that their output swings can be added in phase to allow a larger voltage swing at the output node of the device. Unfortunately, the voltage stress is not equally divided between the two transistors and the common-gate transistor is stressed more, especially across its drain and gate terminals.

An external gate capacitance of C_B is introduced to allow an RF swing at the gate of common-gate transistor. This external capacitance produces a proper in-phase voltage swing at the gate and drain. This approach systematically reduces the drain-gate and drain-source voltage swings of both the common-source and common-gate transistors under large signal operation, which provides more room for reaching a higher output power.

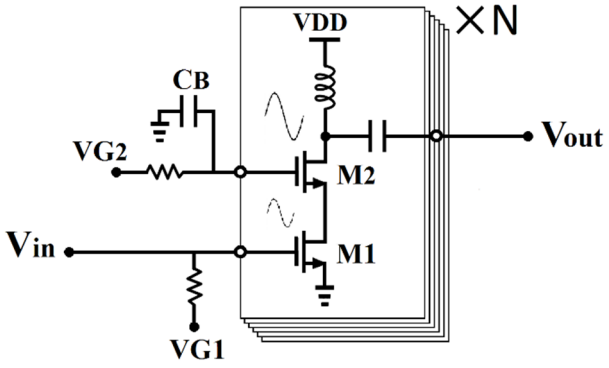


Figure 2.3. Power combining techniques.

2.2. The Proposed Fully Integrated Triple-Mode Tunable Power Amplifier

2.2.1. Macro-Model

As discussed in chapter 1, twenty five and eighteen different frequency bands have been defined by 4G LTE and 5G NR standards, respectively, in the frequency range of 700MHz to 2100MHz. Figure 2.4 shows macro-model of the proposed triple-mode tunable power amplifier. This chapter is targeting two goals, 1) covering multi frequency bands, and 2) providing multi

power modes. The former one, as shown in Figure 2.4, is achieved by using two input matching networks (IMN) and two output matching networks (OMN). IMN1 and OMN1 are covering the lower frequency band of 700MHz to 1000MHz. Besides, IMN2 and OMN2 operate at the higher frequency band of 1400MHz to 2100MHz. There are two voltage-controlled switches at the left and the right sides of each matching network. It also should be mentioned that four switches of S1, using in IMN1/OMN1, are connected together and controlled by an external voltage supply. Similarly, four switches of S2, using in IMN2/OMN2, are controlled by another voltage supply. By turning the S1 or S2 *ON*, the signal path for the lower band (B1) or the higher band (B2) will be closed, respectively. Thus, the power amplifier will operate in that specific frequency range.

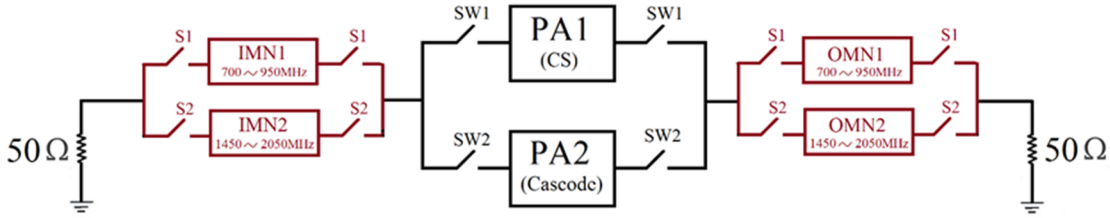


Figure 2.4. Macro-model of the proposed triple-mode tunable power amplifier.

Another goal of this work is to provide multi output power modes. As shown in the macro-model, two different types of power amplifier are used. The first and the second power amplifiers, respectively, are designed based on common-source and cascode topologies. In practice, at the same DC power condition, the latter one can deliver more output power. By using this strategy triple-mode power amplifier is being designed. As shown in Figure 2.4, two switches of SW1 and SW2 with different control voltages are used in order to provide different power states for the proposed PA. By turning *ON* the SW1 and keeping *OFF* the SW2, only PA1 will operate and provide the output power. Similarly, by turning *ON* the SW2 and keeping *OFF* the SW1, only PA2 will provide the output power. Interestingly, there is another power state in the proposed architecture. By keeping both PA1 and PA2 *ON*, and simultaneously turning both SW1 and SW2

ON, the output powers of two PAs will be combined together. Hence, they can totally deliver much more output power. In other words, for saving the battery life of the transceiver, when a low output power is needed, the state of only PA1 can be used. It is called low power mode. By using the state of only PA2, a medium power mode is presented. Finally when it is needed, a high output power can be delivered by using the state of PA1+PA2.

2.2.2. Micro-Model

2.2.2.1. Power Stage Design and DC Biases

Micro-model in transistor level of the proposed triple-mode tunable power amplifier is demonstrated in Figure 2.5. PA1 is formed by six cells which each unit cell consists of power amplifier with common-source topology. Output nodes of these six cells are tied together to use power combining technique. Transistor size of M1 is 1.3mm/120nm in the common-source topology. Likewise, PA2 consists of six cells with cascode topology. In cascode architecture, due to sustaining large voltage swing, size of the common-gate transistor (M2) is designed twice of size of the common-source transistor (M3). The size of the upper and lower transistors are 1.3mm/120nm and 650μm/120nm, respectively. Capacitor of C_B is also used in gate terminal of the common-gate transistor in order to make drain-source voltage swing of two transistors (V_{DS2} and V_{DS3}) in phase. It increases output power of the cascode PA after power combining. In this circuit, optimum value of C_B is 24pF. Furthermore, DC bias condition of PA1 and PA2 is listed in Table 2.2. In this design, PA1 and PA2 are just power stage without any driver stage.

2.2.2.2. Input and Output Matching Networks

As discussed above, for each frequency band (B1 or B2), the challenge is to design an input/output matching network which can convert input/output impedance of three different types of power amplifier (only PA1, only PA2, PA1+PA2) to 50 ohm. Regarding to output matching

network, both power amplifiers (PA1 and PA2) were designed to roughly have an equal output impedance. In this work, the output impedances of all three types of power amplifier (PA1, PA2, PA1+PA2) are less than 1 ohm in both frequency bands. Hence, OMN1 and OMN2 were designed at the lower and the higher frequency bands, respectively, to convert this low impedance to 50 ohm. OMN1 and OMN2 consist of two-section LC (series inductor and parallel capacitor). Table 2.3 listed the components used in the two output matching networks.

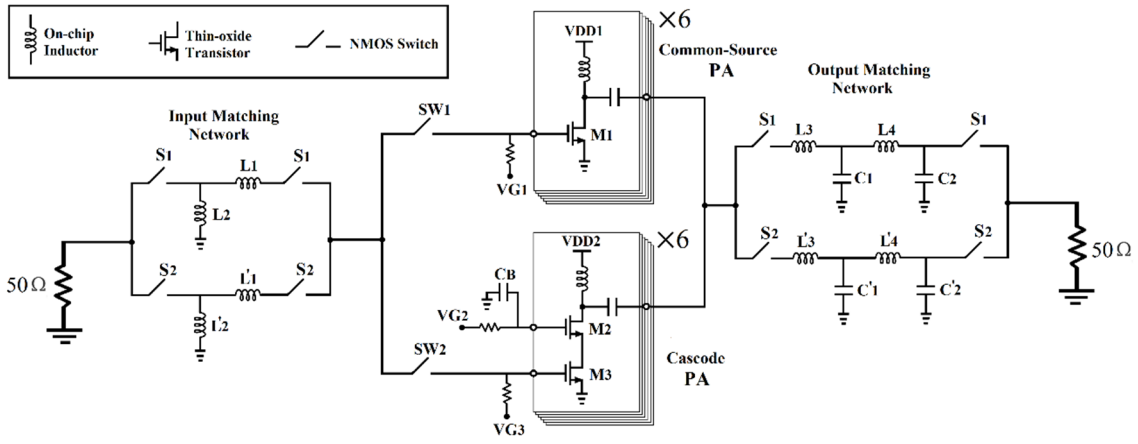


Figure 2.5. Micro-model of the proposed triple-mode tunable power amplifier.

Table 2.2. DC bias conditions of PA1 and PA2

PA1		PA2		
VDD_1	VG_1	VDD_2	VG_2	VG_3
1.5V	1.2V	2.6V	2.1V	1.2V

In addition, in order to match the input impedance of the power amplifier to 50 ohm, input matching network was designed by using two inductors (one series and one parallel). Design parameters of input matching networks are summarized in Table 2.4. It also should be mentioned that DC blocking capacitor is included in SW1 and SW2 design.

Table 2.3. Design parameters of output matching networks

OMN1				OMN2			
L_3	C_1	L_4	C_2	L'_3	C'_1	L'_4	C'_2
360pH	80pF	3.14nH	9.4pF	170pH	34pF	1.4nH	4.4pF

Table 2.4. Design parameters of input matching networks

IMN1		IMN2	
L_1	L_2	L'_1	L'_2
14.2nH	3.67nH	2.08nH	2.38nH

2.2.3. Simulated Results

2.2.3.1. Simulated Small-Signal Results

Scattering Parameters (SP) results of the proposed triple-mode tunable power amplifier are illustrated in Figure 2.6. Combination of three different types of power amplifier and two different frequency bands provides six different states for the proposed multiband multimode power amplifier. Figure 2.6 (a) shows input reflection coefficient (S11) in dB scale. Central frequencies of PA1+PA2/PA1/PA2, respectively, are 780/830/900 MHz at the lower frequency band of B1, and 1.72/1.82/1.92 GHz at the higher band of B2. Figure 2.6 (b) shows output reflection coefficient (S22) in dB scale. S22 is less than -10dB in both frequency ranges of 700MHz to 1000MHz and 1400MHz to 2100MHz, which shows good impedance matching (low reflected power) at the output port. Regarding to power stage gain, Figure 2.6 (c) shows small-signal gain of 6.7/15.0/15.3 dB at the lower band and 4.0/13.2/8.7 dB at the higher band for PA1/PA2/PA1+PA2, respectively.

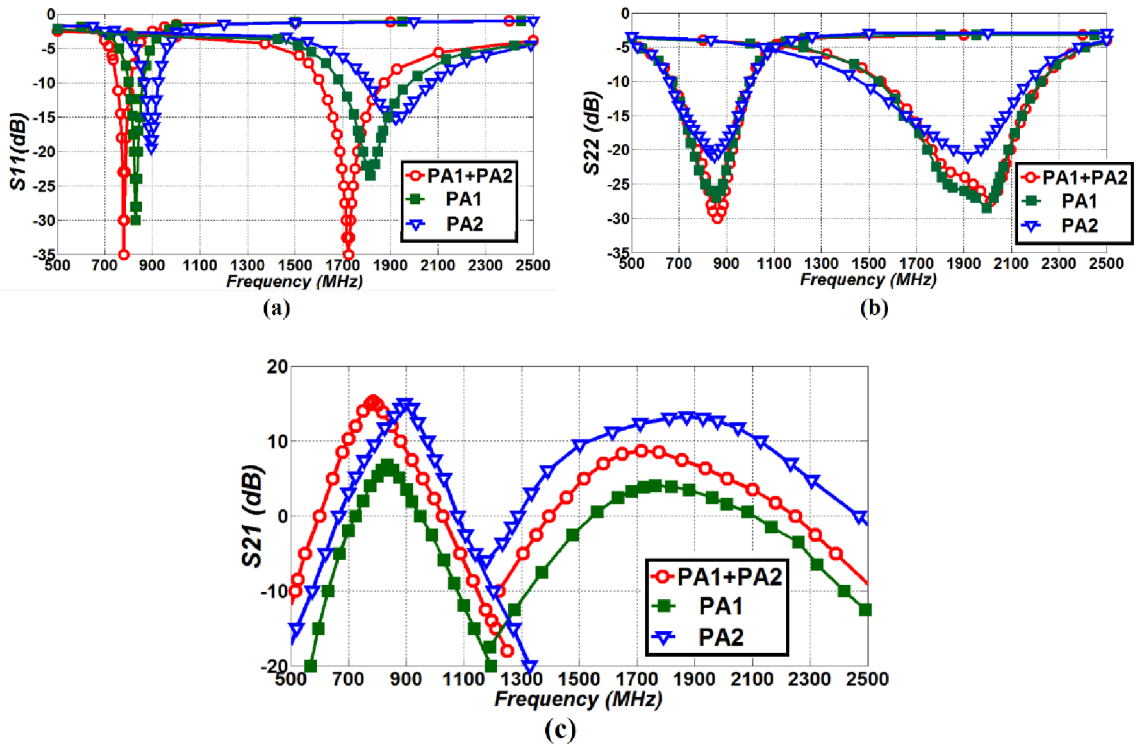


Figure 2.6. Simulated S-parameters results of the proposed triple-mode tunable power amplifier, (a) S11, (b) S22, (c) gain of power stage.

2.2.3.2. Simulated Large-Signal Results

Figure 2.7 shows simulated output power versus frequency for the proposed triple-mode tunable power amplifier. It is clearly illustrating six different states of the proposed PA. At the lower band, saturated output power (Psat) is 16.1/19.8/24.0 dBm for PA1/PA2/PA1+PA2, respectively. At the higher band, Psat is 21.9/23.2/26.2 dBm, respectively, for PA1/PA2/ PA1+PA2. Thus, the proposed architecture provides low/mid/high power modes separately for each frequency bands.

Moreover, performance truth-table of the proposed triple-mode tunable power amplifier is summarized in Table 2.5. It explicitly shows that cascode architecture (PA2) has better performance than common-source (PA1) architecture with respect to power gain, output power, and efficiency.

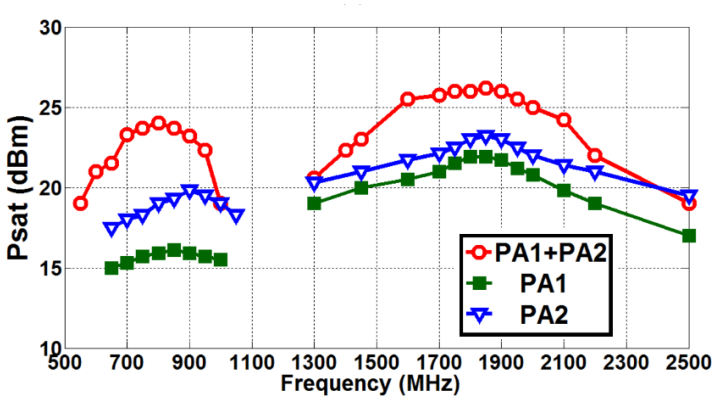


Figure 2.7. Simulated saturated output power result of the proposed triple-mode tunable PA.

Table 2.5. Truth table of triple-mode tunable power amplifier

PA1	PA2	B1	B2	Center Frequency	Power Stage Gain (dB)	Psat (dBm)
ON	OFF	ON	OFF	830MHz	6.8	16.1
ON	OFF	OFF	ON	1.82GHz	4.0	21.9
OFF	ON	ON	OFF	900MHz	15.0	19.8
OFF	ON	OFF	ON	1.92GHz	13.2	23.2
ON	ON	ON	OFF	780MHz	15.3	24.0
ON	ON	OFF	ON	1.72GHz	8.7	26.2

2.2.4. Measured Results

Figure 2.8 shows die-photo of the fully integrated triple-mode tunable power amplifier in 130nm CMOS technology with size of 3.0 mm × 1.5 mm including all bond-pads. Figure 2.9 shows measured S-parameter results of the taped-out chip. Figure 2.9 (a) demonstrates that tunability in two input matching networks of IMN1 and IMN2 does not work. S11 results for both frequency

bands are flat, although there is 50 ohm match in both frequency bands (S11 is less than -10dB in the targeted frequency range).

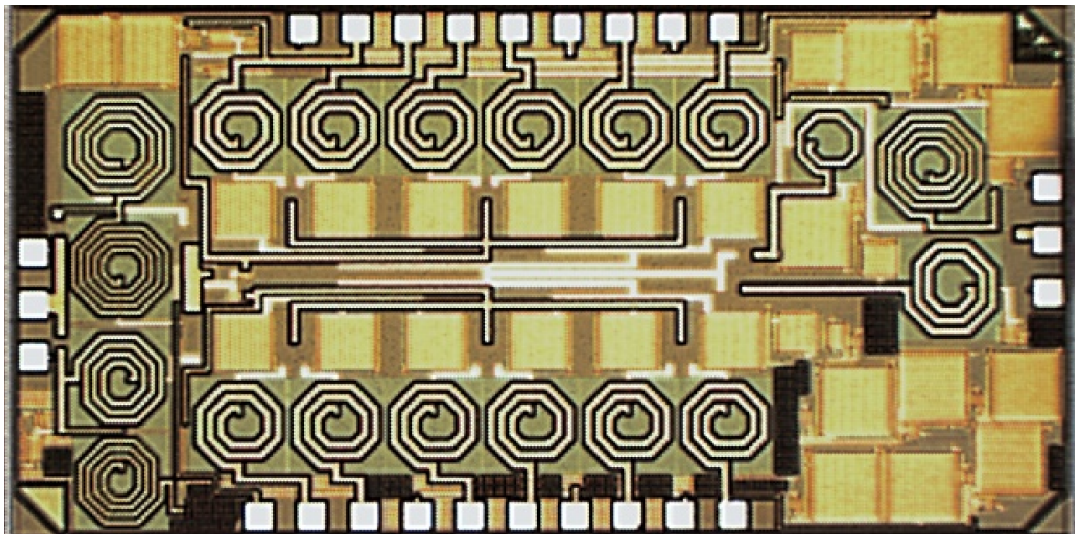


Figure 2.8. Fully integrated triple-mode tunable power amplifier using 130nm CMOS process with size of 3.0 mm × 1.5 mm.

The output reflection coefficient (S22) result, Figure 2.9 (b), shows a better tunability performance. By turning the lower frequency path *ON*, and keep the higher one *OFF*, the power amplifier operates at B1 and OMN1 can provide 50 ohm match to the output port. Likewise, by turning the OMN1 *OFF* and OMN2 *ON,* the power amplifier operates at B2, as a result, there will be a 50 ohm impedance matching at the output port in the higher frequency band.

These small-signal results are related to "only PA2" mode which is supposed to have the best small-signal gain. Figure 2.9 (c) shows small-signal gain result of the proposed tunable power amplifier. Although the proposed PA demonstrates a perfect tunability, the small-signal gain (S21) is around -20dB at both frequency bands. This gain is not enough to consider the proposed tunable power amplifier as a power amplifier. The measured results explicitly show a huge RF leakage/loss through RF path from the input port to the output port.

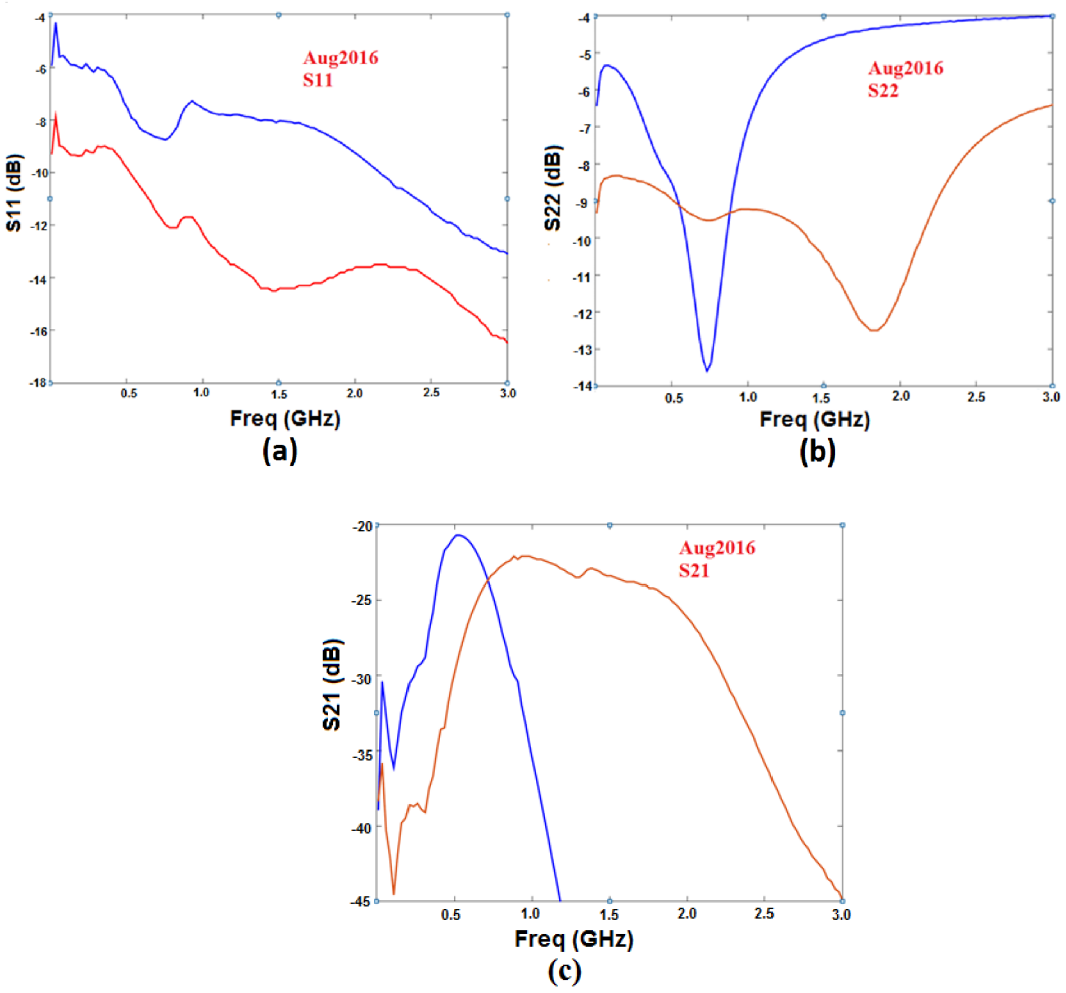


Figure 2.9. Measured S-parameter results of the proposed tunable power amplifier, (a) S11, (b) S22, and (c) S21.

2.3. Discussion

The cascode topology in the proposed tunable power amplifier is designed with the simulation current of 400mA for each unit cell. After measuring the chip, the measured current is only 80mA for each unit cell of cascode. It means the measured current is one-fifth (20%) of the designed current.

M1 metal layer, the nearest metal layer to the active devices in the fabrication process, is used to form the ground plane. Metal sheet resistance for M1 is about 70mΩ per square. After modeling the ground plane by using RFIC simulator, the ground resistance (Rgnd) is calculated

1Ω. This high ground resistance reduces the current of the driver and power stages, which degrades the total performance of the chip. After thorough investigation, two following solutions are found in order to reduce the ground resistance.

1) As mentioned above, M1 metal layer is used to form the ground plane of the chip. As shown in Figure 2.10 (a), ground plane is a grid formed by a square sub-cell with the size of 2.5µm×2.5µm. Generally, there is a hole in the sub-cell of the ground plane due to a) not exceeding maximum pattern density requirement by the fabrication process, b) reducing parasitic capacitance between ground plane and other layers, and c) preventing induced current within the layer. The ground plane used in the chip, has a hole with size of 1.5µm × 1.5µm, which gives 64% of pattern density for M1 metal layer.

The maximum pattern density requirement for M1 metal layer in 130nm CMOS process is 85%, it means percentage of area covered by M1 metal layer over entire chip cannot exceed 85% of the chip area. It will give better results if a smaller hole is used in the sub-cell of the ground plane. Figure 2.10 (b) shows a suggestion for the future tape-out. A hole with size of 1.0µm × 1.0µm is used in the middle of the sub-cell, which provides 84% of pattern density for M1 metal layer. The chip with the grid suggested in Figure 2.10 (b) as a ground plane, will be expected to have a lower ground resistance than the chip presented in this chapter.

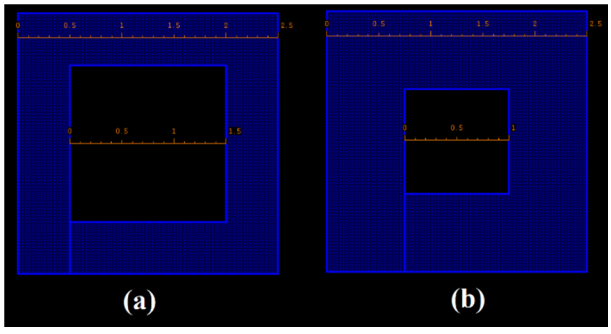


Figure 2.10. Sub-cell of the ground plane with pattern density of (a) 64%, and (b) 84%.

2) The second solution to reduce the ground resistance is to use M1 ground plane on the backplane of inductors. Besides increasing total area of the ground plane in the chip, using an array of M1 on the backplane of the inductors can be used as a shield to isolate the inductors from substrate noises and prevents induced currents in the substrate which leads to lower quality factor. The drawback of using ground plane on backplane of the inductors is higher parasitic capacitance with resulting reduction in the self-resonant frequency.

Because there are too many inductors in the proposed architecture of tunable power amplifier, using M1 ground plane on the backplane of the inductors, increases the total area of ground plane, hence reduces the ground resistance.

Regarding to small-signal results, frequency-tuning capability is achieved in S22 and S21 by switching *ON/OFF* the control voltages of the lower and the higher frequency bands. However, the input reflection coefficient (S11) is not showing capability of tuning the frequency in use.

Reproducing measured S11 results with RFIC simulator concludes that there might be an unexpected short-circuit in gate terminal of the transistor in the power stage. It could be occurred either during the fabrication process or due to using tie-down reverse-biased diode. Tie-down diodes are typically used to prevent gate damages during the fabrication process. If tie-down diode is not fabricated properly, it could short-circuit the gate of the transistor to the substrate and causes RF leakage/loss.

2.4. Conclusion

Modern wireless systems often need multi-band and multi-mode operations to simultaneously support different communication standards. A novel tunable CMOS power amplifier addressing three low/mid/high power modes, is presented in this chapter. The simulation small-signal and large-signal results shows that the proposed PA can cover 4G LTE, 5G NR, and

GSM standards. However, there is discrepancy between measured results and simulation results after measuring the chip. The measured current is about one-fifth of the designed current in the simulation, which shows a high ground resistance of 1 ohm. In future tape-out, it will be tried to reduce the ground resistance by increasing area of the ground plane in layout. Using ground plane in the backplane of the inductors can also reduce the total ground resistance.

S-parameter results show a good tunability, however instead of voltage gain it actually shows loss, which demonstrates a huge RF leakage in the RF path. The input reflection coefficient (S11) is not capable of tuning the operating frequency. The flat S11 could be occurred due to using tie-down reverse-biased diode in the gate of the transistors. If tie-down diode is not fabricated properly, it could short-circuit gate of the transistor to the substrate and causes RF leakage/loss.

CHAPTER 3. DESIGN AND IMPLEMENTATION OF A FULLY INTEGRATED TWO-STAGE MULTI-BAND POWER AMPLIFIER IN 130nm CMOS PROCESS

3.1. Introduction

The design drawback of the architecture presented in the previous chapter was having a low small-signal gain, low power gain, and low efficiency. The gain can be boosted by using a driver stage in the PA. It was mentioned in the previous chapter that cascode architecture has a better RF performance than common-source topology. In this chapter for designing the power stage, cascode topology with optimized number of unit-cell and optimized DC power consumption is being used which provides higher power efficiency. This chapter proposes fully integrated two-stage tunable power amplifier with higher gain, efficiency, and bandwidth with respect to tunable PA presented in chapter 2.

This chapter consists of two parts. A traditional approach of designing a multi-band power amplifier is used in the first part (3.2). In this approach, switches are in shunt path (not RF path), and variable passive components (variable inductors and capacitors) are being utilized in order to tune the operating frequency. This approach is a well-known technique for designing multi-band PA. As a safe plan, this traditional approach is chosen in the first part of this chapter to decrease RF leakage and minimize discrepancy between simulation and measurement results that happened in chapter 2.

In the second part of this chapter (3.3), a dual-band CMOS power amplifier is presented by using two switchable matching networks (one for the lower band and one for the higher band). This technique is similar to what presented in chapter 2, but with a few optimizations. First of all, a driver stage is used to boost the total gain of the power amplifier. Second of all, only cascode topology is being used in the power stage with optimized number of unit-cell and optimized DC

power consumption which increases the power efficiency. Last but not least, this multi-band power amplifier is designed and taped-out without tie-down diodes in order to check whether the issue of the previous tape-out was due to connection of tie-down diodes in the gate of the transistors to the substrate. It is interesting to see whether the S11 flatness (Figure 2.9) will be solved in this design or not.

3.2. Multi-Band Power Amplifier Using Reconfigurable Matching Networks

3.2.1. Macro-Model

Macro-model of the proposed tunable power amplifier is shown in Figure 3.1. A two-stage power amplifier is designed including driver stage to increase the total gain, and power stage to boost the output power. As shown in Figure 3.1, in order to cover multiple frequency bands with one power amplifier, the proposed tunable PA consists of three reconfigurable matching networks. Reconfigurable output matching network (OMN) is used to match output impedance of the power stage to impedance of an antenna (50Ω) in order to drive the antenna effectively.

Similarly, reconfigurable interstage matching network (ISMN) is used to match output impedance of the driver stage to input impedance of the power stage. Moreover, reconfigurable input matching network (IMN) obtains maximum power transfer from input source to the power amplifier by matching input impedance of the driver stage to impedance of an external input source (50Ω). These reconfigurable matching networks are designed to operate at three different bands with center frequency of B1=900MHz, B2=1450MHz, and B3=1900MHz.

3.2.2. Micro-Model

Micro-model of the proposed tunable power amplifier is shown in Figure 3.2. The proposed tunable power amplifier consists of driver stage, power stage, and reconfigurable input/interstage/ output matching networks. The design procedures of these blocks are discussed as follows.

Figure 3.1. Macro-model of the proposed multi-band power amplifier using reconfigurable input, interstage, and output matching networks.

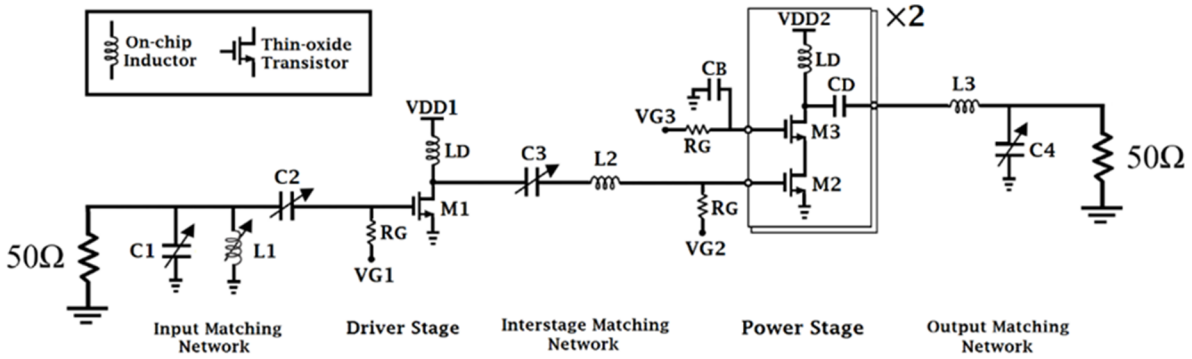


Figure 3.2. Micro-model of the proposed multi-band power amplifier.

3.2.2.1. Driver and Power Stages

As shown in Figure 3.2, a two-stage power amplifier is designed. The driver stage consists of common source topology. Size of the driver stage transistor (M1) is 400µm/120nm. DC bias conditions for gate voltage (V_{G1}) and drain supply voltage (V_{DD1}) are designed to be 0.7V and 1.2V, respectively. Hence, DC current of 60mA flows through M1 transistor.

The power stage is formed by two unit cells where each unit cell consists of cascode topology. Due to power combining, output nodes of these two cells are tied together. The size of the upper and lower transistors in cascode architecture are 2.0mm/120nm and 1.6mm/120nm, respectively. Gate resistor (R_G), drain inductor (L_D), and coupling capacitor (C_D) are 6.2K, 1.2nH, and 70pF, respectively. DC bias conditions of cascode architecture with gate voltages (V_{G2}, V_{G3}) and drain supply voltage (V_{DD2}) are designed 0.6V/1.8V, and 2.4V. Current of 160mA flows

through power stage transistors in each cell (totally 320mA). Transistors in the power stage operate in Class-AB mode.

In addition, capacitor of C_B is used in the gate of the upper transistor (M3) in order to make the gate RF short, and also make drain-source voltage of two transistors (V_{DS2} and V_{DS3}) in phase. It increases output power after power combining in the output node of the power stage. In this circuit, optimum value of C_B is 20pF. DC bias conditions of the driver and the power stages are listed in Table 3.1. Moreover, Table 3.2 summarized the design parameters of the driver and power stages.

Table 3.1. DC bias conditions of the driver and power stages

VG_1	VG_2	VG_3	VDD_1	VDD_2	ID_1	ID_2=ID_3
0.7V	0.6V	1.8V	1.2V	2.4V	60mA	160mA

Table 3.2. Design parameters of the driver and power stages

R_G	L_D	C_D	C_B	W_1	W_2	W_3
6.2KΩ	1.2nH	70pF	20pF	400um	1.6mm	2.0mm

3.2.2.2. Reconfigurable Output Matching Network

As mentioned previously, in order to drive an antenna effectively, reconfigurable output matching network (OMN) is used to match output impedance of the power stage to 50 Ω impedance of the antenna at three targeted frequency bands with center frequency of B1=900MHz, B2=1450MHz, and B3=1900MHz. As shown in Figure 3.2, reconfigurable output matching network consists of a fixed inductor (L3) in series path, and a variable capacitor (C4) in shunt path. Based on output impedance of the power stage at three targeted frequency bands, L3 is equal to

1.0nH and C4 is designed 20pF/5pF/2.6pF for B1/B2/B3, respectively. Design details of the reconfigurable output matching network is shown in Figure 3.3. In order to design the variable capacitor, three capacitors of C4a=2.6pF, C4b=2.4pF, and C4c=15.0pF are used.

In this architecture, C4b and C4c can be added to C4a by turning the respective switches *ON*. At B1, Vcont1 and Vcon2 are supposed to be *ON*, so, C4b and C4c will be added to C4a, and as a result, C4 is equal to C4a+C4b+C4c= 20pF. Similarly, by keeping Vcont1 *ON* and turning Vcont2 *OFF*, only C4b is added to C4a, so, C4=C4a+C4b=5pF. In this case, the operating frequency jumps to B2. By turning both Vcont1 and Vcont2 *OFF*, C4 is equal to C4a=2.6pF and the circuit operates at B3. Design parameters of the reconfigurable output matching network are listed in Table 3.3.

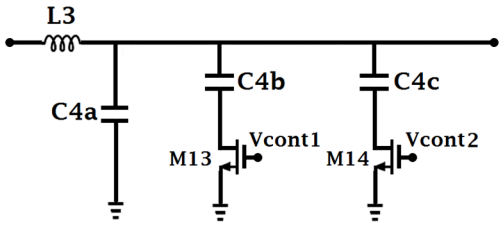


Figure 3.3. Reconfigurable output matching network.

Table 3.3. Design parameters of reconfigurable output matching network

L_3	C_{4a}	C_{4b}	C_{4c}	W_{13}	W_{14}
1.0nH	2.6pF	2.4pF	15pF	1.0mm	600um

3.2.2.3. Reconfigurable Interstage Matching Network

As shown in Figure 3.2, a fixed inductor (L2) and a variable capacitor (C3) in series path are used to form reconfigurable interstage matching network (ISMN) in order to match input impedance of the power stage to output impedance of the driver stage at three targeted frequency bands. L2 is 7.3nH and C3 is designed 10pF/1.6pF/0.8pF at B1/B2/B3, respectively.

Figure 3.4 illustrates design details of the reconfigurable interstage matching network. Three capacitors of C3a=C3b=0.8pF, and C3c=8.4pF are used to form the variable capacitor of C3. In this architecture, by turning Vcont1 and Vcont2 *ON*, C3b and C3c will be added to C3a, so, C3=C3a+C3b+C3c=10pF, and the circuit operates at the lower band (B1). By keeping Vcont1 *ON* and turning Vcont2 *OFF*, C3=C3a+C3b=1.6pF, hence, the operating frequency will be B2. In addition, in order to operate at the higher band of B3, both Vcont1 and Vcont2 are supposed to be switched *OFF*, and C4 will be equal to C4a=0.8pF. Design parameters of reconfigurable interstage matching network are listed in Table 3.4.

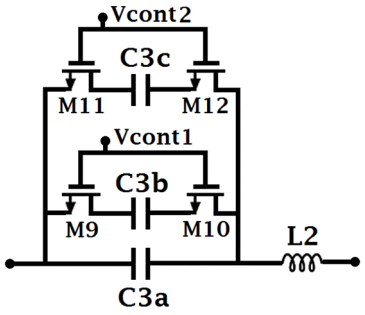


Figure 3.4. Reconfigurable interstage matching network.

Table 3.4. Design parameters of reconfigurable interstage matching network

L_2	C_{3a}	C_{3b}	C_{3c}	$W_9=W_{10}=W_{11}=W_{12}$
7.3nH	0.8pF	0.8pF	8.4pF	200um

3.2.2.4. Reconfigurable Input Matching Network

In order to obtain maximum power transfer from input source to the proposed power amplifier at three targeted frequency bands, a reconfigurable input matching network (IMN) is required to match the input impedance of the driver stage to impedance of an external input source (50Ω). Figure 3.2 shows that the reconfigurable input matching network consists of a variable

capacitor (C2) in series path, a variable inductor (L1) in shunt path, and also a variable capacitor (C1) in shunt path. Based on input impedance of the driver stage, C2 is designed to be 150fF/300fF/300fF, L1 to be 9.25nH/1.95nH/1.95nH, and C1 to be 19pF/11pF/6pF, respectively, at B1/B2/B3.

Figure 3.5 shows design details of the reconfigurable input matching network. Three capacitors of C1a=6pF/C1b=5pF/C1c=8pF, and two capacitors of C2a=C2b=150fF are used to design two variable capacitors of C1 and C2, respectively. Furthermore, two inductors of L1a=9.25nH and L1b=2.4nH form variable inductor of L1 in shunt path. By turning Vcont1 and Vcont2 *ON* and Vcont3 *OFF*, C1b and C1c will be added to C1a, so, C1=C1a+C1b+C1c=19pF, L1=L1a=9.25nH, and C2=C2a=150fF. In this condition, the circuit operates at lower frequency band (B1). By keeping Vcont1 *ON*, switching Vcont2 *OFF*, and Vcont3 *ON*, C1b, L1b, and C2b will be connected in parallel with C1a, L1a, and C2a, respectively. Hence, C1=C1a+C1b=11pF, L1=L1a||L1b=1.95nH, and C2= C2a+C2b=300fF. The circuit enables middle frequency band (B2) in this state. In addition, in order to operate at higher frequency band (B3), Vcont1, Vcont2, and Vcont3 are supposed to be switched, respectively, *OFF*, *OFF*, and *ON*. So, in this condition, C1=C1a=6pF, L1=L1a||L1b=1.95nH, and C2=C2a+C2b=300fF. Design parameters of reconfigurable input matching network is listed in Table 3.5.

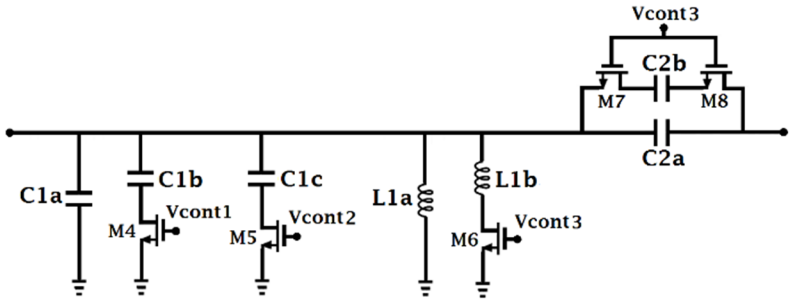


Figure 3.5. Reconfigurable input matching network.

Table 3.5. Design parameters of reconfigurable input matching network

C_{1a}	C_{1b}	C_{1c}	L_{1a}	L_{1b}	C_{2a}	C_{2b}	W_4=W_5	W_6=W_7=W_8
6pF	5pF	8pF	9.25nH	2.48nH	150fF	150fF	600um	200um

3.2.3. Simulated Results

After embedding the designed reconfigurable input, interstage, and output matching networks in Figure 3.2, a complete circuit schematic of the proposed CMOS triple-band power amplifier is illustrated in Figure 3.6. Furthermore, truth-table, and optimum matching parameters of the proposed triple-band power amplifier are summarized in Table 3.6, and Table 3.7, respectively.

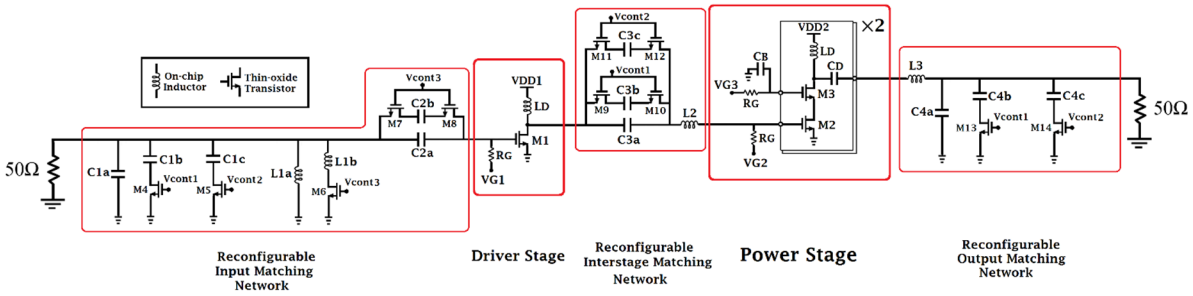


Figure 3.6. Complete circuit schematic of the proposed CMOS tunable power amplifier.

Table 3.6. Truth-table of the proposed triple-band power amplifier

Band	**Center Frequency**	**Vcont1**	**Vcont2**	**Vcont3**
B1	0.90GHz	ON	ON	OFF
B2	1.45GHz	ON	OFF	ON
B3	1.90GHz	OFF	OFF	ON

Table 3.7. Optimum matching parameters of triple-band power amplifier

Band		Band1	Band2	Band3
IMN	C_1	$C_{1a}+C_{1b}+C_{1c}$=19pF	$C_{1a}+C_{1b}$=11pF	C_{1a}=6pF
	L_1	L_{1a}=9.25nH	$L_{1a} \parallel L_{1b}$=1.95nH	$L_{1a} \parallel L_{1b}$=1.95nH
	C_2	C_{2a}=150fF	$C_{2a}+C_{2b}$=300fF	$C_{2a}+C_{2b}$=300fF
ISMN	C_3	$C_{3a}+C_{3b}+C_{3c}$=10pF	$C_{3a}+C_{3b}$=1.6pF	C_{3a}=0.8pF
	L_2	L_2=7.3nH	L_2=7.3nH	L_2=7.3nH
OMN	L_3	L_3=1.0nH	L_3=1.0nH	L_3=1.0nH
	C_4	$C_{4a}+C_{4b}+C_{4c}$=20pF	$C_{4a}+C_{4b}$=5pF	C_{4a}=2.6pF

3.2.3.1. Simulated Small-Signal Results

The simulated Scattering parameters results of the proposed triple-band tunable power amplifier are demonstrated in Figure 3.7. Figures 3.7 (a) and 3.7 (b), respectively, show input reflection coefficient (S11) and output reflection coefficient (S22) in dB scale. By designing reconfigurable input, interstage, and output matching networks, a perfect impedance matching in input and output of the proposed multi-band power amplifier is achieved at three targeted frequency bands. Regarding to small-signal gain (S21) of the proposed triple-band power amplifier, Figure 3.7 (c) indicates gain of 26/27/28 dB at 900/1450/1900 MHz, respectively.

3.2.3.2. Simulated Large-Signal Results

Figure 3.8 shows output power performance of the proposed multi-band power amplifier versus frequency when the PA is in saturation condition (Pin= +5dBm). The proposed triple-band power amplifier provides saturated output power (Psat) of 22.5/23.0/23.2 dBm, and output 1-dB

compression point (P1dB) of 20.0/20.4/20.4 dB at three targeted frequency bands of 900/1450/1900MHz, respectively. Figure 3.9 explicitly demonstrates that B1, B2, and B3 cover frequency range of 700-1150MHz, 1150-1650MHz, and 1650-2200 MHz, and thus providing respective 3-dB bandwidth of 450MHz, 500MHz, and 550MHz. Small-signal and large-signal performances of the proposed two-stage triple-band power amplifier are summarized in Table 3.8.

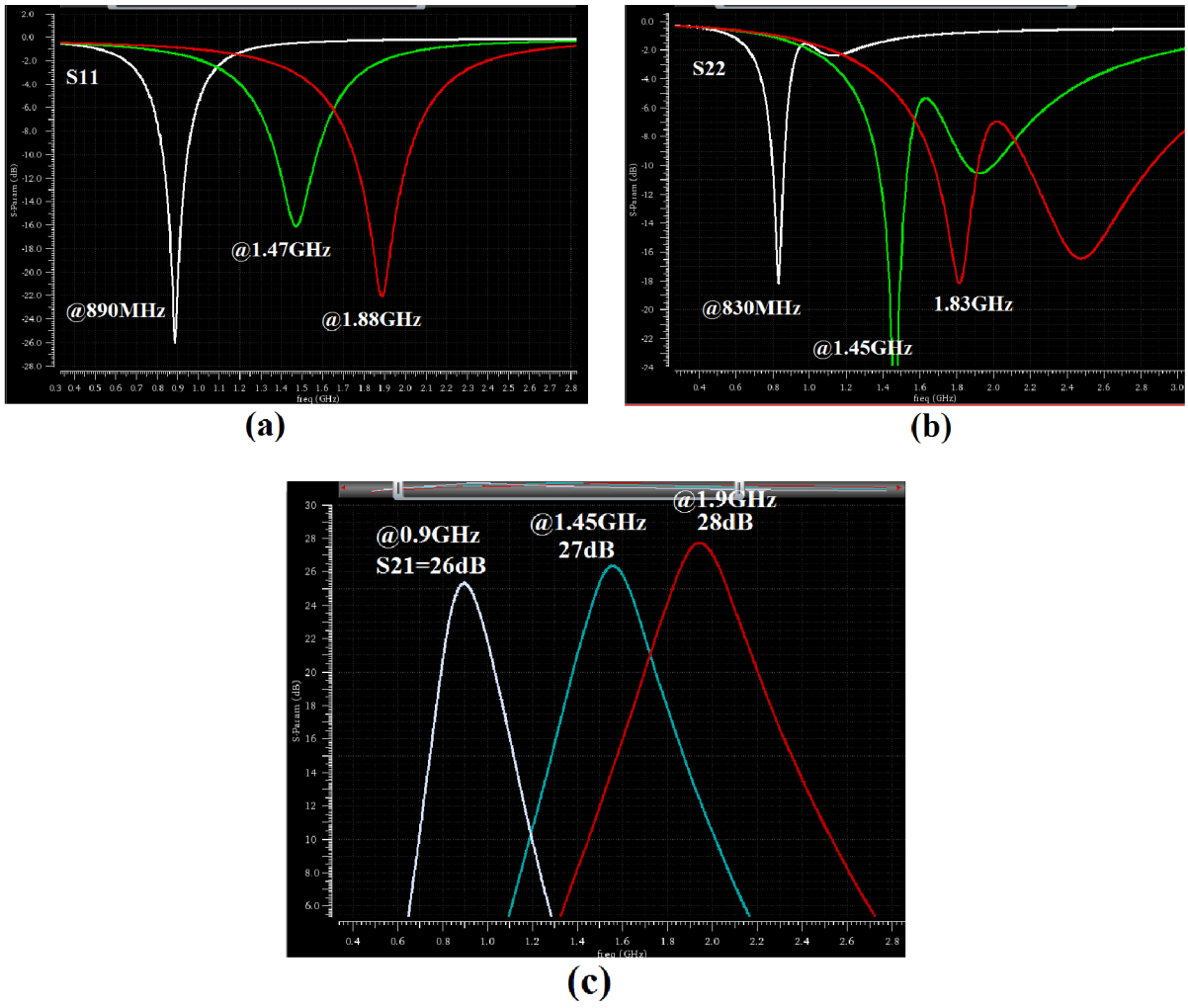


Figure 3.7. Simulated S-parameter results of the proposed triple-band power amplifier, (a) S11 (b) S22, and (c) S21.

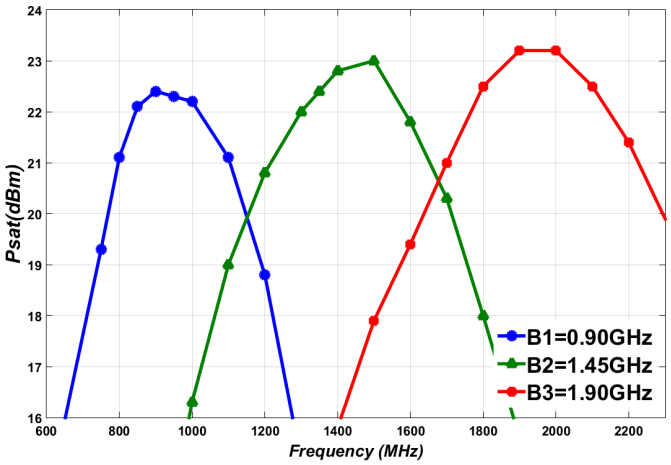


Figure 3.8. Simulated saturated output power versus frequency of the proposed triple-band tunable power amplifier.

Table 3.8. Performance summary of the proposed triple-band power amplifier

Band	Frequency (MHz)	S21 (dB)	Psat (dBm)	PAE (%)	P_{1dB} (dBm)	3-dB Power Bandwidth (MHz)
B1	700-1150	27.8	22.4	21.0	20.0	450
B2	1150-1650	29.4	23.0	23.7	20.4	500
B3	1650-2200	28.6	23.2	25.0	20.4	550

3.2.4. Measured Results

Die-photo of the fully integrated triple-band power amplifier in 130nm CMOS technology is shown in Figure 3.9. The size of the die is 1.5 mm × 1.5 mm including all bond-pads.

Figures 3.10 shows measured S-parameter results of the taped-out chip. The input reflection coefficient (S11) result is shown in Figure 3.10 (a). It clearly illustrates that the designed reconfigurable input matching network has capability of tuning the operating frequency. Likewise, Figure 3.10 (b) shows the output reflection coefficient (S22) result. The reconfigurable output matching network provides tunability for three targeted frequency bands.

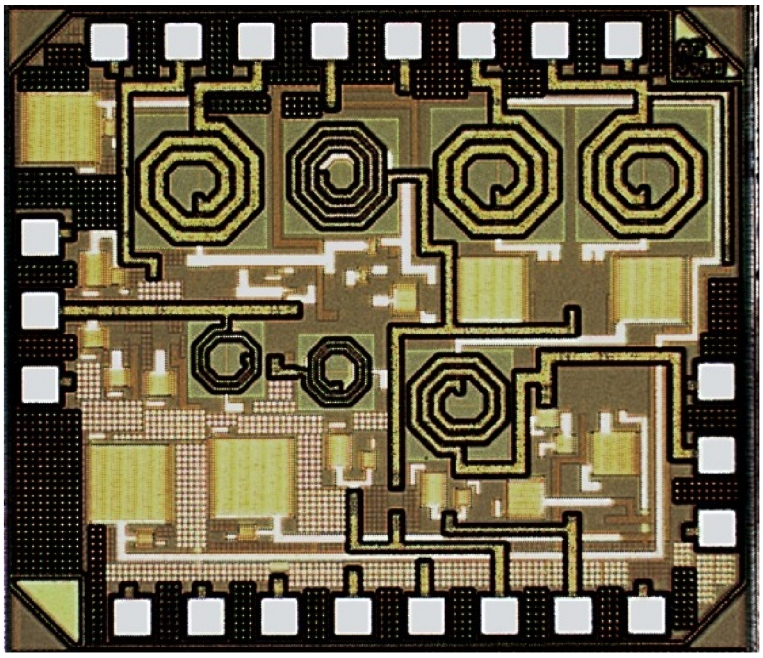


Figure 3.9. Fully integrated triple-band power amplifier using 130nm CMOS process with size of 1.5 mm × 1.5mm.

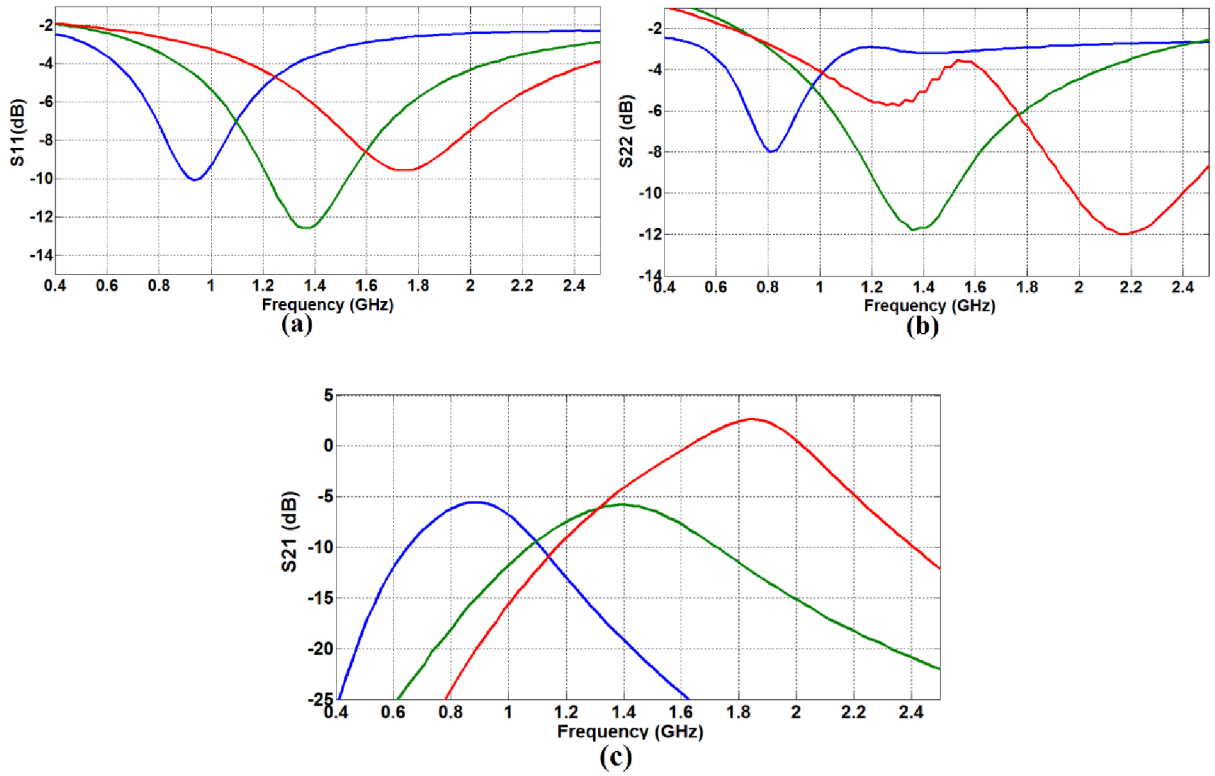


Figure 3.10. Measured S-parameter results of the proposed triple-band power amplifier, (a) S11 (b) S22, and (c) S21.

Figure 3.10 (c) shows the measured small-signal gain (S21) of the proposed triple-band power amplifier. The measured result demonstrates a perfect tunability at expected operating frequencies. However, the S21 gain is around 0dB. The measured results still shows an RF leakage/loss through RF path from input port to the output port, although the measured gain result is approximately 20dB better than recorded gain of the taped-out chip in chapter 2. This improvement concludes that using switches in shunt path (with respect to switches in the RF path) could decrease the amount of RF loss/leakage.

3.3. Multi-Band Power Amplifier Using Switchable Matching Networks

In this section, a dual-band CMOS power amplifier is presented by using two switchable matching networks, one for the lower band and one for the higher band. A driver stage is also used to boost the total gain of the power amplifier.

3.3.1. Macro-Model

Figure 3.11 shows macro-model of the proposed two-stage dual-band power amplifier. Two switchable input and two switchable output matching networks are used to cover the lower and the higher frequency bands. Four switches of S1 are used to switch *ON/OFF* the matching networks related to the lower frequency band of 900MHz. Likewise, four switches of S2 are used to switch *ON/OFF* the matching networks related to the higher frequency band of 1900MHz.

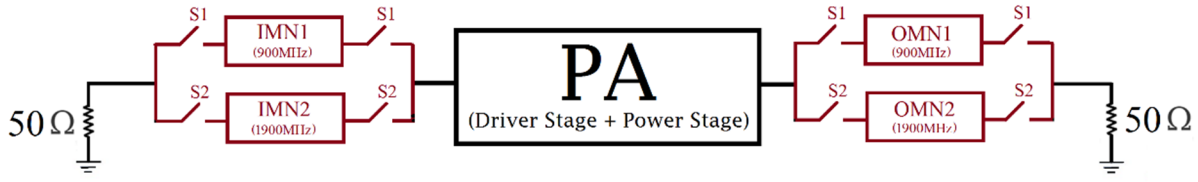


Figure 3.11. Macro-model of the proposed multi-band power amplifier using switchable matching networks.

3.3.2. Micro-Model

Micro-model of the proposed tunable power amplifier is shown in Figure 3.12. The proposed tunable power amplifier consists of driver stage, power stage, and switchable input/ interstage/output matching networks. The driver stage consists of a common-source amplifier with VG1=0.9V and VDD=1.2V, and current of 120mA. The power stage consists of two cells of cascode amplifiers, which each one draws current of 320mA with gate biases of VG2=0.9V, and VG3=2.1V. Size of the driver stage transistor is 400µm/120nm. In power stage, the size of the upper and lower transistors in cascode architecture are 2.0mm/120nm and 1.6mm/120nm, respectively. DC bias conditions of the driver and power stages are listed in Table 3.9. Furthermore, details of the design parameters is depicted in the Figure 3.12. Table 3.10 shows the truth-table of the proposed power amplifier. When the Vcont1 is *ON* and Vcont2 is *OFF*, the PA operates at the lower frequency band. Similarly, the PA operates at the higher frequency band when Vcont1 is *OFF* and Vcont2 is *ON*.

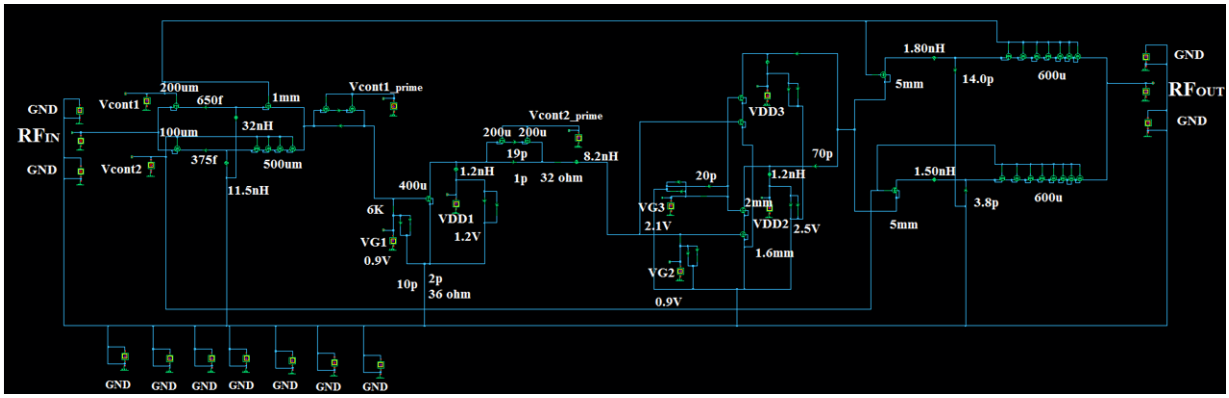


Figure 3.12. Micro-model of the proposed dual-band power amplifier.

Table 3.9. DC bias conditions of the driver and power stages

VG_1	VDD_1	ID_1	VG_2	VG_3	VDD_2=VDD_3	ID_2=ID_3
0.9V	1.2V	120mA	0.9V	2.1V	2.4V	320mA

Table 3.10. Truth-table of the proposed dual-band power amplifier

	Vcont1	Vcont2	Vcont1_prime	Vcont2_prime
B1(900MHz)	ON	OFF	ON	OFF
B2(1900MHz)	OFF	ON	OFF	ON

3.3.3. Simulated Results

The simulated results of the proposed dual-band power amplifier are shown in Figure 3.13. Input reflection coefficient (S11) and output reflection coefficient (S22) in dB scale are shown in Figure 3.13 (a) and (b), respectively. S11 and S22 are less than -10dB in both frequency ranges. Thus, a perfect impedance matching in input and output of the tunable power amplifier is achieved. As shown Figure 3.13 (c), small-signal gain (S21) of the proposed dual-band PA is 29.5dB at the lower frequency band, and 28.2dB at the higher frequency bands. Figure 3.13 (d) shows output power of the proposed power amplifier when the PA is in saturation condition (Pin=0dBm). The proposed dual-band PA provides saturated output power of 24.5/26.2dBm at 900/1900MHz, respectively.

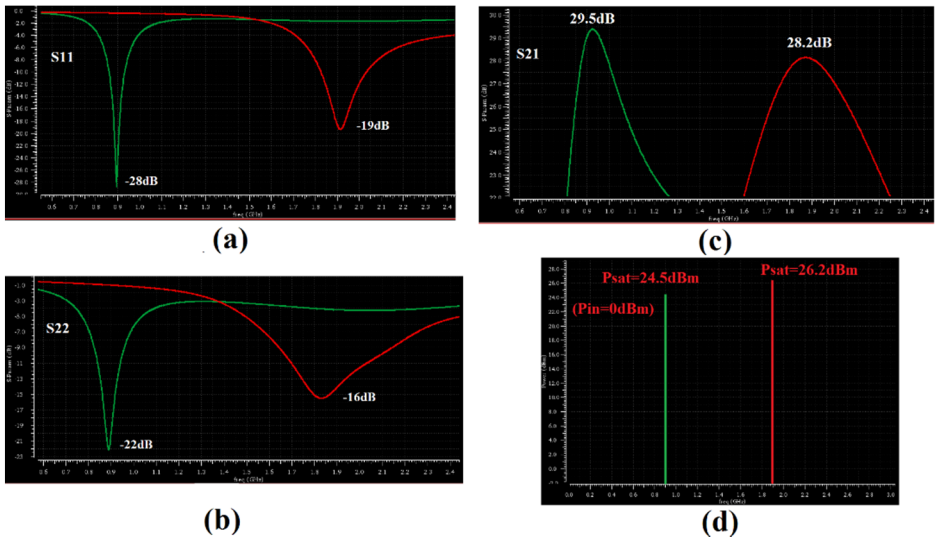


Figure. 3.13. Simulated results of the proposed PA, (a) S11, (b) S22, (c) S21, and (d) saturated output power with Pin of 0dBm.

3.3.4. Measured Results

Figure 3.14 shows die-photo of the fully integrated dual-band power amplifier in 130nm CMOS technology with the size of 1.5 mm × 1.5 mm including all DC and RF bond-pads.

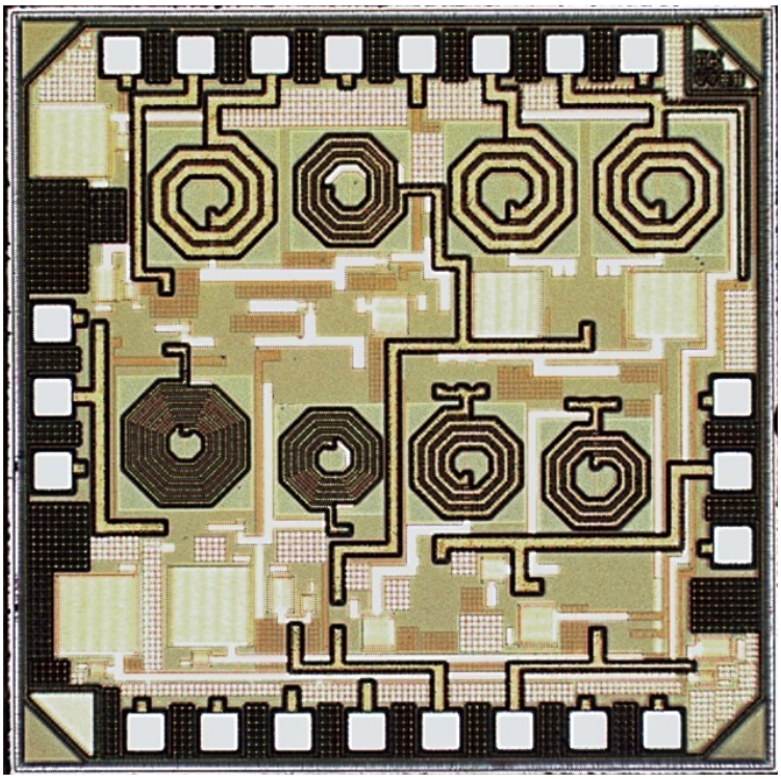


Figure 3.14. Fully integrated dual-band power amplifier using 130nm CMOS process with size of 1.5 mm × 1.5 mm.

Figures 3.15 demonstrates measured results of S-parameter. S11 and S22 show tunability at both the lower and the higher frequency bands. The measured results of S11 and S22 indicate that the switchable matching networks perform properly and have capability to switch the operating frequency from one band to another one, only by turning an external DC control voltage *ON/OFF*. Figure 3.15 (c) shows the measured S21 gain of the proposed dual-band power amplifier. The measured result demonstrates a perfect tunability at expected operating frequencies. However, the S21 gain is around -20dB, and there is huge discrepancy between measured and simulated results.

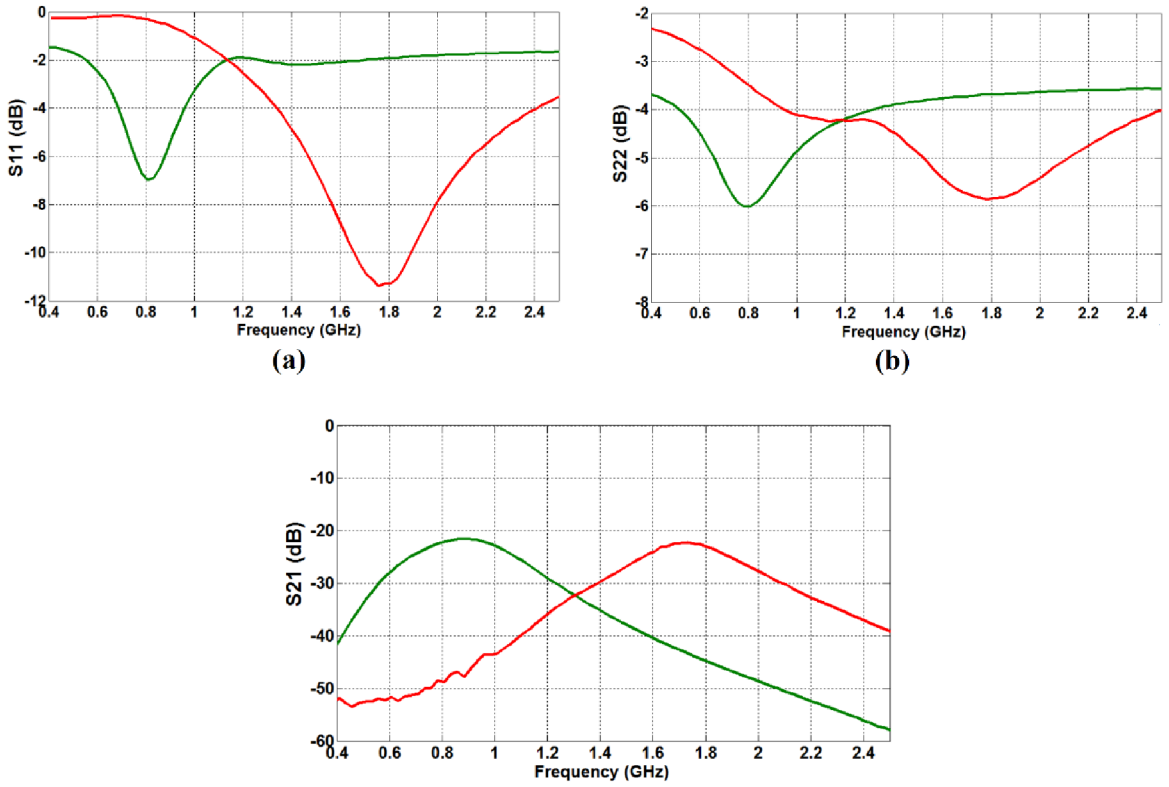


Figure. 3.15. Measured S-parameter results of the proposed dual-band power amplifier, (a) S11, (b) S22, and (c) S21.

3.4. Discussion

As both chips presented in this chapter, are taped-out at the same scheduled fabrication run, the following discussions are correct for both of them. The cascode topology in the chip presented in chapter 2, was designed with simulated current of 400mA. However, each unit cell of cascode could only draw current of 80mA in measurement (20% of the designed current). It was observed that the ground resistance of the chip was 1Ω. It was also discussed in chapter 2 that a grid of ground plane with sub-cell of 2.5µm×2.5µm with a hole in the middle with size of 1.0µm × 1.0µm will cause a lower ground resistance. In this condition, M1 metal layer will have a pattern density of 84%. Moreover, using M1 ground plane on the backplane of the inductors in the circuit increases total area of the ground plane, which leads to a lower ground resistance.

According to the chips presented in this chapter, the designed current is 320mA for a cascode architecture. The measured current is 260mA, 80% of the designed current. Thus, the ground plane is calculated 0.4Ω for these chips.

Turning *ON* some switches in both chips presented in this chapter, impacts the DC performance of the power amplifiers. In the circuit presented in Figure 3.6, turning *ON* the switch of M8 in the input matching network, turns *OFF* the driver stage. Likewise, by turning *ON* either switches of M10 or M12, the current of the power stage drops to zero, which degrades the RF performance of the power amplifier (i.e. no gain).

In the second chip shown in Figure 3.12, switching *ON* the Vcont1_prime and Vcont2_prime makes, respectively, the driver stage and the power stage *OFF*. Based on the truth-table of the proposed dual-band power amplifier (Table 19), when the power amplifier operates at the lower band, Vcont1_prime is *ON*, which leads to a driver stage with no current. Similarly, when the power amplifier operates at the higher band, Vcont2_prime is *ON*. Hence, the power stage will be *OFF*, and the gain will be low. The RFIC simulator could not predict these issues. The solutions for these issues will be addressed in chapter 4.

The chip presented in section 3.3 is designed and taped-out without tie-down diodes in order to check whether the issue of S11 flatness (reported in Figure 2.9) due to connection of tie-down diodes in the gate of the transistors to the substrate, will be solved or not. Interestingly as depicted in Figure 3.15(a), the input reflection coefficient (S11) result shows the expected tunability at the targeted frequency bands.

3.5. Conclusion

Two two-stage multi-band CMOS power amplifiers with different tunability techniques are presented in this chapter. The first approach is a well-known technique for designing multi-

band PA, which uses 1) switches in shunt path and 2) variable passive components. The S-parameter results explicitly show that the designed reconfigurable matching networks provide perfect tunability for three targeted frequency bands. However, the S21 gain is not adequate for an RF power amplifier. This traditional design concludes that using switches in shunt path (with respect to switches in the RF path) could decrease the amount of RF loss/leakage.

In the second part of this chapter, a dual-band power amplifier with switchable matching networks is designed and taped-out. The measured results demonstrate tunability of the proposed PA. The dual-band power amplifier could operate at the lower and the higher frequency bands by switching the respective matching networks *ON* and *OFF*.

As a conclusion, there is a big discrepancy between simulation results and measured results in both taped-out chips in this chapter. The reasons of these discrepancies and the solutions to modify the failure chips will be addressed in the chapter 4.

CHAPTER 4. UNDERSTANDING THE FAILURE OF CHIPS AND FINDING A SOLUTION

4.1. Introduction

As discussed in chapter 2 and chapter 3, although the taped-out chips show a good tunability at the targeted frequency bands, it is observed that there is a huge RF leakage/loss in the circuits, which leads to small-signal loss instead of gain. In the proposed multi-band power amplifier, there are too many switches in RF path from the input port to the output port in order to switch *ON/OFF* the operating frequencies. A 1~2dB loss in each switch, which is not predicted in the RFIC simulator, gives a huge discrepancy between simulation and measurement results.

In this chapter, a thorough investigation is done, which leads to address the major issues regarding to design a high-power RF switch. Bulk-source connection, DC isolation, and DC path of an RF switch are studied, and a solution for each issue is provided. Eventually, an architecture for a high-power RF switch is proposed, and a modified version of a band-switchable CMOS power amplifier is presented by utilizing the proposed switch architecture.

Moreover in section 4.3, the effect of the substrate thickness on RF performance (such as operating frequency and output power) of an RFIC chip is analyzed, which leads to a reliability study towards implementing ultra-thin flexible electronics applications.

4.2. Major Issues Regarding to Design a High-Power RF Switch

4.2.1. Bulk-Source Connection

Metal-oxide-semiconductor (MOS) transistor is a 4-terminal device. Gate, drain and source are the three terminals that are used to control the transistor, but the bulk or body, if not properly biased, may put the transistor inoperable. The P-N junction defined by source-bulk, which is basically a diode, must be reverse-biased to avoid leaking the current from the source terminal to

the substrate. That means that the source potential must always be equal or greater than the bulk potential.

The voltage difference between the source and the bulk (V_{BS}) changes the depletion width of the PN junction, and therefore increases the voltage across the oxide due to the change of the charge in the depletion region. This results in a difference in threshold voltage (V_{TH}) which equals the difference in charge in the depletion region divided by the oxide capacitance. Increase in the threshold voltage can degrade the DC and RF performances of the device, and can end up causing reliability issues. Thus, it is generally recommended to connect the bulk to the source terminal of the device to avoid the body effect.

Figure 4.1 shows the switch architecture which is used in the circuit design of the chips presented in chapter 2 and chapter 3. As shown in Figure 4.1, the bulk terminal of the switch is purposefully connected to the source terminal to avoid the body effect. However, after taping-out and measuring the chips, it is observed that this bulk to source connection can cause a huge RF leakage from source terminal to the substrate, and drastically degrades the RF performance of the circuit. In the proposed tunable power amplifiers designed in chapter 2 and chapter 3, there are approximately 15~20 switches in the RF path for each frequency band. If each switch creates 1~2dB loss due to the RF leakage from source terminal to the substrate, there would be 20~30dB loss in total, and it explains the discrepancy between simulation and measurement results of the chips presented in chapter 2 and chapter 3.

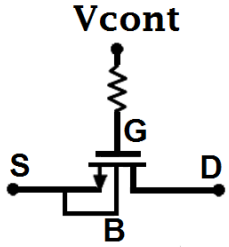


Figure 4.1. Architecture of the switch used in design of the chips presented in chapter 2 and 3.

As a **solution for bulk connection** in design of a high-power RF switch, there are two options, 1) keeping the bulk terminal open, 2) connecting the bulk terminal to the lowest potential in the circuit.

If there is not a contact to the body, the bulk terminal would be free to float, and there would not be any control on the effect of the bulk terminal on the transistor performance. So, it is not wise to keep the bulk terminal float. The best solution is to connect the bulk terminal to the lowest potential in the circuit, which a) prevents forward biasing the source-bulk junction diode, and b) avoid RF leakage from the source terminal to the substrate.

4.2.2. DC Isolation of an RF Switch

As discussed in section 3.4, during measurement of the both chips presented in chapter 3, turning *ON* some switches impacts the performance of the amplification stage (either the driver stage or the power stage). In the circuit presented in Figure 3.6, turning *ON* the switch of M8 drops the DC current of the driver stage close to zero. So, the driver stage will have no DC current, which leads to very low gain. Likewise, by turn *ON* either switches of M10 or M12, the DC current of the power stage will drop to zero, which degrades the RF performance of the power amplifier.

In the second chip presented in Figure 3.14, switching *ON* the Vcont1_prime in the input matching network, makes the driver stage *OFF*. Similarly, switching *ON* the Vcont2_prime in the interstage matching network drops the DC current of the power stage to zero. When the power amplifier operates at the lower band, Vcont1_prime is supposed to be *ON*, which leads to a low gain because the driver stage draws no DC current in this condition. When the power amplifier operates at the higher frequency band, Vcont2_prime is *OFF*. Hence, the power stage will be *OFF*, and the gain will be low. This issue, which the RFIC simulator could not predict, occurs because

there is no DC isolation between switches and the gate of the transistors in the driver stage or power stage.

The **solution** will be to add a blocking capacitor to either side of the switch in order to isolate the switch from the DC biases of the driver or power stages. In other words, the blocking capacitor prevents the effect of the switches on DC performance of the power amplifier.

4.2.3. DC Path for an RF Switch

The drain current of an NMOS transistor in the triode linear region (linear region) is given by the Equation 4.1.

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS} - V_{th}) - \frac{V_{DS}}{2}\right] V_{DS} \tag{4.1}$$

where, μn is the low-field electron mobility in the channel, and Cox the gate oxide capacitance per unity area. This equation is valid only in the triode region when $V_{DS} < V_{GS}-V_{th}$.

The R_{DS}, or the large-signal channel resistance in the triode region is given by,

$$R_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \tag{4.2}$$

When the transistor is in saturation region (or active region) the drain current is given by,

$$I_D = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 \tag{4.3}$$

It concludes that for the MOSFET to work as a switch, it needs to be biased in the triode region. Figure 4.2 shows the relation between drain current (I_D) versus drain-source voltage (V_{DS}) for an ideal MOSFET transistor. The R_{DS} in the triode region is inversely proportional to the size of the transistor, so if a low power dissipation in the transistor is expected, a high W/L aspect ratio is needed, which leads to bigger parasitic capacitances of C_{GS} and C_{GD} [3].

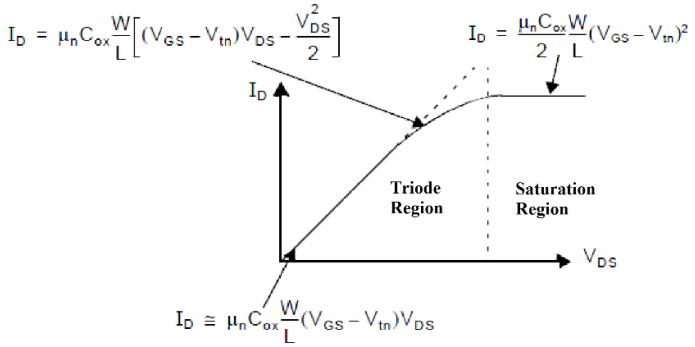


Figure 4.2. NMOS transistor operating regions.

An NMOS transistor operates as a switch when it is biased in triode region and carries a small amount of DC current. After adding two DC-blocking capacitors at both sides of a switch due to isolate the switch as discussed in section 4.2.2, there would not be a DC path for the transistor to flow its current. Thus, it degrades RF performance of the switch.

Moreover, the RFIC simulator could not predict DC behavior of a node connected between the blocking capacitor and the transistor. As an example in the circuit shown in Figure 3.6, the node between switch of M8 and capacitor of C2b has a random and unknown DC voltage according to the RFIC simulator. Likewise, the same happens for the node between switch of M10 and blocking capacitor of C3b.

Obviously, the **solution** is to provide a DC path for switch's current when the switch is ON and operates at triode region. This DC path can be achieved by connecting the drain and/or source of the switch to ground via a resistor (R_{SW}). This resistor of R_{SW} must be high enough to be considered as RF open to prevent RF leakage through ground.

Now, an important question is whether this DC path should consist of only one resistor which connects either source or drain terminal of the switch to ground, or there should be two symmetric R_{SW} connected in both drain and source terminals of the switch. To answer this question, as RFIC simulator could not predict difference between a balanced and an unbalanced

architecture, a simple prototype of a MOS switch with blocking capacitors is implemented on a breadboard in order to investigate which architecture is the best solution for the DC path of a switch. Figure 4.3 shows the prototype of the proposed architecture of a MOS switch. After carefully investigation of a few different scenarios, it is observed that the best architecture is a balanced DC path which consists of two symmetric (and high) resistors in both source and drain terminal of the switch.

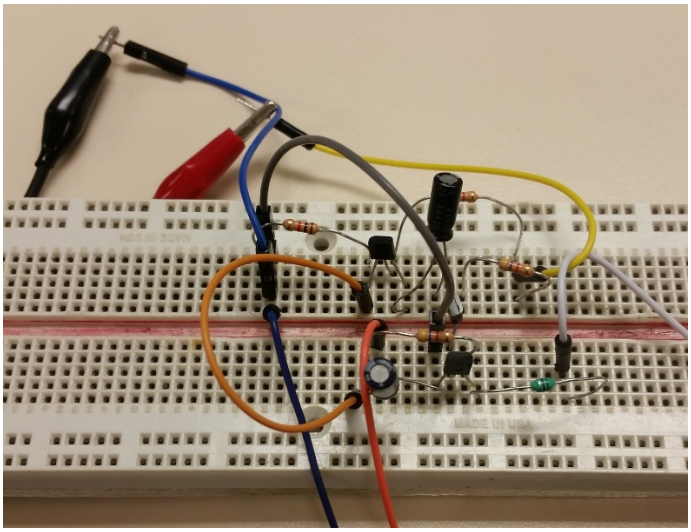


Figure 4.3. Prototype of the proposed switch implemented on a breadboard.

Figure 16 shows architecture of the proposed RF switch to be used in designing of a CMOS tunable power amplifier. Two blocking capacitors of Cj and Cj will be designed based on impedance matching conditions, and Rsw is set to 20kΩ to be an RF open. The bulk terminal is grounded, and the switch is being turned *ON/OFF* by an external control voltage of Vcont.

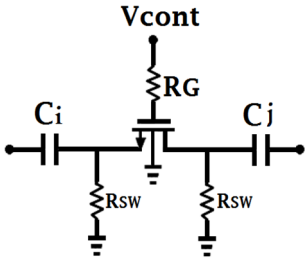


Figure 4.4. Proposed architecture for an RF switch.

4.3. RF Reliability Study of CMOS RFIC for Ultra-Thin Flexible Electronic Applications

4.3.1. Background

Next-generation electronic products are pushing the semi-conductor industry to integrate more ultra-thin and flexible integrated circuits (ICs). Ultra-thin and flexible ICs promote more efficient and cost-effective solutions that impact many applications like wireless communications, wearable electronics, Internet of Things, and healthcare monitoring. One of the main challenges of realizing flexible and ultra-thin ICs is the effect of die-substrate thinning on RF performances of an IC.

There are lot of challenges involved in realizing extremely thin ICs are due to the necessity of highly precise handling process of the ultra-thin ICs and probable electrical performance degradation as a result of die-substrate thinning [70]. The active regions of an extremely thin IC could be damaged due to ultra-thinning and subsequently adversely affect the overall performance of the ICs [71]. Most of the previous works [72]-[73] show the different aspects of IC substrate thinning, but only down to 40 μm. Most of them focus on electrostatic discharge performance, thermal characterization, and modelling of ultra-thin chips [74]. The impact of substrate thinning on overall RF performances of a fully integrated RFIC was never investigated before.

This section presents a radio-frequency reliability studies of fully integrated CMOS RFIC for next generation wireless communication applications involving conformal bodies where wireless communication RFICs will be embedded on ultra-thin flexible packages. As a test case, RF characteristics of a CMOS voltage-controlled oscillator (VCO) chip with multiple die-substrate thicknesses were measured and results are analyzed. Reliability of performances of the VCO chips are characterized and results are compared before and after die thinning from 250 to 50, 35, and 25μm, respectively. The impact on important parameters such as operating frequency, RF output

power, and DC performances due to die-substrate thinning was studied through measurement in this work.

4.3.2. Thinning and Characterization of the Chips

The standard die-substrate thickness of CMOS process is 250–300 µm [75]. Figure 4.5 demonstrates a layer map for 1-poly 6-metal 180 nm CMOS process technology, which has a substrate thickness of 250 µm. In order to accommodate die-to-die variations and some measurement error, 20 VCO chips have been used before and after thinning the die-substrate thickness in this study. Variations of measured results between dies with same thickness are averaged out. In first step, 20 VCO chips with default die-substrate thickness of 250 µm are characterized with respect to RF performances, in particular, operating frequency, and RF output power. In second step, 20 VCO chips are thinned and diced into four different die-substrate thickness tiers as follows: five chips with substrate thickness of 50 µm, five chips with substrate thickness of 35 µm, five chips with substrate thickness of 25 µm, and five chips with substrate thickness of 15 µm. All of the thinned dies are mounted on a thermal-release wafer tape, each having a temporary handle attached, and ready to be assembled with ultra-thin ICs [76].

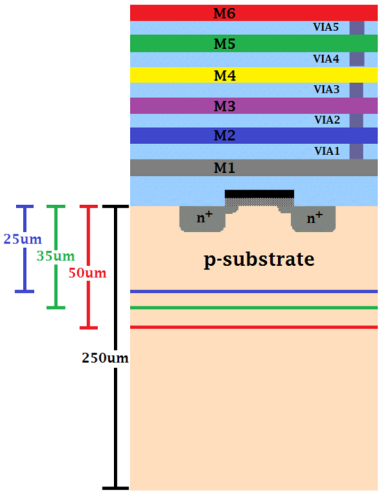


Figure 4.5. Layer map for CMOS 180nm 6-metal, 1-poly technology (The figure is not to the scale).

4.3.3. Results and Discussions

The average of the data related to dies with same thickness is set as a reference for each performance parameter. Die-substrate thickness factor (X) is defined in Equation (4.4) in order to have a better representation of data to compare the effect of different die-substrate thickness on the measured RF parameters.

$$X = \frac{\log(T)}{\log(T_0)} \tag{4.4}$$

where T is the die-substrate thickness of chip in µm, and T_0 is the default die-substrate thickness of 250 µm. Figure 4.6 shows normalized frequency deviation of the chips versus die-substrate thickness factor (X). It is observed that the operating frequency deviates <1% for die-substrate thickness >25 µm.

Figure 4.7 illustrates normalized RF output power deviation versus die-substrate thickness factor of X. It is observed that RF output power increases by 0.5 dB for substrate thickness of 50 µm, by 1 dB for 35 µm and by 1.1 dB for 25 µm.

The DC parameters for different die-substrate thicknesses are summarized in Table 4.1, which shows that the DC parameters remain fairly similar for different substrate thicknesses.

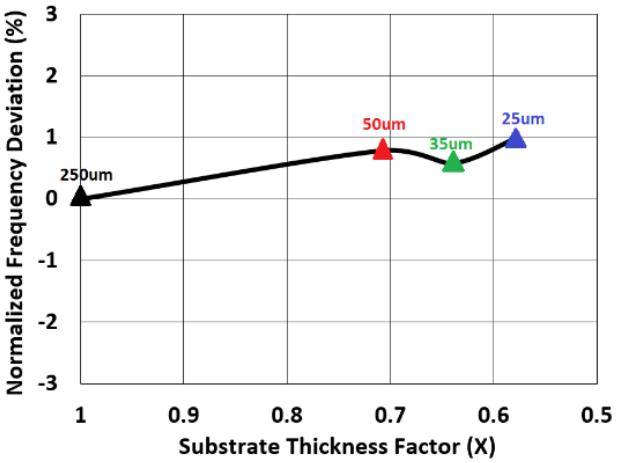


Figure 4.6. Normalized frequency deviation versus die-substrate thickness factor (X).

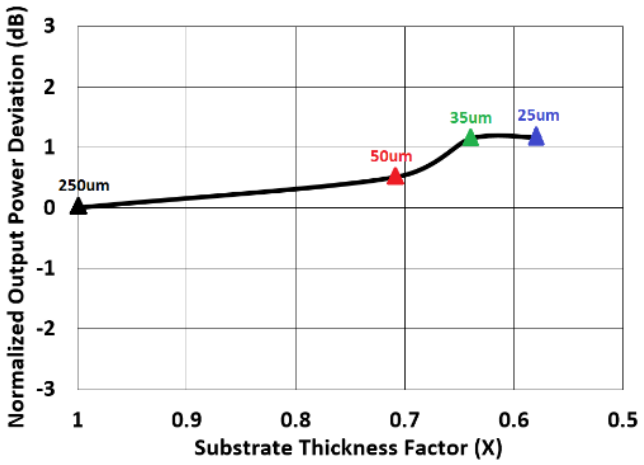


Figure 4.7 Normalized RF output power deviation versus die-substrate thickness factor (X).

Table 4.1. Comparison of DC parameters for different die-substrate thickness

Substrate Thickness (µm)	250	50	35	25
DC Current (mA)	24.55	24.37	25.03	24.20

To reinforce the validity of this reliability study, five VCO chips with substrate thickness of 15 µm were also characterized. However, during the characterization the chips cracked while probing, which indicates a limitation for minimum realizable die-substrate thickness.

The deviations of operating frequency and output power are, respectively, within ±1% and ±1 dB, which (a) shows insensitivity of an RFIC chip to die-substrate thinning, (b) indicates good feasibility towards flexible electronic applications realization.

4.4. A 900/1900-MHz Band-Switchable CMOS Power Amplifier

This section presents a band-switchable RF power amplifier fully-integrated in 130nm CMOS process. A two-stage power amplifier with switchable input and output matching networks is designed in order to tune the center frequency in use. The proposed CMOS PA can operate at 900MHz and 1900MHz as the lower and the higher operating frequencies, respectively. Thus, 4G LTE, 5G NR, and quad-band GSM standards for cellular applications can be covered.

4.4.1. Macro-Model

Macro-model of the proposed band-switchable power amplifier is shown in Figure 4.8. Two input matching networks and two output matching networks are used to match input and output impedances of the power amplifier to 50Ω. Truth-table of the proposed band-switchable power amplifier is indicated in Table 4.2.

By turning-*ON* the S1 and turning-*OFF* the S2, the power amplifier operates at the lower frequency band of 900MHz. In other condition, the power amplifier operates at the higher frequency band of 1900MHz when S1 and S2 are, respectively, switched *OFF* and *ON*. As discussed previously, Figure 4.9 shows architecture of the proposed RF switch which is used for designing S1 and S2. The switch is formed by an NMOS transistor which is being switched *ON* and *OFF* by an external DC control voltage on the gate terminal of the transistor. In order to minimize the power dissipation through substrate, bulk terminal of the transistor is grounded. Moreover, in order to isolate drain and source terminals of the switch from DC supply, two capacitors are used at either side of the switch. Ci and Cj will be designed based on impedance matching conditions in each section of the circuit.

A transistor operates as a switch when it is in triode operating region and carries a small amount of DC current. In this architecture, drain and source terminals of the switch are connected to ground by using resistor of R_{SW} to provide a balanced DC path for the current of the switch. Otherwise, the switch does not operate properly. The switching time is 2ns in this case.

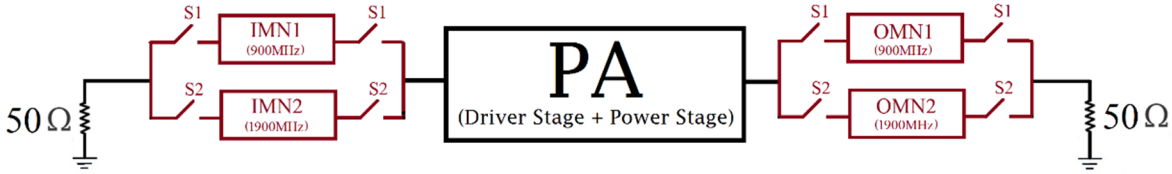


Figure 4.8. Macro-model of the proposed 900/1900MHz band-switchable power amplifier.

Table 4.2. Truth-table of band-switchable power amplifier

Band	Operating Frequency	Vcont1 (S1)	Vcont2 (S2)
B1	900MHz	ON	OFF
B2	1900MHz	OFF	ON

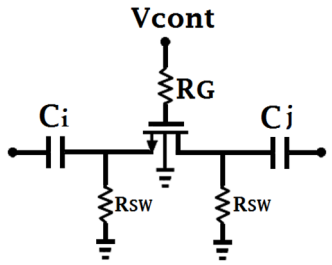


Figure 4.9. Architecture of the proposed RF switch.

4.4.2. Micro-Model

Micro-model in transistor level of the proposed band-switchable power amplifier is illustrated in Figure 4.10. A two-stage power amplifier is designed including driver stage to increase the gain, and power stage to boost the output power. The driver stage consists of common source topology with transistor size of 400µm/120nm, whereas the power stage is formed by one cell of cascode topology with transistors size of 2.5mm/120nm and 2.0mm/120nm. Transistors in the drive stage and the power stage operate in Class-AB mode with DC current of 60mA and 315mA, respectively. The driver stage and power stage DC bias conditions and design parameters are summarized in Table 4.3 and Table 4.4, respectively. In order to obtain maximum power transfer from input source and also drive output antenna effectively, input and output matching networks are designed at both targeted frequency bands of B1=900MHz, B2=1900MHz by using T-matching network and RF switches described earlier. Design parameters of the input matching networks (IMN1/IMN2) and the output matching networks (OMN1/OMN2) are listed in Table 4.5 and Table 4.6, respectively.

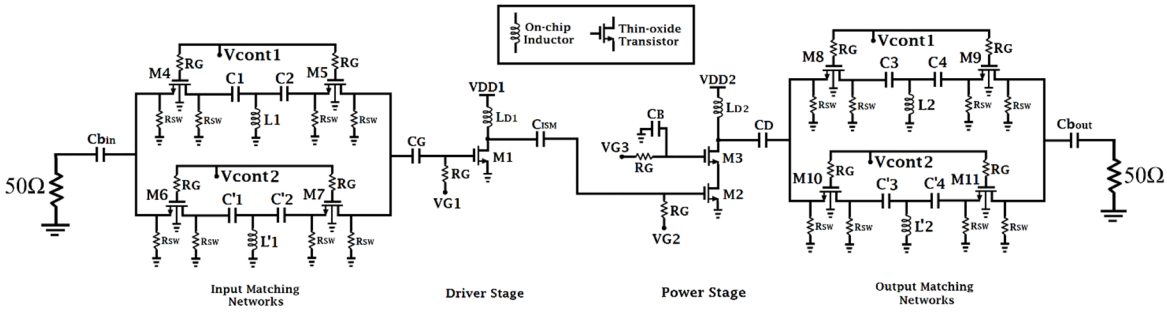


Figure 4.10. Micro-model of the proposed 900/1900MHz band-switchable power amplifier.

Table 4.3. DC bias conditions of the driver and power stages

Driver Stage			Power Stage			
VG_1	VDD_1	ID_1	VG_2	VG_3	$VDD_2=VDD_3$	$ID_2=ID_3$
0.7V	1.2V	60mA	0.7V	1.8V	2.4V	315mA

Table 4.4. Design parameters of driver and power stages

L_{D1}	L_{D2}	C_G	C_{ISM}	C_D	R_G	C_B	W_1	W_2	W_3
2.5nH	2.0nH	500fF	16.0pF	50pF	6KΩ	20.0pF	400um	2.0mm	2.5mm

Table 4.5. Design parameters of input matching networks

C_1	L_1	C_2	C'_1	L'_1	C'_2	R_{SW}	Cb_{in}	$W_4=W_5=W_6=W_7$
1.0pF	21.2nH	5.0pF	0.6pF	7.0nH	2.0pF	20KΩ	30pF	250um

Table 4.6. Design parameters of output matching networks

C_3	L_2	C_4	C'_3	L'_2	C'_4	R_{SW}	Cb_{out}	$W_8=W_{10}$	$W_9=W_{11}$
4.0pF	7.2nH	2.0pF	2.5pF	2.2nH	1.7pF	20KΩ	30pF	2.0mm	250um

4.4.3. Simulated Results

S-parameters results of the proposed band-switchable power amplifier are illustrated in Figure 4.11. Input and output reflection coefficients in dB scale, respectively, are shown in Figure 4.11(a) and Figure 4.11(b). A perfect impedance matching in input and output of the proposed band-switchable PA is achieved at both the lower and the higher frequency bands. Figure 4.11 (c) demonstrates small-signal gain of 31.2/32.0 dB at 900/1900 MHz, respectively.

Figure 4.11 (d) shows large-signal performance of the proposed dual-band power amplifier versus frequency when the PA is in saturation condition (Pin=0dBm). The proposed band-switchable PA provides saturated output power (Psat) of 22.73/23.36 dBm, and repective 3-dB bandwidth of 550/600 MHz at the lower and the higher frequency bands, respectively. Performane of the proposed band-switchable CMOS power amplifier is summarized in Table 4.7.

By setting control voltages of Vcon1 and Vcont2 to *ON/OFF* and *OFF/ON*, respectively, the power amplifier operates at B1 and B2. Saturated output power of 22.72/23.36 dBm, output 1-dB compression point (P1dB) of 20.2/20.8 dBm, and power added efficiency (PAE) of 23.5/26.0% are achieved at 900/1900 MHz, respectively.

Table 4.7. Performance summary of the proposed band-switchable power amplifier

Band	**Frequency (MHz)**	**S21 (dB)**	**Psat (dBm)**	**PAE (%)**	**P_{1dB} (dBm)**	**3-dB Power Bandwidth (MHz)**
B1	775-1325	31.2	22.72	26.5	20.2	550
B2	1650-2250	32.0	23.36	23.0	20.8	600

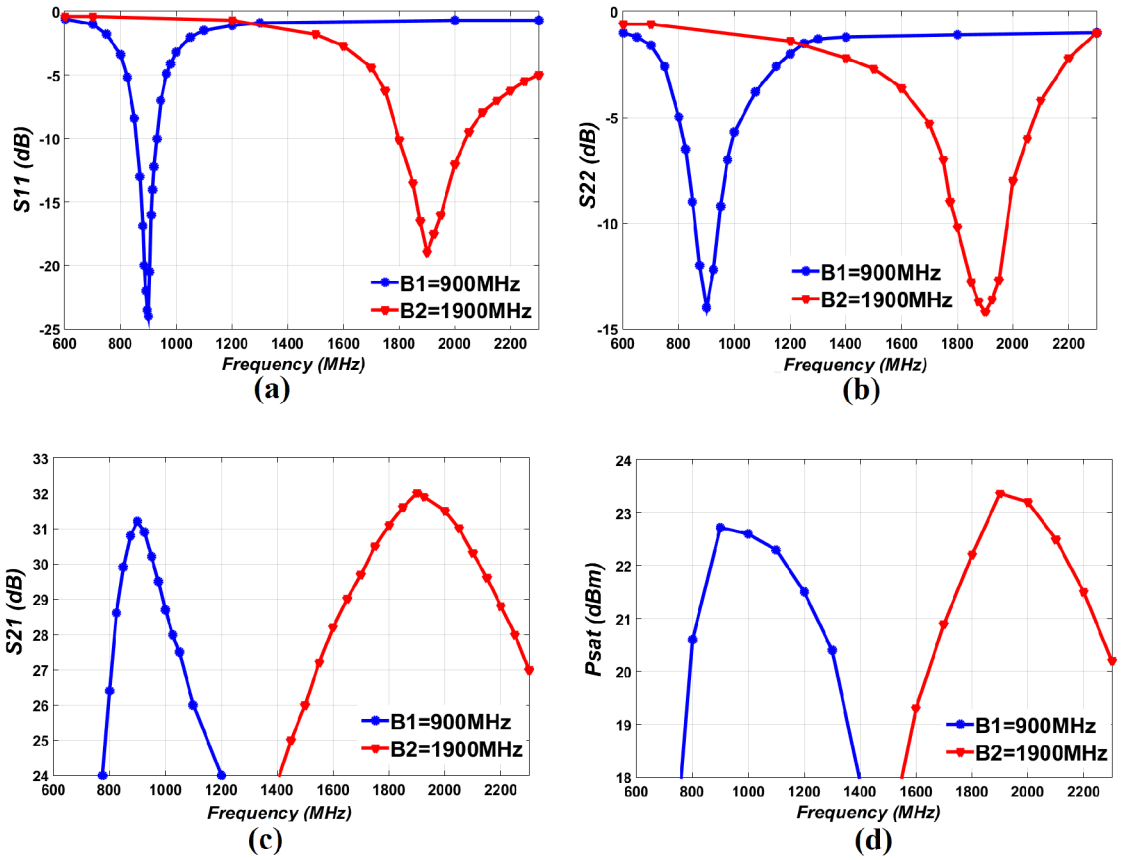


Figure 4.11. Simulated results of the proposed band-switchable PA, (a) S11, (b) S22, (c) S21, and (d) saturated output power (Psat) versus frequency.

4.5. Conclusion

The major issues regarding to design a high-power RF switch are addressed in this chapter. If bulk terminal in a four-terminal transistor is not properly bias, it may degrade DC and RF performances of a device. As discussed in this chapter, connecting the bulk terminal to the source, or keeping the bulk terminal open is not a good idea for designing an RF switch. The best solution is to connect the bulk terminal to the lowest potential in the circuit, which a) prevents forward biasing the source-bulk junction diode, and b) avoid RF leakage from the source terminal to the substrate. During measurement of both chips presented in chapter 3, turning *ON* some switches impacts the performance of the driver stage or the power stage. In other words, there is not a DC isolation between switches and gate terminal of the transistors in the driver and power stages. As

a solution, adding a blocking capacitor prevents the effect of the switches on DC performance of the power amplifier. An NMOS transistor operates as a switch when it operates in triode region and carries a small amount of DC current. Thus, in order to operate properly, this switch need a DC path to flow its current. It is observed that the best architecture is a balanced DC path which consists of two symmetric (and high) resistors in both source and drain terminal of the switch.

Moreover in section 4.3, the effect of the substrate thickness on RF performance parameters, such as operating frequency and output power, of an RFIC chip is studied. The deviations of frequency and output power are, respectively, within ±1% and ±1 dB, and the DC current remains fairly similar for different substrate thicknesses. This reliability study proves that die-substrate thickness does not have huge effect on DC and RF performances of an RFIC chip, which leads toward implementing ultra-thin flexible electronics applications.

Furthermore, a modified version of a band-switchable CMOS power amplifier is presented in this chapter by utilizing the proposed architecture of a high-power switch. However, this design could not be fabricated due to non-availability of fabrication run by a commercial foundry for 130nm CMOS process. This chapter also concludes a lack of precision of the RFIC simulator in predicting the following items,

1. Ground resistance of the chip, which causes a discrepency between the designed and measured DC currencts.
2. Effect of turning-*ON* a switch on the DC performance of the amplification stages.
3. RF leakage through the substrate due to bulk to source connection in a high-power switch, (which is generally recommended to use in order to avoid body effect).
4. Random unknown voltages in the nodes between a blocking capacitor and a amplification transistor.

CHAPTER 5. DESIGN AND IMPLEMENTATION OF A FULLY INTEGRATED BAND-SWITCHABLE POWER AMPLIFIER USING BIT-OPTIMIZED RECONFIGURABLE NETWORK (BORN) IN 180nm CMOS PROCESS

5.1. Introduction

This chapter, for the first time, presents a band-switchable RF power amplifier by using a novel approach toward switching matching networks. In this approach, which is called **B**it **O**ptimized **R**econfigurable **N**etwork **(BORN)**, two matching networks which can be controlled by digital bits will provide three operating frequency bands for the power amplifier.

After thoroughly investigating the failure of chips presented in the previous chapters, and non-availability of fabrication run by a commercial foundry for 130nm CMOS process, the proposed fully integrated BORN PA is designed and implemented in 180nm CMOS process. The simulated and measured results of BORN PA will be presented in this chapter.

5.2. The Proposed RF Switch

Before presenting the proposed BORN architecture, a resistive body floating technique and 6-terminal triple-well NMOS as a robust RF switch topology will be discussed.

5.2.1. Resistive Body-Floating Technique

For improved power handling capacity of an RF switch, body-floating technique is usually employed to cut down the signal loss through body junctions of the transistors [77]. By conventional design, transistor body is usually attached directly to source or drain terminal and drain to source current is negligible under low input power. As input power increases, the diode between drain and body tends to turn on the extreme reversed bias on drain and source, which results in lower input impendence of the transistor [78]. The waveform of the input signal is then clamped, and the P1dB of the circuit will be limited. By connecting a large resistor (R_{SW}) to the

body of the transistor, high input impendence of the transistor is maintained and thus gives the switch better power performance, particularly in the wide-band frequency range.

5.2.2. Triple-Well NMOS

To handle high-voltage signals with typical MOS transistors, device terminals are generally floated. In CMOS process, substrate floating may degrade the performance due to the low substrate resistivity [79]. To solve the problem, triple-well NMOS transistor is used in this design. In such a structure, P-well of the transistor is embedded within a deep N-well to create an isolated body from the P-substrate, as shown in Figure 5.1 [80]-[81]. This detaches the body from the substrate and offers to bias the body of the transistor and deep N-well separately. Thus, design robustness will be improved [82].

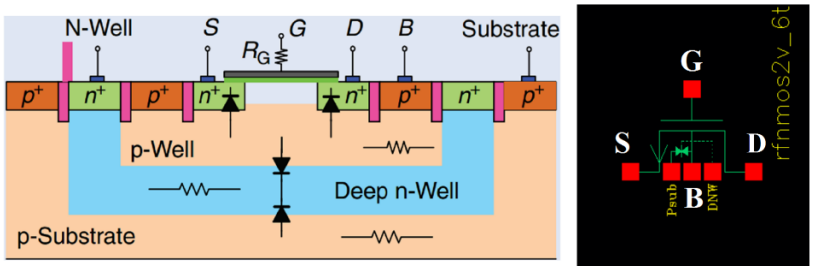


Figure 5.1. Structure of a Triple-well NMOS transistor [83].

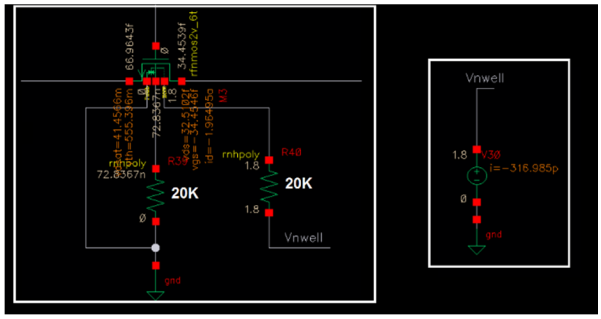


Figure 5.2. 6-terminal triple-well NMOS transistor.

Figure 5.2 shows the proposed architecture of an RF switch which will be used in the design of the proposed BORN power amplifier. A 6-terminal triple-well NMOS is used as a switch,

which the substrate is directly connected to ground, deep n-well is connected to V_{DD} via a 20K resistor, and buried p-well is connected to ground via a 20K resistor. This architecture will be applied to all switches in the circuit.

5.3. Macro-Model of BORN PA

As presented in the previous chapters, a band-switchable power amplifier can be designed by using two impedance matching networks at input side of the PA, and two impedance matching networks at output side of the PA. Each matching network is controlled by an external supply voltage. When control voltage of each matching network is switched *ON*, the power amplifier operates at the respective frequency band. In other words, by setting control voltages of Vcon1 and Vcont2 to *ON/OFF* or *OFF/ON* condition, respectively, the power amplifier operates at the lower or the higher frequency band. Now, an interesting question is what will happen when both control voltages are simultaneously turned *ON*. Is it possible to provide a third frequency band (probably a middle band) in this condition?!

This chapter explains a solution for the question of creating a middle frequency band by simultaneously turning *ON* both the lower and the higher frequency band. This is a novel idea for designing a multi-band power amplifier, which is proposed, for the first time, in this research. The proposed architecture is being called **B**it **O**ptimized **R**econfigurable **N**etwork (**BORN**) because desired frequency band of operation can be selected through the control of digital bits.

Macro-model of BORN PA is shown in Figure 5.3. Two input matching networks and two output matching networks are used to match input and output impedances of the power amplifier to 50Ω. Table 5.1 demonstrates truth-table of BORN PA. The power amplifier operates at the lower frequency band when S1 and S2, respectively, are switched *ON* and *OFF*. In contrast, by turning-*OFF* the S1 and turning-*ON* the S2, the power amplifier operates at the higher frequency

band. In addition, there are two impedance mapping networks in the proposed BORN architecture, which need to be designed properly in order to provide the middle frequency band.

Input mapping network is used to map input impedance of the driver stage to an auxiliary impedance on smith chart in order to achieve the third frequency band when both control voltages are *ON*. Likewise, output mapping network changes output impedance of the power stage to an auxiliary impedance. Therefore, the combination of the two output matching networks, when both control voltages are *ON*, will match this auxiliary impedance to 50Ω at the middle frequency band.

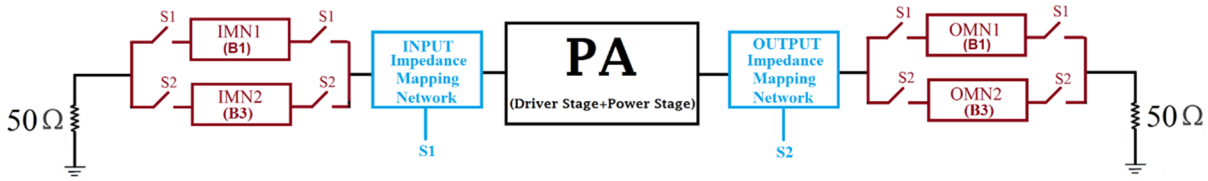


Figure 5.3. Macro-model of BORN PA.

Table 5.1. Truth-table of BORN PA

Band	Operating Frequency	Vcont1 (S1)	Vcont2 (S2)
B1	900MHz	1	0
B2	1400MHz	1	1
B3	1900MHz	0	1

5.4. Micro-Model of BORN PA

Micro-model of the proposed BORN PA is shown in Figure 5.4, which consists of a driver stage, a power stage, two input matching networks, an input mapping network, an output mapping network, and two output matching networks. The design procedures of these blocks are discussed as follows.

5.4.1. Driver and Power Stages

A two-stage power amplifier is designed with a driver stage, and a power stage. The driver stage consists of common-source topology with transistor size of 500µm/180nm. Gate voltage of VG1 and drain supply voltage of VDD1 are designed 1.2V and 1.8V, respectively. Hence, current of 120mA flows through M1 transistor.

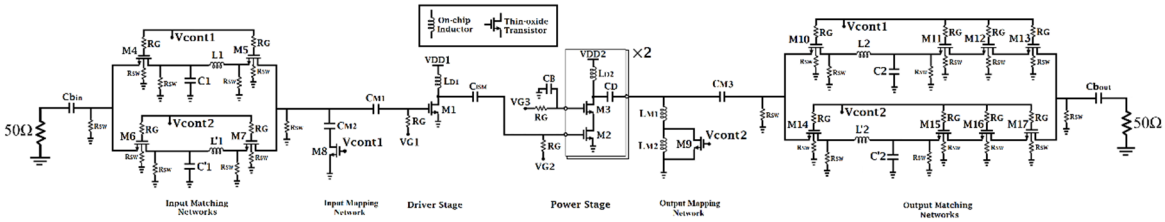


Figure 5.4. Micro-model of BORN PA.

The power stage is formed by two cascode cells, which output nodes of these two cells are tied together due to achieving power combining. Size of the upper and lower transistors in cascode architecture are 2.5mm/180nm and 1.5mm/180nm, respectively, and each cascode cell draws current of 300mA with gate voltages of VG2=1.2V and VG3=3.0V.

Inductors used as inductive load in drain terminals of the driver stage and the power stage are, respectively, 2.7nH, and 2.1nH. Gate resistor of R_G, blocking capacitor of C_{ISM}, and coupling capacitor of C_D are 20K, 45pF, and 45pF, respectively. In addition, capacitor of C_B which is used in gate of the common-gate transistor of the cascode topology, is designed 20pF in order to make a good RF short in the gate of the common-gate transistor, and also make drain-source voltages of VDS2 and VDS3 in phase. It increases output power after power combining in the output node of the power stage. DC bias conditions of the driver and power stages are listed in Table 5.2. Moreover, Table 5.3 summarizes design parameters of the driver and power stages.

Table 5.2. DC bias conditions of driver and power stages

Driver Stage			Power Stage			
VG_1	VDD_1	ID_1	VG_2	VG_3	$VDD_2=VDD_3$	$ID_2=ID_3$
1.2V	1.8V	120mA	1.2V	3.0V	3.6V	300mA

Table 5.3. Design parameters of driver and power stages

L_{D1}	L_{D2}	C_{ISM}	C_D	R_G	C_B	W_1	W_2	W_3
2.7nH	2.1nH	30pF	45pF	20KΩ	20.0pF	500um	1.5mm	2.5mm

5.4.2. The Proposed Input Mapping Network

Figure 5.5 shows architecture of input impedance matching networks which consists of two LC input matching networks of IMN1 and IMN2. The goal is to match Z_{S1}, Z_{S2}, and Z_{S3} to 50Ω, respectively, at three frequency bands of f_1, f_2, and f_3 ($f_1<f_2<f_3$).

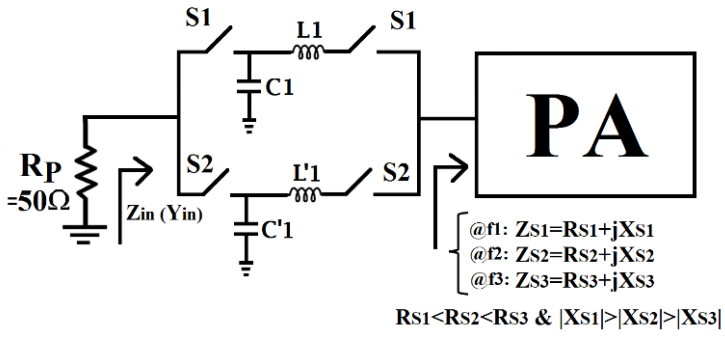


Figure 5.5. Architecture of input matching networks of IMN1 and IMN2.

In order to operating at the lower frequency band of f_1, the switch of S1 is turned *ON* and the switch of S2 is switched *OFF*. By neglecting the effect of IMN2 on IMN1 (assuming switches with good isolation), the following equations can be derived in theoretical calculation for the input impedance of Zin_1 (or the input admittance of Yin_1),

$$Yin_1 = \frac{1}{Zin_1} = \frac{1}{R_{S1} + jX_{S1} + j\omega_1 L_1} + j\omega_1 C_1 \tag{5.1}$$

$$Yin_1 = \frac{j\omega_1 C_1 R_{S1} - \omega_1 C_1 X_{S1} - \omega_1^2 L_1 C_1 + 1}{R_{S1} + j(\omega_1 L_1 + X_{S1})} = \frac{1 - \omega_1(\omega_1 L_1 + X_{S1}) + j\omega_1 C_1 R_{S1}}{R_{S1} + j(\omega_1 L_1 + X_{S1})} \tag{5.2}$$

After multiplying numerator and denominator by the conjugate of the denominator, and simplification,

$$Yin_1 = \frac{R_{S1}}{R_{S1}^2 + (\omega_1 L_1 + X_{S1})^2} + j\,\frac{\omega_1 C_1 R_{S1}^2 - (\omega_1 L_1 + X_{S1}) + \omega_1 C_1 (\omega_1 L_1 + X_{S1})^2}{R_{S1}^2 + (\omega_1 L_1 + X_{S1})^2} \tag{5.3}$$

According to maximum power transfer theorem at the input port of the power amplifier,

$$\mathrm{Re}\{Yin_1\} = \frac{1}{R_P} \tag{5.4}$$

$$\frac{R_{S1}}{R_{S1}^2 + (\omega_1 L_1 + X_{S1})^2} = \frac{1}{R_P} \tag{5.5}$$

Thus,

$$\boxed{L_1 = \frac{R_{S1}\sqrt{\frac{R_P}{R_{S1}} - 1} - X_{S1}}{\omega_1}} \tag{5.6}$$

Moreover,

$$\mathrm{Im}\{Yin_1\} = 0 \tag{5.7}$$

$$\frac{\omega_1 C_1 R_{S1}^2 - (\omega_1 L_1 + X_{S1}) + \omega_1 C_1 (\omega_1 L_1 + X_{S1})^2}{R_{S1} R_P} = 0 \tag{5.8}$$

Hence,

$$\boxed{C_1 = \frac{1}{\omega_1 R_P}\sqrt{\frac{R_P}{R_{S1}} - 1}} \tag{5.9}$$

In order to operate at the higher frequency band of f_3, when the switch of S1 is *OFF* and the switch of S2 is switched *ON*, same calculations for max power transferring lead to

$$\mathrm{Re}\{Yin_3\} = \frac{1}{R_P} \quad \rightarrow \quad \boxed{L'_1 = \frac{R_{S3}\sqrt{\frac{R_P}{R_{S3}} - 1} - X_{S3}}{\omega_3}} \tag{5.10}$$

$$\mathrm{Im}\{Yin_3\} = 0 \quad \rightarrow \quad \boxed{C'_1 = \frac{1}{\omega_3 R_P}\sqrt{\frac{R_P}{R_{S3}} - 1}} \tag{5.11}$$

Furthermore, when both switches of S1 and S2 are simultaneously turned *ON*, the power amplifier operates at the middle frequency band of f_2, inductor of L1 will be in parallel with inductor of L'1, and capacitor of C1 will be in parallel with C'1, which theoretically results in

$$\begin{cases} L''_1 = L_1 \| L'_1 = \dfrac{L_1 . L'_1}{L_1 + L'_1} & (5.12) \\ C''_1 = C_1 \| C'_1 = C_1 + C'_1 & (5.13) \end{cases}$$

According to (5.13) for capacitors,

$$\frac{1}{\omega_2 R_P}\sqrt{\frac{R_P}{R_{S2}} - 1} = \frac{1}{\omega_1 R_P}\sqrt{\frac{R_P}{R_{S1}} - 1} + \frac{1}{\omega_3 R_P}\sqrt{\frac{R_P}{R_{S3}} - 1} \tag{5.14}$$

$$\Rightarrow \frac{1}{f_2}\sqrt{\frac{R_P}{R_{S2}} - 1} = \frac{1}{f_1}\sqrt{\frac{R_P}{R_{S1}} - 1} + \frac{1}{f_3}\sqrt{\frac{R_P}{R_{S3}} - 1} \tag{5.15}$$

By assuming $R_{Si} \ll R_P$ *or* $\frac{R_P}{R_{Si}} \gg 1$, equation (5.15) will be simplified,

$$\Rightarrow \frac{1}{f_2}\sqrt{\frac{R_P}{R_{S2}}} = \frac{1}{f_1}\sqrt{\frac{R_P}{R_{S1}}} + \frac{1}{f_3}\sqrt{\frac{R_P}{R_{S3}}} \tag{5.16}$$

Thus,

$$\boxed{\frac{f_2}{f_1}\sqrt{\frac{R_{S2}}{R_{S1}}}+\frac{f_2}{f_3}\sqrt{\frac{R_{S2}}{R_{S3}}}=1} \tag{5.17}$$

Due to $f_1<f_2<f_3$, the fraction of f_2/f_1 is greater than 1 ($f_2/f_1>1$). As a result, the equation (5.17) can be equal to 1 only if $R_{S2}< R_{S1}$. However, in practical case, the equation (5.17) cannot be equal to 1 due to $f_2/f_1>1$ and $R_{S2}/R_{S1}>1$, which means combination of two input matching networks of IMN1 and IMN2 does not have capability of matching the Z_{S2} to 50Ω at the middle frequency band of f_2 when both switches of S1 and S2 are *ON*. In other words, two matching networks cannot create the third frequency band.

As a solution, Z_{S2} must be mapped, on a smith-chart, to an impedance with a lower resistance than Z_{S1}. In other words, R_{S2} must be mapped to a resistance lower than R_{S1} ($R_{S2}<R_{S1}$). In addition, it should be noted that the position of the impedances of Z_{S1} and Z_{S3} are not critical until $R_{S2}<R_{S1}$ & $R_{S2}<R_{S3}$.

According to the inductors, by plugging (5.6) and (5.10) into (5.12),

$$\frac{R_{S2}\sqrt{\frac{R_P}{R_{S2}}-1}-X_{S2}}{\omega_2}=\left(\frac{R_{S1}\sqrt{\frac{R_P}{R_{S1}}-1}-X_{S1}}{\omega_1}\right)\|\left(\frac{R_{S3}\sqrt{\frac{R_P}{R_{S3}}-1}-X_{S3}}{\omega_3}\right) \tag{5.18}$$

By assuming $|X_{Si}| \gg R_{Si}$, equation (5.18) will be simplified,

$$\frac{|X_{S2}|}{f_2}=\frac{|X_{S1}|}{f_1}\|\frac{|X_{S3}|}{f_3} \tag{5.19}$$

$$\frac{f_2}{|X_{S2}|}=\frac{1}{\frac{|X_{S1}|}{f_1}\|\frac{|X_{S3}|}{f_3}}=\frac{1}{\frac{\frac{X_{S1}}{f_1}\cdot\frac{X_{S3}}{f_3}}{\frac{X_{S1}}{f_1}+\frac{X_{S3}}{f_3}}} \quad\Rightarrow\quad \frac{f_2}{X_{S2}}=\frac{f_3}{X_{S3}}+\frac{f_1}{X_{S1}} \tag{5.20}$$

Thus,
$$\boxed{\frac{f_3}{f_2}\frac{X_{S2}}{X_{S3}}+\frac{f_1}{f_2}\frac{X_{S2}}{X_{S1}}=1} \quad (5.21)$$

Due to $f_1<f_2<f_3$, the fraction of f_3/f_2 is greater than 1 ($f_3/f_2>1$). Therefore, the equation (5.21) can be equal to 1 only if $|X_{S2}|< |X_{S3}|$. However in practical case, $f_2/f_1>1$ and $X_{S2}/X_{S3}>1$ lead to a summation greater than 1 for equation (5.21), which means combination of two input matching networks of IMN1 and IMN2 does not have capability of matching the Z_{S2} to 50Ω at the middle frequency band of f_2 when both switches of S1 and S2 are simultaneously *ON*.

As a solution, Z_{S2} must be mapped, on a smith-chart, to an impedance with a lower reactance than Z_{S3}. In other words, X_{S2} must be less than X_{S3} ($X_{S2}<X_{S3}$) in order to have impedance matching at the middle frequency band. In addition, it should be noted that the position of the impedances of Z_{S1} and Z_{S3} are not critical until $X_{S2}<X_{S1}$ & $X_{S2}<X_{S3}$.

In order to implement the BORN architecture, an input mapping network is proposed in this section, which maps the resistance of R_{S2} to a lower resistance than R_{S1} ($R_{S2}<R_{S1}$), and the reactance of X_{S2} to a lower reactance than X_{S3} ($X_{S2}<X_{S3}$).

Input impedance of the driver stage, presented in section 5.4.1, is 2-j160 at the lower frequency, and 30-j81 at the higher frequency. The proposed BORN architecture not only matches these two impedances to 50Ω at the respective frequencies, but also matches input impedance of the driver stage to 50Ω at the middle frequency band, when both input matching networks are switched *ON*.

In electrical engineering, for component connected in parallel, the inverse total impedance is the sum of the inverses of the component impedances. Hence, the equivalent impedance (Z_{eq}) can be calculated by following equation,

$$Z_{eq} = Z_1 \| Z_2 = \frac{Z_1.Z_2}{Z_1+Z_2} \quad (5.22)$$

This relationship results in a total impedance that is less than the smallest of the individual impedances. When impedances are connected in parallel, each impedance in parallel has the same full voltage of the source applied to it. However, more current flows from the source than would flow for any of them individually, so the total impedance is lower.

Figure 5.6 shows input impedance of the driver stage of BORN PA at three targeted frequency bands on smith-chart, before and after impedance mapping. Circles show the original impedances before impedance mapping, and stars show the auxiliary impedances after impedance mapping. As mentioned, a parallel combination of the input impedances at B1 and B3 (green and red circle), will result a lower impedance, which cannot match the input impedance of the PA at B2 (yellow circle) to 50Ω. Therefore, the solution is to map this input impedance (yellow circle) to an auxiliary impedance (yellow star), which leads to an impedance matching to 50Ω at the middle frequency band, when both input matching networks are switched *ON*.

Figure 5.7 demonstrates the input mapping network, which consists of a series capacitor of CM1, and a capacitor of CM2 in shunt path. CM2 can be switched ON and OFF by transistor of M8. CM1 and CM2 are 2pF and 6pF, respectively, and size of the transistor of M8 is 1.0mm. Design parameters of the input mapping network is listed in Table 5.4. When Vcont1 is applied to the gate of M8, the switch is ON, and capacitor of CM2 will be connected in parallel. As a results, it moves the input impedance of the driver stage of BORN PA to a lower impedance (to the left on smith-chart). In contrast, when Vcont1 is not applied to the gate of M8, the input impedances stay fairly without changes on smith-chart.

Truth-table of the input mapping network is shown in Table 5.5. At the lower frequency band, Vcont1 is ON, which results an impedance mapping from 2-j60 to a lower impedance of 1.3-j24. At the middle frequency band, Vcont1 is ON and impedance of 6-j95 will be mapped to a

lower impedance of 0.5-j15. Transistor of M8 is switched OFF at the higher frequency band, which results a little change from 30-j81 to 20-j51. These auxiliary impedances at three targeted frequency band, provide Bit Optimized Reconfigurable Network (BORN) at the input of the power amplifier.

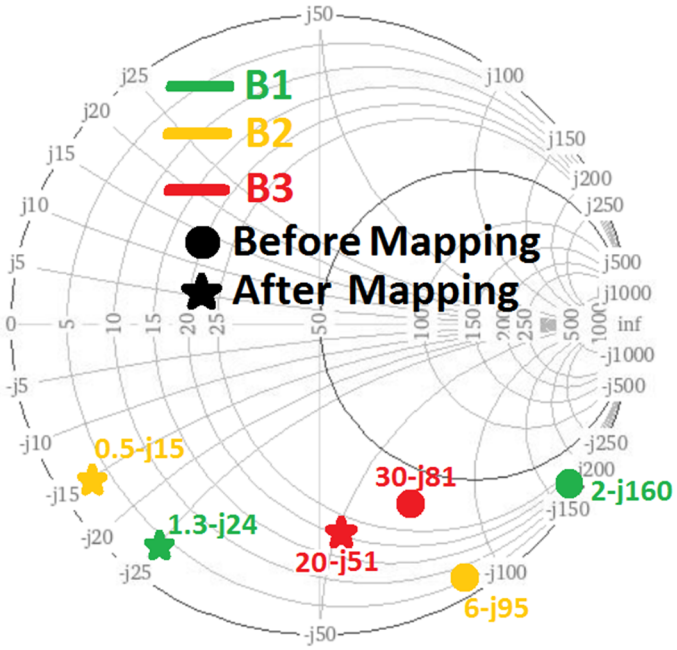


Figure 5.6. Input impedance of the driver stage of BORN PA at three targeted frequency bands on smith-chart, before and after impedance mapping.

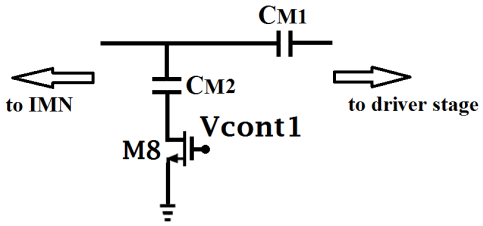


Figure 5.7. The proposed input mapping network of BORN PA.

Table 5.4. Design parameters of input mapping network

C_{M1}	C_{M2}	W_8
2.0pF	6.0pF	1.0mm

Table 5.5. Truth-table of input mapping network

Band	Vcont1 (S1)
B1	ON
B2	ON
B3	OFF

5.4.3. The Proposed Input Matching Network

An input matching network is being used at input side of a power amplifier to match input impedance of the PA to 50Ω. Figure 5.8 shows two switchable input matching networks of the proposed BORN PA. IMN1 and IMN2 match input impedance of the driver stage of the BORN PA to 50Ω at the lower and the higher frequency bands, respectively. IMN1 consists of a series inductor of L1 and a shunt capacitor of C1, which can be switched *ON* and *OFF* by two transistors of M4 and M5. Likewise, IMN2 consists of a series inductor of L'1 and a shunt capacitor of C'1, which can be switched *ON* and *OFF* by M6 and M7. In order to increase the power handling of these RF switches, all four switches are designed by triple-well transistors, and use resistive bulk floating technique by connecting bulk terminal to ground via a resistor of R_{SW}. Details parameters of the input matching networks are listed in Table 5.6.

Combination of these two input matching networks, when both control voltages are switched *ON*, matches the input impedance of the BORN PA to 50Ω at the middle frequency band. When Vcont1 and Vcont2 are simultaneously switched *ON*, inductor of L1 will be in parallel with L'1 (L_{total}=L1||L'1), and C1 in parallel with C'1 (C_{total}=C1+C'1), which results a 50Ω match at the middle frequency band.

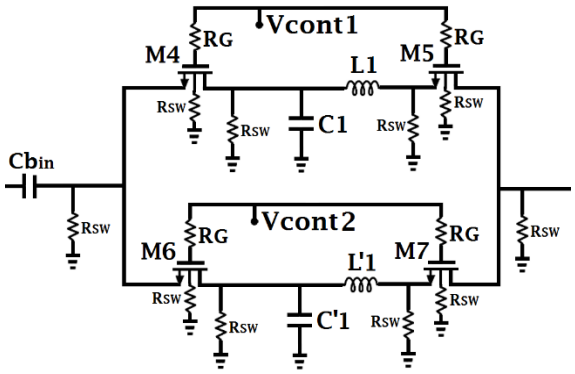


Figure 5.8. The proposed input matching network of BORN PA.

Table 5.6. Design parameters of input matching networks

Cb_{in}	C_1	L_1	C'_1	L'_1	R_G	R_{SW}	$W_4=W_5=W_6=W_7$
8.0pF	4.0pF	9.0nH	1.7pF	5.5nH	20KΩ	20KΩ	500um

5.4.4. The Proposed Output Mapping Network

The proposed BORN architecture matches the output impedance of the power stage to 50Ω, not only at the lower and the higher frequency bands, but also at the middle frequency band when both output matching networks are switched *ON*.

Figure 5.9 shows output impedance of the power stage of BORN PA at three targeted frequency bands on smith-chart, before and after impedance mapping. Circles show the original impedances before impedance mapping, and stars show the auxiliary impedances after impedance mapping. A parallel combination of the output impedances at the lower and the higher frequency bands (green and red circle), will result a lower impedance than each one, which cannot match the output impedance of the PA to 50Ω at the middle frequency band (yellow circle). Therefore, the solution is to map these impedance to auxiliary impedances (shown with stars) in order to achieve 50Ω match at the middle frequency band, when both matching networks are switched *ON*.

Figure 5.10 demonstrates the output mapping network, which consists of series capacitor of C_{M3}, inductor of L_{M1} in shunt path, and inductor of L_{M2} which can be switched *ON* and *OFF* by transistor of M9. C_{M3}, L_{M1}, and L_{M2} are 45pF, 0.5nH, and 1.5nH, respectively, and size of the transistor of M9 is 500µm. Design parameters of output mapping network are listed in Table 5.7.

When switch Vcont1 is applied to the gate of M8, the switch is *ON*, and capacitor of C_{M2} will be connected in parallel. As a results, it moves the input impedance of the driver stage of BORN PA to a lower impedance (to the left on smith-chart). In contrast, when Vcont1 is not applied to the gate of M8, the input impedances stay fairly without changes on smith-chart.

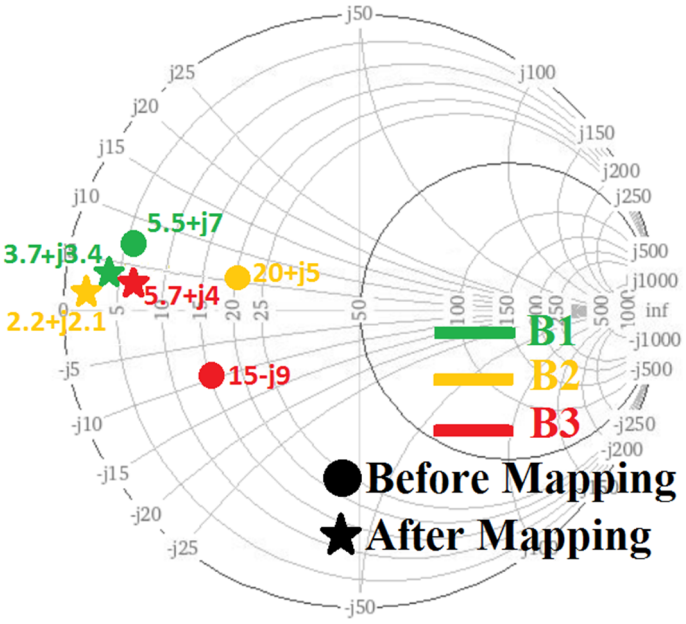


Figure 5.9. Output impedance of the power stage of BORN PA at three targeted frequency bands on smith-chart, before and after impedance mapping.

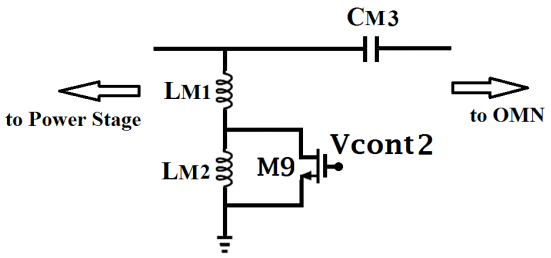


Figure 5.10. The proposed output mapping network of BORN PA.

Truth-table of the output mapping network is shown in Table 5.8. At the lower frequency band, the switch of M9 is *OFF*, thus two inductors are in series and the total inductance will be 2.0nH. It results an impedance mapping at the lower frequency band from 5.5+j7 to 3.7+j3.4. At the middle and the higher frequency bands, the switch of M9 is *ON*, and inductor of L_{M2} will be bypassed. Hence, the total inductance will be 0.5nH. The output impedance of the power stage will be mapped from 20+j5 to 2.2+j2.1 at B2, and from 15-j9 to 5.7+j4 at B3. These auxiliary impedances at three targeted frequency band, provide Bit Optimized Reconfigurable Network (BORN) at the output of the power amplifier.

Table 5.7. Design parameters of output mapping network

L_{M1}	L_{M2}	C_{M3}	W_9
0.5nH	1.5nH	45pF	500um

Table 5.8. Truth-table of output mapping network

Band	**Vcont2 (S2)**
B1	OFF
B2	ON
B3	ON

5.4.5. The Proposed Output Matching Network

An output matching network matches output impedance of a power amplifier to 50Ω. Figure 5.11 demonstrates two switchable output matching networks of the proposed BORN PA. OMN1, which matches output impedance of the power stage to 50 Ω at the lower frequency band, consists of a series inductor of L2 and a shunt capacitor of C2. Likewise, OMN2, which consists

of a series inductor of L'2 and a shunt capacitor of C'2, matches output impedance of the power stage to 50 Ω at the higher frequency band.

When both control voltage are switched *ON*, combination of these two output matching networks, matches output impedance of the BORN PA to 50Ω at the middle frequency band. When Vcont1 and Vcont2 are simultaneously switched *ON*, inductor of L2 will be in parallel with L'2 (L_{total}=L2||L'2), and C2 in parallel with C'2 (C_{total}=C2+C'2), which results a 50Ω match at the middle frequency band.

All switches in the proposed output matching network, are designed by triple-well transistors, and use resistive bulk floating technique by connecting bulk terminal to ground via a resistor of R_{SW}. In addition, in order to improve the power handling capability of the output matching network, three switches stacked in series are used in right side of each matching network. Details parameters of the output matching networks are listed in Table 5.9.

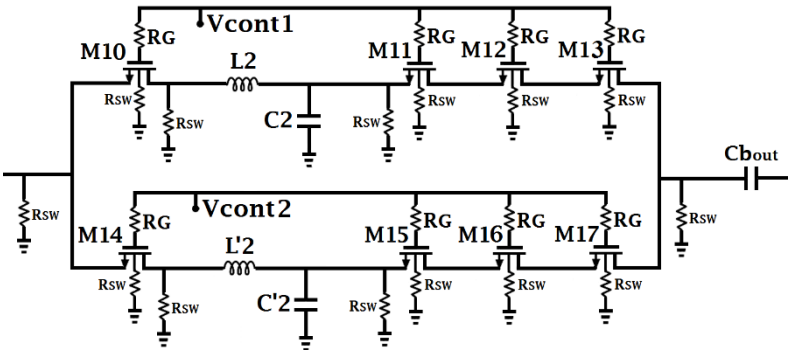


Figure 5.11. The proposed output matching network of BORN PA.

Table 5.9. Design parameters of output matching networks

C_2	L_2	C'_2	L'_2	Cb_{out}	W_{10}=W_{14}	W_{11}=W_{12}=W_{13}=W_{15}=W_{16}=W_{17}
6.6pF	2.4nH	1.7pF	1.2nH	30pF	2.0mm	1.0mm

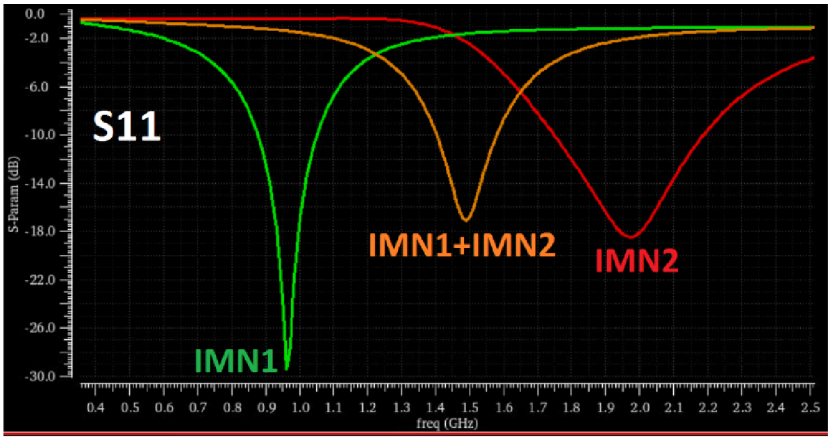
5.5. Simulated Results of BORN PA

As discussed in chapter 2 and chapter 3, measured current of a power amplifier highly depends on ground resistance of the chip. In order to have a fair comparison between simulation and measurement results of the proposed BORN PA, it is a good idea to calculate the ground resistance of the taped-out chip first, then apply this ground resistance into simulation results of the BORN PA. After calculating the ground resistance of 0.7Ω, and considering it in the simulation set-up, small-signal and large-signal simulation results of the proposed BORN PA are presented in this section.

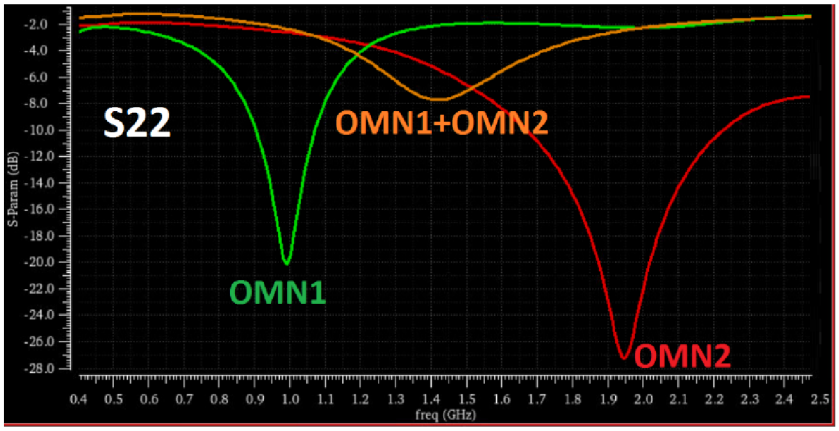
5.5.1. Simulated Small-Signal Results

The simulated S-parameters results of the proposed BORN PA are demonstrated in Figure 5.12. By setting control voltages of Vcon1 and Vcont2 to *ON/OFF* and *OFF/ON*, respectively, the power amplifier operates at the lower and the higher frequency bands. When both control voltages are simultaneously switched ON, the power amplifier operates at the middle frequency band. Figures 5.12 (a) and 5.12 (b), respectively, show input reflection coefficient (S11) and output reflection coefficient (S22) in dB scale. By designing input matching, input mapping, output mapping, and output matching networks, a perfect impedance matching in input and output of the proposed BORN PA is achieved at three targeted frequency bands.

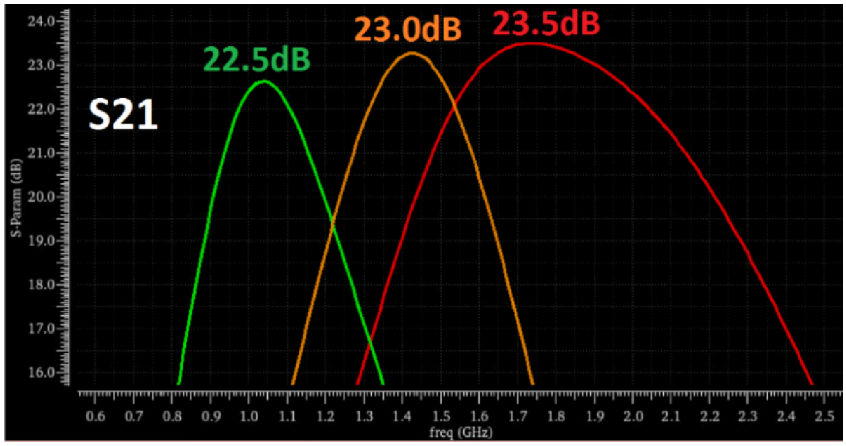
Regarding to small-signal gain (S21) of the proposed BORN PA, Figure 5.12 (c) indicates that small-signal gain is 22.0dB at the lower, 22.5dB at the middle, and 23.0 dB at the higher frequency bands.



(a)



(b)



(c)

Figure 5.12. Simulated S-parameters results of the proposed BORN PA, (a) S11, (b) S22, and (c) S21.

5.5.2. Simulated Large-Signal Results

Figure 5.13 shows simulated output power of the proposed BORN power amplifier versus frequency when the PA is in saturation condition (Pin= +5dBm). The proposed BORN PA delivers saturated output power (Psat) of 23.0/23.0/23.0dBm, output 1-dB compression point (P1dB) of 20.5/21.0/21.0dB, power added efficiency (PAE) of 13.5/13.5/13.5%, and respective 3-dB bandwidth of 450/500/550MHz at three targeted frequency bands, respectively.

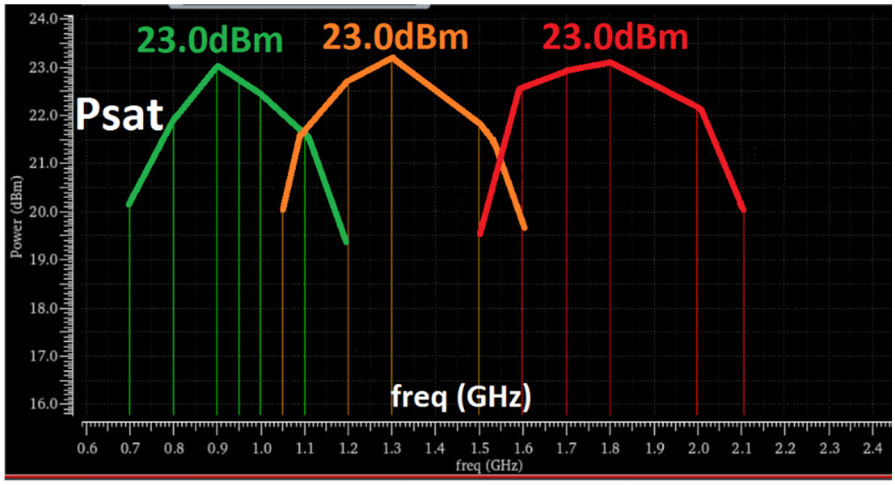


Figure 5.13. Simulated saturated output power versus frequency of the proposed BORN PA.

5.6. Measured Results of BORN PA

Regarding to design the proposed BORN power amplifier, all devices and passive components are selected from TSMC 180nm CMOS process, and the simulations is done in Cadence simulation set-up. After finishing physical layout of the design, design rule check (DRC) is performed to check if the chip layout satisfies a series of recommended parameters called design rules in the process. Eventually, the layout versus schematic (LVS) is performed to check whether the layout corresponds to the original schematic in terms of number of active devices and passive components and connections between them.

Figure 5.14 shows die-photo of the proposed BORN power amplifier designed and taped out in 180nm CMOS process with size of 3.1 mm × 1.6 mm including all DC and RF bond-pads.

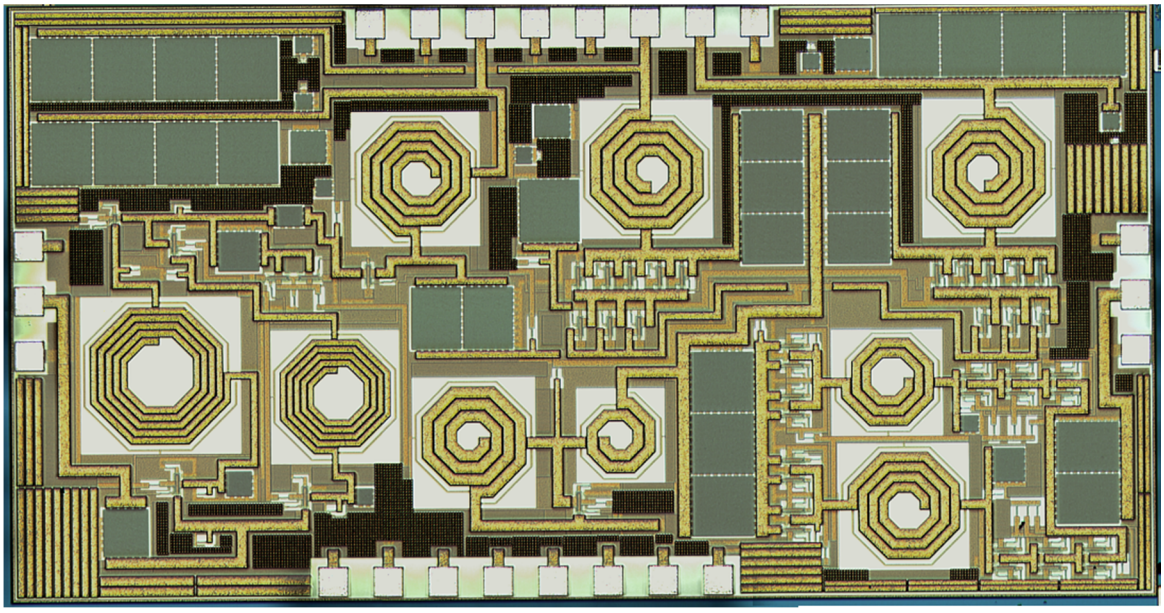


Figure 5.14. Fully integrated BORN PA using 180nm CMOS process with size of 3.1mm × 1.6 mm.

5.6.1. Measurement Set-Up

After receiving the fabricated chip, it is characterized in Radio Frequency Integrated Circuits (RFIC) lab in NDSU ECE Department by using the following equipment,

- Elite 300 Probe Station
- Agilent N5230A PNA-L Network Analyzer
- Anristsu MG 3700A Vector Signal Generator
- Tektronix RSA3408B Real-Time Spectrum Analyzer

Figure 5.16 shows four probes which are used to characterize the die chip. Two GSG RF probes are used to apply RF signals, and two 8-pin DC probes are used to provide DC voltages to the chip.

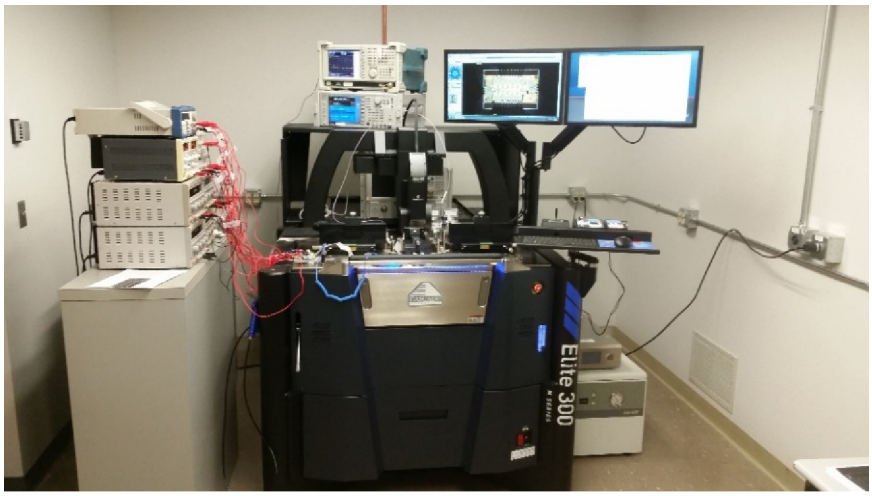


Figure 5.15. Measurement set-up in NDSU RFIC Lab.

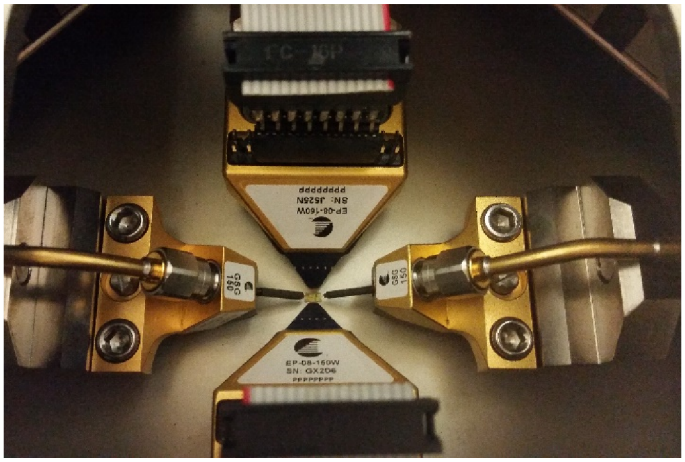


Figure 5.16. RF and DC probes used to characterize the BORN PA.

The proposed BORN power amplifier is designed with simulated current of 120mA for the driver stage, and 2×300mA for two cascode cells as the power stage. In order to calculate the ground resistance of the chip, at DC bias condition same as simulation, currents of amplification stages of the BORN PA are measured. Figure 5.17 shows measured current of the driver stage as 51mA with supply voltage of 1.8V. The measured current of two cascode cells of the power stage are 201mA and 205mA with supply voltage of 3.6V. Thus, the ground resistance has been calculated 0.7Ω after a thorough modeling.

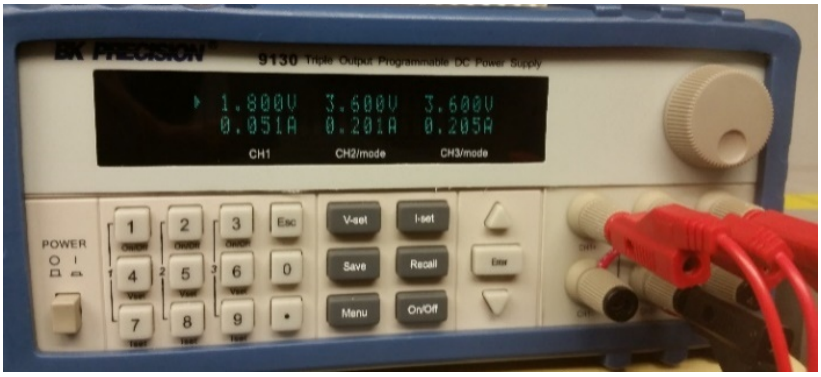


Figure 5.17. Measured currents of amplification stages of the proposed BORN PA.

5.6.2. Measured Small-Signal Results

Figures 5.18 (a) and 5.18 (b), respectively, show the measured results of input reflection coefficient (S11) and output reflection coefficient (S22) in dB scale, which demonstrates a perfect impedance matching in input and output of the proposed BORN power amplifier at three targeted frequency bands. When control voltages of Vcon1 and Vcont2 are set to *ON/OFF* and *OFF/ON*, respectively, the power amplifier operates at the lower and the higher frequency bands. Moreover, the PA operates at the middle frequency band when both control voltages are simultaneously switched ON.

Figure 5.18 (c) shows measured small-signal gain (S21) of the proposed BORN PA. The gain is 15.8dB at the lower, 17.0dB at the middle, and 16.0 dB at the higher frequency bands. In addition, reverse isolation of S12 is shown in Figure 5.18 (d). Reflected signals at the output port of a power amplifier, can pass through the amplifier in the reverse direction. This unwanted reverse transmission can cause the reflected signals to interfere with the desired fundamental signal flowing in the forward direction. Therefore, reverse isolation is important to quantify. The measured S12 reverse gain of the proposed BORN PA shows a perfect reverse isolation at three targeted frequency bands.

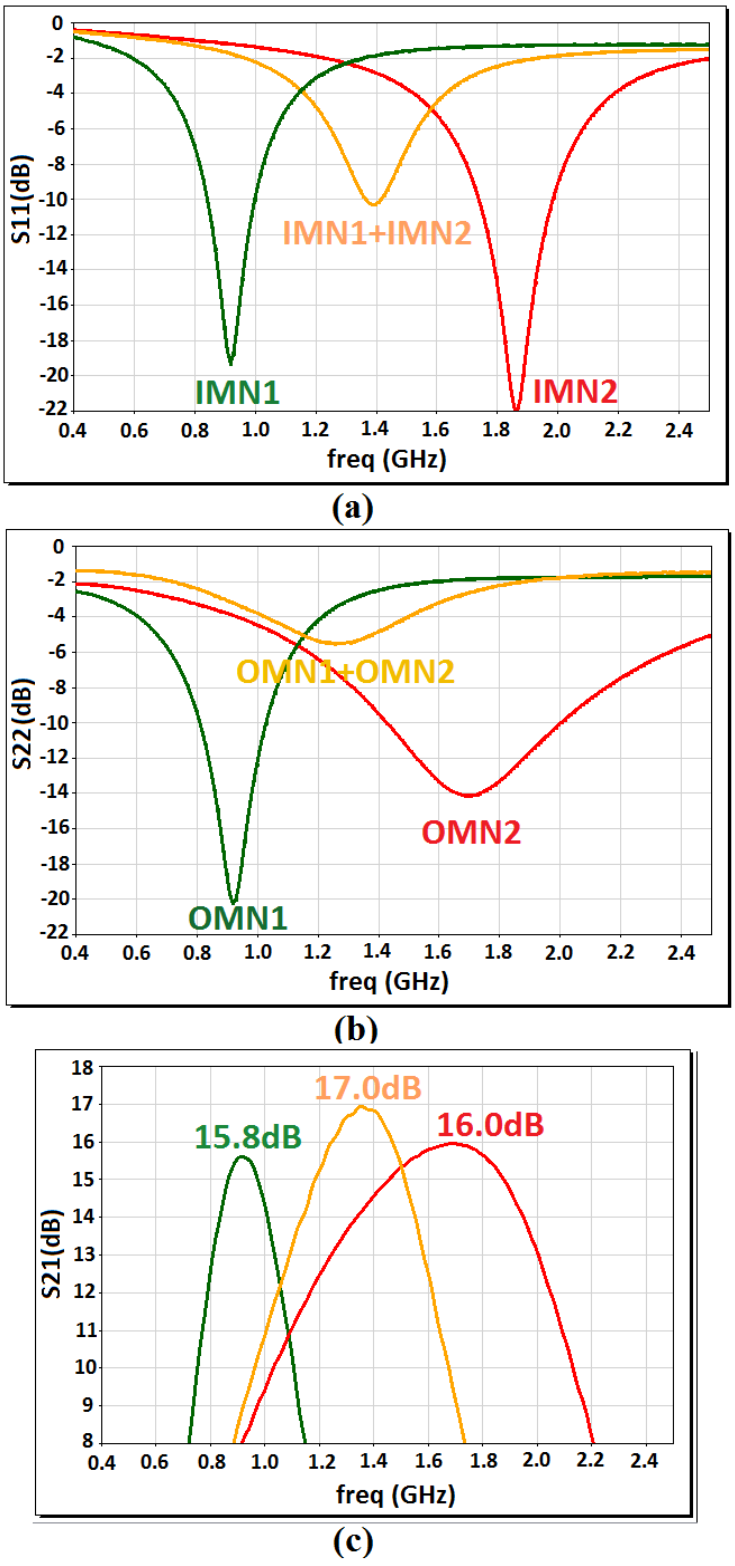
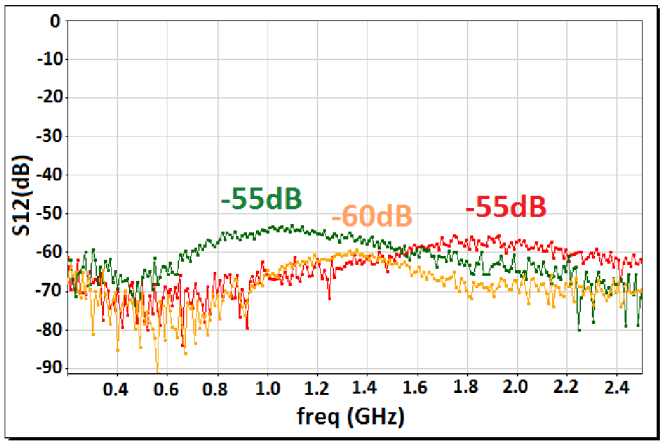


Figure 5.18. Measured S-parameter results of the proposed BORN PA, (a) S11, (b) S22, (c) S21 gain, and (d) S12 reverse isolation.



(d)

Figure 5.18. Measured S-parameter results of the proposed BORN PA, (a) S11, (b) S22, (c) S21 gain, and (d) S12 reverse isolation (continued).

5.6.3. Measured Large-Signal Results

In order to measure large-signal performance of the proposed BORN power amplifier, an RF signal from signal generator, is applied to input port of the power amplifier. At the output port of the PA, the output signal will be measured by using a spectrum analyzer. Before starting measuring large-signal performance of the PA, the cable loss must be calculated. Thus, the input and output RF probes are being short-circuit by using a THRU standard (shown in Figure 5.19). Figure 5.20 shows the cable loss at the lower and the higher frequency bands. A 0dBm signal is applied to the system, and -2.9dBm is delivered at the output spectrum, which results a cable loss of -2.9dB at the lower frequency band. Likewise, the cable loss at the higher frequency band is measured -3.8dB. The cable loss at the middle frequency band can be assumed -3.4dB.

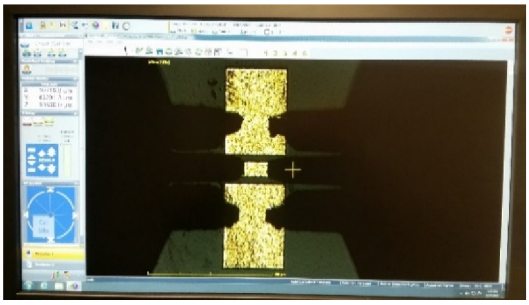


Figure 5.19. Cable loss measurement set-up using a THRU standard.

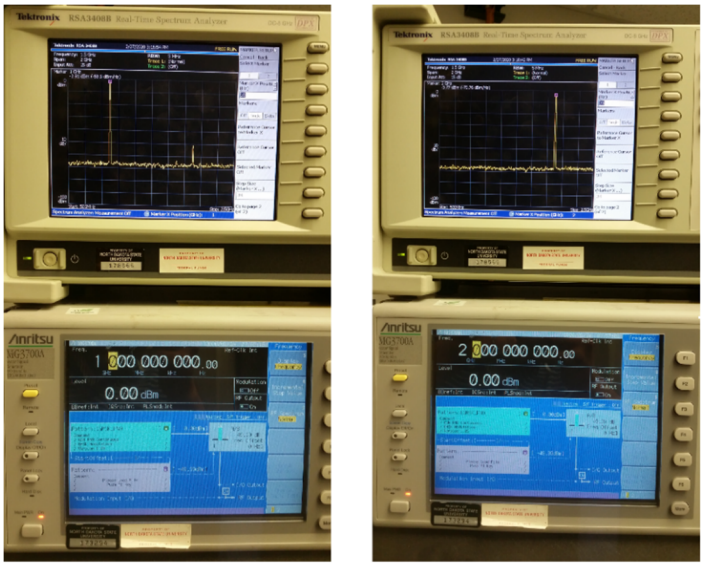


Figure 5.20. Cable loss measurement at the (a) lower, and (b) higher frequency bands.

Figure 5.21 shows output power of the proposed BORN PA when the PA is in saturation condition (Pin= +10dBm) at three targeted frequency bands. The proposed BORN PA provides saturated output power (Psat) of 21.25/22.25/23.0 dBm at 960/1317/1750 MHz, respectively.

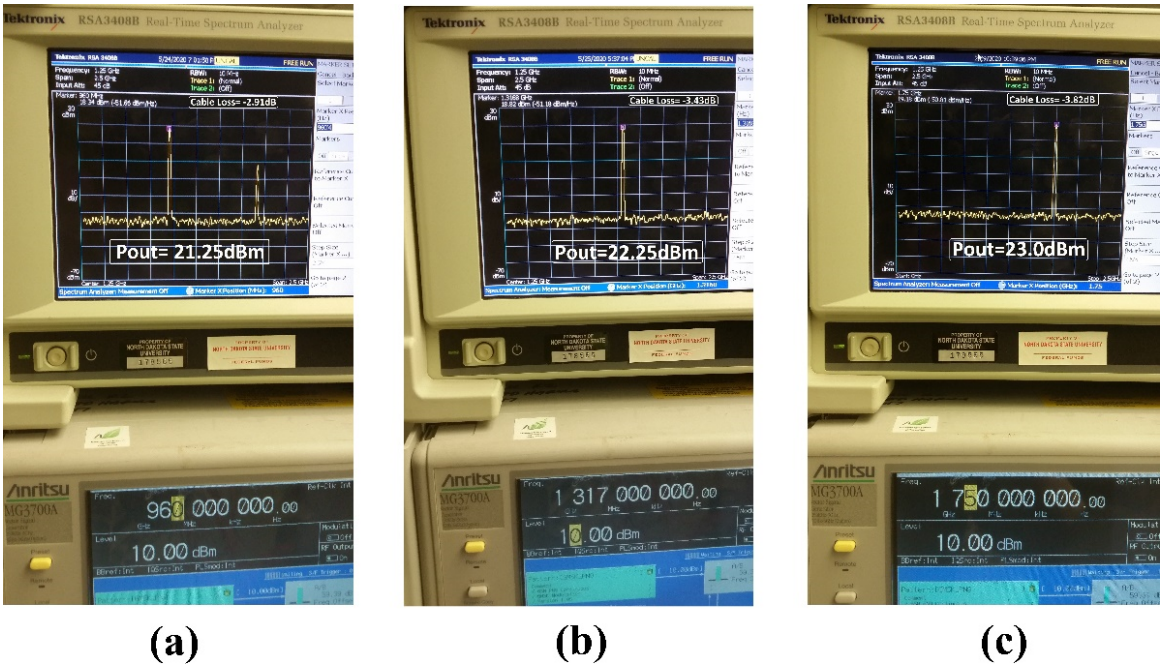


Figure 5.21. Measured saturated output power (Psat) of BORN PA at the (a) lower, (b) middle, and (c) higher frequency bands.

Figure 5.22 shows measured output power of the proposed BORN power amplifier versus frequency when the PA is in saturation condition (Pin= +10dBm). In addition, the measured output power is compared with the respective simulated output power at each operating frequency. The solid line is the measured result and the dotted line is simulated result. The proposed BORN PA delivers measured saturated output power (Psat) of 21.25/22.25/23.0dBm at three targeted frequency bands. It is explicitly demonstrated that B1, B2, and B3 can cover frequency range of 775-1175MHz, 1050-1475MHz, and 1500-2050 MHz, and thus provide respective 3-dB bandwidth of 400MHz, 425MHz, and 550MHz.

By setting control voltages of Vcon1 and Vcont2 to *ON/OFF, ON/ON,* and *OFF/ON*, the power amplifier operates, respectively, at the lower, the middle, and the higher frequency bands. For these three conditions, large-signal performance is measured across different input powers (-10dBm to +14dBm), as shown in Figure 5.23. For three evaluated modes, output 1-dB compression point (P1dB) is 19.5dBm/20.0dBm/21.0dBm, and the peak of power-added efficiency (PAE) is 9%, 11%, and 13% at 960MHz, 1317MHz, and 1750MHz, respectively.

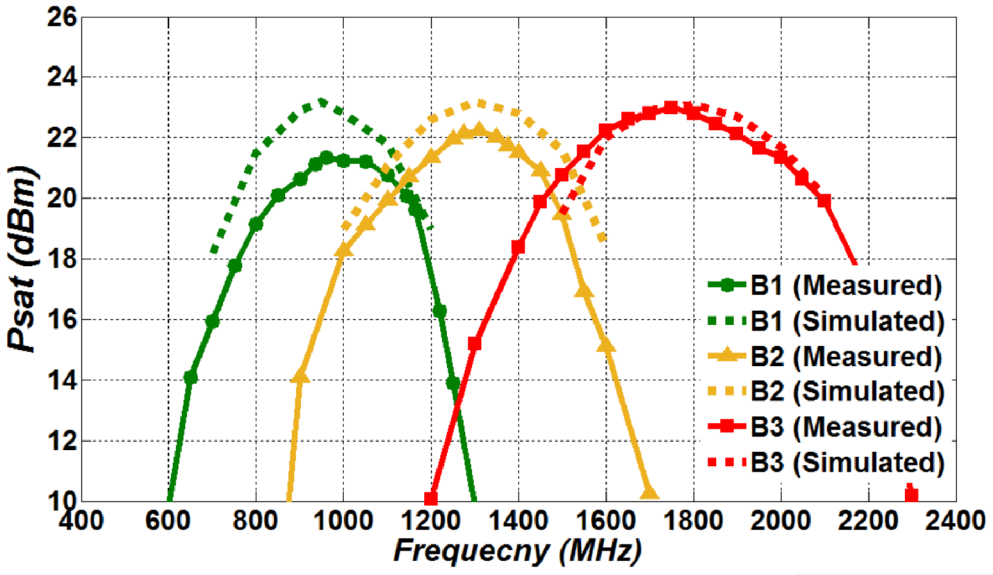


Figure 5.22. Comparison between measured and simulated output powers of the proposed BORN power amplifier versus frequency.

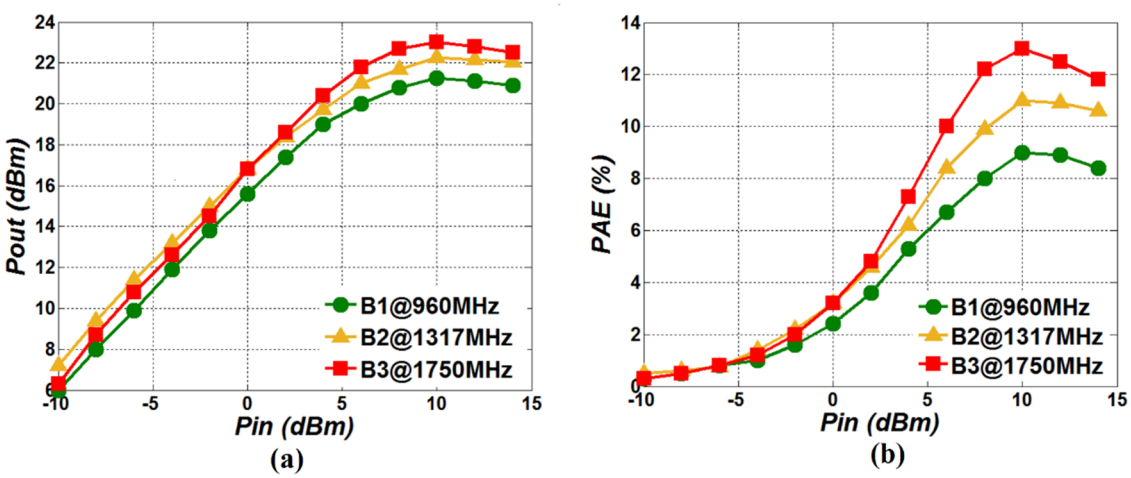


Figure 5.23. Measured large-signal performance with respect to input power (Pin) at three targeted frequency bands, for (a) output power, and (b) power added efficiency.

Table 5.10 shows performance comparison of the proposed BORN PA with the state-of-the-art multi-band PA at the similar frequency range. Although the tunable power amplifiers reported in [38] fabricated in CMOS process, an off-chip input matching network has been used. The proposed BORN PA, which is fully integrated, has higher output saturated power and P1dB. In addition, power gain is not sufficient in the tunable PA reported in [38]. Dual-band PA reported in [39], utilizes two different power amplifiers for the lower and the higher frequency bands and has low bandwidth. Dual-band PA reported in [40] uses off-chip matching network, commercial components and also suffers from low output power, and low P1dB.

Moreover in the [42], [45], and [49], special fabrication processes, such as 10W Gallium Nitride (GaN) HEMT, GaAs FET, Micro-Electro-Mechanical-System (MEMS) switches, are required in order to design a multi-band tunable PA which are not suitable for implementing a fully integrated single-chip power amplifier in terms of the cost and level of integration with other functional blocks of an RF transceiver.

The promising results show that the proposed BORN PA can be a practical solution for RF multiband applications by achieving the highest bandwidth.

Table 5.10. Comparison of the proposed BORN PA with state-of-the-art multi-band PA

	[38]	[39]	[40]	[42]	[45]	[49]	**This Work**	
Year	2007	2015	2006	2016	2017	2005	**Sim.**	**Meas.**
Freq (GHz)	2.4/5.2	0.9/1.9	0.85/1.9	0.88-0.95	0.8/1.06/1.3	0.9/1.5/2.0	**0.9/1.4/1.9**	**0.9/1.4/1.9**
Gain (dB)	10.4/5.1	32/29	24/15	21	12/12/12	14/12/14	**22/22.5/23**	**15.8/17/16**
Psat (dBm)	13/9	26/26	15/18	25	42/42/42	30/30/30	**23/23/23**	**21.3/22.3/23**
PAE (%)	18/12	19/25	18/17	25	52/56/56	60/61/62	**13/13/13**	**9/11/13**
P1dB (dBm)	11/8	26/26	15/17	21.5	-	-	**20.5/21/21**	**19.5/20/21**
BW (MHz)	-	90/200	200/200	70	550	200/300/400	**450/500/550**	**400/450/550**
Area (mm^2)	1.5×1.5	3.0×3.0	0.4×1.3	0.9×0.7	PCB	PCB	**3.1×1.6**	
Type	Tunable Inductor Off-chip IMN	Low-band PA, High-band PA	Off-chip Matching Network	External IMN and OMN on PCB	Continuous Doherty PA	MEMS Switches	**Fully Integrated BORN PA**	
Process	CMOS 0.18um	CMOS 0.11um	CMOS 0.25um	GaAs HBT	GaN HEMT	GaAs FET	**CMOS 0.18um**	

5.7. Conclusion

This chapter presents a fully integrated band-switchable CMOS power amplifier using bit-optimized reconfigurable network (BORN). The measured S-parameters results demonstrate a perfect impedance matching in input and output of the proposed BORN PA at three targeted frequency bands. The proposed BORN PA delivers saturated output power (Psat) of 21.25/22.25/ 23.0dBm at 960MHz/1317MHz/1750MHz, respectively. Moreover, the proposed BORN PA provides respective 3-dB bandwidth of 400MHz/425MHz/550MHz, output 1-dB compression point (P1dB) of 19.5dBm/20.0dBm/21.0dBm, and power-added efficiency (PAE) of 9/11/13% at the lower, middle, and higher frequency bands, respectively. The promising results show that the proposed BORN PA can be a practical solution for RF multiband applications in terms of the cost and level of integration with other functional blocks of an RF transceiver.

CHAPTER 6. CONCLUSIONS AND FUTURE WORKS

6.1. Technical Contributions

The explosively growing demands on higher data rates in mobile communications is pushing a quick development of standards like 4G LTE and 5G NR. The use of multi-band approach, where the frequency bands can be selectable to achieve the highest communication data rate, is therefore highly desired to reduce transceiver complexity and cost. A fully integrated single-chip tunable CMOS power amplifier is the best solution in terms of the cost and level of integration with other functional blocks of RF transceiver.

In chapter 2 proposes a novel tunable CMOS power amplifier addressing three low/mid/high power modes. The results show that cascode topology has a better performance than common-source topology with respect to gain and efficiency. In chapter 3, a dual-band CMOS power amplifier is presented by using two switchable matching networks, one for the lower frequency band and one for the higher frequency band. The measured results demonstrate that the switchable matching networks perform properly and have capability to switch the operating frequency. Moreover, by a thorough modeling of ground plane, designing a better M1 ground plane, and also using ground plane on the backplane of the inductors, it was observed that current of the power amplifier reaches to 80% of the designed current, with respect to 20% for the chip presented in chapter 2.

In chapter 4, a thorough investigation is done regarding to discrepancy between simulation and measured results in the taped-out chips in 130nm CMOS process, which leads to address major issues regarding to design a high-power RF switch. Bulk-source connection, DC isolation, and DC path of an RF switch are studied, and a solution for each issue is provided. Eventually, an

architecture for a robust high-power RF switch is proposed by utilizing a resistive body floating technique and 6-terminal triple-well NMOS.

Furthermore, the effect of the substrate thickness on RF performance parameters, such as operating frequency and output power, of an RFIC chip is also studied. The deviations of frequency and output power are, respectively, within ±1% and ±1 dB, and the DC current remains fairly similar for different substrate thicknesses. This reliability study proves that die-substrate thickness does not have huge effect on DC and RF performances of an RFIC chip, which leads toward implementing ultra-thin flexible electronics applications.

This chapter also concludes a lack of precision of the RFIC simulator in predicting the ground resistance of a chip, RF leakage through substrate due to bulk connection, and effect of turning-ON a switch on the DC performance of the amplification stages.

Chapter 5, for the first time, proposes a band-switchable RF power amplifier by using a novel approach toward switching matching networks. In this approach, which is called **B**it **O**ptimized **R**econfigurable **N**etwork (BORN), two matching networks which can be controlled by digital bits will provide three operating frequency bands for the power amplifier. The proposed fully integrated BORN PA is designed and implemented in 180nm CMOS process.

The measured S-parameters results demonstrate a perfect impedance matching in input and output of the proposed BORN PA at three targeted frequency bands. The proposed BORN PA delivers saturated output power (Psat) of 21.25/22.25/23.0dBm at 960MHz/1317MHz/1750MHz, respectively. Moreover, the proposed BORN PA provides respective 3-dB bandwidth of 400/425/ 550MHz, output 1-dB compression point (P1dB) of 19.5/20.0/21.0dBm, and power-added efficiency (PAE) of 9/11/13% at the lower, middle, and higher frequency bands, respectively. The promising results show that the proposed BORN PA can be a practical solution for RF multiband

applications in terms of the cost and level of integration with other functional blocks of an RF transceiver.

6.2. Future Works

The research work described in this dissertation represents starting points for several future researches and developments. The proposed architecture is being called Bit Optimized Reconfigurable Network (BORN) because desired frequency band of operation can be selected through the control of digital bits. As a future work, a digital control circuitry can be designed in order to select the operating frequency band, which leads to achieve the highest communication data rate. The power amplifier (PA) is a key block in an RF transceiver. To lower the costs and allow full integration of a complete radio System-on-Chip (SoC), it is desirable to integrate the entire transceiver and the PA in a single CMOS chip. In addition, by applying the proposed BORN architecture to the different functional blocks of a transceiver, a fully integrated BORN transceiver can be implemented which consists of BORN LNA, BORN down-converter, BORN VCO, BORN up-converter, and BORN PA.

For high-data rate communications, highly-linear PAs will be welcomed in the future. Such a trend can already be observed for WLAN, 4G LTE, and 5G NR standards. Thus, PAs should show high linearity performance with high efficiency. For a more thorough understanding of nonlinearity characteristics, rigorous analysis of nonlinearity in CMOS devices should be carried out. In addition, advanced linearity and efficiency enhancement techniques can be used in a digital compact form so that they can be easily adapted to compact mobile terminals.

Moreover, a fully integrated BORN PA, and ultimately BORN transceiver, can be designed in mm-wave frequency band, which provides a higher data rate and bandwidth for 5G frequency range 2 (FR2).

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APPENDIX. RELATED PUBLICATIONS

[1] D. Mitra, **S. B. Hamidi,** P. Roy, C. Biswas, A. Biswas, and D. Dawn, "A Radio-Frequency (RF) Reliability Study of CMOS RF Integrated Circuits (RFIC) for Ultra-Thin Flexible Electronics Applications," *IET Electronics Letters,* Jan 2020 ***(D. Mitra and S. B. Hamidi contributed equally to this paper as co-first author)***

[2] **S. Babak Hamidi,** and Debasis Dawn, "A 900/1900-MHz Band-Switchable CMOS Power Amplifier," 7th *IEEE MTT-S International Microwave & RF Conference (IMaRC)*, Dec 2019.

[3] **S. Babak Hamidi,** and Debasis Dawn, "Fully Integrated LTE-Band CMOS Tunable Power Amplifier," 18th *IEEE Wireless and Microwave Technology Conference (WAMICON)*, April 2017.

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[5] Arka Biswas, **S. Babak Hamidi,** Chitralekha Biswas, Palash Roy, Dipankar Mitra, and Debasis Dawn, "A Novel CMOS RF Energy Harvester for Self-Sustainable Applications," 19th *IEEE Wireless and Microwave Technology Conference (WAMICON)*, April 2018.

[6] Debasis Dawn, Jabir Patel, Mohammad Nasry, and **S. Babak Hamidi,** "A Novel RF Energy Harvester," 7th *IEEE MTT-S International Microwave & RF Conference (IMaRC)*, Dec 2019.