DESIGN OF PIEZOELECTRIC ENERGY HARVESTING AND SUPERCAPACITOR CHARGING CIRCUITS USING OPTIMIZED DUTY-CYCLE OF BUCK CONVERTER

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Design of Piezoelectric Energy Harvesting and Supercapacitor

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The Supervisory Committee certifies that this *disquisition* complies with North Dakota State University's regulations and meets the accepted standards for the degree of

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ABSTRACT

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Energy harvesting has been proved to be an innovative solution to replace the batteries in remote power supply applications. Unfortunately, the limited capacity and low efficiency of power conversion restrict the practical applications of energy harvesting in daily-life. After a systematic review of research on energy harvesting in power management perspective, a circuit design, which targets low-frequency mechanical vibrations, is presented. With the classical piezoelectric cantilever setup, the maximum charging current of a supercapacitor can be obtained by optimizing the duty-cycle of a buck converter through software implemented pulse width modulation. The results of experiments prove the capacitive electric model of the piezoelectric element, the existence of maximum charging current of the supercapacitor, and the adaptive control of the designed circuits. With the duty-cycle optimized to 2.17%, a maximum charging current of 17.36 mA is measured, which is approximately 4 times that obtained in related researches. An active radio frequency identification (RFID) application is proposed to utilize the harvested power of 67.2 μW. In addition, the digital design in field programmable gate array (FPGA) is integrated using AMIS 0.5 μm CMOS process technology to reduce system power dissipation.

ACKNOWLEDGEMENTS

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CHAPTER 1. INTRODUCTION

Piezoelectric materials can be used to transform mechanical energy in ambient vibration into electrical energy, which can be stored and used to power other ultra low-power devices such as radio frequency identification (RFID) tags. Since these ultra low-power devices are wireless, it becomes necessary that those devices have their own independent power supplies. In tradition, electric power is supplied from bulky batteries which have environment unfriendly chemical ingredients. Most importantly, the batteries have limited life-cycles and need to be replaced periodically.

With the development of wireless sensor network (WSN) and microelectrome-chanical systems (MEMS) technologies, intelligent sensors are developed and embedded in remote locations. For instance, structural health monitoring (SHM) sensors are embedded in the bridges, medical sensors are implanted in the human body, and global positioning system (GPS) sensors are attached to animals to track their behaviors in wildlife. Locating the sensors just to replace the batteries could be very time-consuming and expensive. In the case of embedded sensors, the accessibility is even impossible and destructive. If a stress energy scavenging technology is realized, the life-span of those sensors could be significantly extended by eliminating the batteries.

There are many researches that successfully realize energy harvesting in the labs, but the total power efficiency of the designed system is constrained by the tradeoff among the efficiencies of each subsystems. For instance, some researchers pay much attention to maximizing the output power of the piezoelectric element, but the useful power stored in the energy buffer is degraded by the significant power loss in the designed converter. Based on systematic analysis of piezoelectric energy harvesting in power management perspective, the maximum charging current of a supercapacitor with optimized duty-cycle is investigated in this work.

In Chapter two, the previous researches are classified into conversion, transfer,

buffering, and consumption efficiencies along the power flow during energy harvesting in a power management perspective. The electrical model of the piezoelectric element, the maximum power point tracking technique, and the characteristics of charging a supercapacitor are introduced in Chapter three. The circuit design and implementation are described in Chapter four. Experimental setup and results are presented in Chapter five. Conclusion is in Chapter six.

CHAPTER 2. BACKGROUND

In 2004, Sodano et al. [1] presented a comprehensive review of piezoelectric energy harvesting, in which researches were summarized in categories including piezoelectric theoretical fundamental, mechanical vibration, power efficiency, storage circuitry, and wearable application. Generally, the motivations of power management focus on efficiency improvement by reducing power dissipation, which increases system stability, saves cost, and reduces impact on the environment. The solutions to improve the efficiency of energy harvesting system can be categorized into four blocks along the energy harvesting power flow path. They include optimizations in conversion efficiency of the energy source, transfer efficiency from the source to the load, buffering efficiency of the energy storage device, and consumption efficiency of the load. The architecture of the energy harvesting system in power management perspective is shown in Figure 1.

In the subsystem dealing with conversion efficiency, many researchers have established mathematic models for a variety of piezoelectric structures such as polyvinylidene fluoride (PVDF) film, unimorph, bimorph, diaphragm, and cymbal structures, etc. However, the requirement of high strain eliminates the practical applications of those structures. Due to the capacitive characteristic of piezoelectric materials, a converter is needed for power regulation in the subsystem dealing with transfer efficiency. A variety of control mechanisms, such as feed-forward, feedback, and self-adaptive regulations, etc. have been proposed to improve the transfer efficiency. In buffering subsystem, many devices such as capacitor, battery, and supercapacitor, etc. are used as the energy storage devices. In addition, many wearable applications such as RFID tag have been proposed for the load subsystem. Although efficiency optimizations have been proposed in each subsystem, it is important to consider the entire system together. Otherwise, the gain in one subsystem may degrade the per-
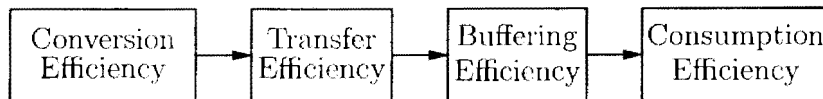
Figure 1. Power Management Flowchart of Energy Harvesting System.

formance of another. In this chapter, a systematic review of efficiency optimizations in energy conversion, transfer, buffering, and consumption are presented in Sections 2.1, 2.2, 2.3, and 2.4, respectively.

2.1. Conversion Efficiency

In general, energy conversion efficiency is the ratio between the useful output of an energy conversion machine and the input. One of the most effective methods to extract vibration energy is to use a piezoelectric ceramic to convert mechanical energy into electrical energy. In 1984, a PVDF film based 100 mg converter was designed by Hausler et al. [2] and implanted between the ribs of a dog. The converter harvested a fraction of the energy expended by respiration system to power an implantable microprocessor controlled insulin delivery pump with glucose sensor. The harvested power was only 17 μW with 0.5% effective extension of the ribs. In literature, this research can be termed as the first energy harvesting research targeting a biomedical application.

In 1991, Smits et al. [3] analyzed the mechanics of a piezoelectric bimorph under the influence of an externally applied electric field. The electromechanical coupling of the bimorph structure was tested under various mechanical boundary conditions such as a momentum at the end of the beam, a force applied perpendicular to the tip of the beam, and a uniform force applied over the entire length of the beam, etc. The derived equations about electromechanical coupling are helpful in understanding the conversion scheme of the bimorph structure. In 1996, William et al. [4] proposed an electromagnetic micro-power generator with dimensions of 2 mm × 5 mm × 1 mm.

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Power outputs of $1\mu W$ at 70 Hz and 0.1 mW at 330 Hz were measured with a 50 μm vibration deflection.

In 1999, Goldfarb et al. [5] presented an analytical model of the piezoelectric power generation. They found that the induced energy from piezoelectric element was stored in the ceramic and rebounded backward to the mechanical vibrations. The experiments indicated an anti-intuitive result that the maximum conversion efficiency occurred when the vibration frequency was much smaller than the piezoelectric resonant frequency. In cantilever boundary condition, the frequency response and output current could be accurately predicted by measuring the properties of the piezoelectric element and its acceleration rate. The damping effect of the piezoelectric element was also discussed.

In 2003, Kim et al. [6] found that the substrate thickness of a clamped diaphragm structure changed the distribution of the applied stress. In 2004, they [7] also investigated the strengths of metal-ceramic composite piezoelectric cymbal structure under a strong strain environment. The power of 30 mW was generated from the cymbal structure with a 5 $k\Omega$ load resistor. Although the cymbal structure was suitable for energy harvesting under a strong strain environment, the efficiency of power generation was only 7.5%. In 2007, Kim et al. [8] further investigated the energy generation capability of a 10-layer cymbal structure to power an LED device.

2.2. Transfer Efficiency

In order to make the energy harvested from the piezoelectric element more available to low-power loads, a variety of researches have proposed solutions to improve the transfer efficiency before the energy was stored. These proposed circuits include a flyback converter for impedance match between the source and the load, self-adaptive duty-cycle control for maximum power-point tracking, passive control by

step-down converter without a digital signal processor (DSP), and AC power supply with synchronized switches, etc.

In 2002, Kasyap et al. [9] used a piezoelectric composite cantilever beam as energy harvesting source and designed a flyback converter whose input impedance does not depend on end load. With impedance match between the piezoelectric source and the converter, a peak power efficiency of 20% was achieved with 80% flyback converter efficiency under 0.8 mW mechanical input power. In 1998, Amirtharajah et al. [10] proposed a prototype DSP system powered by its own generator and a low-power voltage regulator. Although the generated power is only 400 μW, it proved that a portable digital system can be powered entirely from ambient vibrations.

In 2002, Ottman et al. [11] presented an adaptive control scheme using the charging current versus duty-cycle curve, which is similar to the maximum power-point tracking in a photovoltaic system. The maximum charging current of 4.3 mA was available with the optimal duty-cycle of 3.18% at a rectifier voltage of 20.4 V, which approximated to the half of the open-circuit voltage of 45 V. With the highest mechanical excitation level of 95.31 V open-circuit voltage, the harvested power increased 4 times from 16.43 mW to 70.42 mW with 18.87 mW converter power loss. They concluded that with a higher excitation levels the gain of output power will further increase, but other DC-DC converter topologies need to be used. The adaptability of the control scheme allowed the energy harvesting circuit to be used on different vibration structures and parameters such as material properties and levels of mechanical vibrations. However, the DSP based controller consumes much more than the harvested power. In 2003, Ottman et al. [12] tried to solve the power loss problem of DSP controller by using a step-down converter operating in discontinuous conduction mode with optimal duty-cycle. They concluded that with predetermined switch frequency of 1 kHz, the optimal duty-cycle approached a constant 3.16% with

$\pm$ 0.25% level bias of mechanical excitation. The harvested power increased from 9.45 mW by direct charging to 30.66 mW with 65% converter efficiency.

In 2005, Siebert et al. [13] found that the piezoelectric power-supply frequency was several orders of magnitude lower than the integrated circuit operation frequency. Therefore, a digital system directly using AC power supply from energy harvesters was designed with power-on-reset circuit, self-timed circuit, and dynamic memory, etc. The design achieved correct computations with supply power frequency up to 250 kHz. In 2006, Le et al. [14] proposed a new power conversion circuits with a higher efficiency to interface a piezoelectric power generator than that of a conventional diode rectifier. Four kinds of rectification circuits including a passive half-wave rectifier, a synchronous half-wave rectifier, a passive full-wave rectifier, and a synchronous full-wave rectifier were proposed. Although a comparator was used to reduce the voltage drop across diodes, the power consumption of the comparator outweighed the power reduction from diode voltage drops.

In the same year, Makihara et al. [15] presented a novel circuit which only had two diodes with a selecting switch, which decreased the voltage drop between piezoelectric voltage and storage voltage from 1.2 V to 0.6 V. In 2007, Cao et al. [16] introduced both feedback and feed-forward control scheme into the DC-DC pulse width modulation boost converter for electromagnetic energy harvesting. The designed circuit could adjust the duty-cycle of the converter following the variations of the input voltage to get optimized transfer efficiency.

2.3. Buffering Efficiency

Because of the low current output capability of piezoelectric devices, the harvested energy can not be directly used by most electronics without accumulating a significant amount of charge in energy storage devices such as capacitors or rechargeable batteries. According to the following researches, capacitors are appropriate for

quick energy charge and discharge while rechargeable battery has better applications in sustainable power supply.

In 1997 Umeda et al. [17] investigated the impact of the load capacitance on the efficiency of the energy harvesting system. They found that as the capacitance increased the electrical charge increased. In addition, as the initial voltage increased the stored charge increased and the efficiency increased. A maximum efficiency of 35% was obtained, which was three times that of a solar cell. In 2003, Sodano et al. [18] investigated the possible power output from piezoelectric plate in cantilever configuration. He emphasized using a capacitor as a method of energy storage for direct energy access and rechargeable nickel metal hydride battery for sustainable power supply. With a power output of $1.5\ mW - 2\ mW$ from aluminum test plate, which mimic the resonance of an automobile compressor, a 40 mAh battery could be charged around one hour to power a Casio LW22H watch for more than two years. In 2004, Sodano et al. [19] continued presenting the result of charging various sized batteries using piezoelectric energy harvesting. After deriving a numerical equations relating the energy efficiency and the vibration parameters, the time of charging various sized 1.2 V rechargeable batteries to 90% capacity was measured with three different input vibrations including resonance, chirp, and random. They found that the output current of Macro Fiber Composites (MFC) is too small to charge batteries with the exception of strong input signal, because each segment of piezoelectric material in MFC could be modeled as a small power source.

In 2006, Simjee et al. [20] proposed that by using feed-forward pulse frequency modulation (PFM) regulator, open-circuit voltage samples for maximum power point tracking (MPPT), and supercapacitor for energy storage, the life-span of wireless sensor node would extend to over 20 years at basic communication standard. The MPPT calculation was approximated with tracking error less than 5%. At the

microcontroller working frequency of 4 MHz, the full-charged supercapacitor could power the sensor node to communicate at the rate of 25.6 $kbps$ for 9.54 hrs.

2.4. Consumption Efficiency

In an effort to incorporate computers and digital systems into our daily lives, researches have investigated the possibility and practicability of embedding them into our clothes or implanting inside our biological parts such as brain, arm, and heart. The use of energy harvesting devices to capture the energy in daily life is a captivating idea and has been one of the main stimuli facilitating the rapid growth of researches in this field. Therefore, in parallel with improving the energy output efficiency from the source, a tremendous amount of researches have investigated how to develop more effective ultra low-power applications, which are in the scale of the harvested energy.

In 1996, Starner et al. [21] estimated the harvestable power level from peoples' daily motions including body heat, exhalation of 1.0 W, blood pressure of 0.93 W, breathing band of 0.83 W, arm motion of 60 W, and finger motion of 6.9 $-$ 19 mW. Specific attention was paid to more practical footfall motion of 67 W energy harvesting, in which power regulator of 90% efficiency and energy storage units including capacitor and rechargeable batteries were used. He envisioned the possibility of harnessing the energy wasted during the people's everyday actions to power his or her wearable computing devices such as mobile phone.

In 1997, Post et al. [22] presented various conductive textiles, data and power distributions, and sensing circuitry could be incorporated into wash-and-wear clothing. A kind of fabric breadboard using pieced conductive and nonconductive fabrics were sewn. They combined electronic components into conventional textiles to create wearable computing. In 2001, Elvin et al. [23] proposed a similar technique for powering a wireless communication sensor solely by a piezoelectric beam. In 2001, Ramsey et al. [24] investigated the feasibility of using piezoelectric materials as

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a power supply for MEMS applications. The 33 and 31 modes of piezoelectric operations were compared. They proposed that a transversely loaded membrane had the mechanical advantage in converting applied pressure into piezoelectric energy. By designing a square PZT-5A membrane driven by blood pressure, the study concluded that a piezoelectric generator of the size 1 cm^2 might be able to power a MEMS application in μW power range.

In 2003, Churchill et al. [25] demonstrated the feasibility of a wireless sensor node whose power was derived solely from ambient environment. The piezoelectric energy was scavenged from a specimen loaded in three-point bending with 75 μm to 300 μm vibration amplitude and 60 Hz to 180 Hz vibration frequencies. The harvested energy was first stored in a 47 μF capacitor before it was supplied to the wireless sensor node. The size of the energy storage capacitor could be adjusted to provide different power levels. The time interval between regulation voltages from 2.5 V to 9.5 V varies from 30 s to 160 s with different vibration densities. These strain energy harvesting methods might be deployed within smart autonomous, self-powered wireless sensor networks for monitoring structures in aerospace, automotive, civil, and medical applications.

In conclusion, when the energy harvesting material structure is designed and a load application is fixed, the only optimization that can be done is on the transfer and buffering efficiencies. Most of the researches on transfer efficiency optimize the designed circuit to make sure that the output power of piezoelectric element is maximized. However, the low efficiency of transfer subsystem and absence of buffering subsystem degrade the energy available for the load subsystem. Therefore, it is crucial to consider the transfer and buffering subsystems together in designing a robust energy harvesting system.

CHAPTER 3. THEORY

This chapter investigates the theory of operation and electrical model of a piezoelectric element, maximum power-point tracking, and charging a supercapacitor. The piezoelectric element subjected to cantilever vibrations can be modeled as a sinusoidal current source with a parasitic capacitance [11]. The generated AC power needs to be converted to DC power before the load can use it. In Section 3.1, the classical electrical model of the piezoelectric element will be presented. Section 3.2 deals with the theory of maximum power generation by the piezoelectric element. After a basic introduction of a supercapacitor, methods of maximizing the charging current in the supercapacitor are investigated in Section 3.3.

3.1. Electrical Model of Piezoelectric Element

Piezoelectric materials can transform mechanical energy into electrical energy and vice versa, which enable them widely used as sensors or actuators. Their applications in energy harvesting are recognized due to the recent campaign for clean energy. Several materials exhibit the piezoelectric effect. For instance, Lead Zirconate Titanate (PZT) is one of the most widely used piezoelectric materials. In each PZT crystal unit cell, the positive and negative electrical charges are separated, but symmetrically distributed, so the PZT crystal is electrically neutral under normal condition. When a mechanical stress is applied, the structural symmetry is disturbed. The resulting structural asymmetry, which results in charge asymmetry, generates internal electrical field or voltage drop across the material. Piezoelectricity is a result of the combined effect of the electrical behavior of each unit cell, which can be represented as

$$D = \epsilon E \tag{1}$$

where D is the electric displacement of generated charge, ϵ is the permittivity of the material, and E is the applied electric field strength. According to Hooke's Law of elasticity

$$S = sT \qquad (2)$$

where S is the strain of the material, s is the compliance of the material, and T is the applied stress. Combining the equations (1) and (2) yields the equations,

$$S = [s^E]T + [d^t]E \qquad (3)$$

$$D = [d]T + [\epsilon^T]E \qquad (4)$$

where $[d]$ is the matrix of direct piezoelectric effect and $[d^t]$ is the matrix of converse piezoelectric effect, in which superscript the t stands for matrix transposition. The superscripts E and T in equation (3) and (4) indicate a constant electric field and stress, respectively. According to the ANSI IEEE 176 standard, the strain-charge relationship underlying the direct piezoelectric effect of equation (4) in three dimension can be expanded to

$$
\begin{pmatrix} D_1 \\ D_2 \\ D_3 \end{pmatrix} =
\begin{pmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & 0 \\ d_{31} & d_{32} & d_{33} & 0 & 0 & 0 \end{pmatrix}
\begin{pmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{pmatrix} +
\begin{pmatrix} \epsilon_{11} & 0 & 0 \\ 0 & \epsilon_{22} & 0 \\ 0 & 0 & \epsilon_{33} \end{pmatrix}
\begin{pmatrix} E_1 \\ E_2 \\ E_3 \end{pmatrix}
$$

$$(5)$$

From the equation (5), the four piezoelectric coefficients, d_{ij}, e_{ij}, g_{ij} and h_{ij} can be defined as

$$d_{ij} = \left(\frac{\partial D_i}{\partial T_j}\right)^E = \left(\frac{\partial S_i}{\partial E_j}\right)^T \tag{6}$$

$$e_{ij} = \left(\frac{\partial D_i}{\partial S_j}\right)^E = -\left(\frac{\partial T_i}{\partial E_j}\right)^S \tag{7}$$

$$g_{ij} = -\left(\frac{\partial E_i}{\partial T_j}\right)^D = \left(\frac{\partial S_i}{\partial D_j}\right)^T \tag{8}$$

$$h_{ij} = -\left(\frac{\partial E_i}{\partial S_j}\right)^D = -\left(\frac{\partial T_i}{\partial D_j}\right)^S \tag{9}$$

where d_{ij}, e_{ij} correspond to the direct piezoelectric effect and the g_{ij}, h_{ij} correspond to the converse piezoelectric effect. Therefore, the energy generated by the piezoelectric materials can be modeled as the energy stored in a capacitor. If the electrodes are placed along the direction of the applied external force, the generated energy can be modeled as

$$W_{33} = \frac{1}{2}Q_{33}V_{33} \tag{10}$$

where Q_{33} and V_{33} can be represented by

$$Q_{33} = d_{33}F_3 \tag{11}$$

$$V_{33} = \frac{T}{WL}F_3 g_{33}. \tag{12}$$

In equation (12), the T, W, and L are the thickness, width, and length of the

piezoelectric element. F is the applied force and g_{33}, d_{33} depend upon the material properties.

3.2. Maximum Power Point Tracking

A vibrating piezoelectric element can be modeled as a sinusoidal current source $i_p(\omega t)$ in parallel with its internal electrode capacitor C_p as shown in Figure 2. The magnitude of current source I_p varies with the mechanical stimulations and not the external load. While a vibrating piezoelectric element generates AC power, most of the electrical loads require a DC power supply. Therefore, the first stage of the energy harvesting circuit is an AC-DC rectifier connected to the output of the piezoelectric element. In the following analysis, the rectifier/filter capacitor C_{rect} is assumed to be large such that the output voltage V_o is essentially constant. The load is modeled as a resistance R_l. The diodes $D_1 - D_4$ in the full-wave rectifier are assumed to be ideal.

The ideal current generated from the piezoelectric element $i_p(\omega t)$ and the rectified output current $i_o(\omega t)$ are shown in Figure 3. The waveform of the voltage across the piezoelectric electrode capacitor, $V_p(\omega t)$ can be divided into four operation intervals. During interval I, the voltage $V_p(\omega t)$ is equal to the voltage V_{rect} and the current $i_p(\omega t)$ is positive, so the diodes D_1 and D_4 are conducting. When the current $i_p(\omega t)$ becomes negative at $\omega t = \pi$, the capacitor C_p is discharged. Thus, the voltage $V_p(\omega t)$ is decreased and all diodes are reversed-biased during interval II. The insulation between the piezoelectric element and the load continues until the voltage $V_p(\omega t)$ is reversed to $-V_{rect}$ at $(k+1)\pi$. Then, the diodes D_2 and D_3 conduct and the voltage $V_p(\omega t)$ becomes equal to $-V_{rect}$ during interval III. When the current $i_p(\omega t)$ becomes positive at 2π, the voltage $V_p(\omega t)$ changes back to V_{rect} during interval IV. When the magnitude of voltage $V_p(\omega t)$ is smaller than V_{rect}, all diodes are reversed-biased and no current flows through the resistive load during intervals II and IV. During intervals I and III, the output current flows through the rectifier capacitor C_{rect} and

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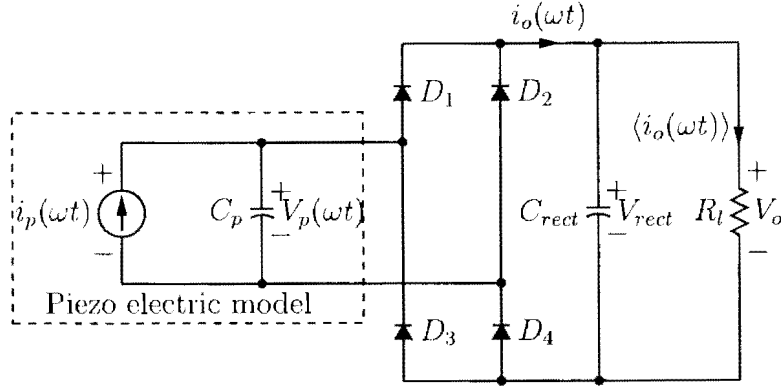
Figure 2. Piezoelectric Capacitive Model with a Full-wave Rectifier and Loads.
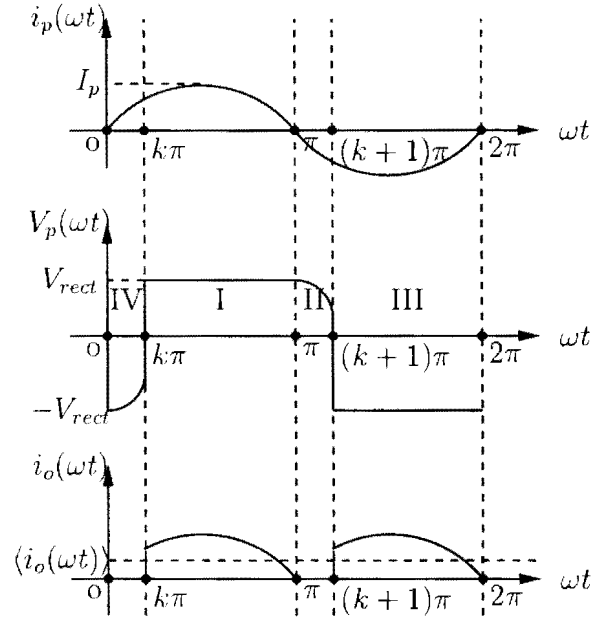
Figure 3. Voltage and Current Waveforms of a Full-wave Rectifier Circuit.

the resistive load R_l. Assuming $C_{rect} \gg C_p$, most of the generated current is delivered to the resistive load instead of charging the electrode capacitor C_p when the diodes are conducting. The output current $i_o(\omega t)$ can be represented in each period as,

$$
i_o(\omega t) = \begin{cases} 0, & \text{for } 0 \leq \omega t \leq k\pi \qquad (13a) \\ |i_p(\omega t)|, & \text{for } k\pi \leq \omega t \leq \pi. \qquad (13b) \end{cases}
$$

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The DC component of the output current $\langle i_o(\omega t) \rangle$ can be evaluated as

$$\langle i_0(\omega t) \rangle = \frac{1}{\pi} \int_{k\pi}^{\pi} I_p \sin(\omega t) d(\omega t). \tag{14}$$

Equation (14) can be written as

$$\langle i_0(\omega t) \rangle = \frac{I_p}{\pi}(1 + \cos k\pi). \tag{15}$$

In order to compute the DC component of the output current $\langle i_o(\omega t) \rangle$, the term of $\cos k\pi$ in equation (15) can be evaluated using the current-voltage relationship of the electrode capacitor C_p, which is

$$C_p \frac{dV_p}{dt} = I_p \sin \omega t. \tag{16}$$

Multiplying both sides of equation by dt and integrating over the period from 0 to $k\pi$ yields

$$\omega \int_{-V_{rect}}^{V_{rect}} C_p dV_p = \int_0^{k\pi} I_p \sin \omega t \, d\omega t \tag{17}$$

which can be reduced to

$$\cos k\pi = 1 - \frac{2\omega C_p V_{rect}}{I_p}. \tag{18}$$

Substituting for $\cos k\pi$ from equation (18) in equation (15), the DC component of the output current $\langle i_o(\omega t) \rangle$ can be represented as

$$\langle i_o(\omega t) \rangle = \frac{2I_p}{\pi} - \frac{2V_{rect}\omega C_p}{\pi}. \tag{19}$$

The output power of the piezoelectric element can be shown to vary with the value of the rectifier voltage V_{rect} as

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$$P(\omega t) = \frac{2V_{rect}}{\pi}(I_p - V_{rect}\omega C_p). \tag{20}$$

Based on the piezoelectric capacitive model with a full-wave rectifier and resistive load, the peak output power of the piezoelectric element occurs when

$$V_{rect} = \frac{I_p}{2\omega C_p} \tag{21}$$

which is approximately half of the peak open-circuit voltage of the piezoelectric element. The peak output power of the piezoelectric element is given by

$$P(\omega t)_{max} = \frac{I_p^2}{2\omega \pi C_p}. \tag{22}$$

However, the electrical characteristics of the buck converter and supercapacitor should also be considered in order to maximize the output power in the buffering subsystem.

3.3. Charging a Supercapacitor

A supercapacitor is an electric double-layer capacitor that has an ultra high power density, a low equivalent series resistance (ESR), and a low leakage current, compared to common batteries. Since supercapacitors have the capability to quickly soak up energy compared with the long charging period of batteries, they have become an active energy buffer helping the effort of the green energy campaign. For instance, since the supercapacitor can be charged and discharged at the same current rate, it has been utilized in energy storage applications such as vehicle regenerative braking [26] and wireless sensor nodes [20]. Although the charging and discharging of the supercapacitor is simple, it still presents some unique challenges unlike batteries. A supercapacitor with zero charge behaves like a short circuit to a charging source. Most power supplies fold back output current in response to a perceived short circuit,

which makes them unsuitable for charging the supercapacitors. In addition, the supercapacitor has a low series inductance which allows easy stabilization with switch mode chargers [27].

There are three modes of charging a supercapacitor: constant current charging, constant power charging, and AC line charging. Constant current charging is the simplest form with a controllable charging current. Since the power generated by the piezoelectric element has the characteristic of high voltage with low current, a buck converter is usually an essential topology. The buck converter not only regulates the output voltage to an applicable range but also strengthens the current driving capability of the piezoelectric element. In addition, the continuous output current of the buck converter overwhelms other switching mode convertors in the supercapacitor charging application. The electric model of the charging circuit for a supercapacitor with a buck converter and a piezoelectric element is shown in Figure 4, in which the equivalent parallel resistance of the supercapacitor is represented by R_c. The regulated charging current i_c can be represented in the continuous conduction mode as,

$$i_c = \frac{\langle i_o(\omega t) \rangle}{k} \tag{23}$$

in which $\langle i_o(\omega t) \rangle$ and k are the DC component of input current and the duty-cycle of the buck converter, respectively. The relationship between input and output voltages of the buck converter is given by

$$V_o = k V_{rect}. \tag{24}$$

Using equation (19), (23), and (24), the charging current of the supercapacitor can be represented as
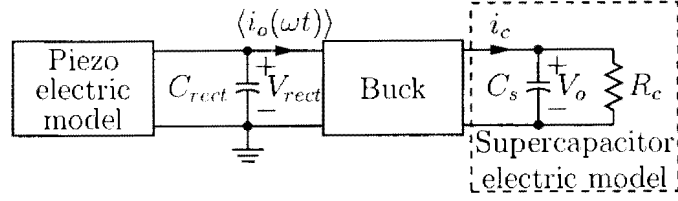
Figure 4. Electric Model of Charging a Supercapacitor.

$$i_c = \frac{2I_p}{\pi k} - \frac{2V_o\omega C_p}{\pi k^2}. \tag{25}$$

Besides the high power density of the supercapacitor, the voltage and current relationship of the supercapacitor still maintains as

$$\frac{dV_o}{dt} = \frac{i_c}{C_s}. \tag{26}$$

Since the capacitance of supercapacitor is so large that the output voltage across the supercapacitor is almost constant when the charging current is in the limiting range. If the charging current is maximized, the product of voltage and current of the supercapacitor is maximized. In addition, the power losses or supercapacitor heating can be expressed as [28].

$$P_{loss} = \frac{V_o^2}{R_c}. \tag{27}$$

According to the theory in Section 3.2, the output power of the piezoelectric element can be represented by equation (20). Using equations (20) and (27), the net harvested power delivered to the supercapacitor can be represented as

$$\sum P = \frac{2V_{rect}}{\pi}(I_p - V_{rect}\omega C_p) - \frac{V_o^2}{R_c}. \tag{28}$$

Therefore, the energy storage efficiency of the supercapacitor is proportional to the charging current with constant input power. In order to estimate the maximized

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charging current of a supercapacitor, substituting $x = k^{-1}$ in Equation (25) yields

$$i_c = \frac{2I_p}{\pi}x - \frac{2V_o\omega C_p}{\pi}x^2 \tag{29}$$

which is equivalent to

$$i_c = -\frac{2V_o\omega C_p}{\pi}(x - \frac{I_p}{2V_o\omega C_p})^2 + \frac{I_p^2}{2\pi V_o\omega C_p}. \tag{30}$$

The charging current of supercapacitor i_c can be maximized only when x is equal to $\frac{I_p}{2V_o\omega C_p}$, which means the optimum duty-cycle is given by

$$k(optimized) = \frac{2V_o\omega C_p}{I_p} \tag{31}$$

and the corresponding maximized charging current of supercapacitor is

$$i_c(max) = \frac{I_p^2}{2\pi V_o\omega C_p}. \tag{32}$$

CHAPTER 4. IMPLEMENTATION

The architecture of a piezoelectric energy harvesting circuit is shown in Figure 5. A buck converter is designed to regulate the power flow from the piezoelectric element to the load. A feedback control system is designed to optimize the duty-cycle based on the charging current of the supercapacitor C_s. The charging current is measured as a voltage across the current sensing resistor R_s. The signal representing the charging current is amplified, digitized, and sent to an FPGA for optimal duty-cycle computation. Initially, the duty-cycle will be set at 100%. The FPGA automatically decreases the duty-cycle until the charging current of the supercapacitor is maximized according to equation (32). The FPGA maintains the duty-cycle until the vibration level of the piezoelectric element is disturbed. In Section 4.1, the components used in the buck converter are designed. The implementation of feedback control system is introduced in Section 4.2.

4.1. DC-DC Buck Converter

The classical circuit diagram of buck converter using a power MOSFET is shown in Figure 6 [29]. For the buck converter, the average output voltage V_o is less than the input voltage V_s, and this is used to stepping down the high voltage output of the piezoelectric element. The waveforms of the inductor current i_L, capacitor current i_c, and capacitor voltage V_c are shown in Figure 7. The circuit operation can be divided into Mode I and Mode II. Mode I occurs from kT to T when the transistor Q_1 is switched off and the freewheeling diode D_m conducts due to the energy stored in the inductor L. The inductor current continues to flow through the capacitor C, the load R_l, and the freewheeling diode D_m. The inductor current falls until transistor Q_1 is switched on. The freewheeling diode D_m is turned off from 0 to kT in Mode II. The equivalent circuits of Mode I and Mode II are shown in Figures 8 and 9, respectively.

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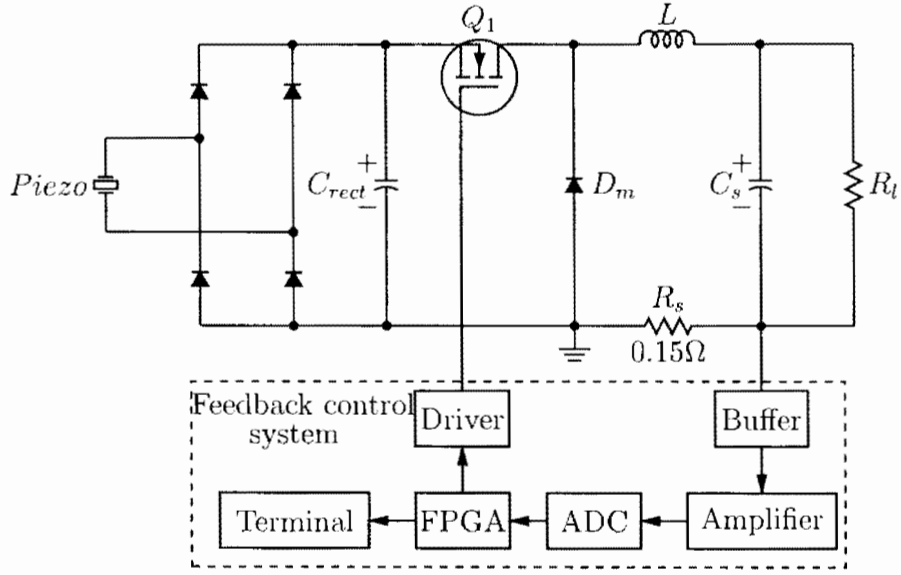
Figure 5. Architecture of Piezoelectric Energy Harvesting System.
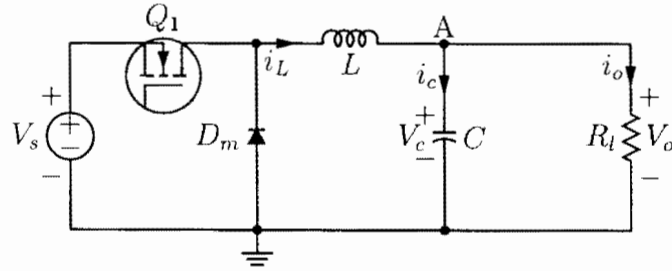
Figure 6. Schematic of a Classical DC-DC Buck Converter.

Although the transistor Q_1 has finite turn-on resistance and nonlinear v-i characteristics, they are generally neglected in the derivations. The current flowing through the inductor L is assumed to rise and fall linearly in Mode II and I, respectively. The voltage and current of the inductor is given by

$$v_L = L\frac{di}{dt}. \tag{33}$$

Assuming that the inductor current rises linearly from level I_1 to I_2 during 0 to kT in Mode II. According to the KVL, yields
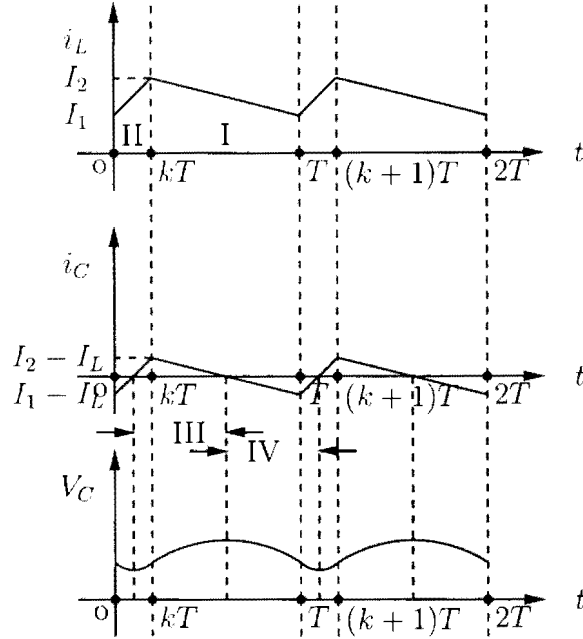
Figure 7. Waveforms of a Classical DC-DC Buck Converter.
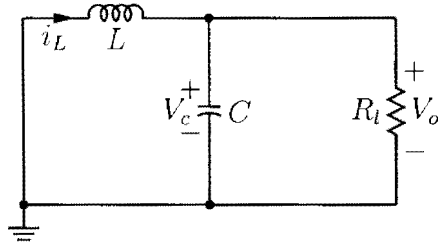
Figure 8. Equivalent Schematic of Buck Converter in Mode I.
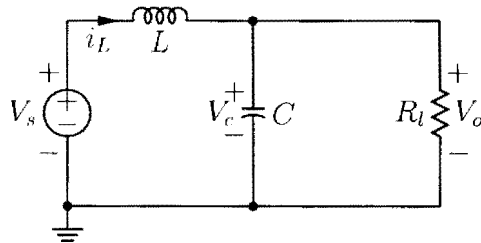
Figure 9. Equivalent Schematic of Buck Converter in Mode II.

$$V_s - V_o = L\frac{I_2 - I_1}{kT} = L\frac{\Delta I}{kT} \tag{34}$$

so the kT can be represented as

$$kT = \frac{\Delta I \cdot L}{V_s - V_o}. \tag{35}$$

Similarly, assuming the inductor current falls linearly from I_2 to I_1 during $(1 - k)T$ in mode I. The $(1 - k)T$ can be evaluated by

$$-V_o = -L\frac{\Delta I}{(1 - k)T} \tag{36}$$

, which is equivalent to

$$(1 - k)T = \frac{\Delta I \cdot L}{V_o} \tag{37}$$

where $\Delta I = I_2 - I_1$ represents the peak-to-peak ripple current of the inductor L. Using ΔI in both equations of (35) and (37), yields

$$\Delta I = \frac{(V_s - V_o)kT}{L} = \frac{V_o(1 - k)T}{L} \tag{38}$$

from which the relationship between output voltage V_o and input voltage V_s can be derived as

$$V_o = kV_s. \tag{39}$$

Assuming a lossless circuit of buck converter, the relationship between the input and the output currents is given by

$$I_s = kI_o. \tag{40}$$

Therefore, the switching period T can be evaluated by

$$T = \frac{\Delta I \cdot L \cdot V_s}{V_o(V_s - V_o)} \tag{41}$$

and the peak-to-peak ripple current flowing through the inductor L is given by

$$\Delta I = \frac{V_o(V_s - V_o)}{f \cdot L \cdot V_s}. \tag{42}$$

Using KCL at node A of Figure 6, the instantaneous inductor current i_L can be obtained as

$$i_L = i_c + i_o. \tag{43}$$

Assuming the load ripple current to be negligible, the average capacitor current during one half cycle can be expressed as

$$I_c = \frac{\Delta I}{4} \tag{44}$$

The capacitor voltage is expressed as

$$V_c = \frac{1}{C} \int_0^{\frac{T}{2}} i_c dt + V_c(t = 0) \tag{45}$$

so the peak-to-peak ripple voltage across the capacitor is obtained as

$$\Delta V_c = \frac{\Delta I}{8fC}. \tag{46}$$

Substituting the value of ΔI from equation (42) in equation (46), yields

$$\Delta V_c = \frac{V_o(V_s - V_o)}{8LCf^2 V_s} \tag{47}$$

or

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$$\Delta V_c = \frac{V_s k (1 - k)}{8 L C f^2}. \tag{48}$$

From equations (39), (42), and (47), the absolute maximum voltage and current ratings of the circuit element can be obtained. For instance, the maximum voltage drop between the source and drain of the power MOSFET Q_1 appears when Q_1 is turned off and the input voltage is maximum. Similarly, the peak current flowing through the switch is equal to the maximum current flowing through the inductor when Q_1 is conducting. From the peak-to-peak ripple current of inductor in equation (42), the peak current flowing through the inductor can be obtained as

$$I_2 - I_1 = \Delta I = \frac{V_o(V_s - V_o)}{f \cdot L \cdot V_s} \tag{49}$$

or

$$I_2 = \frac{V_o(V_s - V_o)}{f L V_s} + I_1. \tag{50}$$

In equation 50, I_1 and I_2 are minimum and maximum values of the inductor current, respectively. In order to minimize the power dissipation of the conducting freewheeling diode, a zener diode with a low forward voltage drop is used. The zener diode has only 5 μA leakage current when reverse biased at 29.7 V. In addition, it has 115 mA surge current which is five times higher than the calculated minimum peak inductor current of 26.8 mA. The absolute maximum ratings of the power MOSFET used in the design have $V_{dss} = 200$ V, $I_d = 18$ A with a turn-on resistance of only 0.15 Ω, which results in a lower conduction loss. The switching frequency of power MOSFET is set to 1 kHz. Since the maximum open-circuit DC voltage measured from the piezoelectric element is about 20 V, a 33 μF, 35 V voltage rate electrolytic capacitor is used as the rectifier capacitor. For energy storage, the design uses a 400 F,

2.7 V supercapacitor. In order to maintain the continuous current flow through the inductor, the design employs a 140 mH inductor.

4.2. Feedback Control System

In order to adaptively control the duty-cycle of the buck converter according to the charging current, an analog-to-digital converter (ADC) is used to sample the voltage across a 0.15 Ω current sense resistor shown in Figure 5. Before conversion, a 2-pole Sallen-Key anti-alias filter with cut-off frequency of 500 kHz is designed. The configuration of the ADC subsystem and the schematic of the filter are shown in Figures 10 and 11, respectively. Since the rate of the variation of the charging current is small, the bandwidth of the anti-alias filter is sufficient for current sampling. The ADC is configured to sample the current once per second and send the data to the FPGA through the serial peripheral interface (SPI). After conversion, the ADC works in the shutdown mode.

4.2.1. Sample charging current

The ADC converts a voltage signal in the range of $0 - 3.3$ V to a 12-bit digital data from 0 to 4095. The ADC uses three line interface including signals $\overline{CS}$, $SCLK$, and $SDATA$ to send the sampled data to the FPGA. The SPI can be timed up to 20 MHz. The $\overline{CS}$ is a chip select signal, which initiates the AD conversion and frames the serial interface. The $SCLK$ is a serial clock signal, which controls both the conversion rate and the timing of the serial bitstream on the serial data signal $SDATA$. In addition, the ADC uses the supply voltage V_{dd} as a voltage reference, which enables the device to operate in full-scale sampling from rail to rail. The shutdown mode of the ADC is utilized to eliminate the power consumption during the sampling process.

The operation of AD convertor begins with $\overline{CS}$ going low, which initiates the conversion process and data transfer. From the falling edge of $\overline{CS}$, the subsequent
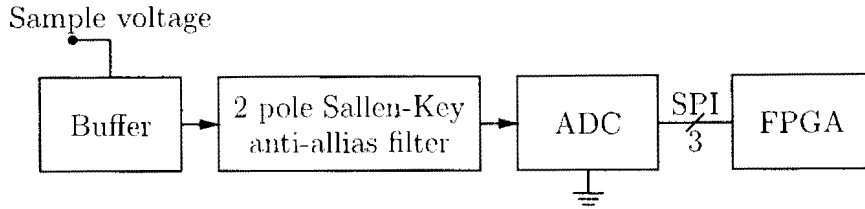
Figure 10. Architecture of an Analog to Digital Conversion Subsystem.
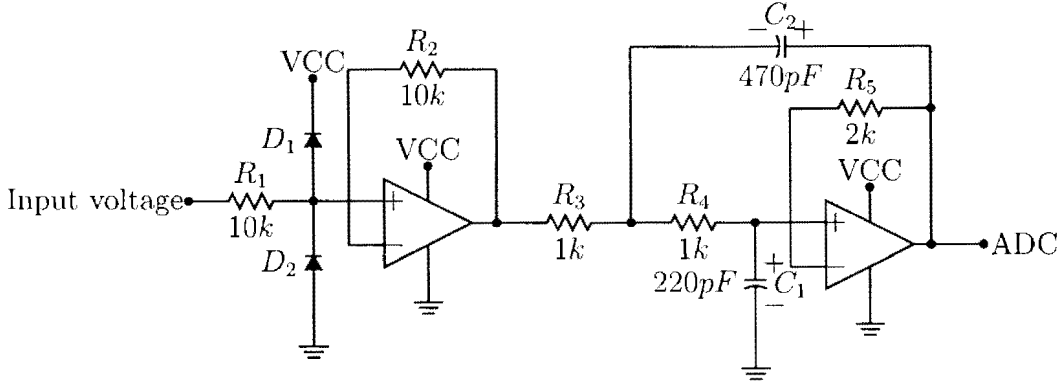
Figure 11. Schematic of Input Buffer with 2-pole Sallen-Key Anti-alias Filter.

rising and falling edges of $SCLK$ will be enabled. At the falling edge of $\overline{CS}$, the $SDATA$ comes out of high impedance state and the AD converter moves from track mode to the hold mode. The converter moves back from the hold mode to the track mode on the 13th rising edge of $SCLK$. The $SDATA$ will be placed back into tri-state after the 16th falling edge of $SCLK$, or at the rising edge of $\overline{CS}$. The minimum quiet time between each AD conversion is 50 ns. Sixteen $SCLK$ cycles are required to read a complete sample result from the AD converter. The sampled bits are clocked out on the falling edge of $SCLK$. The converter produces four leading zeros on $SDATA$ followed by 12 data bits with most significant bit (MSB) first. That is, the least significant (LSB) bit will be valid on the 16th falling edge of $SCLK$. The details of timing the ADC can be found in the datasheet of LTC1407A-1.

The assembly code to control the ADC is provided in the Appendix B. Before AD conversion, the FPGA will make sure that the $\overline{CS}$ and the counter of the bits are set to high and 24, respectively. Then, the $SCLK$ signal is set and reset at line

28
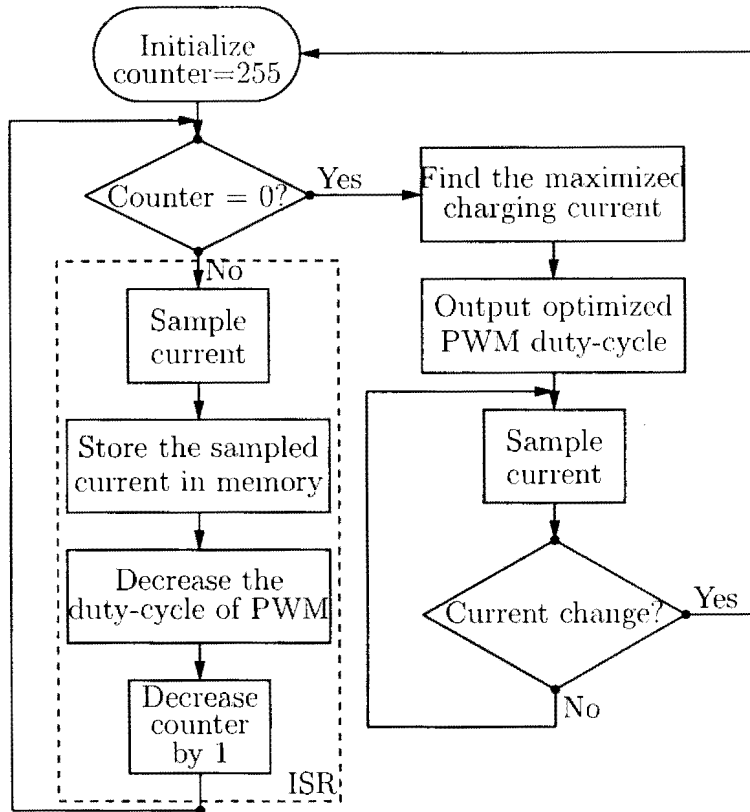
Figure 12. Flowchart of Duty-cycle Generation in FPGA.

434 and 436. The numbers of line correspond to the command in Appendix B. Once the $SCLK$ is set to low, the data bit will be available on the line $SDATA$ after maximum 40 ns data access time. The data bit is read in on line 437. Then, the data bits will be cyclically shifted into the registers sB, sC, and sD from line 438 to line 440. After 24 cycles, the upper byte and lower byte of the data are stored into the registers of "$data\_up$" and "$data\_down$" at line 445 and 444, respectively. In the end, the flag register of ADC, sE will be set at line 453 before leaving the interrupt service routines at line 455.

4.2.2. Optimized duty-cycle acquisition

The flowchart of optimized duty-cycle generation is shown in Figure 12. During system initialization, the output duty-cycle is set to 100% and an 8-bit counter in FPGA is set to 255. Then, the duty-cycle is decreased 0.39% per second, during

which the sampled current is stored in the on-chip memory. After 256 steps, the optimized duty-cycle corresponding to maximized charging current is obtained. The total process time to obtain the optimized duty-cycle is about 4 minutes, which can be reconfigured depending on the required resolution of duty-cycle. Once the mechanical vibration level of the piezoelectric element changes, the sampled instantaneous charging current is changed. The program will re-initialize to obtain a new optimized duty-cycle.

4.2.3. Software defined PWM

The pulse width modulation (PWM) is implemented by using the instructions executed by a PicoBlaze processor in the FPGA. The architecture and top-level source code in VHDL of digital system in the FPGA are shown in Figure 13 and Appendix A, respectively. The software implementation indicates that the dynamics of PWM are totally controlled by the instruction executions in the processor. The two key parameters of PWM are the pulse repetition frequency (PRF) and the resolution of duty-cycle. The design uses the PRF of 1 kHz with resolution of 8-bits, which means each step of duty-cycle can be resolved at time interval of $\frac{1\ ms}{2^8} = 3.90625\ \mu s$.

The PicoBlaze processor from Xilinx is a highly predictable processor requiring precise two clock cycles to execute one instruction. Although the PicoBlaze processor can be clocked faster in a higher speed grade of FPGA devices, the design makes direct use of a 50 MHz crystal oscillator on a development board. The PicoBlaze processor is able to execute 25 million instructions per second (MIPS) or one instruction every 40 ns. The number of instructions which can be executed within the 3.90625 μs time interval to support the PRF and duty-cycle resolution is $\lfloor \frac{3.90625\ \mu s}{40\ ns} \rfloor = 97$ where $\lfloor \rfloor$ indicates rounding the operand to the nearest integer smaller than itself.

The PWM generation in the design is periodic. It is quite common for software implemented PWM in microcontroller to only support burst of pulses in order to have
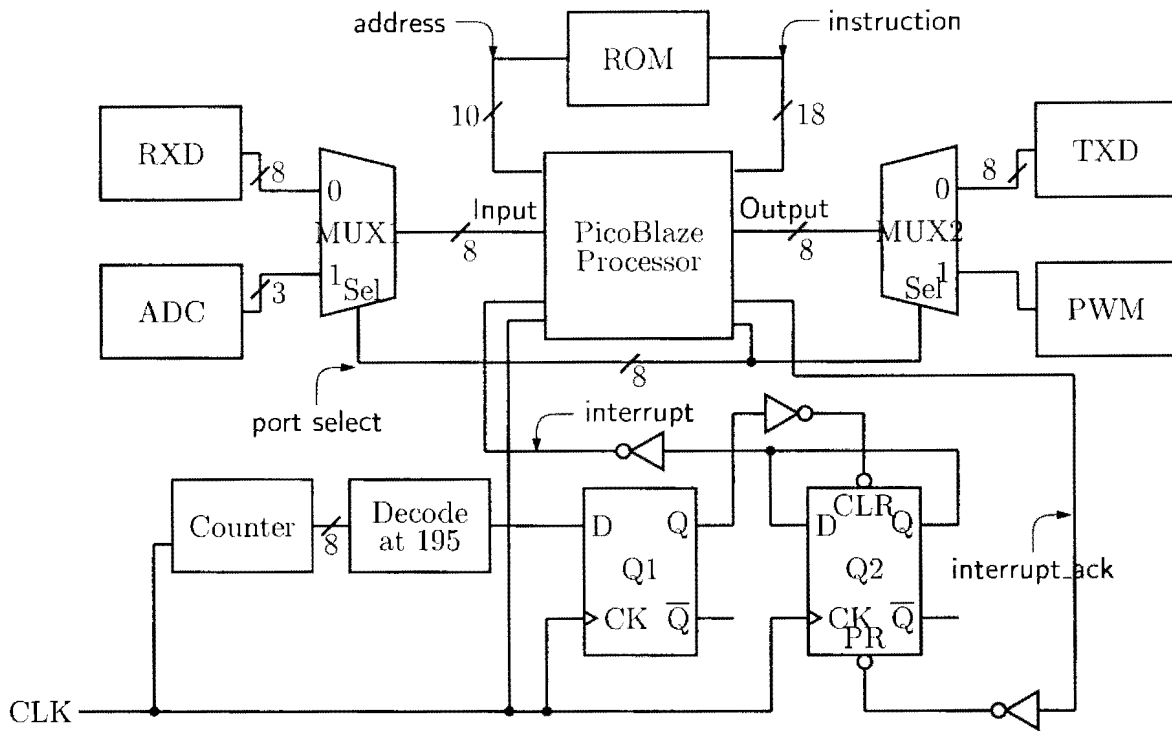
Figure 13. Architecture of Digital System in FPGA.

time to perform other tasks. Such a compromise in the case of microcontroller will not be required when using an FPGA embedded with the high performance PicoBlaze processor. Increasing PRF or increasing the duty-cycle resolution will reduce the number of instructions which can be executed during each step. In the end, there will only be enough instructions available to generate the PWM itself. Higher clock rates can be a solution only when the speed grade of FPGA is compatible, which is the delay in ns of the configurable logic blocks (CLB) in FPGA. However, 97 instructions in this design are adequate to generate the PWM signal and still have approximately 50% of the processor resources available for higher level control tasks such as dealing with the universal asynchronous receiver/transmitter (UART), processing the text commands from the terminal, and communicating with the ADC through the SPI.

If the PWM implementation code is put in the main program, there will be fluctuations in the PRF and duty-cycle as various processor tasks take more or less

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time to complete. In order to provide an accurate PRF, duty-cycle resolution, and high degree of consistency in each period, the design uses an interrupt mechanism to control the timing of the duty-cycle generation. As shown in Figure 13, the design uses an 8-bit counter and decoder to set the buffered interrupt input signal *"interrupt"*. The counter has 196 integer states and generates the interrupt pulses with a 50 MHz clock input. This is equivalent to interrupt every $196 \times 20\ ns = 3.92\ \mu s$ with a corresponding PRF of 996.5 Hz. The interrupt signal will be cleared by the interrupt acknowledgement signal of the processor *"interrupt_ack"*. Although the design of FPGA provides a fixed PRF, this setup could be upgraded by reconfiguring the FPGA in the field. During each interruption, a 24-bit duty-cycle register increases by one. The value of the duty-cycle register is compared with the value of a preset PWM register to update the duty-cycle output. The upper 16-bit of the duty-cycle register is used to time the AD conversion once per second. The ADC and interrupt flag registers are set accordingly to the corresponding processing in the ISR. After the program counter returns from ISR, the sampled data is compared with expected value computed during initialization process. If the value is smaller, the value of the PWM register will decrease. Therefore, the duty cycle output will also decrease until the sampled value becomes equal to the pre-computed value.

The code of ISR is provided in Appendix B. A PicoBlaze processor interrupt signal forces the program counter to interrupt vector. Therefore, at the program memory address of hex $3FF$, the code must direct the program counter to the ISR, which is achieved by a simple *"JUMP"* instruction at line 457. Once the program counter jumps to the address with label ISR, instruction *"DINT"* at line 405 will disable additional interruptions. At first, the contents of registers $s0$, $s1$, and $s2$ are stored in a scratch pad memory (SPM), so the registers are free to be used in the ISR without effecting the main code after interrupt returns. The

ISR also has the responsibility to communicate with the ADC once per second besides PWM generation. That is the reason why the ISR uses three SPM registers "pwm_duty_counter1/2/3" to count the number of interruptions from line 406 to line 415. It is noted that the SPM register "PWM_duty_counter1" is the register to progress through the 256 steps from hex 00 to FF of each PWM cycle. The SPM register "PWM_channel" holds the preset duty-cycle in the ISR at line 416.

As shown in line 417, preset value in the register "PWM_channel" is compared with the counter value in register "PWM_duty_counter1". The instruction "COMP" in line 417 is the functional equivalent to the instruction "SUB" except the subtraction result is discarded. However, the carry flag is set if the subtraction result is negative. Therefore, if the duty-cycle value is greater than the current counter value, then the carry flag is set and this corresponds to the requirement of PWM output to be high. At line 418, the instruction "SLA" shifts the status of the carry flag left into the LSB of the $s9$ register. Then, the "pwm_output_port" port is driven to high at line 419. Because the ADC samples the voltage once per second, the total number of interruptions during one second is 256000, which is equal to hex $03E800$. After setting the interrupt flag register sF at line 454, the program counter returns to *main* program with interrupts enabled, and it is ready to respond to the next interrupt of PWM.

CHAPTER 5. EXPERIMENT

5.1. Experiment Setup

The experimental setup of the piezoelectric energy harvesting system is shown in Figure 14. The experiment uses the piezoelectric element QuickPack, QP20W, from Mide Inc. as power source, which is shown in Figure 15. The bimorph piezoelectric element has two 10 *mil* depth piezoelectric materials stacked in one epoxy. The specifications of the piezoelectric element are shown in Table 1. The equivalent capacitance of piezoelectric element is only 0.2 μF, which is much smaller than the 33 μF rectifier capacitor in Figure 2. Therefore, most of the power generated from the piezoelectric element will flow into the load when the diodes conduct. One edge of the piezoelectric element is fixed on a mechanical wave vibrator in the horizontal cantilever configuration as shown in Figure 16. The mechanical wave vibrator has frequency range of 0.1 to 5 kHz with vibration amplitude up to 7 mm at a vibration frequency of 1 Hz. According to its data sheet, the maximum vibration amplitude will decrease when the vibration frequency is increased. Since the vibrator requires a minimum driving signal of ± 8 V, 0.5 A, an accurate variable-frequency signal generator and a power amplifier are used to generate the driving signal.

The harvested energy from the piezoelectric element is rectified and regulated using a converter circuit whose printed circuit board (PCB) implementation is shown in Figure 17. The ADC module samples the charging current of the supercapacitor and sends the information to the PicoBlaze processor in a Spartan-3E FPGA. The generated PWM signal from the FPGA's general-purpose I/O drives the power MOSFET in the buck converter through a buffer. Meanwhile, the information on charging current and duty-cycle is sent to a terminal through a serial RS232 port. The baud rate of the serial communication is set to 115200.
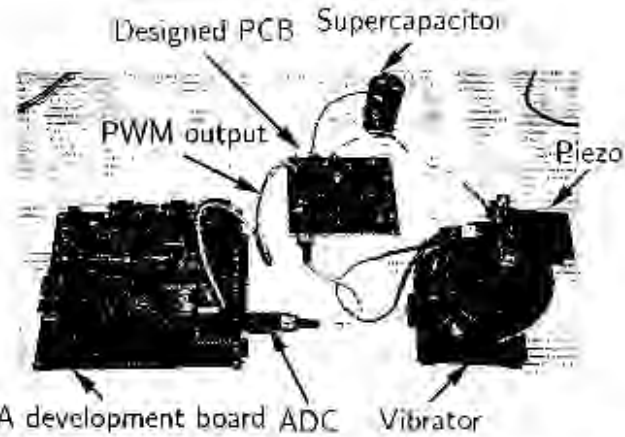
Figure 14. Experiment Setup of Piezoelectric Energy Harvesting System.

Figure 15. Packaged Piezoelectric Element QP20W from Mide Inc.

Figure 16. Cantilever Configuration of Piezoelectric Element on a Vibrator.

5.2. Experiment Result

At first, the piezoelectric element was tested under open circuit configuration. The open circuit peak-to-peak voltage $V_{oc}(p-p)$ generated from the piezoelectric

35

3.69 inch

4.31 inch
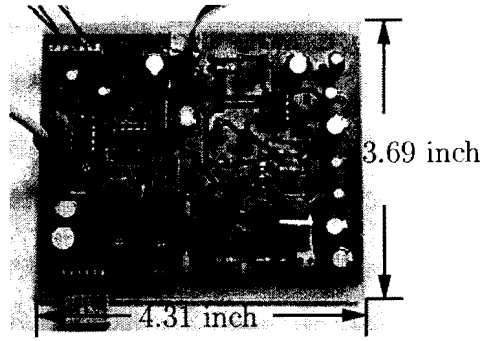
Figure 17. PCB Board of a Buck Converter with Peripheral Interfaces.

Table 1. Specifications of Piezo, QuickPack QP20W

Specifications	value
Device size, inch	$2.00 \times 1.50 \times 0.03$
Device weight, oz	0.28
Active elements	1 stack of 2 piezos
Piezo wafer size, inch	$1.81 \times 1.31 \times 0.01$
Device capacitance, μF	0.20
Full scale voltage range, V	± 200

element is about 87.0 V and its root mean square (RMS) value $V_{oc}(rms)$ is about 28.9 V. The piezoelectric element is paralleled with a resistive load and the RMS value of the output voltage is measured with different resistances as shown in the Figure 18. When the resistive load is set to 100 $k\Omega$ and 1 $M\Omega$, the RMS values of the output voltage are approximately 5 V and 22 V, respectively. The corresponding output powers of the piezoelectric element are 0.25 mW and 0.48 mW. When the resistive load is increased above 2 $M\Omega$, it behaves as an open-circuit and the RMS value of output voltage approximates to the open-circuit voltage of 28.9 V. This demonstrates the power generation capability of the piezoelectric element at 7 Hz vibration level.

In the second experiment, the piezoelectric element is paralleled with a 100 μF capacitor without resistive load. When the vibration frequency is maintained at 7 Hz, the capacitor can be charged up to 20.3 V. After a resistive load is added, the voltage

Table 2. Design Performance Benchmark

Specifications	Ottoman (2002)	Zhou
Optimized duty-cycle	3.18% or 3.16%	2.17%
Maximized charging current, mA	4.3	17.36
Rectifier voltage, V	20.4	20.3
Open-circuit voltage, V	40	28.9
PWM frequency, kHz	1	1
Converter efficiency	65%	67.4%
Setup time, s	360	250

Table 3. Device Resource Utilization of Spartan-3E FPGA

Specifications	Used	Available	Utilization
# of flip-flops	108	9312	1%
# of occupied slices	118	4656	2%
# of 4 input LUTs	199	9312	2%
# of bonded IOBs	24	232	10%
# of RAMB16s	1	20	5%
# of BUFGMUXs	1	24	4%

of which the capacitor is charged on will depend upon the load resistance. When the resistance is increased, the voltage will increase, because the discharge current through the resistance is decreased. The relationship between output power and the capacitor voltage is shown in Figure 19. As the resistive load is increased from 10 $k\Omega$ to 1 $M\Omega$, the mean output voltage will increase from 420 mV to 10.12 V, and the output power will increase from 0.02 mW to 0.1 mW. Although, the mean output voltage keeps on increasing while the resistive load is increased, the output power is decreased after the mean output voltage reaches 10 V. The maximum output power of 0.1 mW is available when the mean output voltage is around 10 V, which is approximately half of the open-circuit voltage V_{oc} (mean) of 20.3 V. The result proves the existence of the maximum output power point for the piezoelectric element at 7 Hz vibration level.

In order to estimate the power generation capability of the piezoelectric element at other vibration levels, the piezoelectric element is set to vibrate at 14 Hz. Because

the strain of the piezoelectric element at 14 Hz is much smaller than that at 7 Hz, the mean output voltage at 14 Hz is only 1.14 V. The buck converter was connected between the piezoelectric element and the load with a manually adjusted duty-cycle. The relationship between input voltage of the buck converter and the duty-cycle is shown in Figure 20. When the duty-cycle is decreased from 6.25% to 0.39%, the input voltage of the buck converter will increase from 0.2 V to 1.9 V with a 500 $k\Omega$ load. Similarly, the input voltage of the buck converter will increase from 0.128 V to 0.912 V with a 50 $k\Omega$ load. From the equations of the maximum output power of piezoelectric element [11], the maximum output power will be obtained when the input voltage of the buck converter is half of the open-circuit voltage of the piezoelectric element. Therefore, the optimum duty-cycles are 3.13% and 1.56% for 500 $k\Omega$ and 50 $k\Omega$ loads, respectively. Similarly, the input voltage of the buck converter can be adjusted to around 10 V at a vibration frequency of 7 Hz. The corresponding output voltage across the 93 $k\Omega$ resistive load is 2.5 V. Therefore, the transfer efficiency of buck converter is about 67.4%.

In the third experiment, a designed feedback control system is added to test the performance of the designed circuit as shown in Figure 21. The relationship between the sampled charging current of the supercapacitor and the duty-cycle is provided. When the vibration level of the piezoelectric element is 7 Hz with $V_{oc}(rms)$ of 28.9 V, the measured charging current is very small until the duty-cycle is decreased to 25%. The charging current increases significantly when duty-cycle is decreased from 10% to 2%. However, a duty-cycle smaller than 1.4% degrades the charging current of the supercapacitor significantly. The maximum charging current of 17.36 mA is measured when the duty-cycle is optimized to 2.17%.

As observed in the second experiment, the measured maximum output power of piezoelectric element is about 100 μW at 7 Hz. Then, the estimated value of I_p is
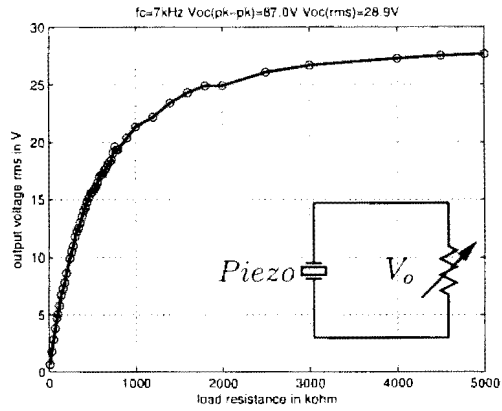
Figure 18. Output Voltage of Piezo with a Direct Resistive Load.
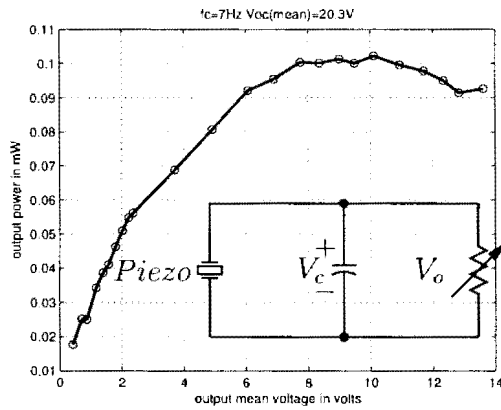
Figure 19. Output Power versus Mean Output Voltage.
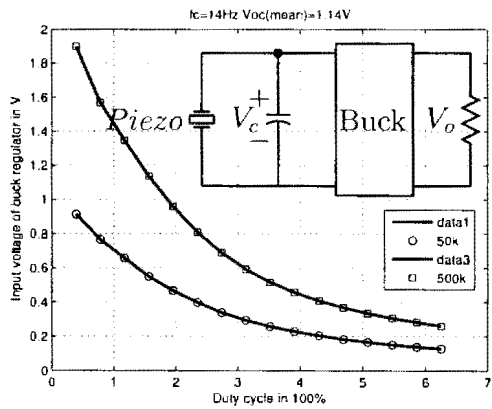
Figure 20. Input Voltage versus Duty-cycle.
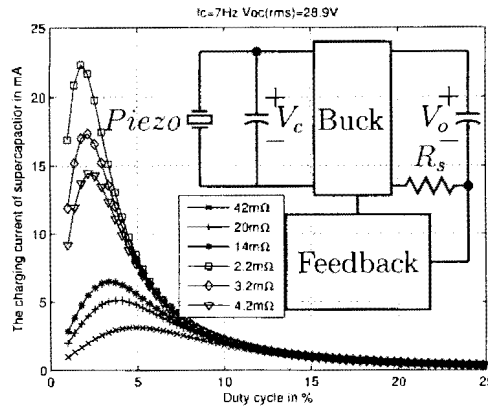
Figure 21. Charging Current of Supercapacitor versus Duty-cycle.

Table 4. Electrical Specifications of Different Supercapacitors I

Specifications	PC-10	BCAP0025	BCAP0050	BCAP0150
Capacitance, F	10	25	50	150
Voltage, V	2.5	2.7	2.7	2.7
DC ESR, $m\Omega$	0.18	42	20	14
Operation temp, $°C$	$-40 \sim 70$	$-40 \sim 65$	$-40 \sim 65$	$-40 \sim 65$
Power density, W/kg	660	2900	3100	1700
Energy density, Wh/kg	6.9mAh	3.62	3.62	4.34
Leakage current, mA	0.04	0.045	0.075	0.5

about 4.89 μA. Using Equation (31) with $\omega = 7\ Hz$ and $C_p = 0.2\ \mu F$, the estimated V_o will be about 6 mV. At this point, if the piezo is just connected with a 93 $k\Omega$ resistive load, the output voltage can stabilize at 2.5 V, which means the output power of piezo is about 67.2 μW. With the same input impedance as in Figure 18, the value of I_p will be about 70.7 μA. Using Equation (32), the estimated i_c is 15.08 mA, which is close to the measured value of 17.36 mA. With different supercapacitors,

Table 5. Electrical Specifications of Different Supercapacitors II

Specifications	BCAP0310	BCAP350	NESSCAP
Capacitance, F	310	350	400
Voltage, V	2.5	2.5	2.7
DC ESR, $m\Omega$	2.2	3.2	4.2
Operation temp, $°C$	$-40 \sim 65$	$-40 \sim 65$	$-40 \sim 60$
Power density, W/kg	5600	3900	5340
Energy density, Wh/kg	4.48	5.1	6.23
Leakage current, mA	0.45	1	1

both the maximum charging current and optimum duty-cycle are increased when the ESR of the supercapacitor is decreased, which is shown in Figure 21. However, there is also a tradeoff between the charging current and energy density in choosing a proper supercapacitor. A variety of supercapacitors with different specifications are shown in Table 4 and Table 5.

As shown in the Table 2, although the rectifier voltage and the efficiency of the converter are the same as in previous researches, the charging current of the supercapacitor is improved by a factor of 4, because the supercapacitor can quickly soak up the power generated from piezoelectric element. In addition, only 69.4% of the time used in other researches is needed to scan the full duty-cycle range. As shown in Table 3, only about 1 – 2% FPGA resource is used to adaptively optimize the duty-cycle. As measured from Xilinx power analyzer, the total quiescent and dynamic power consumption of FPGA are about 81 mW and 3 mW, respectively. Based on the ultra high frequency (UHF) RFID research [30], a DC power of 16.7 μW extracted from RF signal is necessary to power the RFID tag internal logic. With the energy of 67.2 μW harvested from piezoelectric element, the front-stage voltage-multiplier of the RFID tag can be eliminated. In addition, the reading distance of an active RFID tag can be further extended by harvesting the energy from piezoelectric element.

In order to prove the feasibility of designing a stand-alone energy harvesting system, the digital design in FPGA is synthesized using different process technologies. The specifications of ASIC design with different process technologies are shown in Table 6. Both core area and power consumption are decreased with smaller process node. The power consumption of about 0.86 mW in 90 nm process is close to the harvested power of 0.1 mW. The architecture of synthesized ASIC design is shown in Figure 22.

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Table 6. Specifications of ASIC Design

Specifications	AMIS	IBM 7HP	TSMC	TSMC
Technology	$0.5\ \mu m$	$180\ nm$	$130\ nm$	$90\ nm$
Cells	6574	4917	4446	4579
Core area μm^2	2,690,703	38,204	57,585	28,362
Leakage power nW	812	0	95	244,173
Dynamic power nW	165,216,621	5,615,867	1,828,778	612,870
Total power nW	165,217,434	5,615,867	1,828,873	857,044
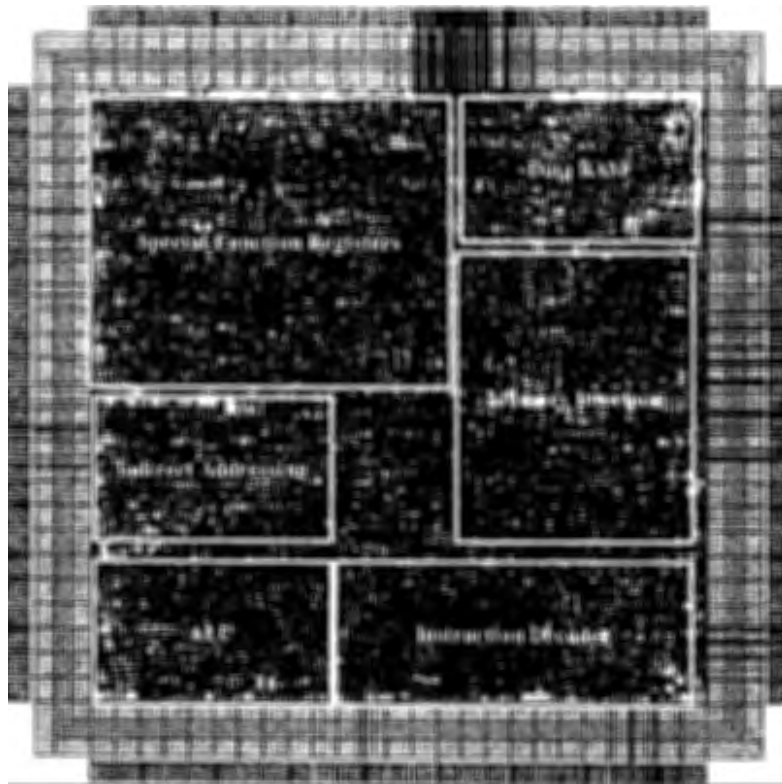
Figure 22. Die Photograph of ASIC Core Design.

CHAPTER 6. CONCLUSION

Due to the high power density of the supercapacitor, the output voltage is almost constant. Therefore, the charging current is critical in evaluating the efficiency of energy storage in the supercapacitor. With the designed feedback control system, the charging current of the supercapacitor can be maximized by using the optimized duty-cycle for the buck converter. The maximum charging current of 17.36 mA is measured when the duty-cycle is optimized to 2.17%. Since the power consumption of the processor in the FPGA is significant, an application specific integrated circuit (ASIC) is simulated to estimate the power budget of stand-alone energy harvesting system.

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APPENDIX A. TOP-LEVEL FPGA DESIGN IN VHDL

```
--- Company: North Dakota State University
--- Engineer: Zhou Zhao
---
--- Create Date:      15:13:28 05/25/2007
--- Design Name:      pwm auto
--- Module Name:      pwm_auto - Behavioral
--- Project Name:     pwm auto
--- Target Devices: xc3s500e-4fg320
--- Tool versions:   ise 8.2i
--- Description:
---
--- Dependencies:
---
--- Revision:
--- Revision 0.01 - File Created
--- Additional Comments:
---


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


--- Uncomment the following library declaration if
    instantiating
```

```vhdl
-- any Xilinx primitives in this code.
-- library UNISIM;
-- use UNISIM.VComponents.all;


entity pwm_auto is
port(
        adc_sclk      : out     std_logic;
        adc_cs        : out     std_logic;
        adc_sdata     : in      std_logic;
        led           : out     std_logic_vector(7 downto 0);
        pwm_out       : out     std_logic;
        lcd_d         : inout   std_logic_vector(7 downto 4);
        lcd_rs        : out     std_logic;
        lcd_rw        : out     std_logic;
        lcd_e         : out     std_logic;
        clk           : in      std_logic;
        simple_io     : out     std_logic_vector(3 downto 0)
    );
end pwm_auto;


architecture Behavioral of pwm_auto is


component kcpsm3
port(
        address       : out std_logic_vector(9 downto 0);
        instruction   : in      std_logic_vector(17 downto 0);
```

```vhdl
        port_id       : out    std_logic_vector(7 downto 0);

        write_strobe  : out    std_logic;

        out_port      : out    std_logic_vector(7 downto 0);

        read_strobe   : out    std_logic;

        in_port       : in   std_logic_vector(7 downto 0);

        interrupt     : in   std_logic;

        interrupt_ack : out std_logic;

        reset         : in   std_logic;

        clk           : in   std_logic
    );
end component;


component pwm_auto_rom
port(
        address       : in   std_logic_vector(9 downto 0);

        instruction   : out    std_logic_vector(17 downto 0);

        clk           : in   std_logic
    );
end component;


signal sig_address       : std_logic_vector(9 downto 0);

signal sig_instruction    : std_logic_vector(17 downto 0);

signal sig_port_id        : std_logic_vector(7 downto 0);

signal sig_out_port       : std_logic_vector(7 downto 0);

signal sig_in_port        : std_logic_vector(7 downto 0);

signal sig_write_strobe   : std_logic;
```

```vhdl
signal sig_read_strobe      : std_logic;
signal sig_interrupt       : std_logic := '0';
signal sig_interrupt_ack   : std_logic;
signal sig_reset           : std_logic := '0';
signal interrupt_count     : integer range 0 to 195 := 0;
signal interrupt_event     : std_logic;
signal lcd_output_data     : std_logic_vector(7 downto 4);
signal lcd_drive           : std_logic;
signal lcd_rw_control      : std_logic;


begin

processor: kcpsm3
port map(
        address        => sig_address ,
        instruction    => sig_instruction ,
        port_id        => sig_port_id ,
        write_strobe   => sig_write_strobe ,
        out_port       => sig_out_port ,
        read_strobe    => sig_read_strobe ,
        in_port        => sig_in_port ,
        interrupt      => sig_interrupt ,
        interrupt_ack  => sig_interrupt_ack ,
        reset          => sig_reset ,
        clk            => clk
    );
```

```vhdl
program_rom: pwm_auto_rom
port map(
        address      => sig_address,
        instruction  => sig_instruction,
        clk          => clk
    );


interrupt_control: process(clk)
begin
  if clk'event and clk='1' then

    if interrupt_count=195 then
      interrupt_count <= 0;
      interrupt_event <= '1';
    else
      interrupt_count <= interrupt_count + 1;
      interrupt_event <= '0';
    end if;

    if sig_interrupt_ack='1' then
      sig_interrupt <= '0';
    elsif interrupt_event='1' then
      sig_interrupt <= '1';
    else
      sig_interrupt <= sig_interrupt;
```

```vhdl
        end if;


    end if;
end process interrupt_control;


input_ports: process(clk)
begin
    if clk'event and clk='1' then


        case sig_port_id(1 downto 0)is
            when "01" => sig_in_port <= adc_sdata & "0000000";
            when "10" => sig_in_port <= led_d & "0000";
            when others => sig_in_port <= "XXXXXXXX";
        end case;
    end if;
end process input_ports;


output_ports: process(clk)
begin
if clk'event and clk='1' then
    if sig_write_strobe = '1' then


        if sig_port_id(7) = '1' then
            led <= sig_out_port;
        end if;
```

```vhdl
        if sig_port_id(2) = '1' then
          pwm_out <= sig_out_port(0);
        end if;


        if sig_port_id(3) = '1' then
          adc_sclk <= sig_out_port(0);
          adc_cs <= sig_out_port(1);
        end if;


        if sig_port_id(6) = '1' then
          lcd_output_data   <= sig_out_port(7 downto 4);
          lcd_drive         <= sig_out_port(3);
          lcd_rs            <= sig_out_port(2);
          lcd_rw_control    <= sig_out_port(1);
          lcd_e             <= sig_out_port(0);
        end if;


      end if;
   end if;
end process output_ports;


lcd_rw <= lcd_rw_control and lcd_drive;
lcd_d <= lcd_output_data when (lcd_rw_control = '0' and
    lcd_drive = '1') else "ZZZZ";


simple_io(3 downto 0) <= "1111";
```

```
end Behavioral;
```

APPENDIX B. CONTROL CODE IN ASSEMBLY

led_port	EQU	,	$80
led_0	EQU	,	$01
led_1	EQU	,	$02
led_2	EQU	,	$04
led_3	EQU	,	$08
led_4	EQU	,	$10
led_5	EQU	,	$20
led_6	EQU	,	$40
led_7	EQU	,	$80
lcd_port	EQU	,	$40
lcd_e	EQU	,	$01
lcd_rw	EQU	,	$02
lcd_rs	EQU	,	$04
lcd_drive	EQU	,	$08
lcd_4	EQU	,	$10
lcd_5	EQU	,	$20
lcd_6	EQU	,	$40
lcd_7	EQU	,	$80
pwm_output_port	EQU	,	$04
pwm_out	EQU	,	$01
adc_control_port	EQU	,	$08
adc_sclk	EQU	,	$01

adc_cs	EQU	,	$02
adc_input_port	EQU	,	$01
adc_sdata	EQU	,	$80
delay_1us_constant	EQU	,	17
character_a	EQU	,	$61
character_b	EQU	,	$62
character_c	EQU	,	$63
character_d	EQU	,	$64
character_e	EQU	,	$65
character_f	EQU	,	$66
character_g	EQU	,	$67
character_h	EQU	,	$68
character_i	EQU	,	$69
character_j	EQU	,	$6A
character_k	EQU	,	$6B
character_l	EQU	,	$6C
character_m	EQU	,	$6D
character_n	EQU	,	$6E
character_o	EQU	,	$6F
character_p	EQU	,	$70
character_q	EQU	,	$71
character_r	EQU	,	$72
character_s	EQU	,	$73

character_t	EQU	,	$74
character_u	EQU	,	$75
character_v	EQU	.	$76
character_w	EQU	,	$77
character_x	EQU	,	$78
character_y	EQU	,	$79
character_z	EQU	,	$7A
character_A_	EQU	,	$41
character_B_	EQU	,	$66
character_C_	EQU	,	$67
character_D_	EQU	,	$68
character_E_	EQU	,	$69
character_F_	EQU	,	$70
character_G_	EQU	,	$71
character_H_	EQU	,	$72
character_I_	EQU	,	$73
character_J_	EQU	,	$74
character_K_	EQU	,	$75
character_L_	EQU	,	$76
character_M_	EQU	,	$77
character_N_	EQU	,	$78
character_O_	EQU	,	$79
character_P_	EQU	,	$80
character_Q_	EQU	,	$81
character_R_	EQU	,	$82

```
character_S_          EQU          , $83

character_T_          EQU          , $84

character_U_          EQU          , $85

character_V_          EQU          , $86

character_W_          EQU          , $87

character_X_          EQU          , $88

character_Y_          EQU          , $89

character_Z_          EQU          , $5A


character_0           EQU          , 72

character_1           EQU          , 73

character_2           EQU          , 80

character_3           EQU          , 81

character_4           EQU          , 82

character_5           EQU          , 83

character_6           EQU          , 84

character_7           EQU          , 85

character_8           EQU          , 86

character_9           EQU          , 87


character_colon       EQU          , 88

character_stop        EQU          , 70

character_semicolon   EQU          , 89

character_minus       EQU          , 69

character_divide      EQU          , 71

character_plus        EQU          , 67
```

```
character_comma          EQU          , 68
character_less           EQU          , 96
character_greater        EQU          , 98
character_equals         EQU          , 97
character_space          EQU          , 50
character_CR             EQU          , 19
character_question       EQU          , 99
character_dollar         EQU          , 54
character_exclaim        EQU          , 51
character_BS             EQU          , 8


sample_counter           EQU          , 0
pwm_duty_counter1        EQU          , 1
pwm_duty_counter2        EQU          , 2
pwm_duty_counter3        EQU          , 3
counter                  EQU          , 4


pwm_channel              EQU          , 5


data_up                  EQU          , 6
data_down                EQU          , 7



VHDL "Rom_form.vhd","pwm_auto_rom.vhd""pwm_auto_rom"



                         ORG          0
cold_start:              CALL         init_lcd
```

```
                    CALL        init_adc
        LOAD        s0 , $00
                    STORE       s0 , sample_counter
                    STORE       s0 , pwm_duty_counter1
                    STORE       s0 , pwm_duty_counter2
                    STORE       s0 , pwm_duty_counter3
                    STORE       s0 , counter
                    LOAD        s0 , $10
                    STORE       s0 , pwm_channel
                    EINT
warm_start:         LOAD        sF , $00
wait_interrupt:     COMP        sF , $00
                    JUMP        Z , wait_interrupt
                    COMP        sE , $00
                    JUMP        Z , display
                    LOAD        sE , $00
                    FETCH       s5 , data_up
                    COMP        s5 , $05
                    JUMP        C , pwm_auto
                    JUMP        NZ , counter_update
                    FETCH       s5 , data_down
                    COMP        s5 , $71
                    JUMP        C , pwm_auto
counter_update:     FETCH       s5 , counter
                    ADD         s5 , 1
                    STORE       s5 , counter
```

```
pwm_auto:        FETCH      s5 , sample_counter
                 COMP       s5 , $3C
                 JUMP       NZ, display
                 LOAD       s5 , $00
                 STORE      s5 , sample_counter
                 FETCH      s5 , counter
                 COMP       s5 , $1E
                 JUMP       NC, stop
                 FETCH      s5 , pwm_channel
                 SUB        s5 , 1
                 JUMP       NZ, update_pwm
                 LOAD       s5 , $01
update_pwm:      STORE      s5 , pwm_channel
stop:            LOAD       s5 , $00
                 STORE      s5 , counter
display:         LOAD       s5 , $10
                 CALL       lcd_cursor
                 CALL       write_Duty
                 CALL       write_space
                 CALL       write_Cycle
                 CALL       write_colon
                 FETCH      s5 , pwm_channel
                 SR0        s5
                 SR0        s5
                 SR0        s5
                 SR0        s5
```

```
LOAD        s8 , s5

CALL        hex_to_ascii

CALL        lcd_write_data

FETCH       s5 , pwm_channel

AND         s5 , $0F

LOAD        s8 , s5

CALL        hex_to_ascii

CALL        lcd_write_data

CALL        write_H

LOAD        s5 , $20

CALL        lcd_cursor

CALL        write_ADC

CALL        write_colon

FETCH       s5 , data_up

SR0         s5

SR0         s5

SR0         s5

SR0         s5

LOAD        s8 , s5

CALL        hex_to_ascii

CALL        lcd_write_data

FETCH       s5 , data_up

AND         s5 , $0F

LOAD        s8 , s5

CALL        hex_to_ascii

CALL        lcd_write_data
```

```
FETCH       s5 , data_down

SR0         s5

SR0         s5

SR0         s5

SR0         s5

LOAD        s8 , s5

CALL        hex_to_ascii

CALL        lcd_write_data

FETCH       s5 , data_down

AND         s5 , $0F

LOAD        s8 , s5

CALL        hex_to_ascii

CALL        lcd_write_data

CALL        write_H

CALL        write_space

FETCH       s5 , counter

SR0         s5

SR0         s5

SR0         s5

SR0         s5

LOAD        s8 , s5

CALL        hex_to_ascii

CALL        lcd_write_data

FETCH       s5 , counter

AND         s5 , $0F

LOAD        s8 , s5
```

```
                    CALL        hex_to_ascii
                    CALL        lcd_write_data
                    CALL        write_H
                    JUMP        warm_start
hex_to_ascii:       SUB         s8 , 16
                    JUMP        C,  number
                    ADD         s5 , $07
number:             ADD         s5 , $30
                    RET
write_Duty:         LOAD        s5 , character_D_
                    CALL        lcd_write_data
                    LOAD        s5 , character_u
                    CALL        lcd_write_data
                    LOAD        s5 , character_t
                    CALL        lcd_write_data
                    LOAD        s5 , character_y
                    CALL        lcd_write_data
                    RET
write_Cycle:        LOAD        s5 , character_C_
                    CALL        lcd_write_data
                    LOAD        s5 , character_y
                    CALL        lcd_write_data
                    LOAD        s5 , character_c
                    CALL        lcd_write_data
                    LOAD        s5 , character_l
                    CALL        lcd_write_data
```

```
                              LOAD        s5 , character_e
                              CALL        lcd_write_data
                              RET
write_space :                 LOAD        s5 , character_space
                              CALL        lcd_write_data
                              RET
write_colon :                 LOAD        s5 , character_colon
                              CALL        lcd_write_data
                              RET
write_ADC :                   LOAD        s5 , character_A_
                              CALL        lcd_write_data
                              LOAD        s5 , character_D_
                              CALL        lcd_write_data
                              LOAD        s5 , character_C_
                              CALL        lcd_write_data
                              RET
write_H :                     LOAD        s5 , character_H_
                              CALL        lcd_write_data
                              RET
init_adc :                    LOAD        s6 , $F2
                              OUT         s6 , adc_control_port
                              RET
init_lcd :                    CALL        delay_20ms
                              LOAD        s4 , $30
                              CALL        lcd_write_inst4
                              CALL        delay_20ms
```

```
              LOAD      s4 , $30
              CALL      lcd_write_inst4
              CALL      delay_1ms
              LOAD      s4 , $30
              CALL      lcd_write_inst4
              CALL      delay_40us
              LOAD      s4 , $20
              CALL      lcd_write_inst4
              CALL      delay_40us
              LOAD      s5 , $28
              CALL      lcd_write_inst8
              LOAD      s5 , $06
              CALL      lcd_write_inst8
              LOAD      s5 , $0C
              CALL      lcd_write_inst8
              LOAD      s5 , $01
              CALL      lcd_write_inst8
              CALL      delay_1ms
              CALL      delay_1ms
              CALL      lcd_clear
              RET
lcd_clear :   LOAD      s5 , $01
              CALL      lcd_write_inst8
              CALL      delay_1ms
              CALL      delay_1ms
              RET
```

```
lcd_write_inst4:    AND      s4 , $F8
                    OUT      s4 , lcd_port
                    CALL     lcd_pulse_e
                    RET

lcd_write_inst8:    LOAD     s4 , s5
                    AND      s4 , $F0
                    XOR      s4 , lcd_drive
                    CALL     lcd_write_inst4
                    CALL     delay_1us
                    LOAD     s4 , s5
                    AND      s4 , $0F
                    SL0      s4
                    SL0      s4
                    SL0      s4
                    SL0      s4
                    XOR      s4 , lcd_drive
                    CALL     lcd_write_inst4
                    CALL     delay_40us
                    LOAD     s4 , $F0
                    OUT      s4 , lcd_port
                    RET

lcd_write_data:     LOAD     s4 , s5
                    AND      s4 , $F0
                    OR       s4 , $0C
                    OUT      s4 , lcd_port
                    CALL     lcd_pulse_e
```

```
                    CALL        delay_1us
                    LOAD        s4 , s5
                    SL1         s4
                    SL1         s4
                    SL0         s4
                    SL0         s4
                    OUT         s4 , lcd_port
                    CALL        lcd_pulse_e
                    CALL        delay_40us
                    LOAD        s4 , $F0
                    OUT         s4 , lcd_port
                    RET
lcd_pulse_e :       XOR         s4 , lcd_e
                    OUT         s4 , lcd_port
                    CALL        delay_1us
                    XOR         s4 , lcd_e
                    OUT         s4 , lcd_port
                    RET
lcd_cursor :        TEST        s5 , $10
                    JUMP        Z, set_line2
                    AND         s5 , $0F
                    OR          s5 , $80
                    CALL        LCD_write_inst8
                    RET
set_line2 :         AND         s5 , $0F
                    OR          s5 , $C0
```

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```
                          CALL        LCD_write_inst8
                          RET
delay_1us:                LOAD        s0, delay_1us_constant
loop_1us:                 SUB         s0, 1
                          JUMP        NZ, loop_1us
                          RET

delay_2us:                LOAD        s1, 2
loop_2us:                 CALL        delay_1us
                          SUB         s1, 1
                          JUMP        NZ, loop_2us
                          RET

delay_10us:               LOAD        s1, 16
loop_10us:                CALL        delay_1us
                          SUB         s1, 1
                          JUMP        NZ, loop_10us
                          RET

delay_20us:               LOAD        s1, 32
loop_20us:                CALL        delay_1us
                          SUB         s1, 1
                          JUMP        NZ, loop_20us
                          RET

delay_40us:               LOAD        s1, 55
loop_40us:                CALL        delay_1us
                          SUB         s1, 1
                          JUMP        NZ, loop_40us
                          RET
```

```
delay_1ms:      LOAD    s2 , 37
loop_1ms:       CALL    delay_40us
                SUB     s2 , 1
                JUMP    NZ, loop_1ms
                RET

delay_20ms:     LOAD    s3 , 32
loop_20ms:      CALL    delay_1ms
                SUB     s3 , 1
                JUMP    NZ, loop_20ms
                RET

delay_1s:       LOAD    s4 , 80
loop_1s:        CALL    delay_20ms
                SUB     s4 , 1
                JUMP    NZ, loop_1s
                RET

ISR:            DINT
                FETCH   s7 , pwm_duty_counter1
                ADD     s7 , 1
                STORE   s7 , pwm_duty_counter1
                FETCH   s7 , pwm_duty_counter2
                ADDC    s7 , 0
                STORE   s7 , pwm_duty_counter2
                FETCH   s7 , pwm_duty_counter3
                ADDC    s7 , 0
                STORE   s7 , pwm_duty_counter3
                FETCH   s7 , pwm_duty_counter1
```

```
            FETCH       s6 , pwm_channel

            COMP        s7 , s6

            SLA         s9

            OUT         s9 , pwm_output_port

            FETCH       s7 , pwm_duty_counter1

            COMP        s7 , $00

            JUMP        NZ, isr_return

            FETCH       s7 , pwm_duty_counter2

            COMP        s7 , $E8

            JUMP        NZ, isr_return

            FETCH       s7 , pwm_duty_counter3

            COMP        s7 , $03

            JUMP        NZ, isr_return

            CALL        init_adc

            LOAD        s6 , 22

            LOAD        sA , $F0

            OUT         sA , adc_control_port

adc_loop :  LOAD        sA , $F1

            OUT         sA , adc_control_port

            LOAD        sA , $F0

            OUT         sA , adc_control_port

            IN          sB , adc_input_port

            SL0         sB

            SLA         sC

            SLA         sD

            SUB         s6 , 1
```

```
                    JUMP      NZ, adc_loop

                    CALL      init_adc

                    STORE     sC, data_down

                    STORE     sD, data_up

                    LOAD      s7, $00

                    STORE     s7, pwm_duty_counter2

                    STORE     s7, pwm_duty_counter3

                    FETCH     s7, sample_counter

                    ADD       s7, 1

                    STORE     s7, sample_counter

                    OUT       s7, led_port

                    LOAD      sE, $FF

isr_return:         LOAD      sF, $FF

                    RETI      ENABLE

                    ORG       $3FF

                    JUMP      ISR
```
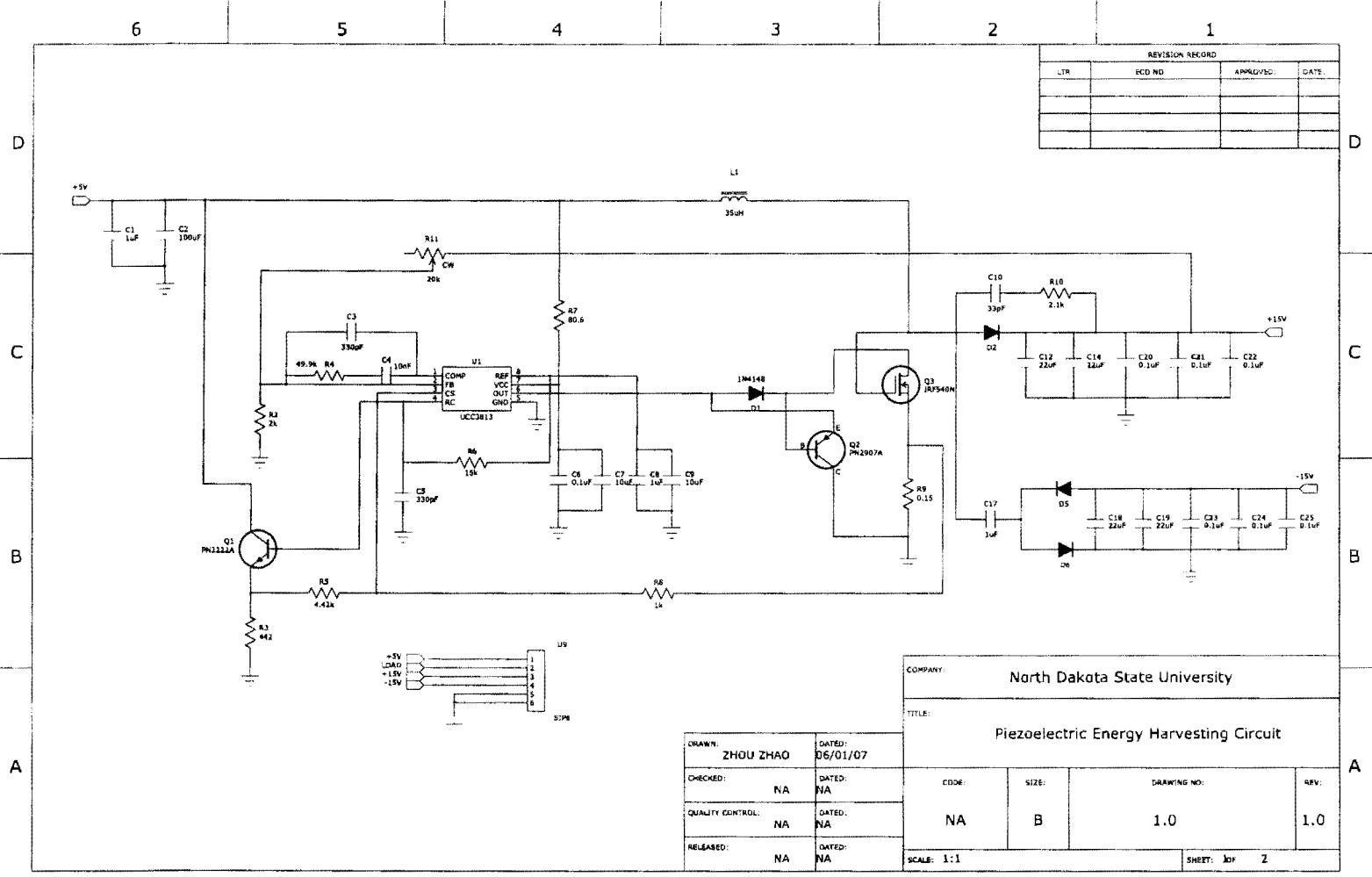
APPENDIX C. SCHEMATIC DIAGRAM OF PCB

COMPANY: North Dakota State University

TITLE: Piezoelectric Energy Harvesting Circuit

DRAWN: ZHOU ZHAO	DATED: 06/01/07				
CHECKED: NA	DATED: NA	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL: NA	DATED: NA	NA	B	1.0	1.0
RELEASED: NA	DATED: NA	SCALE: 1:1		SHEET: 1of 2	

REVISION RECORD

LTR	ECO NO	APPROVED:	DATE:

REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

IRFB40N
G
D S
Q4

L1
140mH

LOAD

U7
PIEZO

U2
DF01M

C11
33uF

D3
1N4754A

C13
100uF

+5V

R18
1.5k

D4
1N5817

LM741CN
R17
1.5k
U6

U3
VCC VB
HIN HO
LIN VS
COM LO
IR2301

C16
4.7uF

C15
4.7uF

U11
SIP6

PWM

R15
CW
5k

OP-77

R14
1k

U4

R12
20k
CW

+15V

OP-77

U5

R13
20k
CW

+15V

ADC ADC

U10
SIP6

R16
10k
CW

-15V

COMPANY:
North Dakota State University

TITLE:
Piezoelectric Energy Harvesting Circuit

DRAWN: ZHOU ZHAO	DATED: 06/01/07
CHECKED: NA	DATED: NA
QUALITY CONTROL: NA	DATED: NA
RELEASED: NA	DATED: NA

| CODE: NA | SIZE: B | DRAWING NO: 1.0 | REV: 1.0 |

SCALE: 1:1   SHEET: 2 OF 2